V23814-N1306-M130

Parallel Optical Link: PAROLI™ Tx AC

V23815-N1306-M130

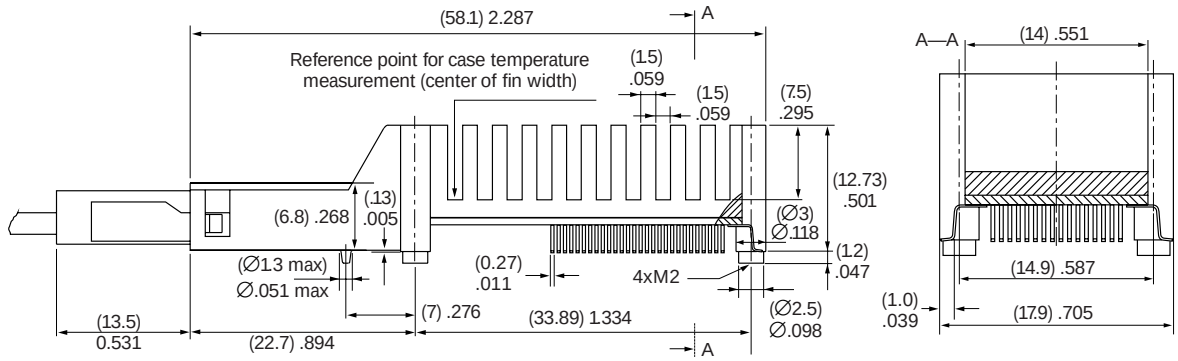
Parallel Optical Link: PAROLI™ Rx AC

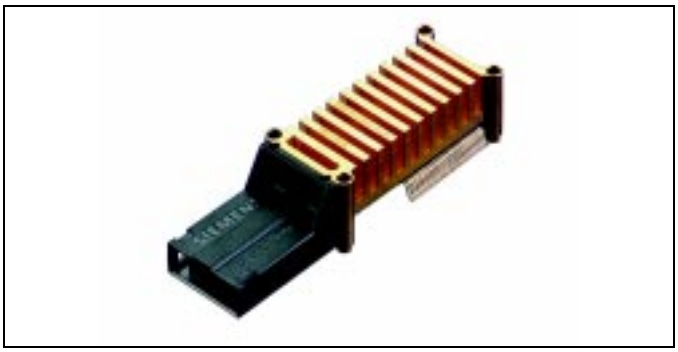
V23815-N1306-M150

Parallel Optical Link: PAROLI™ Rx AC

Preliminary

Dimensions in (mm) inches





FEATURES

- **Power supply 3.3 V**
- **Multistandard differential signal electrical interface**
- **12 electrical data channels**
- **Asynchronous, AC-coupled optical link**
- **12 optical data channels**
- **Transmission data rate of 500-2500 Mbit/s per channel, total link data rate up to 30 Gbit/s**
- **Transmission distance up to 200 m (depending on fiber dispersion)**
- **Transmitter: 840 nm VCSEL (Vertical Cavity Surface Emitting Laser) technology**
- **Receiver: 840 nm PIN diode array**
- **Fiber ribbon: 62.5 µm graded index multimode fiber**
- **SMC optical port, MT based ferrule**
- **SMD technology**
- **Transmitter: Class 1 FDA and Class 3A IEC laser safety compliant**

APPLICATIONS

Telecommunication

- **Switching equipment**
- **Access network**

Data Communication

- **Interframe (rack-to-rack)**
- **Intraframe (board-to-board)**
- **On board (optical backplane)**
- **Interface to SCI and HIPPI 6400 standards**

Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Supply Voltage (V_{CC}–V_{EE}) ..... –0.3 V to 4.5 V
Data/Control Input Levels (V)(1) ..... –0.5 V to V_{CC}+0.5 V
Data Input Differential Voltage ($|V_{ID}|$)(2) ..... 2.0 V
Operating Case Temperature (T_{CASE})(3) ..... 0°C to 80°C
Storage Ambient Temperature (T_{STG}) ..... –20°C to 100°C
Operating Moisture ..... 20% to 85%
Storage Moisture ..... 20% to 85%
Soldering Conditions Temp/Time (T_{SOLD}, t_{SOLD})(4) .... 260°C/10s
ESD Resistance (all pins to V_{EE}, human body model)(5) ..... 1 kV

Notes

1. If data inputs are operated in CML mode, with V_{IN} biased, the module may be damaged if more than two data pins are shorted to ground. Also it may be damaged if both pins of a corresponding input (P and N pins) are shorted to ground.
2. $|V_{ID}|$=|(input voltage of non-inverted input minus input voltage of inverted input)|.

3. Measured at case temperature reference point (see dimensional drawing).
4. Reflow soldering.
5. To avoid electrostatic damage the handling precautions as for MOS devices must be taken into account.

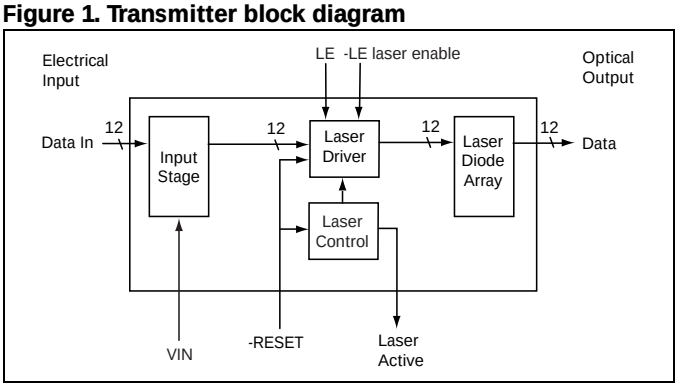
DESCRIPTION

PAROLI is a parallel optical link for high-speed data transmission. A complete PAROLI system consists of a transmitter module, a 12-channel fiber optic cable, and a receiver module. The transmitter V23814-N1306-M130 supports LVDS, CML and LVPECL differential signals. Two different receiver modules are available: The module V23815-N1306-M130 provides LVDS electrical outputs, module V23815-N1306-M150 provides adjustable CML output levels which also supports LVPECL input stages.

Transmitter V23814-N1306-M130

The transmitter module converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) diode array into parallel optical output signals. All input data signals are Multistandard Differential Signals (LVDS compatible, they also support LVPECL and CML because of the wide common mode input range). The electrical interface (LVDS, LVPECL or CML) is selected by the inputs VIN. The data rate is 500-2500 Mbit/s for each channel. Electrical input data should be DC balanced within 144 bits. The maximum time interval of consecutive 0's and 1's (run length) should not exceed 72 bits. This will ensure that the output jitter values given for the transmitter and receiver in this data sheet will be met. Otherwise, jitter values might be exceeded.
A logic low level at -RESET switches all laser outputs off. During power-up -RESET must be used as a power-on reset which disables the laser driver and laser control until the power supply has reached a 3 V level.
An additional Laser Active output is low if a laser fault is detected or -RESET is forced to low.
All nondata signals have LVCMOS levels.
Transmission delay of the PAROLI system is at a maximum of 1 ns for the transmitter, 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Figure 1. Transmitter block diagram



LASER SAFETY

The transmitter of the AC coupled Parallel Optical Link (PAROLI) is a FDA Class 1 laser product. It complies with FDA regulations 21 CFR 1040.10 and 1040.11. The transmitter is also an IEC Class 3A laser product as defined by IEC 825-1.To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.
The PAROLI module must be operated under the specified supply, temperature operating conditions (supply voltage between 3.0 V and 3.6 V, case temperature between 0°C and 80°C) under any circumstances to ensure laser safety.

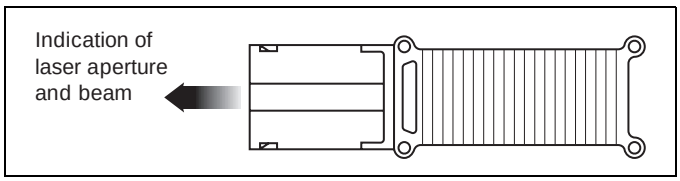
Caution

Do not stare into beam or view directly with optical instruments. The use of optical instruments with this product may lead to eye hazard.

Note

Any modification of the module will be considered an act of "manufacturing," and will require, under law, recertification of the product under FDA (21 CFR 1040.10 (i)).

Laser Emission



Laser safety design considerations

To ensure laser safety for all input data patterns each channel is controlled internally and will be switched off if the laser safety limits are exceeded.
An internal control unit switches the respective data channel output off if the input duty cycle permanently exceeds 57%. The alerter will not disable the channel below an input duty cycle of 57% under all circumstances.
The minimum alerter response time is 1 µs with a constant high input, i.e. in the input pattern the time interval of excessive high input (e.g. '1's in excess of a 57% duty cycle, consecutive or non-consecutive) must not exceed 1 µs, otherwise the respective channel will be switched off. The alerter switches the respective channel from off to on without the need of resetting the module if the input duty cycle is no longer violated.
All of the channel alerters operate independently, i.e. an alert within a channel does not affect the other channels. To decrease the power consumption of the module unused channel inputs can be tied to high input level. In this way a portion of the supply current in this channel is triggered to shut down by the corresponding alerter.

TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

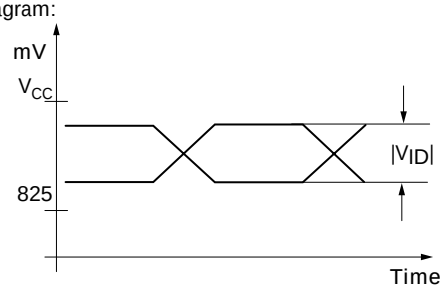
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	3.0	3.6	V
Noise on Power Supply(1)	N_{PS1}		10	mV
Noise on Power Supply(2)	N_{PS2}		100	
Data Input Voltage Range(6)	V_{LVDSI}	825	V_{CC}	
Data Input Differential Voltage(3, 6)	$\|V_{ID}\|$	80	1000	
Signal Input Skew(4)	t_{SPN}		30	ps
Signal Input Rise/Fall Time(5)	t_R, t_F	60	300	
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time(7)	t_R, t_F		20	ns

Notes

Voltages refer to V_{EE}=0 V.

1. Noise frequency is 1 kHz to 1 MHz. Voltage is peak-to-peak value.
2. Noise frequency is 1 MHz to 2 GHz. Voltage is peak-to-peak value.
3. $|V_{ID}|$=|(input voltage of non-inverted input minus input voltage of inverted input)|.
4. Skew between positive and negative inputs measured at 50% level.
5. 20%–80% level.
6. Level diagram:



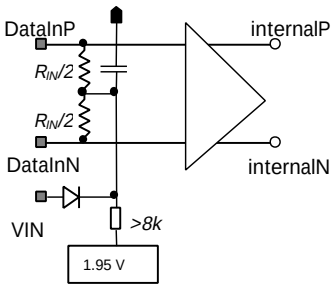
7. Measured between 0.8 V and 2.0 V.

Transmitter Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		350	450	mA
Power Consumption	P		1.2	1.6	W
Data Rate per Channel(1)	D_R	500		2500	MBit/s
LVCMOS Output Voltage Low	$V_{LVCMOSOL}$			0.4	V
LVCMOS Output Voltage High	$V_{LVCMOSOH}$	2.5			V
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output Current High(2)	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output Current Low(3)	$I_{LVCMOSOL}$			4.0	mA
Data Differential Input Impedance(4)	R_{IN}	80		120	Ω
Data Input(5) Differential Current	$\|I_I\|$			5.5	mA

Notes

1. To achieve best jitter performance electrical input data should be DC balanced within 144 bits. Maximum time interval of consecutive '0's and '1's (run length) should be 72 bits.
2. Source current.
3. Sink current.
4. Input Stage.



5. At 400 mV input swing

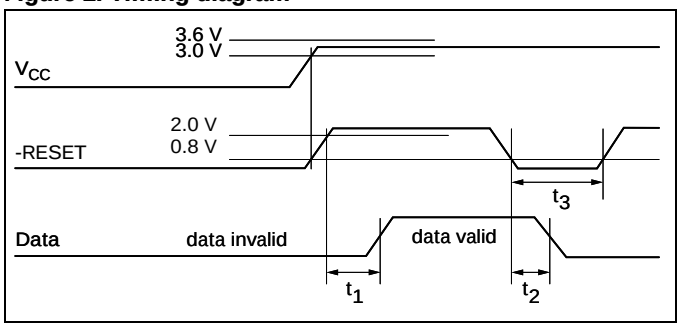
Parameter	Symbol	Min.	Max.	Units
Optical Rise Time(1)	t_R		200	ps
Optical Fall Time(1)	t_F			
Random Jitter (14σ)	J_R		0.23	UI
Deterministic Jitter	J_D		0.20	UI
Channel-to-channel skew(2)	t_{CSK}		75	ps
Launched Average Power	P_{AVG}	–11.0	–6.0	dBm
Launched Power Shutdown	P_{SD}		–30.0	
Center Wavelength	λ_C	820	860	nm
Spectral Width (FWHM)	$\Delta\lambda$		2	
Relative Intensity Noise	RIN		–116	dB/Hz
Extinction Ratio (dynamic)	ER	6.0		dB

Notes

Optical parameters valid for each channel.

1. 20%–80% level.
2. With input channel-to-channel skew 0 ps and a maximum data input channel-to-channel average deviation and swing deviation of 5%.

Figure 2. Timing diagram



Parameter	Symbol	Min.	Max.	Units
-RESET on Delay Time	t_1		100	ms
-RESET off Delay Time	t_2		50	µs
-RESET Low Duration(1)	t_3	10		µs

Note

1. Only when not used as power on reset. At any failure recovery, -RESET must be brought to low level for at least t_3.

Transmitter Pin Description

Pin#	Pin Name	Level/Logic	Description
1	V_{CC}		Power supply voltage of laser driver
2	t.b.l.o.		to be left open
3			
4			
5			
6	LA	LVCMOS Out	Laser Active High=normal operation Low=laser fault or -RESET low
7	V_{EE}		Ground
8	VIN		Input VIN rail CML: VIN = Reference Supply (e.g. V_{CC}) LVPECL, LVDS: VIN = V_{EE}
9	t.b.l.o.		to be left open
10	t.b.l.o.		to be left open
11	V_{EE}		Ground
12	V_{EE}		Ground
13	DI01N	Signal In	Data Input #1, inverted
14	DI01P	Signal In	Data Input #1, non- inverted
15	V_{EE}		Ground
16	V_{EE}		Ground
17	DI02N	Signal In	Data Input #2, inverted
18	DI02P	Signal In	Data Input #2, non- inverted
19	V_{EE}		Ground
20	V_{EE}		Ground
21	DI03N	Signal In	Data Input #3, inverted
22	DI03P	Signal In	Data Input #3, non- inverted
23	V_{EE}		Ground
24	V_{EE}		Ground
25	t.b.l.o.		to be left open
26	DI04N	Signal In	Data Input #4, inverted
27	DI04P	Signal In	Data Input #4, non- inverted
28	V_{EE}		Ground
29	DI05N	Signal In	Data Input #5, inverted
30	DI05P	Signal In	Data Input #5, non- inverted
31	V_{EE}		Ground
32	V_{EE}		Ground
33	DI06N	Signal In	Data Input #6, inverted
34	DI06P	Signal In	Data Input #6, non- inverted
35	V_{EE}		Ground
36	V_{EE}		Ground
37	DI07N	Signal In	Data Input #7, inverted
38	DI07P	Signal In	Data Input #7, non- inverted
39	V_{EE}		Ground
40	V_{EE}		Ground
41	DI08N	Signal In	Data Input #8, inverted
42	DI08P	Signal In	Data Input #8, non- inverted
43	V_{EE}		Ground
44	V_{EE}		Ground
45	V_{EE}		Ground
46	DI09N	Signal In	Data Input #9, inverted
47	DI09P	Signal In	Data Input #9, non- inverted
48	t.b.l.o.		to be left open
49	V_{EE}		Ground
50	V_{EE}		Ground
51	DI10N	Signal In	Data Input #10, inverted
52	DI10P	Signal In	Data Input #10, non- inverted
53	V_{EE}		Ground
54	V_{EE}		Ground
55	DI11N	Signal In	Data Input #11, inverted
56	DI11P	Signal In	Data Input #11, non- inverted
57	V_{EE}		Ground
58	V_{EE}		Ground
59	DI12N	Signal In	Data Input #12, inverted
60	DI12P	Signal In	Data Input #12, non- inverted
61	V_{EE}		Ground
62	VIN		VIN rail CML: VIN = Reference Supply (e.g. V_{CC}) LVPECL, LVDS: VIN = V_{EE}
63	t.b.l.o.		to be left open
64	-RESET	LVCMOS In	High=laser diode array is active Low=switches laser diode array off This input has an internal pull-down resistor to ensure laser safety switch off in case of unconnected -RESET input
65	V_{EE}		Ground
66	V_{EE}		Ground

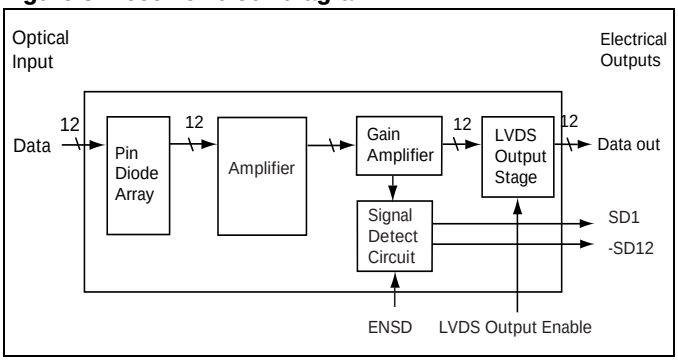
Pin#	Pin Name	Level/Logic	Description
67	LE	LVCMOS In	Laser ENABLE. High active. High=laser array is on if -LE is also active. Low=laser array is off. This input can be used for connection with an Open Fiber Control (OFC) circuit to enable IEC class 1 links. Has an internal pull-up, therefore can be left open.
68	-LE		Laser ENABLE. Low active. Low=laser array is on if LE is also active. This input can be used for connection with an Open Fiber Control (OFC) circuit to enable IEC class 1 links. Has an internal pull-down, therefore can be left open.
69	t.b.l.o.		to be left open
70	t.b.l.o.		to be left open
71	t.b.l.o.		to be left open
72	V_{CC}		Power supply voltage of laser driver

DESCRIPTION

Receiver V23815-N1306-M130

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, transimpedance amplifiers, and gain amplifiers. All output data signals are Low Voltage Differential Signals (LVDS). The data rate is 500-2500 Mbit/s for each channel. Optical input data should be DC balanced within 144 bits. The maximum time interval of consecutive 0's and 1's (run length) should not exceed 72 bits. This will ensure that the output jitter values given for the transmitter and receiver in this data sheet will be met. Otherwise, jitter values might be exceeded.
Additional Signal Detect outputs (SD1 active high / SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.
A logic low at LVDS Output Enable sets all data outputs to logic low. SD outputs will not be effected.
All nondata signals have LVCMOS levels. Transmission delay of the PAROLI system is at a maximum 1 ns for the transmitter, 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Figure 3. Receiver block diagram



TECHNICAL DATA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{CC}	3.0	3.6	V
Noise on Power Supply(1)	N_{PS1}		10	mV
Noise on Power Supply(2)	N_{PS2}		100	
Differential LVDS Termination Impedance	R_t	80	120	Ω
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time(3)	t_R, t_F		20	ns
Optical Input Rise/Fall Time(4)	t_R, t_F		200	ps
Input Extinction Ratio	ER	5.0		dB
Input Center Wavelength	λ_C	820	860	nm

Notes

Voltages refer to V_{EE}=0 V.

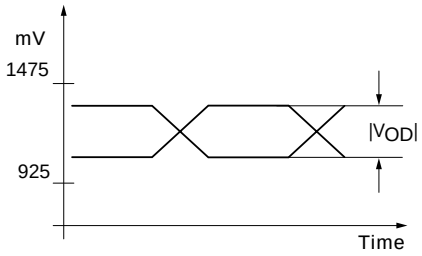
1. Noise frequency: 1 kHz to 1 MHz.
2. Noise frequency: 1 MHz to 2 GHz.
3. Measured between 0.8 V and 2.0 V.
4. 20%–80% level.

Receiver Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		250	350	mA
Power Consumption	P		0.8	1.3	W
LVDS Output Low Voltage(1,4)	V_{LVDSOL}	925			mV
LVDS Output High Voltage(1,4)	V_{LVDSOH}			1475	
LVDS Output Differential Voltage(1, 2, 4)	$\|V_{OD}\|$	250		400	
LVDS Output Offset Voltage(1, 3, 4)	V_{OS}	1125		1275	
LVDS Rise/Fall Time(5)	t_R, t_F			300	ps
LVCMOS Output Voltage Low	$I_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$I_{LVCMOSOH}$	2500			
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output(8) Current High	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output(9) Current Low	$I_{LVCMOSOL}$			4.0	
Random Jitter(6, 7) (14σ)	J_R			0.31	UI
Deterministic Jitter(6)	J_D			0.08	UI
Channel-to-channel skew(10)	t_{CSK}			75	ps

Notes

1. Level Diagram:



2. $|V_{OD}|$=|(output voltage of non-inverted output minus output voltage of inverted output)|.
3. V_{OS}=1/2 (output voltage of inverted output + output voltage of non-inverted output).
4. LVDS output must be terminated differentially with R_t.
5. Measured between 20% and 80% level with a maximum capacitive load of 4 pF.
6. With no optical input jitter.
7. At sensitivity limit of -17.0 dBm at infinite ER.
8. Source current
9. Sink current
10. With input channel-to-channel skew 0 ps.

Parameter	Symbol	Min.	Typ.	Max.	Units
Data Rate Per Channel(1)	D_R	500		2500	Mbit/s
Sensitivity (Average Power)(2)	P_{IN}			–17.0	dBm
Saturation (Average Power)(2)	P_{SAT}	–6.0			
Signal Detect Assert Level(3)	P_{SDA}			–18.0	
Signal Detect Deassert Level(3)	P_{SDD}	–26.0			
Signal Detect Hysteresis(3)	P_{SDA}– P_{SDD}	1.0	2.5	4.0	dB
Return Loss of Receiver	A_{RL}	12			

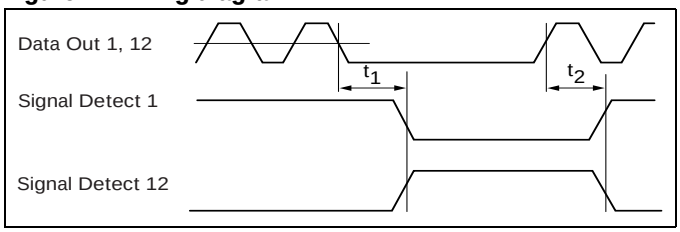
Notes

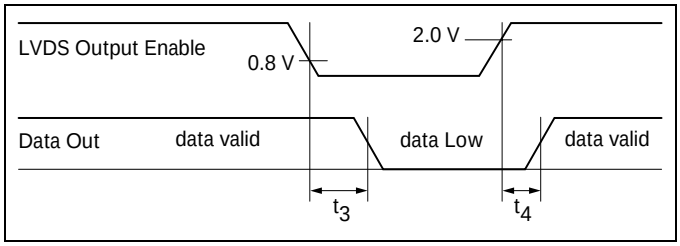
Optical parameters valid for each channel.

1. Optical input data should be DC balanced within 100 ns. Maximum time interval of consecutive '0's and '1's (run length) should not exceed 50 ns.
2. Measured with a DC balanced pattern (within 144 bits) with a maximum run length of 72 bits. BER=10^{-12}. Extinction ratio=infinite.
3. P_{SDA}: Average optical power when SD switches from unactive to active.

   P_{SDD}: Average optical power when SD switches from active to unactive.

Figure 4. Timing diagram





Parameter	Symbol	Max.	Units
Signal Detect Deassert Time	t_1	10	µs
Signal Detect Assert Time	t_2		
LVDS Output Enable off Delay Time	t_3	20	ns
LVDS Output Enable on Delay Time	t_4		

Receiver Pin Description

Pin#	Pin Name	Level/Logic	Description
1	V_{EE}		Ground
2	V_{CC1}		Power supply voltage of preamplifier
3	V_{CC2}		Power supply voltage of analog circuitry
4	t.b.l.o.		to be left open
5	-RESET	LVCMOS In	High=normal operation Low=sets all Data Outputs to low This input has an internal pull-up resistor which pulls to high level when this input is left open
6	SD1	LVCMOS Out	Signal Dectect on fiber #1. High=signal of sufficient AC power is present on fiber #1 Low=signal on fiber #1 is insufficient
7	V_{CC3}		Power supply voltage of digital circuitry
8	V_{EE}		Ground
9	t.b.l.o.		to be left open
10	V_{EE}		Ground
11	V_{EE}		Ground
12	V_{EE}		Ground
13	DO01P	LVDS Out	Data Output #1, non-inverted
14	DO01N	LVDS Out	Data Output #1, inverted
15	V_{EE}		Ground
16	V_{EE}		Ground
17	DO02P	LVDS Out	Data Output #2, non-inverted
18	DO02N	LVDS Out	Data Output #2, inverted
19	V_{EE}		Ground
20	V_{EE}		Ground
21	DO03P	LVDS Out	Data Output #3, non-inverted
22	DO03N	LVDS Out	Data Output #3, inverted
23	V_{EE}		Ground
24	V_{EE}		Ground
25	t.b.l.o.		to be left open
26	DO04P	LVDS Out	Data Output #4, non-inverted
27	DO04N	LVDS Out	Data Output #4, inverted
28	V_{EE}		Ground
29	DO05P	LVDS Out	Data Output #5, non-inverted
30	DO05N	LVDS Out	Data Output #5, inverted
31	V_{EE}		Ground
32	V_{EE}		Ground
33	DO06P	LVDS Out	Data Output #6, non-inverted
34	DO06N	LVDS Out	Data Output #6, inverted
35	V_{EE}		Ground
36	V_{EE}		Ground
37	DO07P	LVDS Out	Data Output #7, non-inverted
38	DO07N	LVDS Out	Data Output #7, inverted
39	V_{EE}		Ground
40	V_{EE}		Ground
41	DO08P	LVDS Out	Data Output #8, non-inverted
42	DO08N	LVDS Out	Data Output #8, inverted
43	V_{EE}		Ground
44	V_{EE}		Ground
45	V_{EE}		Ground
46	DO09P	LVDS Out	Data Output #9, non-inverted
47	DO09N	LVDS Out	Data Output #9, inverted
48	t.b.l.o.		to be left open
49	V_{EE}		Ground
50	V_{EE}		Ground
51	DO10P	LVDS Out	Data Output #10, non-inverted
52	DO10N	LVDS Out	Data Output #10, inverted
53	V_{EE}		Ground
54	V_{EE}		Ground
55	DO11P	LVDS Out	Data Output #11, non-inverted
56	DO11N	LVDS Out	Data Output #11, inverted
57	V_{EE}		Ground
58	V_{EE}		Ground
59	DO12P	LVDS Out	Data Output #12, non-inverted
60	DO12N	LVDS Out	Data Output #12, inverted
61	V_{EE}		Ground
62	V_{EE}		Ground
63	V_{EE}		Ground
64	t.b.l.o.		to be left open
65	V_{EE}		Ground
66	V_{CC3}		Power supply voltage of digital circuitry
67	-SD12	LVCMOS Out low active	Signal Detect on fiber #12 Low=signal of sufficient AC power is present on fiber #12 High=signal on fiber #12 is insufficient
68	ENSD	LVCMOS In	High=SD1 and SD12 function enabled Low=SD1 and SD12 are set to permanent active.Internal pull-up pulls to high level when input is left open.
69	t.b.l.o.		to be left open
70	V_{CC2}		Power supply voltage of LVDS outputs
71	V_{CC1}		Power supply voltage of amplifier
72	V_{EE}		Ground

DESCRIPTION

Receiver V23815-N1306-M150

The PAROLI receiver module converts parallel optical input signals into parallel electrical output signals. The optical signals received are converted into voltage signals by PIN diodes, transimpedance amplifiers, and gain amplifiers. The differential data outputs are adjustable CML signals. The output differential voltage (swing) is adjusted by an external resistor connected to the REFR module input, the output average is adjustable by external pull-up resistors. The data rate is 500-2500 Mbit/s for each channel. Optical input data should be DC balanced within 144 bits. The maximum time interval of consecutive 0's and 1's (run length) should not exceed 72 bits. This will ensure that the output jitter values given for the transmitter and receiver in this data sheet will be met. Otherwise, jitter values might be exceeded.

Additional Signal Detect outputs (SD1 active high / SD12 active low) show whether an optical AC input signal is present at data input 1 and/or 12. The signal detect circuit can be disabled with a logic low at ENSD. The disabled signal detect circuit will permanently generate an active level at Signal Detect outputs, even if there is insufficient signal input. This could be used for test purposes.

A logic low at Output Enable sets all data outputs to logic low. SD outputs will not be effected.

All nondata signals have LVCMOS levels. Transmission delay of the PAROLI system is at a maximum 1 ns for the transmitter, 1 ns for the receiver and approximately 5 ns per meter for the fiber optic cable.

Figure 5. Receiver block diagram

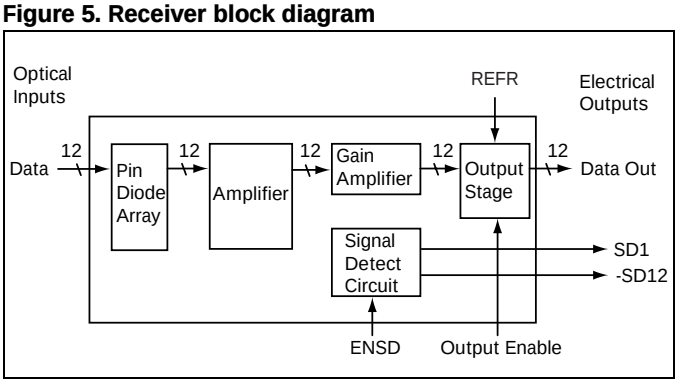
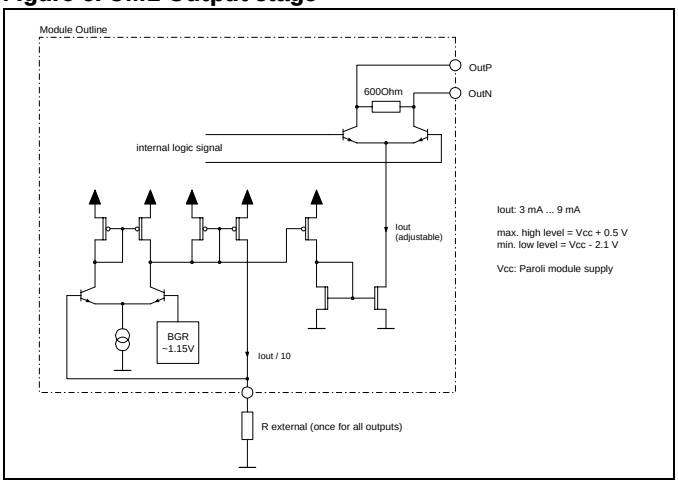


Figure 6. CML Output stage



TECHNICAL DATA

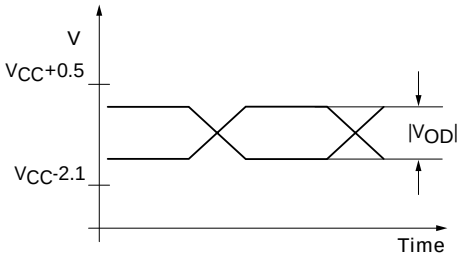
Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{CC}	3.0	3.6	V
Noise on Power Supply(1)	N_{PS1}		10	mV
Noise on Power Supply(2)	N_{PS2}		100	
Output Current(3)	I_{out}	3	9	mA
Output Voltage(4)	V_{out}	V_{CC}-2.1	V_{CC}+0.5	V
Output Differential Voltage(4, 5)	V_{OD}	80	800	mV
Output Load RC Time Constant	t_{RC}		150	ps
LVCMOS Input High Voltage	$V_{LVCMOSIH}$	2.0	V_{CC}	V
LVCMOS Input Low Voltage	$V_{LVCMOSIL}$	V_{EE}	0.8	
LVCMOS Input Rise/Fall Time(6)	t_R, t_F		20	ns
Optical Input Rise/Fall Time(7)	t_R, t_F		200	ps
Input Extinction Ratio	ER	5.0		dB
Input Center Wavelength	λ_C	820	860	nm

Notes

Voltages refer to V_{EE}=0 V.

1. Noise frequency: 1 kHz to 1 MHz.
2. Noise frequency: 1 MHz to 2 GHz.
3. $I_{out} \approx 10 * 1.15\ V / R_{external}$. Resistor $R_{external}$ to be connected externally between REFR and V_{EE}.
4. Level Diagram:



5. $V_{OD} = I_{out} * 300\ \Omega \parallel R_{LOAD}$. The output current range of 3mA to 9mA corresponds to V_{OD} = 130 mV.. 385 mV for R_{LOAD} = 50 Ω. $|V_{OD}|$=|(output voltage of non-inverted output minus output voltage of inverted output)|.
6. Measured between 0.8 V and 2.0 V.
7. 20%-80% level.

Receiver Electro-Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Current	I_{CC}		130+18 I_{out}	200+24 I_{out}	mA
Power Consumption(1)	P		0.6	1.0	W
Rise/Fall Time(2)	t_R, t_F			250	ps
LVCMOS Output Voltage Low	$I_{LVCMOSOL}$			400	mV
LVCMOS Output Voltage High	$I_{LVCMOSOH}$	2500			

Parameter	Symbol	Min.	Typ.	Max.	Units
LVCMOS Input Current High/Low	$I_{LVCMOSI}$	–500		500	µA
LVCMOS Output(3) Current High	$I_{LVCMOSOH}$			0.5	mA
LVCMOS Output(4) Current Low	$I_{LVCMOSOL}$			4.0	
Random Jitter(5, 6) (14σ)	J_R			0.31	UI
Deterministic Jitter(5)	J_D			0.08	UI
Channel-to-channel skew(7)	t_{CSK}			75	ps

Notes

1. Calculated for I_{out}=3 mA.
2. Measured between 20% and 80% level.
3. Source current.
4. Sink current.
5. With no optical input jitter.
6. At sensitivity limit of -17.0 dBm at infinite ER.
7. With input channel-to-channel skew 0 ps.

Parameter	Symbol	Min.	Typ.	Max.	Units
Data Rate Per Channel(1)	D_R	500		2500	Mbit/s
Sensitivity (Average Power)(2)	P_{IN}			–17.0	dBm
Saturation (Average Power)(2)	P_{SAT}	–6.0			
Signal Detect Assert Level(3)	P_{SDA}			–18.0	
Signal Detect Deassert Level(3)	P_{SDD}	–26.0			
Signal Detect Hysteresis(3)	P_{SDA}– P_{SDD}	1.0	2.5	4.0	dB
Return Loss of Receiver	A_{RL}	12			

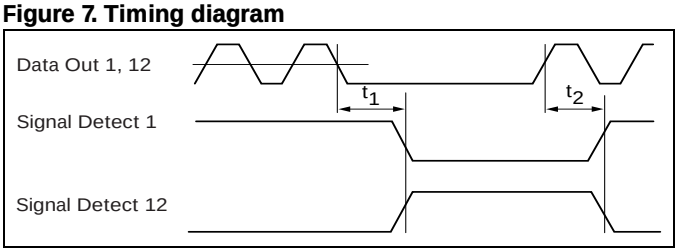
Notes

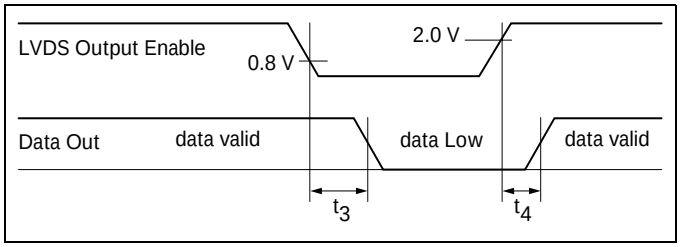
Optical parameters valid for each channel.

1. Optical input data should be DC balanced within 144 bits. Maximum time interval of consecutive '0's and '1's (run length) should not exceed 72 bits.
2. Measured with a DC balanced pattern (within 144 bits) with a maximum run length of 72 bits. BER=10^{-12}. Extinction ratio=infinite.
3. P_{SDA}: Average optical power when SD switches from unactive to active.

   P_{SDD}: Average optical power when SD switches from active to unactive.

Figure 7. Timing diagram





Parameter	Symbol	Max.	Units
Signal Detect Deassert Time	t_1	10	µs
Signal Detect Assert Time	t_2		
LVDS Output Enable off Delay Time	t_3	20	ns
LVDS Output Enable on Delay Time	t_4		

Figure 8. Interfacing to CML

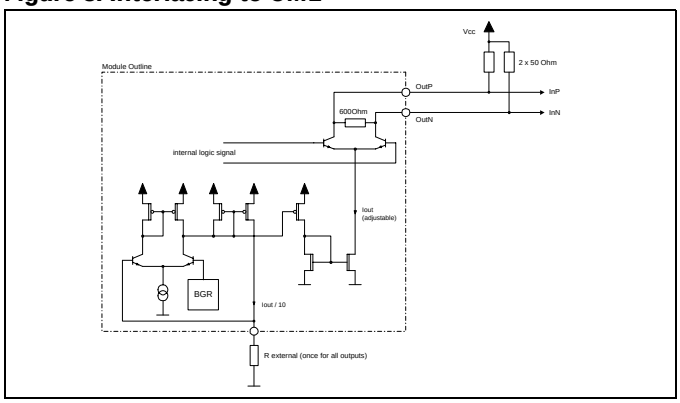
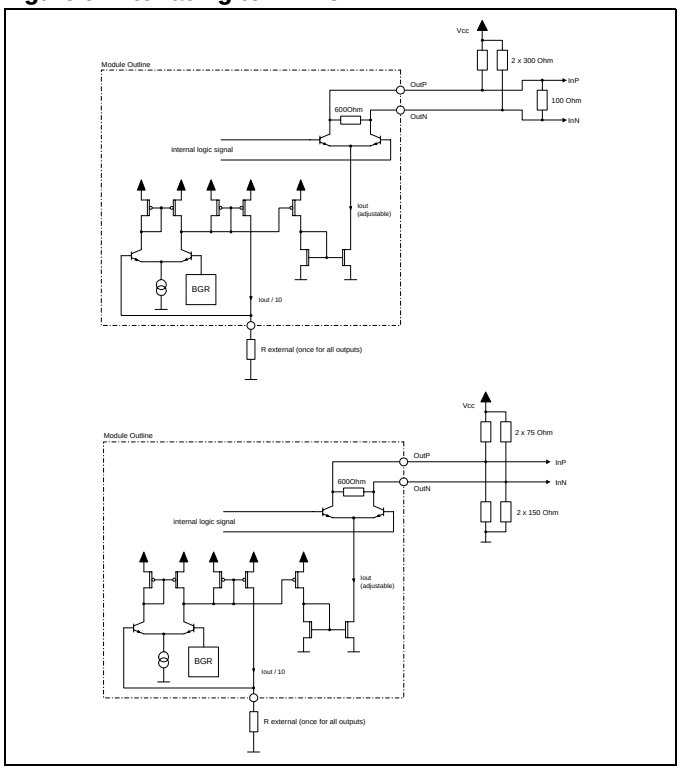


Figure 9. Interfacing to LVPECL



Receiver Pin Description

Pin#	Pin Name	Level/Logic	Description
1	V_{EE}		Ground
2	V_{CC1}		Power supply voltage of preamplifier
3	V_{CC2}		Power supply voltage of analog circuitry
4	t.b.l.o.		to be left open
5	-RESET	LVCMOS In	High=normal operation Low=sets all Data Outputs to low This input has an internal pull-up resistor which pulls to high level when this input is left open
6	SD1	LVCMOS Out	Signal Dectect on fiber #1. High=signal of sufficient AC power is present on fiber #1 Low=signal on fiber #1 is insufficient
7	V_{CC3}		Power supply voltage of digital circuitry
8	V_{EE}		Ground
9	t.b.l.o.		to be left open
10	V_{EE}		Ground
11	V_{EE}		Ground
12	V_{EE}		Ground
13	DO01P	Signal Out	Data Output #1, non-inverted
14	DO01N	Signal Out	Data Output #1, inverted
15	V_{EE}		Ground
16	V_{EE}		Ground
17	DO02P	Signal Out	Data Output #2, non-inverted
18	DO02N	Signal Out	Data Output #2, inverted
19	V_{EE}		Ground
20	V_{EE}		Ground
21	DO03P	Signal Out	Data Output #3, non-inverted
22	DO03N	Signal Out	Data Output #3, inverted
23	V_{EE}		Ground
24	V_{EE}		Ground
25	t.b.l.o.		to be left open
26	DO04P	Signal Out	Data Output #4, non-inverted
27	DO04N	Signal Out	Data Output #4, inverted
28	V_{EE}		Ground
29	DO05P	Signal Out	Data Output #5, non-inverted
30	DO05N	Signal Out	Data Output #5, inverted
31	V_{EE}		Ground
32	V_{EE}		Ground
33	DO06P	Signal Out	Data Output #6, non-inverted
34	DO06N	Signal Out	Data Output #6, inverted
35	V_{EE}		Ground
36	V_{EE}		Ground
37	DO07P	Signal Out	Data Output #7, non-inverted
38	DO07N	Signal Out	Data Output #7, inverted
39	V_{EE}		Ground
40	V_{EE}		Ground
41	DO08P	Signal Out	Data Output #8, non-inverted
42	DO08N	Signal Out	Data Output #8, inverted
43	V_{EE}		Ground
44	V_{EE}		Ground
45	V_{EE}		Ground
46	DO09P	Signal Out	Data Output #9, non-inverted
47	DO09N	Signal Out	Data Output #9, inverted
48	t.b.l.o.		to be left open
49	V_{EE}		Ground
50	V_{EE}		Ground
51	DO10P	Signal Out	Data Output #10, non-inverted
52	DO10N	Signal Out	Data Output #10, inverted
53	V_{EE}		Ground
54	V_{EE}		Ground
55	DO11P	Signal Out	Data Output #11, non-inverted
56	DO11N	Signal Out	Data Output #11, inverted
57	V_{EE}		Ground
58	V_{EE}		Ground
59	DO12P	Signal Out	Data Output #12, non-inverted
60	DO12N	Signal Out	Data Output #12, inverted
61	V_{EE}		Ground
62	V_{EE}		Ground
63	V_{EE}		Ground
64	REFR		Adjustment of output current by connecting external Resistor to V_{EE}.
65	V_{EE}		Ground
66	V_{CC3}		Power supply voltage of digital circuitry
67	-SD12	LVCMOS Out low active	Signal Detect on fiber #12 Low=signal of sufficient AC power is present on fiber #12 High=signal on fiber #12 is insufficient
68	ENSD	LVCMOS In	High=SD1 and SD12 function enabled Low=SD1 and SD12 are set to permanent active.Internal pull-up pulls to high level when input is left open.
69	t.b.l.o.		to be left open
70	V_{CC2}		Power supply voltage of LVDS outputs
71	V_{CC1}		Power supply voltage of amplifier
72	V_{EE}		Ground

Optical Port

Designed for Siemens Simplex MT Connector (SMC)

- Port outside dimensions: 15.4 mm x 6.8 mm (width x height)
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Alignment pins fixed in module port
- Integrated mechanical keying
- process plug (SMC dimensions) included with every module
- cleaning of port and connector interfaces necessary prior to mating

Features of Siemens Simplex MT Connector (SMC)

(as part of optional PAROLI fiber optic cables)

- Uses standardized MT ferrule
- MT compatible fiber spacing (250 µm) and alignment pin spacing (4600 µm)
- Snap-in mechanism
- Ferrule bearing spring loaded
- Not strain-relieved
- Integrated mechanical keying

Cleaning and Soldering Process for Transmitter and Receiver

Special care must be taken to remove residuals from the soldering and washing process, which can impact the mechanical function. Avoid the use of aggressive organic solvents like ketones, ethers, etc. Consult the supplier of the PAROLI modules and the supplier of the solder paste and flux for recommended cleaning solvents.
The following common cleaning solvents will not affect the module: deionized water, ethanol, and isopropyl alcohol. Air-drying is recommended to a maximum temperature of 100°C. Do not use ultrasonics.
During soldering, heat must be applied to the leads only, to ensure that the case temperature never exceeds 100°C. The module must be mounted with a hot-bar soldering process using a SnPb solder type, e.g. S-Sn63Pb37E, in accordance with ISO 9435.

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