Network Products

VNS67802
P672 HDLC CONTROLLER
Packet And Cell Engines (PACE) family

VLSI Technology
A Subsidiary of Philips Semiconductors

OVERVIEW

The P672 (VNS67802) is the cost effective, low power member of VLSI's Packet And Cell Engine family providing 672-channel HDLC controller and ATM cell delineation functionality.

Unique Scalable Time-sliced Architecture

The P672 uses a unique, patent pending, time-sliced state machine architecture for performing packet and cell delineation functions. It includes a scatter/gather DMA engine, 32/64-bit 33 MHz PCI V2.1 compliant bus for system configuration and HDLC packet transfers, and a Utopia Level 2 compliant bus for ATM cell transfers. VNS67802 can perform HDLC packet and ATM cell delineation for up to 672 logical channels.

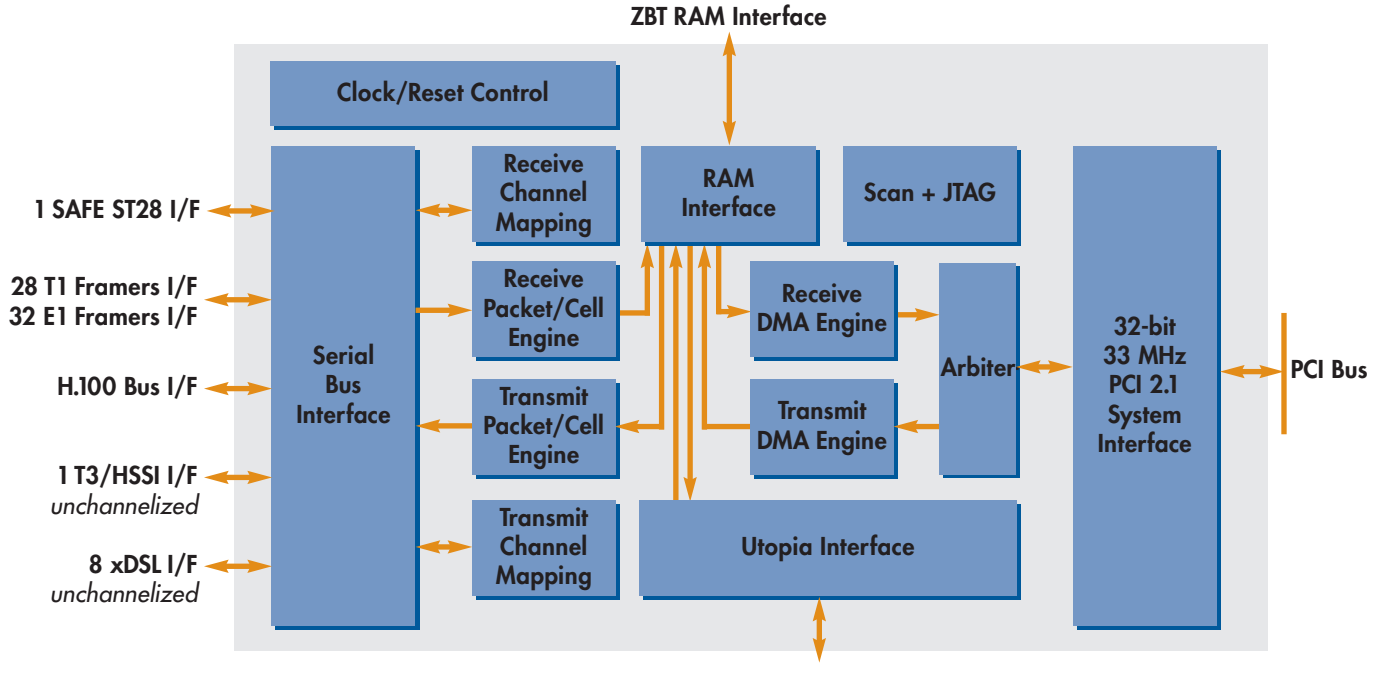
Lower Cost, Smaller Board Space

This device can interface directly with up to 28 T1 or 32 E1 framers, 1 unchannelized DS3 or HSSI channel, 8 xDSL channels, up to 672 DS0 channels via a H.100 bus, and up to 28 T1 framers via a proprietary interface, for a combined throughput of up to 64 Mbps.

FEATURES

- 672 full duplex HDLC channels
- 1 full duplex DS3 or HSSI channel
- 16 HDSL and 8 ADSL channels
- 28 T1 or 32 E1 channels
- Up to 28 T1 channels via a proprietary interface to the VNS67700 ST28 Framer
- Combined throughput of up to 64 Mbps
- Delineates HDLC packets or ATM cells per logical channel
- Flexible and powerful mapping of DS0 physical to logical channels
- HDLC flag insertion, bit stuffing, CRC-16/32 generation for each transmit channel
- HDLC flag detection, bit de-stuffing and CRC-16/32 calculation for each receive channel
- Detects a valid ATM cell by framing to the HEC in the receive direction, and inserts a HEC value for each ATM cell in the transmit direction.
- 672 channel scatter gather DMA engine transfers packets to and from host memory using a flexible descriptor structure
- External ZBT SRAM allows large burst transfers providing efficient PCI bus utilization
- 32/64-bit 33 MHz PCI V2.1 compliant bus interface for system configuration and packet transfers
- Utopia Level 2 compliant bus interface for ATM cell transfers

P672 Block Diagram



- Seamless interface to SAFE Framer family
- IEEE 1149.1 JTAG boundary scan
- 3.3V CMOS with 5V tolerant I/O
- 329-pin PBGA
- VLSI's PACE family also includes the VNS67800 controller with 2048 channels

DESCRIPTION

HDLC PACKETS

P672 performs HDLC flag insertion/detection, bit stuffing/de-stuffing and CRC-16/32 generation/detection for each transmit and receive channel. On the receive side, packet length violation, abort sequence detection, and octet alignment violation are checked and reported. The packets are then transferred to host memory via a scatter-gather DMA controller. On the transmit side, packets are aborted in case of underflows and idle flags are transmitted between packets.

ATM CELLS

In the receive path, P672 searches for the cell boundaries by framing to the Header Error Check (HEC). The cell engine then transfers the ATM cells to an external SAR via a Utopia Level 2 interface. Abnormal cases are detected and reported. In the transmit path the P672 calculates and inserts a HEC value for the header. Idle cells are transmitted when there are no more valid cells to be transmitted.

The P672 uses an efficient scatter-gather DMA engine that minimizes PCI bus access while transferring packets to and from host memory. External ZBT SRAM for intermediate FIFO storage improves PCI bus utilization by allowing large burst transfers. Scatter/gather feature allows packet data to be placed anywhere within a specified address space.

APPLICATIONS

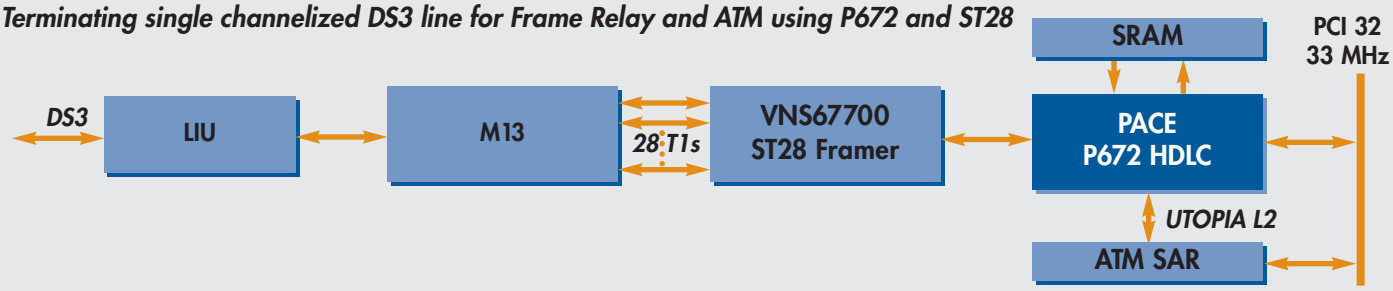
- ATM & Frame Relay Switches
- Universal Access Concentrators
- xDSL Access Multiplexors
- Routers
- Wireless Base Station Controllers

STANDARD

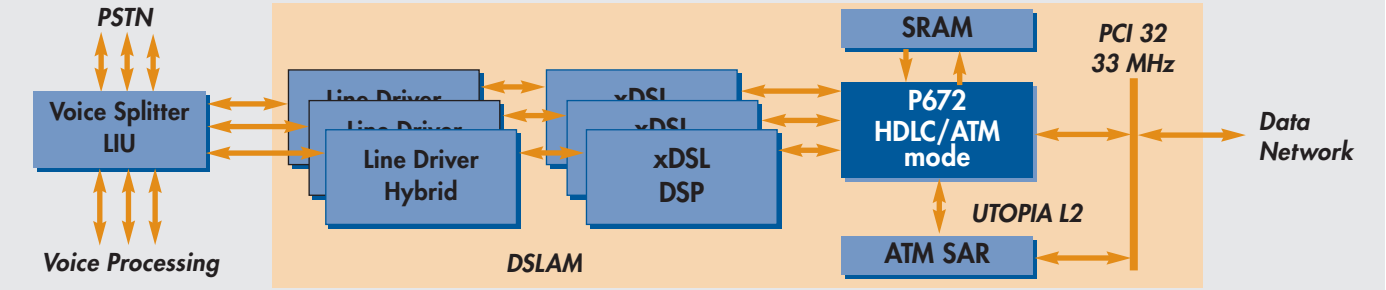
- ATM Forum af-phy-0039 Utopia Level 2, version 1.0, 6/95
- ECTF H.100 Hardware Compatibility Specification: CT Bus revision 1.0
- PCI Local Bus Specification, Rev. 2.1, 6/95
- ITU-T Recommendation Q.921, ISDN User-Network Interface-Data Link Layer Specification, 3/93
- ITU-T Recommendation I.432, B-ISDN User-Network Interface-Physical Layer Specification, 3/93

Application Diagrams

Terminating single channelized DS3 line for Frame Relay and ATM using P672 and ST28



P672 in a DSLAM product



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