VITESSE
SEMICONDUCTOR CORPORATION

Advance Product Information

VSC7211

Gigabit Interconnect Chip

Features

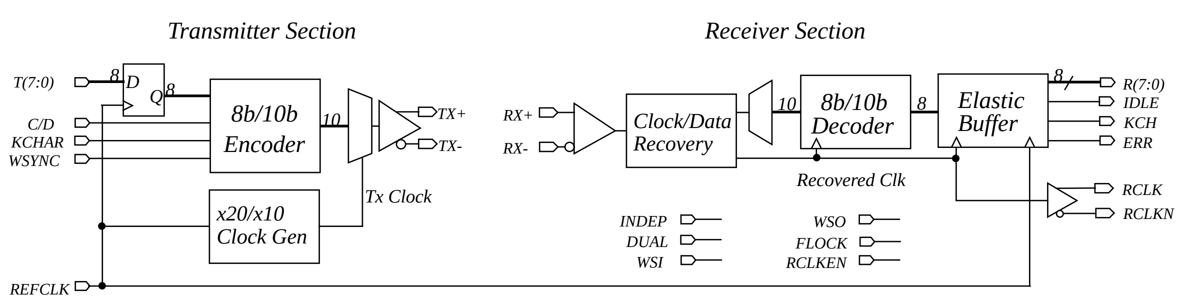
- ANSI X3T11 Compatible Fibre Channel Transceiver
- 8B/10B Encoder/Decoder
- Received Data Aligned to Recovered Clock or REFCLK Input
- Clock Multiplier Generates Baud Rate Clock
- Elastic Buffers in Receiver for Chip-to-Chip Alignment
- Deskewing of +/- 2 Bits Cable Skew at the Receiver Across Multiple Chips
- Compatible with VSC7214
- 1.3 Watts Typical
- 3.3V Power Supply
- 64-Pin Thermally Enhanced PQFP Package

General Description

The VSC7211 is a highly integrated 8-bit parallel-to-serial and serial-to-parallel transceiver chip used for high bandwidth interconnection between busses, backplanes and subsystems over copper cable, fiber optics and printed circuit boards. There are two speed-grades of the VSC7211 available, the -11 and -13. The -11 transceiver provides a typical data transfer rate of 800 Mb/s (8 bits at 100 MHz), while the -13 has a typical data transfer rate of 1000 Mb/s (8 bits at 125 MHz). The VSC7211 contains an 8B/10B encoder, serializer, deserializer, 8B/10B decoder and an elastic buffer which provide the user with a simple interface for transmitting data serially and recovering it correctly on the receive side.

The VSC7211 functions identically to the “A” channel of the VSC7214 so that multiple chips can be used in parallel to implement any number of parallel serial links. This interface is aimed at providing simplicity, ease of use and flexibility for customers transferring data at multi-gigabit speeds.

VSC7211 Block Diagram



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Transmit Interface

Transmitter Data Bus

The VSC7211 bus interface has an 8-bit input byte of transmit data, **T(7:0)** along with a transmit clock (**REFCLK**). **REFCLK** is also used as the reference clock for the on-chip clock multiplying PLL and can be operated at either 1/10 or 1/20 of the serial data rate depending upon the **DUAL** input. When **DUAL** is LOW, **REFCLK** is 1/10th of the baud rate and latches data on the rising edge of **REFCLK**. In this single-edge mode, **REFCLK** should be running between 98MHz and 130MHz (See Figure 4). When **DUAL** is HIGH, the frequency of **REFCLK** should be half of the byte transfer rate, ranging between 49MHz and 65MHz and the clock multiplier generates the internal baud rate clock at 20 times **REFCLK**. (See Figure 5)

Note that **REFCLK** is input to a PLL which generates the actual clock that latches the **T(7:0)** into the VSC7211 and is NOT used to directly latch the data. This is an especially important issue when **DUAL** is HIGH since the falling edge is NOT used. The PLL places the 2x rising edges coincident with the **REFCLK** rising edge and halfway between the **REFCLK** rising edges in this mode.

C/D is provided at the input port to control the transmitted data along with **KCHAR** and **WSYNC** as shown in Table 1. Normally **C/D** is LOW in order to transmit data. If **C/D** is HIGH and **KCHAR** is LOW, then a Fibre Channel defined IDLE Character (K28.5 = ‘0011111010’ or ‘1100000101’ depending on disparity) is transmitted and the data bus is ignored. If **C/D** is HIGH and **KCHAR** is HIGH, a set of Fibre Channel defined special characters are selected by the data bus (see Table 2). If **C/D** and **WSYNC** are HIGH then a special Word Sync Event is transmitted.

Table 1: Transmit Data Controls

WSYNC	*KCHAR*	*C/D*	*Encoded 10-bit Output*
X	0	0	Data Character
0	0	1	Idle Character
X	1	0	Data Character
0	1	1	Special Kxx.x Character
1	X	1	Word Sync Event

8B/10B Encoder

The VSC7211 contains an 8B/10B encoder which translates the 8-bit input data into a 10-bit encoded data character (See Appendix A). When **KCHAR** is LOW and **C/D** signal is HIGH, the encoder ignores **T(7:0)** and generates an **IDLE** character (K28.5). If the **C/D** and **KCHAR** are both HIGH, then **T(7:0)** selects the special data character shown in Table 2. If **T(7:0)** does not contain a value listed in the Table 2 when **C/D** and **KCHAR** are HIGH, then the output of the encoder is undefined. It is the user’s responsibility to provide data on **T(7:0)** when **C/D** and **KCHAR** are HIGH.

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Table 2: Special Characters (Selected when C/D and KCHAR are HIGH)

Code	*T(7:0)*	*Comment*	*Code*	*T(7:0)*	*Comment*
K28.0	000 11100	User Defined	K28.6	110 11100	User Defined
K28.1	001 11100	User Defined	K28.7	111 11100	User Defined
K28.2	010 11100	User Defined	K23.7	111 10111	User Defined
K28.3	011 11100	User Defined	K27.7	111 11011	User Defined
K28.4	100 11100	User Defined	K29.7	111 11101	User Defined
K28.5	101 11100	IDLE	K30.7	111 11110	User Defined

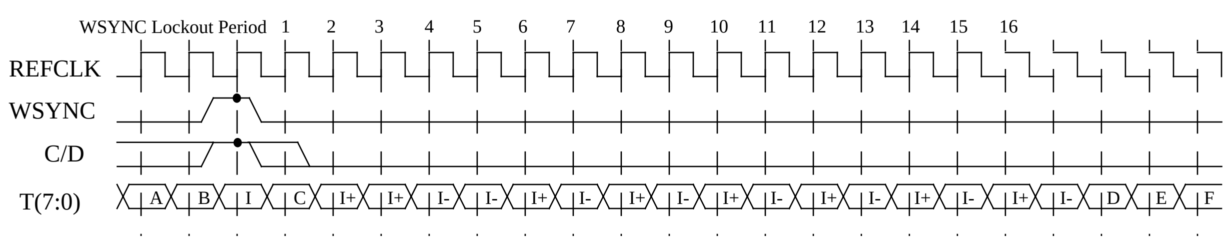
Serializer

The 10-bit output from the encoder is fed into a multiplexer which serializes the parallel data using the synthesized transmit clock. The serial output port (**TX**) consists of a differential PECL output buffer operating at either 10 or 20 times the input clock rate. A loop back control pin, **LBEN**, is provided to internally connect the serial output directly to the serial input on the chip for diagnostics. When **LBEN** is asserted HIGH, the internal loopback path is enabled and the CRU is connected to TX. When **LBEN** is LOW, the internal loopback is disabled and the CRU is connected to RX.

Word_Sync Generation

Due to Word Alignment requirements in the Receiver, the transmitter of the VSC7211 must be capable of generating a Word Synchronization Event (a.k.a WSE). When **WSYNC** and **C/D** are HIGH, the encoder will generate a WSE which is a unique pattern that consists of either 'I+, I+, I-, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-' or 'I-, I-,I+, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+' (where 'I'= K28.5) depending on the current running disparity of data. This pattern is a total of 16 **REFCLK** periods and is recognized by the receiver as a unique pattern which is used for word alignment. After **WSYNC** and **C/D** go HIGH, the transmitter ignores the **WYSNC** input for the next 16 **REFCLKs** in order to insert the WSE into the serial stream as shown in Figure 1 below. **WSYNC** would be recognized if re-asserted at the rising **REFCLK** edge numbered 16 in the diagram, so that the D, E and F characters would become the start of a second Word Sync Event.

Figure 1: Word Sync Event Timing



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Receiver Interface

Clock and Data Recovery

The VSC7211 contains a Clock Recovery Unit (CRU) which accepts the differential serial inputs on the **RX** PECL input (when **LBEN** is LOW), extracts the high-speed clock and retimes the data. If **LBEN** is HIGH, internal transmit data will be connected to the clock recovery inputs and the **RX** pins will be ignored which allows for on-chip loopback diagnostics. The CRU is completely monolithic and requires no external components. It automatically locks on data and if the data is not present, will automatically lock to the **REFCLK**. This maintains a very well behaved recovered clock, **RCLK/RCLKN,** which does not contain any slivers and will operate at a frequency of the **REFCLK** reference +/- 100 ppm. The use of an external Lock-to-Reference pin is not needed.

The Clock Recovery Unit must perform bit synchronization which occurs when the CRU locks onto and properly samples the incoming serial data as described in the previous paragraph. When the CRU is not locked onto the serial data, the 10-bit data out of the decoder is invalid which results in numerous 8B/10B decoding errors or disparity errors. When the link is disturbed (i.e. cable disconnected), then the CRU will require a certain amount of time to lock onto data which is specified in the AC Timing Specification for “Data Acquisition Lock Time”.

Deserializer and Character Alignment

The retimed serial data stream is converted into 10-bit characters by the deserializer which uses a clock generated by dividing down the recovered high-speed clock. A special 7-bit “Comma” pattern (‘0011111xxx’ or ‘1100000xxx’) is recognized by the receiver and allows it to find the 10-bit character boundary. Note that this pattern is found in three special characters, K28.1, K28.5 and K28.7, however, K28.5 is chosen as the unique IDLE character. Only K28.1 and K28.5 are recognized by the receiver as defining the character framing boundary.

Character alignment occurs when the deserializer aligns incoming serial data to the proper location within the 10-bit character. If the receiver identifies four consecutive “Comma” patterns in the incoming data stream which are misaligned to the current framing location, then the receiver will resynchronize the recovered data in order to align the data to the new “Comma” patterns. Resynchronization ensures that the last “Comma” character is output on the internal 10-bit bus so that bits 0 through 9 equal ‘0011111xxx’ or ‘1100000xxx’. If the 4 “Comma” patterns are aligned with the current framing location then resynchronization will not change the current alignment. Resynchronization is always enabled and cannot be turned off. After character resynchronization the VSC7211 ensures that the 8-bit data sent by the transmitting VSC7211 will be recovered by the receiving VSC7211 in the same bit locations (i.e. **T(7:0)** = **R(7:0)**).

10B/8B Decoder

The 10-bit character from the deserializer is decoded in the 10B/8B decoder as described in Appendix A, Table 14 (for Data Characters) and Table 15 (for Special Kxx.x Characters). If the 10-bit character does not match any valid value, then an Out-of-Band Error is generated which is output on the receiver status bus. Similarly, if the running disparity of the character does not match the expected value, a Disparity Error is generated. Appendix A discusses disparity which will not be described in this text.

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Elastic Buffer and Chip-to-Chip Deskewing

An elastic buffer is provided in the receiver in order to align the decoded data to both the selected word clock (i.e. either **RCLK/RCLKN** or **REFCLK**) as well as to the other VSC7211/VSC7214s. The VSC7211 outputs recovered data on **R(7:0)** and status on **ERR**, **IDLE** and **KCH** timed to either the recovered clock (**RCLK/RCLKN**) if **RCLKEN** is HIGH or **REFCLK** if **RCLKEN** is LOW. Since the serial data into the receiver may be generated by a transmitter having slightly different **REFCLK** frequency and/or phase, the elastic buffers are required to provide chip-to-chip alignment. Even if the serial inputs are generated from the same **REFCLK**, differences in routing may introduce phase differences in multiple chip configurations which require deskewing in the elastic buffers.

If **RCLKEN** is HIGH, the recovered clock (**RCLK/RCLKN**) are complementary outputs at 1/10th or 1/20th the baud rate of the incoming data depending upon **DUAL**. If **RCLKEN** is LOW, then **RCLK** is HIGH, **RCLKN** is LOW and the data/status are timed to **REFCLK**. If **DUAL** is HIGH, data at the output port is synchronously clocked out on both positive and negative edges of the selected word clock which should be 1/20th the baud rate. If **DUAL** is LOW, the data is clocked out of the VSC7211 only on the rising edge of the selected word clock which should be 1/10th the baud rate. The term “word clock” will be used for whichever clock, **RCLK/RCLKN** or **REFCLK**, is selected by **RCLKEN**. The timing waveforms of the output data/status are shown in Figures 7 and 8.

The data coming from the decoder is clocked into the elastic buffer by recovered clock from the CRU. The data is clocked out of the elastic buffers with the selected word clock. The recovered clock could have a different phase and frequency than the word clock. If the word clock is the same frequency as the **REFCLK** on the transmitter which provides data to the receiver, then **FLOCK** should be HIGH. If the transmitter is at a different frequency than the word clock, then **FLOCK** must be LOW.

When **FLOCK** is LOW, in order to accommodate the differences between the transmit **REFCLK** and the word clock, elastic buffers are incorporated in the VSC7211 for passing data across the internal recovered clock boundary to the word clock domain. As a result of these frequency differences, it is necessary to insert or delete IDLE characters as the word clock drifts in phase relative to the recovered parallel data stream. It is the users responsibility to ensure that the frequency at which IDLEs are transmitted accommodates the frequency differences in their systems. Not meeting the IDLE density requirements could result in Underrun/Overrun Errors.

The elastic buffer is designed to allow a maximum phase drift of +/-2 serial clock bit times between re-synchronizations, which sets a limit on the maximum data packet length allowed between IDLEs. This maximum packet length depends on the frequency difference between the transmitting and receiving devices' **REFCLKs**. Let ΔT represent phase drift in bit times, and let 2PI represent one full 10-bit character of phase drift. Limiting phase drift to two bit times means the following equation must be met:

(1) $\Delta T <= 0.2 * 2PI$

Let L be the number of 10-bit characters transmitted, and let ΔF be the frequency offset in ppm. The total phase drift in bit times is given by:

(2) $\Delta T = (\Delta F/10^6) * L * 2PI$

A simple expression for maximum packet length as a function of frequency offset is derived by substituting (2) in (1) and solving for L:

(3) $L <= (0.2 * 10^6)/\Delta F$

As an example, if the frequency offset is 200ppm, then the maximum packet length should not be more than 1K Bytes. To increase the maximum packet length (L), decrease the frequency offset (Delta-F). The maximum skew tolerance between the serial inputs of multiple VSC7211/VSC7214 operating in parallel is +/-2 bit times.

Word Alignment

Depending upon the operational mode of the VSC7211, the receiver may also have to perform Word Alignment where data from multiple VSC7211/VSC7214s are considered synchronous. If the data from all the transmitting devices (i.e. the **T(7:0)** busses) is viewed as an Nx8-bit word, then all the receivers should recover the identical word. For example, if a transmit pattern across four chips was ‘ABCD’, ‘EFGH’, ‘IJKL’,... the receivers should recover the same pattern, not a misaligned pattern such as ‘ABGD’, ‘EFKH’, ‘IJXL’...”. Therefore, a Word Sync Event has been defined which helps the receiving VSC7211s to align the multiple chips to a single word clock.

Within the receiver there are elastic buffers to deskew the multiple chips and align them to a common word clock. The buffers allow the chips’ inputs to be skewed up to +/-2 bit times in order to accommodate circuit imperfections, differences in transmission delay and jitter/wander. This allows easy implementation of robust systems.

In order to perform Word Alignment, a Word Sync Event must be seen across all chips within the +/-2 bit time window. As a model for understanding, consider the case where four VSC7211 transmitters send 32-bits of data to the receivers via copper media which has small cable length differences causing a chip-to-chip skew of less than +/- 2 ns. On the transmitting VSC7211s, when **WSYNC** goes LOW, a special pattern, called the Word Sync Event, will be transmitted on all chips simultaneously. This pattern will consist of either I+, I+, I-, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I- or I-, I-,I+, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+ (where” I” = K28.5) depending on the current running disparity of data. This pattern is a total of 16 **REFCLK** periods and is recognized by the receivers as a unique pattern used for word realignment. Upon recognition of this pattern, the receivers will reposition their recovered data within the elastic buffers in order to align all chips and remove any chip-to-chip skew. This ensures that each transmitted Nx8-bit word is recovered correctly.

Receiver State Machine

Each receiver contains a Loss of Synchronization State Machine (LSSM) which is responsible for detecting and handling loss of bit, channel, word and word clock synchronization in a controlled manner. There are three states in the LSSM: LOSS_OF_SYNC, RESYNC and SYNC_ACQUIRED as shown in the state diagram of Fig.2. The RESYNC state is entered when four consecutive 10-bit words have been received which contain the 7-bit Comma character (e.g. four consecutive K28.5 IDLE characters). After entering the RESYNC state, the VSC7211 will stay in it until a valid, non-comma transmission is received, then it transitions to the SYNC_ACQUIRED state indicating a normal operating condition. The LOSS_OF_SYNC state is entered whenever four consecutive invalid transmissions have been detected or when the occurrences of invalid transmission outnumber valid transmissions by four. The VSC7211 receiver will stay in the LOSS_OF_SYNC state until four continuous IDLE characters are received and then go into RESYNC state.

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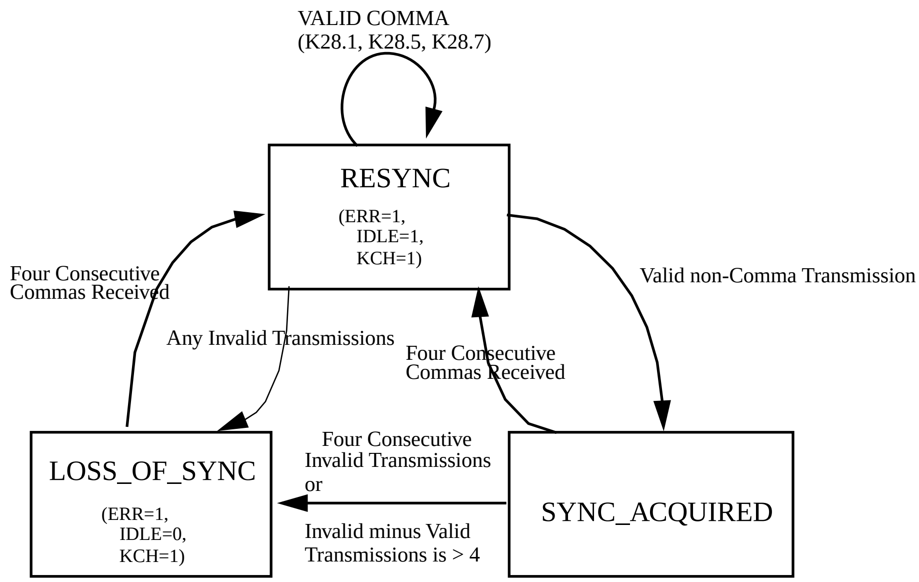
Figure 2: State Diagram of the Loss of Synchronization State Machine.



Link Status Outputs

On the receiver output bus, the **ERR**, **KCH** and **IDLE** form status for the receiver as shown below. Since this status is encoded, multiple conditions could occur simultaneously so the states are prioritized as indicated (1 being highest priority). For example, if both Out-of-Band and Disparity Errors occur, only an Out-of-Band Error is reported because it has higher priority

Table 3: Link Status Outputs

ERR	*KCHn*	*IDLEn*	*Priority*	*Link Status*
0	0	0	7	**Valid Data Transmission:** A valid data character with correct disparity was received. The correctly decoded version of this character, per Appendix A, is on **R(7:0).**
0	0	1	1	**Underun/Overun Error:** The elastic buffer has not been able to add/drop an IDLE when required. Data on **R(7:0)** is invalid.
0	1	0	6	**Kxx.x Special Character Detected (not IDLE):** A valid 8B/10B special character with correct disparity was received. The correctly decoded version of this character, per Table 2, is on **R(7:0).**
0	1	1	5	**IDLE Detected:** A valid IDLE character(K28.5) with correct disparity was received. The correctly decoded version of this character, per Table 2, is on **R(7:0).**
1	0	0	3	**Out-of-band Error Detected**: A character was received which was not a valid 8B/10B data character as defined in Appendix A or a special character as defined in Table 2. Data on **R(7:0)** is invalid.
1	0	1	4	**Disparity Error Detected:** A character was received which did not have the expected disparity as defined in Appendix A. **R(7:0)** is invalid.
1	1	0	2	**Loss of Synchronization:** The receiver state machine is in the Loss-of-Sync State. Data on **R(7:0)** is invalid.
1	1	1	2	**RESYNC:** The receiver state machine is in the Resynchronization state. Data on **R(7:0)** is a decoded version of K28.1, K28.5 or K28.7.

Special Considerations:

For a receiver to be fully initialized, the character framing boundary must be defined and the elastic buffer must be centered. Data received prior to receiver initialization may not be recovered correctly. It is the user's responsibility to ensure that the receiver is properly aligned prior to sending user data. As previously described, four consecutive Commas (K28.1 or K28.5) establish the framing boundary. The elastic buffer is always re-centered when a Word Sync Event is received. Four consecutive Commas will also re-center the elastic buffer, but only if they either produce a change in the framing boundary or if they are the first four-Comma sequence after a change in the LBEN input. When the LBEN input is changed, sufficient time must be allowed for the Clock Recovery Unit to lock onto RX data before attempting to define a new framing boundary with four consecutive Commas. Refer to the data acquisition lock time specification in Table 9.

The Word Sync Event may be received while **LBEN** is HIGH so that the receiver of the VSC7211 requiring initialization may perform it through its own transmitter. This method of initialization does not work effectively if INDEP is LOW and chip-to-chip alignment is required. In this case, the Word Sync Event is used to deskew all of the chips and must come from the actual transmitters.

The VSC7211 has been carefully designed so that "realignment" of properly aligned data will not result in corruption of data. However, if character alignment or word alignment takes place in which the relationship of the incoming serial data to the output parallel data is changed, then the potential exists for the data prior to the synchronization event to be corrupted or duplicated. This is acceptable because the misaligned data represents an error condition where data is not valid anyway.

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Using Multiple VSC7211s in Parallel

Multiple VSC7211s can be used in parallel to form wider bus widths. This is accomplished by supplying all "transmitting" VSC7211s with the same **REFCLK** so that all output data is synchronous. On the receive side, all VSC7211s would be supplied with the same **REFCLK** (although it may be different than the REFCLK on the transmitters) and all **RCLKENs** set LOW. This will force the recovered data to be output from all the chips at the same clock edge. This allows proper channel-to-channel alignment across chip boundaries. The Word Sync Output (**WSO**) and Word Sync Input (**WSI**) are added to accomplish synchronization between multiple receivers.

In this case, IDLEs will have to be added to or dropped from all the chips at the same time. In order to implement this, one receiving VSC7211 is arbitrarily chosen as the "Master" and its **WSO** output is driven to the **WSI** inputs of all the VSC7211s in the receiver, including itself. **WSO** is asserted prior to the VSC7211 adding/dropping IDLEs so all the VSC7211s will operate simultaneously. **WSO** uses a simple 3-bit serial protocol, synchronous to **REFCLK**, for indicating to other VSC7211s the required action. '000' indicates no action is required. '101' indicates that the "Master" receiver has seen a Word Sync Event. The relative timing relationship between seeing a Word Sync Event and seeing '101' on the WSI in the other channels allows these channels to word-synchronize with the "Master" receiver. '110' indicates that the next IDLE encountered in the receive data stream should be deleted. '111' indicates that an IDLE should be inserted after the next IDLE encountered in the receive data stream. Note that the arbitrarily chosen "Master" must always be an active channel. When using many VSC7211s in parallel, loading on WSO may force the use of a buffer in order to resynchronize **WSO** to **REFCLK**. This should be accomplished by delaying every **WSI** input to another device by three **REFCLKs** in external circuitry.

When not using multiple VSC7211s in parallel, tie **INDEP** HIGH and **WSI** LOW.

Modes of Operation:

The **RCLKEN**, **FLOCK**, **INDEP**, **LBEN** and **DUAL** pins completely configure the VSC7211. **LBEN** and **DUAL** have been explained previously. However, the interaction of the other three pins requires some explanation. A brief description of these mode pins is below with detail multi-chip applications examples of each mode after that.

Table 4: Summary of Mode Input pin function

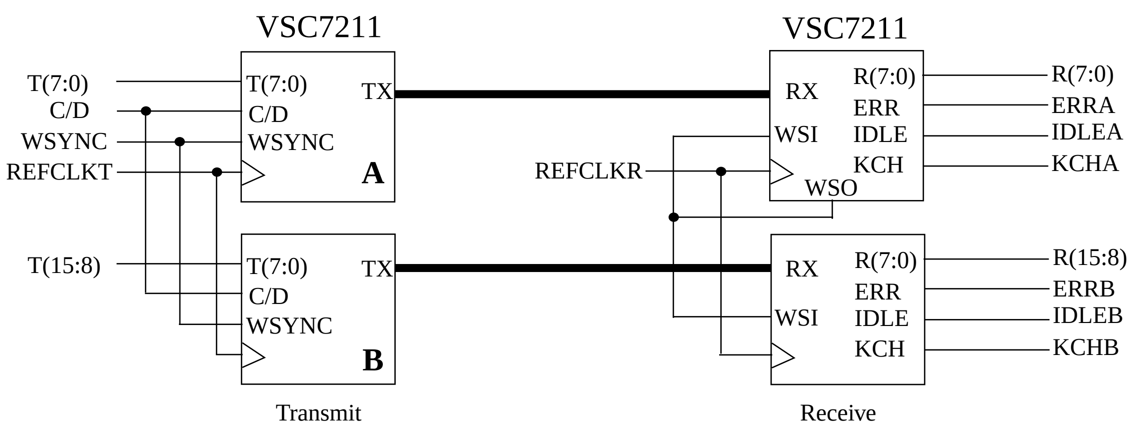
MODE PIN	*HIGH*	*LOW*
FLOCK	The transmitter generating serial data to the receiver is at the same frequency as the selected word clock. IDLE insertion/ deletion is disabled.	The transmitter generating serial data to the receiver is not at the same frequency as the selected word clock. IDLE insertion / deletion is enabled.
RCLKEN	**R(7:0)** is synchronous to **RCLK /RCLKN**	**R(7:0)** is synchronous to **REFCLK**
INDEP	Single chip mode where Word alignment is not enabled.	Multiple chip configuration where chip-to-chip Word alignment is enabled. IDLE insertion/deletion occurs on all chips at the same time if enabled by **FLOCK=LOW**.

COMMON MODES OF MULTIPLE CHIP OPERATION:

RCLKEN**=LOW,** FLOCK**=LOW,** INDEP**=LOW:**

This is a common multiple chip application where a group of VSC7211/VSC7214s in one system communicates with multiple chips in another system over copper cable or fiber optics (See Figure 3). This could be viewed as a remote Nx8-bit bus extender. Multiple receivers can be used in parallel because the receivers' output busses are synchronous to a common **REFCLK**. The transmitters' **REFCLKs** and the receivers' **REFCLKs** are at potentially different frequencies. Word Alignment is enabled because all chips are considered related. The "Master" receiver must be active since it is the source for all chip-to-chip alignments. IDLEs must be transmitted on all chips simultaneously so the **C/D** inputs could be connected together. An IDLE on a single chip is not allowed. Consequently, only one of the **IDLE** receiver output is necessary for determining when all N chips contain IDLEs. IDLEs must be inserted periodically in the transmit data stream to ensure proper insertion/deletion of IDLEs to accommodate the differences in **REFCLK**s between the transmitting chips and receiving chips. The "Master" receiver's **WSO** output is connected to all the other VSC7211/VSC7214s' **WSI**s. Simultaneous Word Sync Events from the transmitters will initialize the receivers and establish chip-to-chip alignment. After this, IDLEs are added/dropped by all the receivers at the same time.

Figure 3: Mode 0: 2x8-bit Bus Extender (Remote)



RCLKEN=LOW, FLOCK=HIGH, INDEP=LOW:

This is the same as the previous example (see Figure 3) except REFCLKT=REFCLKR. This is a common application where a VSC7211 in one board communicates with another board over a backplane and a common clock source supplies REFCLKs to all VSC7211s. Because the transmit and receive clocks are at the same frequency, IDLEs are not inserted or dropped. Because the receive data is synchronized to REFCLK, this is a multiple chip application. Word Alignment is needed to keep the receive data from each VSC7211 to be grouped together into an Nx8-bit Word. A Word Sync Event must be received by all chips prior to transmitting user data but is not needed otherwise. **WSI** should be connected to **WSO**. Since the system is frequency locked, IDLEs will not be added/dropped so IDLEs may be transmitted on each channel without regard to activity on other channels or IDLE density requirements.

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AC Characteristics

Figure 4: Transmit Timing Waveforms with DUAL = 0

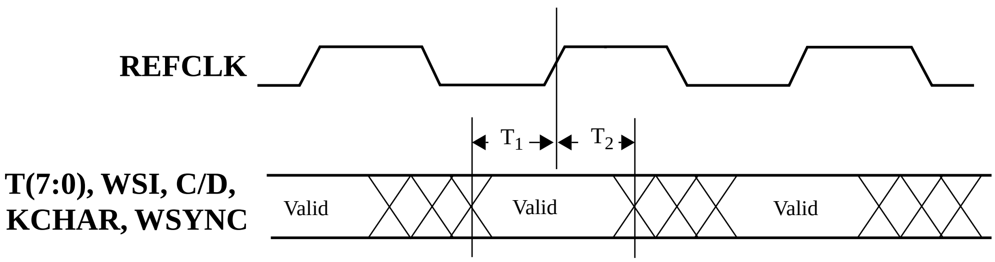

Table 5: Transmit AC Characteristics (with DUAL = 0)

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Input setup time to the rising edge of **REFCLK**	1.5	—	ns.	Measured between the valid data level of the input and the 1.4V point of **REFCLK**
T_2	Input hold time after the rising edge of **REFCLK**	1.0	—	ns.	

Figure 5: Transmit Timing Waveforms with DUAL = 1

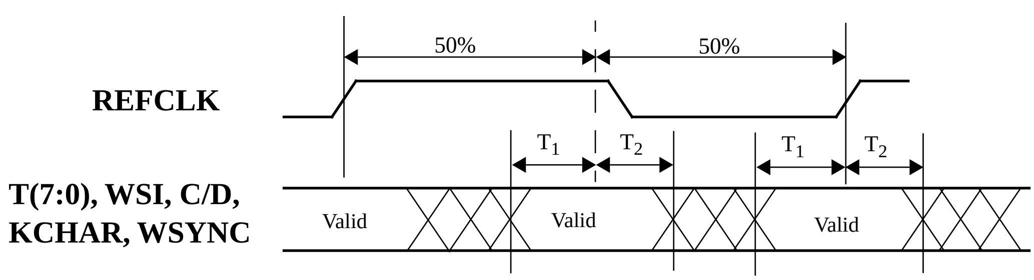

Table 6: Transmit AC Characteristics (with DUAL = 1)

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Input setup time to the rising edge of **REFCLK** or the midpoint between rising edges.	1.5	—	ns.	Measured between the valid data level of the input and the 1.4V point of **REFCLK**
T_2	Input hold time after the rising edge of **REFCLK** or the midpoint between rising edges	1.0	—	ns.	

Figure 6: Serial Transmit Timing Waveforms

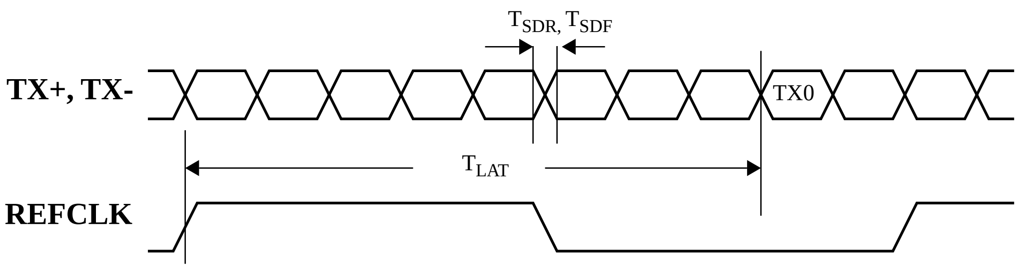

Table 7: Transmit AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{SDR}, T_{SDF}	**TX+/-** rise and fall time	—	330	ps.	Measured between 20% to 80% of the valid data level
T_{LAT}	Latency from the rising edge of **REFCLK** to **TX**	20bc-0.6ns	20bc-0.1	ns.	bc = Bit clocks

Figure 7: Receive Timing Waveforms With DUAL = 0

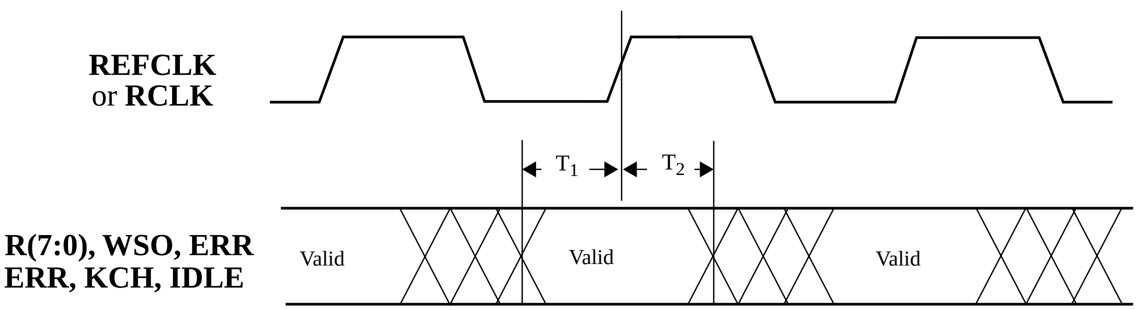

Table 8: Receive AC Characteristics

<table>
<tr><th>Parameters</th><th>Description</th><th>Min</th><th>Max</th><th>Units</th><th colspan="2">Conditions</th></tr>
<tr><td rowspan="2">T_1</td><td rowspan="2">Output valid time before the rising edge of REFCLK or RCLK</td><td>5.0</td><td>—</td><td>ns.</td><td>At 100MHz</td><td rowspan="4">Measured between the valid data level of the outputs and the 1.4V point of REFCLK or RCLK (10pF Load)</td></tr>
<tr><td>3.0</td><td>—</td><td>ns.</td><td>At 130MHz</td></tr>
<tr><td>T_2</td><td>Output valid time after the rising edge of REFCLK (RCLKEN=0)</td><td>1.0</td><td>—</td><td>ns.</td><td rowspan="2"></td></tr>
<tr><td>T_2</td><td>Output valid time after the rising edge of RCLK (RCLKEN=1)</td><td>2.0</td><td>—</td><td>ns.</td></tr>
</table>

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Figure 8: Receiver Timing Waveforms with DUAL = 1

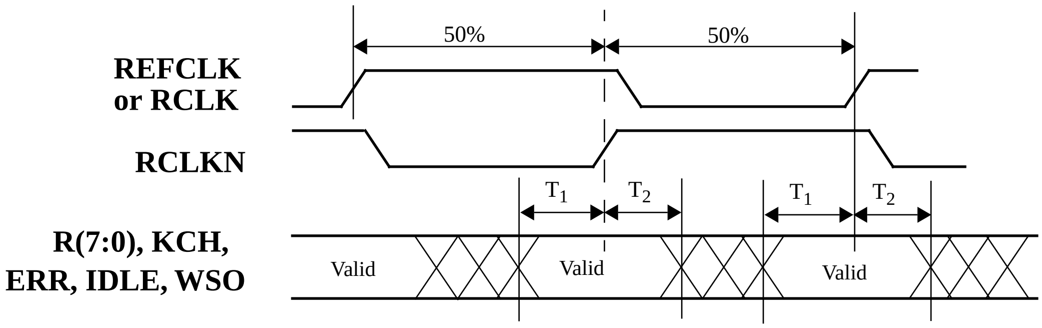

Table 9: Receiver AC Characteristics

Parameter	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	Outputs valid prior to **RCLK/RCLKN** or **REFCLK** rise	3.0	—	ns.	Measured between the 1.4V point of **REFCLK, RCLK** or **RCLKN** and a valid level of the outputs. All outputs driving 10pF load.
T_2	Outputs valid after **RCLK** or **RCLKN** rise (**RCLKEN**=HIGH)	2.0	—	ns.	
T_2	Outputs valid after the rising edge of **REFCLK** or the midpoint between the rising edges (**RCLKEN**=LOW)	1.0	—	ns.	
T_3	Deviation of the rising edge of **RCLK** to the rising edge of **RCLKN** from nominal.	-500	500	ps.	Nominal delay is 10 bit times.
T_4	Deviation of **RCLK/ RCLKN** period from **REFCLK** period	-1.0	1.0	%	Whether or not locked to serial data
T_r, T_f	Output rise and fall time	—	2.4	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$, into 10 pf. load.
R_{lat}	Latency from **RX+/-** to **R(7:0)**	33bc+5.7ns	84bc+7.4ns	ns	bc = Bit clock periods ns = Nano second
T_{lock}	Data acquisition lock time	—	2500	bc	8B/10B IDLE pattern. Tested on a sample basis

Figure 9: REFCLK Timing Waveforms

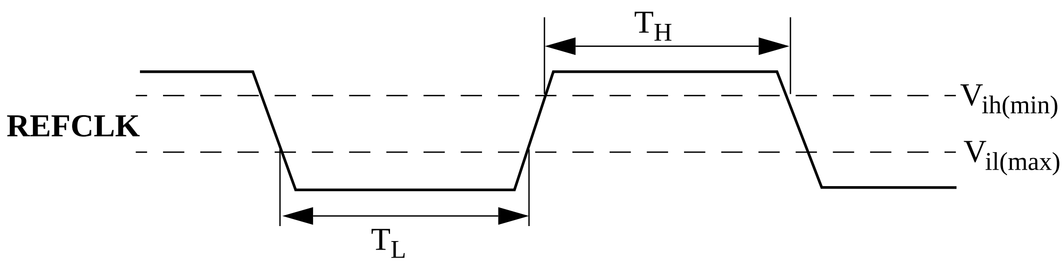

Table 10: Reference Clock Requirements

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR-11	Frequency Range (for -11 part)	98	110	MHz	**DUAL** = 0
		49	55	MHz	**DUAL** = 1
FR-13	Frequency Range (for -13 part)	120	130	MHz	**DUAL** = 0
		60	65	MHz	**DUAL** = 1
FO	Frequency Offset	-200	200	ppm.	Mean frequency offset between **REFCLK** (Tx) and **REFCLK** (Rx)
DC	**REFCLK** duty cycle	35	65	%	Measured at 1.5V
T_H,T_L	**REFLCK** pulse width	3	—	ns.	
T_{RCR},T_{RCF}	**REFCLK** rise and fall time	—	1.0	ns.	Between $V_{il(max)}$ and $V_{ih(min)}$

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DC Characteristics

Parameters	Description	Min.	Typ	Max.	Units	Conditions
V_{OH}	TTL output HIGH voltage	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	TTL output LOW voltage	—	—	0.5	V	I_{OL} = +1.0mA
V_{IH}	TTL input HIGH voltage	2.0	—	—	V	
V_{IL}	TTL input LOW voltage	0	—	0.8	V	
I_{IH}	TTL input HIGH current	—	50	500	µA	V_{IN} =2.4V
I_{IL}	TTL input LOW current	—	—	-500	µA	V_{IN} =0.5V
ΔV_{OUT}	Differential Output Swing. (| TX+ - TX- |)	500	—	1100	mV	50Ω to V_{DD} - 2.0V
ΔV_{IN}	Differential Input Swing. (| RX+ - RX- |)	200	—	1600	mV	
V_{DD}	Power supply voltage	3.14	—	3.47	V	3.3V ± 5%
P_D	Power dissipation	—	1.5	1.8	W	Outputs open
I_{DD}	Supply current	—	450	520	mA	Outputs open

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD})..0.5V to +4V
PECL DC Input Voltage, (V_{INP})..-0.5V to V_{DD} +0.5V
TTL DC Input Voltage, (V_{INT})..-0.5V to 5.5V
DC Voltage Applied to Outputs for High Output State ....-0.5V to V_{DD} + 0.5V
TTL Output Current (I_{OUT}), (DC, Output High)..50mA
PECL Output Current, (I_{OUT}), (DC, Output High) ....-50mA
Case Temperature Under Bias, (T_C)..-55^o to +125^{o}C
Storage Temperature, (T_{STG})..-65^{o}C to +150^{o}C

Recommended Operating Conditions

Power Supply Voltage, (V_{DD})..+3.3V±5%
Operating Temperature Range, ...0^{o}C Ambient to +90^{o}C Case

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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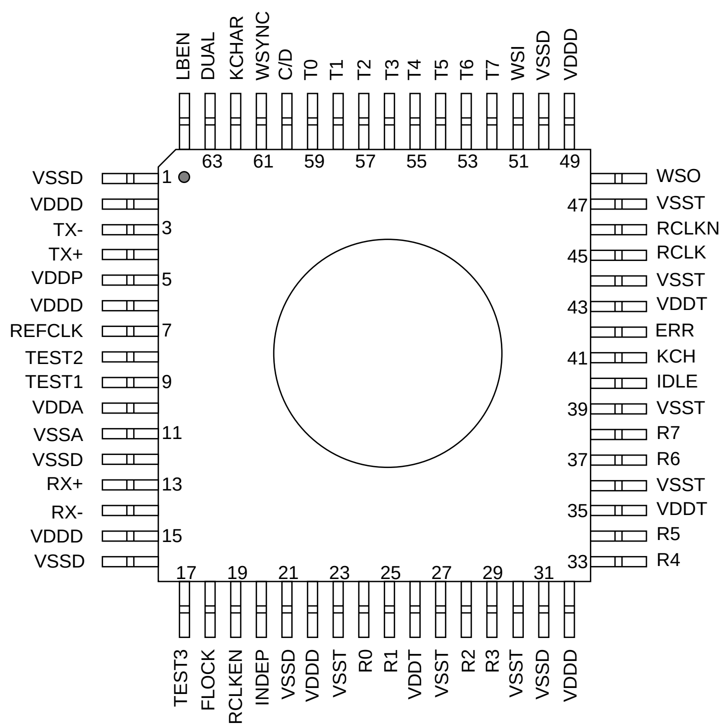
Package Pin Descriptions

Figure 10: Pin Diagram



(Top View)
Exposed Heat Sink is not electrically connected.

Table 11: Pin Identification

Pin#	*Name*	*Description*
52,53,54,55, 56,57,58,59	**T(7:0)**	INPUT - TTL: Transmit data synchronous to **REFCLK** to be encoded and serialized onto **TX**.
60	**C/D**	INPUT - TTL: Command/Data. If **KCHAR**=**C/D**=LOW, then **T(7:0)** is used to generate transmit data. If **KCHAR**=**C/D**=HIGH then Special Kxx.x Characters are transmitted based upon the value of **T(7:0)**. If **KCHAR**=LOW and **C/D**=HIGH, IDLE characters are transmitted.
62	**KCHAR**	INPUT - TTL: Special Kxx.x CHARacter enable. If **KCHAR**=**C/D**=LOW, then **T(7:0)** is used to generate transmit data. If **KCHAR**=**C/D**=HIGH then Special Kxx.x Characters are transmitted based upon the value of **T(7:0)**. If **KCHAR**=LOW and **C/D**=HIGH, IDLE characters are transmitted.
61	**WSYNC**	INPUT - TTL: Word SYNC enable. When **WSYNC** and **C/D** are HIGH, the transmitter will send the Word Sync Event.

Pin#	*Name*	*Description*
4, 3	**TX+, TX-**	OUTPUT - Differential. These pins output the serialized transmit data. (AC coupling is recommended.)
38,37,34,33, 29,28,25,24	**R(7:0)**	OUTPUT - TTL: **R**eceive data synchronous to **RCLK/RCLKN** if **RCLKEN**=HIGH or **REFCLK** if **RCLKEN**=LOW.
40	**IDLE**	OUTPUT - TTL: **IDLE** detect. When HIGH, an IDLE character has been detected by the decoder and is on **R(7:0).**
41	**KCH**	OUTPUT - TTL: **K**xx.x **CH**aracter detect. When HIGH, a special Kxx.x character has been detected by the decoder and is on **R(7:0)**
42	**ERR**	OUTPUT - TTL: **ERR**or detect. When HIGH, an invalid 10-bit character or a disparity error has been detected so the data on **R(7:0)** is invalid.
13, 14	**RX+, RX-**	INPUT - Differential: These pins receive the serialized input data when **LBEN** is LOW. They are internally biased at VDD/2 with internal resistors. When **LBEN** is HIGH, these inputs are ignored. (AC coupling is recommended.)
45, 46	**RCLK, RCLKN**	OUTPUT - TTL: **R**ecovered **CL**oc**K** outputs. If **RCLKEN** is HIGH, the recovered data on **R(7:0)** is synchronous to the recovered clock, **RCLK/RCLKN**. When LOW, recovered data is synchronous to **REFCLK**, **RCLK** is HIGH and **RCLKN** is LOW.
7	**REFCLK**	INPUT - TTL: **REF**erence **CL**oc**K** is used to latch the transmit data and serves as the reference for the clock multiplier PLL at either 1/10th (DUAL=LOW) or 1/20th (DUAL=HIGH) of the serial baud rate. It is also used to synchronize **R(7:0)** when **RCLKEN** is LOW.
64	**LBEN**	INPUT - TTL: **L**oop **B**ack **EN**able. When asserted HIGH, an internal version of **TX** is connected to the CRU and **RX** is ignored. When LOW, **RX** is connected to the CRU. A change in the state of **LBEN** ensures that the next four-Comma sequence will re-center the elastic buffer.
19	**RCLKEN**	INPUT - TTL: **RCLK** **EN**able. When HIGH, the recovered data on **R(7:0)** is synchronous to the recovered clock, **RCLK/RCLKN**. When LOW, recovered data is synchronous to **REFCLK**, **RCLK** is HIGH and **RCLKN** is LOW.
20	**INDEP**	INPUT - TTL: **INDEP**endent Receiver Mode. When HIGH, the receiver is considered independent of any other VSC7211/VSC7214s so word alignment is disabled. When LOW, all VSC7211/VSC7214s receiver channels are considered synchronous and chip-to-chip alignment is enabled.
63	**DUAL**	INPUT - TTL: **DUAL** clock Mode. When LOW, **REFCLK** is 1/10th the baud rate and **T(7:0)** is latched on the rising edges of **REFCLK**. When HIGH, **REFCLK** is 1/20th the baud rate and **T(7:0)** is latched on both the rising edge of **REFCLK** and halfway between rising edges.
18	**FLOCK**	INPUT - TTL: **F**requency **LOCK**ed Mode. When HIGH, the transmitter generating serial data on **RX** operates at the same frequency as **REFCLK** so IDLEs should not be inserted or deleted. When LOW, the two ends of the link are not frequency locked so IDLEs must be inserted and deleted.
51	**WSI**	INPUT - TTL: **W**ord **S**ync **I**nput. When using multiple VSC7211/VSC7214s in parallel, **WSI** informs other chips when to Insert/Drop IDLEs. When using a single VSC7211, tie **WSI** to **WSO**.
48	**WSO**	OUTPUT - TTL: **W**ord **S**ync **O**utput. When using multiple VSC7211/VSC7214s in parallel, **WSO** indicates when another chip will Insert or Drop IDLEs at the next opportunity. When using a single VSC7211, tie **WSI** to **WSO**.

Pin#	Name	Description
9, 8, 17	**TEST1** **TEST2** **TEST3**	INPUT - TTL: Factory **TEST** inputs. For normal use these should be HIGH.
10	**VDDA**	Analog power supply to the PLL.
11	**VSSA**	Analog Ground to the PLL.
5	**VDDP**	PECL I/O power supply.
2,6,15,22, 32,49	**VDDD**	Digital Power Supply.
1,12,16, 21,31,50	**VSSD**	Digital Ground
26,35,43	**VDDT**	TTL Output Power Supply
23,27,30,36, 39,44,47	**VSST**	TTL Output Ground

NOTE: VSS, VSST and VSSA should be connected to a common ground plane.

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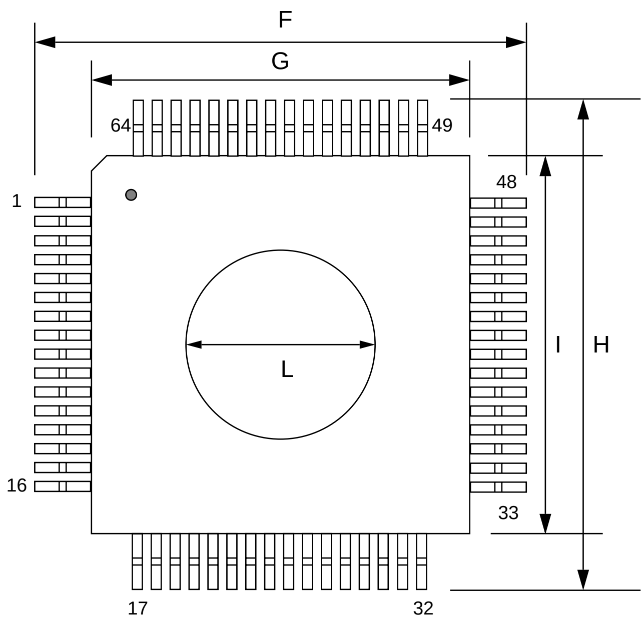
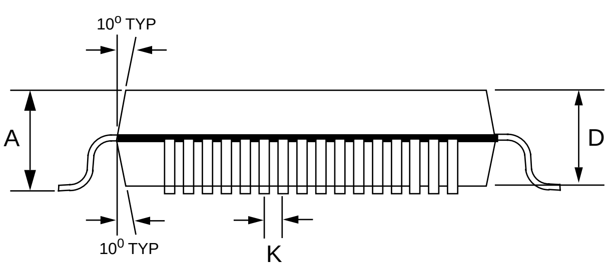
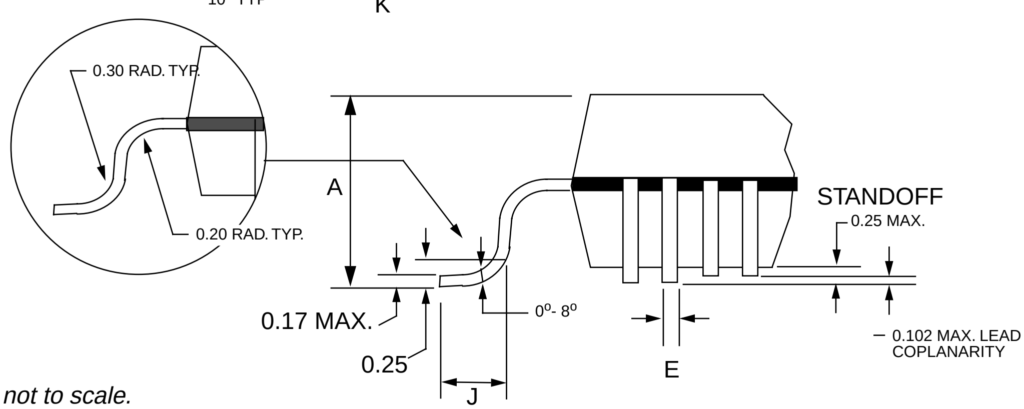
Package Information

64-Pin Thermally Enhanced PQFP



Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+0.10
E	0.30	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	±.15
K	0.50	BASIC
L	3.56	±.50 DIA.





NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.
Heat spreader is not electrically connected.

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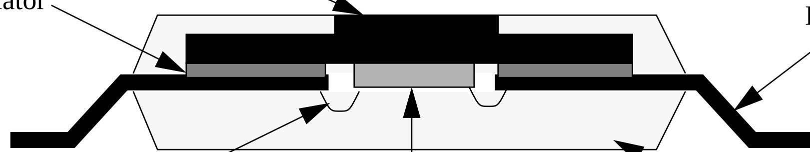
Package Thermal Characteristics

The VSC7211 is packaged into a thermally-enhanced plastic quad flatpack (PQFP). This package adheres to the industry-standard EIAJ footprint for a 10x10mm body but has been enhanced to improve thermal dissipation with the inclusion of an exposed Copper Heat Spreader. The package construction is as shown in Figure 11.

Figure 11: Package Cross Section



The thermal resistance for the VSC7211 package is improved through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the lead frame through the heat spreader overlap of the lead frame.

Table 12: 64-Pin PQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	2.5	$^oC/W$
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads for a non-thermally saturated board.	37	$^oC/W$
θ_{ca-100}	Thermal resistance from case to ambient in 100 LPFM air	31	$^oC/W$
θ_{ca-200}	Thermal resistance from case to ambient in 200 LPFM air	28	$^oC/W$
θ_{ca-400}	Thermal resistance from case to ambient in 400 LPFM air	24	$^oC/W$
θ_{ca-600}	Thermal resistance from case to ambient in 600 LPFM air	22	$^oC/W$

The VSC7211 is designed to operate at a maximum case temperature of up to 90 ^oC. The user must guarantee that the maximum case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC7211 in still air if the ambient temperature does not exceed 24^oC (24^oC = 90^oC - 1.8W * 37$^oC/W$). If operation above these ambient temperatures is required, then an appropriate heatsink must be used with the part or adequate airflow must be provided.

Ordering Information

The part number for this product is formed by a combination of the device number and package type as shown below:

VSC7211 QP -xx

Device Type
VSC7211: Backplane Interface Chip

Package Type
QP: 64-Pin Thermally Enhanced PQFP, 10mm Body

Speed Grade
-11: 980-1100 MHz, -13: 1200 to 1300 MHz

Revision History

1.0 Initial Release

1.1

1.2 Modified IDLE density requirements to be consistent with VSC7214. Changed Vout to a minimum of 500mV. Rewrote "Special Considerations" section on p8.

Notice

This document contains information about a product during its fabrication or early sampling phase of development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

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Appendix A: 8B/10B Codes

The VSC7211 provides Fibre Channel specified 8B/10B encoding and decoding with running disparity which bounds the run length of the code and maintains DC balance. This improves the quality of the transmitted data, which makes clock recovery possible at the receiver.

Fibre Channel nomenclature refers to encoded bytes as “transmission characters.” The Fibre Channel Standard specifies two kinds of bytes: data bytes and special bytes. Each valid transmission character is given a name using the convention Zxx.x, where Z is the control variable of the unencoded byte. If the byte is a data byte the control character is a “D”. If the byte is a special byte the control character is a “K.” The **C/D** input provides indicates whether the transmission word is Data (LOW) or a Special Character (HIGH).

The VSC7211 accepts the FC-1, unencoded bit notation as specified below, with H being the most significant bit in a byte.

H G F E D C B A   Z

The 8B/10B encoding acts on three bit and five bit sub-blocks respectively as grouped below:

H G F   E D C B A

The valid data character name is an annotation of the control character (D or K), plus the decimal value of the second sub-block (EDCBA), plus a decimal point (“.”), and the decimal value of the first sub-block (HGF). Refer to the example below:

H G F	E D C B A	FC-1 Notation
1 0 1	1 1 1 0 0	FC-1 Value
5	28	Decimal Value
K28.5		Character Name

The 8B/10B encoding adds two additional bits to the transmission character. Bit “i” is added to the five bit sub-block and bit “j” is added to the three bit sub-block. The 8 bit, FC-1 notation expands to the 10 bit encoded notation as shown below:

J H G F   I E D C B A

There are two encoded characters for each transmission character. One is for a negative beginning disparity and one is for a positive beginning disparity. Positive disparity refers to more “ones” than “zeros” in the previously transmitted sub-block. Running disparity is calculated per sub-block rather than per character. The use of two encoded transmission characters results in a DC balanced transmission, in which an equal number of zeros and ones are transmitted. Some sub-blocks are disparity neutral, which means that the sub-block contains an equal number of ones and zeros. Disparity neutral sub-blocks cause no changes in current running disparity. The transmitter encodes the input and selects between the two possible 10-bit patterns based upon the current running disparity.

Each transmission character has four representations - character name, unencoded binary representation (FC-1 value), encoded negative running disparity representation, and encoded positive disparity representation. The following table shows all the valid data character values defined by the Fibre Channel Standard. The table after the data characters shows the valid special characters.

The bits are transmitted serially with bit "A" first followed in order by bits "B," "C," "D," "E," "I," "F," "G," "H," and "J."

Table 13: Valid Data Characters

Data Byte Name	*Bits HGF EDCBA*	*Current RD- abcdei fghj*	*Current RD+ abcdei fghj*	*Data Byte Name*	*Bits HGF EDCBA*	*Current RD- abcdei fghj*	*Current RD+ abcdei fghj*
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001

Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010

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Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000

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Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 14: Valid Special Characters

Special Code Name	Current RD- abcdei fghj	Current RD+ abcdei fghj	T(7:0)	Special Code Name	Current RD- abcdei fghj	Current RD+ abcdei fghj	T(7:0)
K28.0	001111 0100	110000 1011	000 11100	K28.6	001111 0110	110000 1001	110 11100
K28.1	001111 1001	110000 0110	001 11100	K28.7	001111 1000	110000 0111	111 11100
K28.2	001111 0101	110000 1010	010 11100	K23.7	111010 1000	000101 0111	111 10111
K28.3	001111 0011	110000 1100	011 11100	K27.7	110110 1000	001001 0111	111 11011
K28.4	001111 0010	110000 1101	100 11100	K29.7	101110 1000	010001 0111	111 11101
K28.5	001111 1010	110000 0101	101 11100	K30.7	011110 1000	100001 0111	111 11110

**Reserved – Valid transmission characters which are not defined for use by the Fibre Channel standard.*

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