Framers and Mappers

Features:

System / Packet Interface

- 32-bit Industry Compliant POS-PHY-3, Single-PHY Packet Interface
- 32-bit Industry Compliant UTOPIA-3, Single-PHY Cell Interface

Physical Layer Channelization Support

- STS-48c / STM-16c

Payload Processing

- Transparent Mode - Direct SPE Mapping
- ATM Cell Processing
- Programmable HDLC / PPP Encapsulation

SONET / SDH Processing

- Full Section, Line, and Path Termination and Generation
- Performance Monitoring and Reporting
- Enhanced Bit Error Rate Monitoring
- Section and Path Trace Buffers
- Full Overhead Insertion and Extraction and Status Monitoring Through Dedicated Access Ports

General Description

The VSC9142 is a dual mode SONET/SDH to Packet/ATM framing device that integrates the physical layer components of 2.5 Gbps clock and data recovery and serialization/deserialization into a single device. In the Packet over SONET (POS) mode, this device can be used in equipment interconnecting IP/PPP/HDLC data over public or private SONET/SDH networks. Similarly, in the ATM over SONET (ATM) mode, this device can be used in equipment interconnecting ATM switches. In addition, the VSC9142 can be used in various applications involving LAPS (X.85/Y.1321) and Ethernet over SONET/SDH protocols.

Features of the VSC9142 include: Full insertion/extraction of the transport overhead, bit error rate and extensive SONET/packet/cell performance monitoring, packet/cell filtering and discarding functionalities, transmit and receive, JTAG TAP controller, and an 8-bit CPU interface with 8 general purpose I/O ports.

The high-speed component provides data and clock in the transmit direction, and selectable reference clock frequencies and sources for both the transmit and receive directions. The VSC9142 can facilitate both internal and external looptiming applications and also provides a 4-bit LVDS interface in both transmit and receive direction for use in STS-192 applications. When using the 4-bit interface, the serializing/deserializing blocks of the VSC9142 can be shut down for power savings.

This highly integrated device provides a complete low-power physical layer solution on a single chip for Packet/ATM over SONET/SDH at the STS-48 rate.

Features Continued:

Line Interface

- 4-bit 622 MHz OIF Parallel Interface and Synchronization for STS-192 Applications
- 2.5 Gb/s Serial Line Interface with Integrated CMU and CDR
- Power-Save Mode for Unused I/Os

Special Features

- Extensive Packet / Cell Peformance Monitoring Features
- 16 Kb Packet / Cell FIFO for Full Packet Encapsulation
- Programmable Error Discarding and Label Filtering
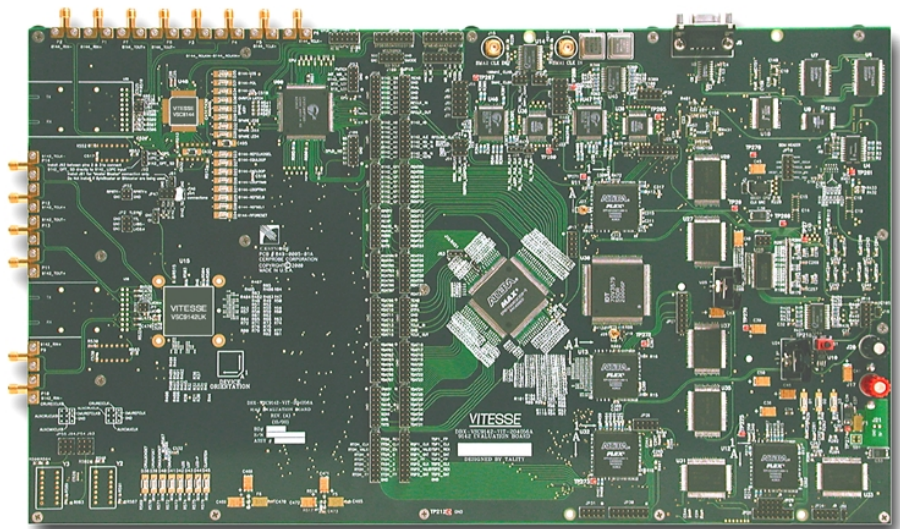- Rx and Tx Timestamp Feature for Performance Monitoring Applications

Miscellaneous Features

- Generic 8-bit CPU Interface
- Compliant JTAG Boundary Scan Interface
- Five Loopback Modes for Test and Diagnostic Applications
- 0.18 micron CMOS, 320-pin TBGA, 2.5 Watts

VSC9142 Block Diagram
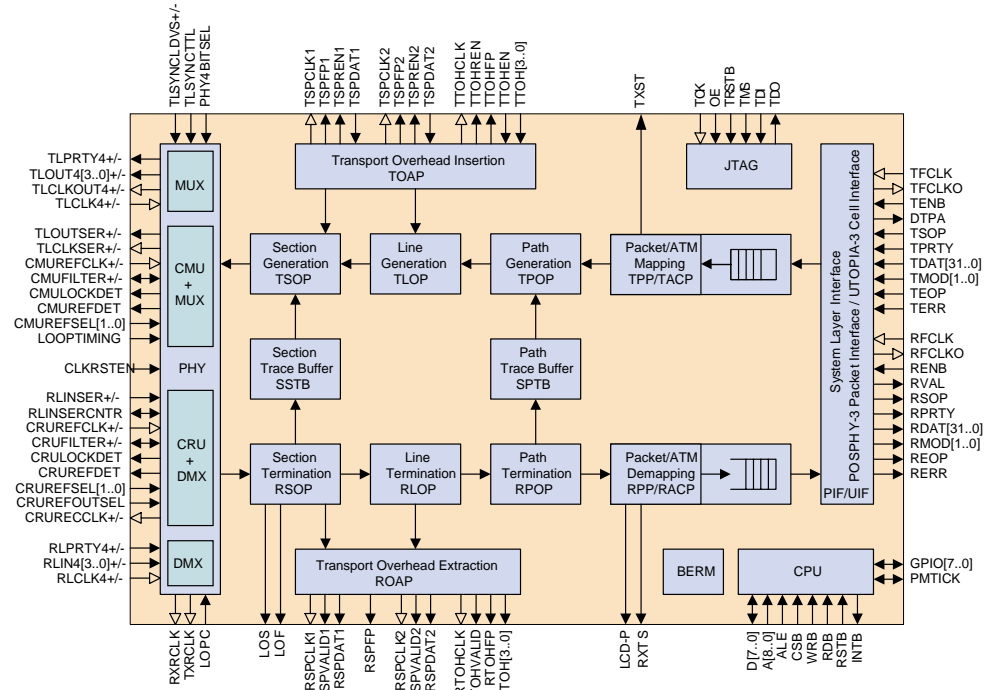
VSC9142 Reference Board

For more information on Vitesse Products visit the Vitesse web site at www.vitesse.com **or contact Vitesse Sales at** (800) VITESSE **or** sales@vitesse.com

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