New Products

32-BIT RISC SINGLE-CHIP MICROCONTROLLER

V850E/IA2

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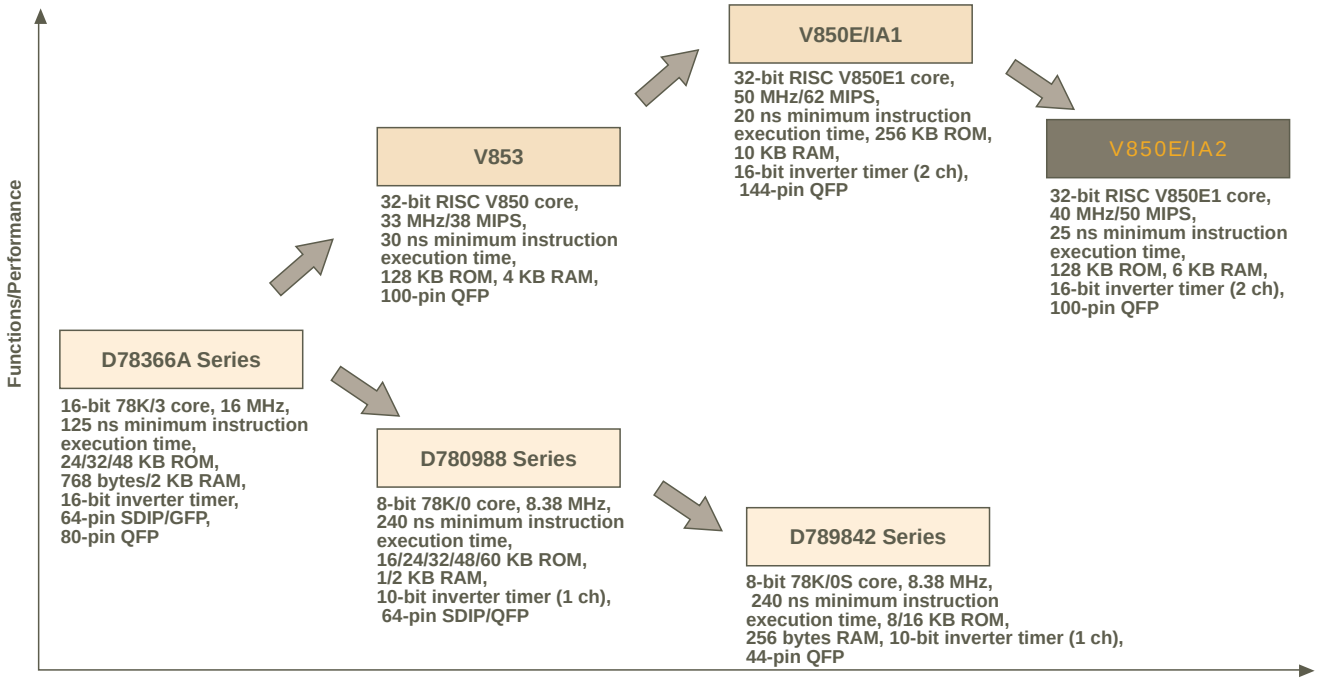

Fig. 1 Microcontrollers for Inverter Control

Introduction

Inverter control is now prevalent in a wide range of fields, including industrial machines, consumer appliances, and automotive electrical equipment, and is mainly used for motor revolution control. A major feature of inverter control is the ability to vary the speed of a motor's revolutions efficiently and without the use of gears. In industrial applications, general-purpose inverters and AC servo motors are being used embedded in a variety of FA equipment to provide the delicate control necessary for machines that operate in environments with extreme torque variations, such as pumps and elevators. In consumer applications, inverter control is used in air conditioners, refrigerators, washing machines, and other household appliances, and is popular due to its low-noise, energy-saving features. The high power efficiency and fine control of inverter control is also making it attractive for use in automotive electronics applications such as hybrid cars and power steering. As its features become more fully exploited in these fields, the application range of inverter control is expected to grow rapidly in the near future.

The current lineup of microcontrollers for inverter control offered by NEC ranges from the μPD780988 and μPD789842 Series that incorporate an 8-bit CPU core to the V850E/IA1 featuring a 32-bit RISC CPU core (Fig. 1). In the V850E/IA1, the 2-channel configuration of the on-chip 3-phase sine-wave and encoder input timers allows independent control of 2-motor systems, and the further incorporation of two A/D converters makes it possible to measure the motor drive current. An FCAN serial interface, essential for automotive applications, is also provided. All these functions, as well as 256 KB of mask ROM and 10 KB of RAM, are available packaged in a 144-pin LQFP (a flash memory product with identical specifications is also available). The V850E/IA2 to be introduced here is the second iteration of the V850E/IAx Series of ASSPs (Application Specific Standard Products) for inverter control incorporating a V850E1 core. With this product, NEC has achieved improved usability by adding to the basic functions of the V850E/IA1 and incorporating a regulator, and a superior cost performance by deleting selected functions to enable packaging in a compact 100-pin LQFP (Table 1).

The V850E/IA2 is another step in NEC's aim

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Item	V850E/IA1	V850E/IA2	Remarks
CPU core	V850E1	V850E1	
Operation speed	50 MHz	40 MHz	
Flash version ROM	256 KB	128 KB	
Flash version RAM	10 KB	6 KB	
Mask version ROM	256 KB	128 KB	
Mask version RAM	10 KB	6 KB	
Timers	3-phase sine-wave PWM x 2 ch	3-phase sine-wave PWM x 2 ch	Buffer/compare register and INT added in IA2
	16-bit up/down counter timer x 2 ch	16-bit up/down counter timer x 1 ch	
	16-/32-bit general-purpose timer x 1 ch	16-/32-bit general-purpose timer x 1 ch	
	16-bit general-purpose timer x 1 ch	16-bit general-purpose timer x 1 ch	Output OFF function via INTP4 added in IA2
	6-bit interval timer x 1 ch	6-bit interval timer x 1 ch	
UART	3 ch	1 ch	
CSI	2 ch	1 ch	
UART/CSI	Not provided	1 ch	Shared in IA2
FCAN	1 ch	Not provided	
A/D	10-bit resolution x 2 units (total of 16 inputs)	10-bit resolution x 2 units (total of 14 inputs)	A/D trigger added and Avref/Avdd shared in IA2
DMA	4 ch	4 ch	Start triggers added in IA2
PKG	144-pin QFP 20 x 20 mm 0.5 mm pitch	100-pin QFP 14 x 14 mm 0.5 mm pitch	
ROMless	Provided	Provided	
Regulator	Not provided	Provided (external Tr required)	New function in IA2
V_{DD}	3.3 V ± 0.3 V, 5.0 V ± 0.5 V	5.0 V ± 0.5 V	

Table 1 Specification Comparison of IA1 and IA2

to further enhance inverter control application support by extending its lineup of 32-bit RISC V850E Family ASSPs (Fig. 2).

Features

The V850E/IA2 is a second-iteration ASSP for inverter control incorporating the newly developed high-performance 32-bit RISC CPU core V850E1, which takes its place as the central CPU core in the current age of system LSI.

1. Realization of high-performance 50 MIPS

The V850E1 CPU core, which is a core optimized to enable easy design of semicustom ICs, operates at up to 40 MHz and has a performance of 50 MIPS (Million Instructions Per Second: Dhrystone-benchmark-based conversion using the VAX-11/780 as a base). Due to pipelining optimization, the V850E architecture employed in the V850E1 CPU core has shown a 10 percent improvement in performance compared to conventional V850 CPU architecture operating at the same frequency. Moreover, by adding instructions that are compatible with high-level languages and CISC-like instructions, it has been possible to improve the efficiency of object codes in a C compiler by 10 to 20 percent over the V850 CPU architecture, while at the same time maintaining upward compatibility at the object level.

2. Compact design through multiplexed bus

The V850E/IA2 is provided with a single-chip mode, in which the internal ROM is used, a ROMless mode, and an external expansion mode to allow the memory and I/O to be expanded externally. The bus is configured as a multiplexed address/data bus.

3. Peripheral functions for inverter control

The V850E/IA2 includes a 2-channel 3-phase sine-wave PWM output timer, a 2-channel 16-bit up/down counter for encoder input, which is used to measure the number of motor revolutions and revolution direction, and two 10-bit resolution A/D converters. With these peripheral functions, the aforementioned high-speed, high-performance CPU can be used to measure the motor drive pattern currently being output, the number of revolutions, and the drive current in order to calculate the next drive pattern, thereby enabling detailed and precise inverter control (including feedback).

4. Three-system independently configured serial interface

The interfaces provided include a 2-channel asynchronous serial interface (UART) and a

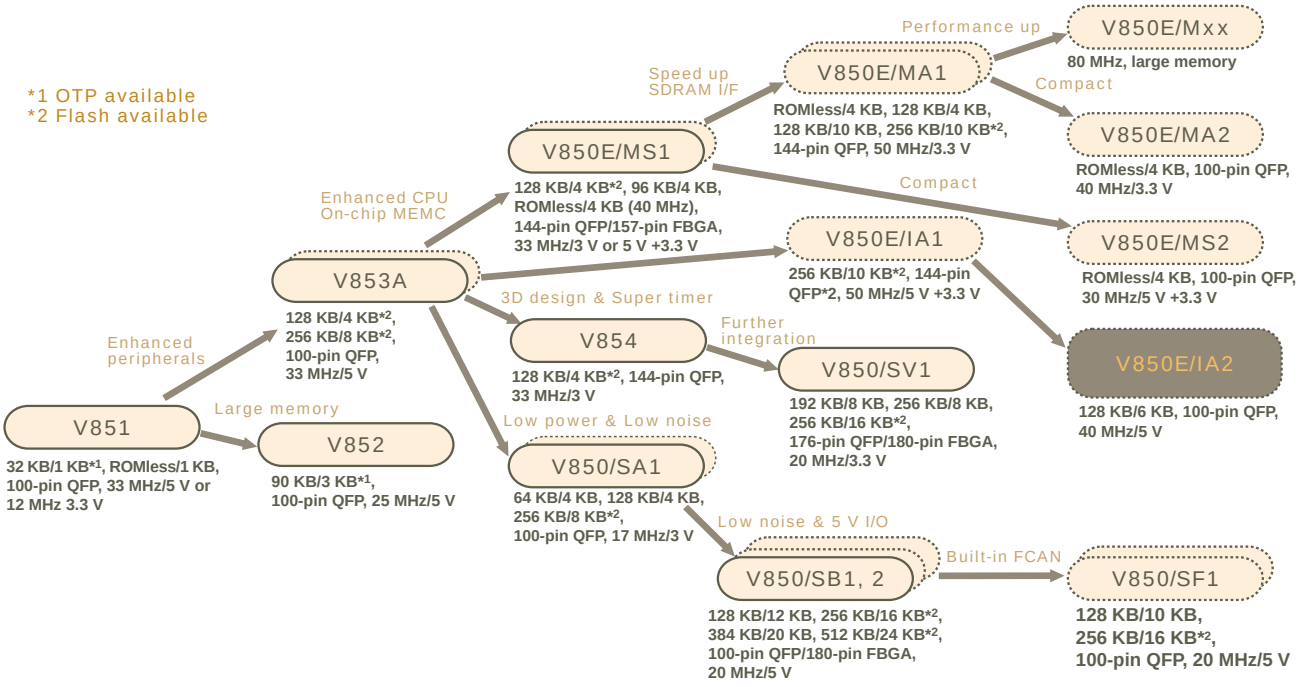

Fig. 2 V850 Family Lineup

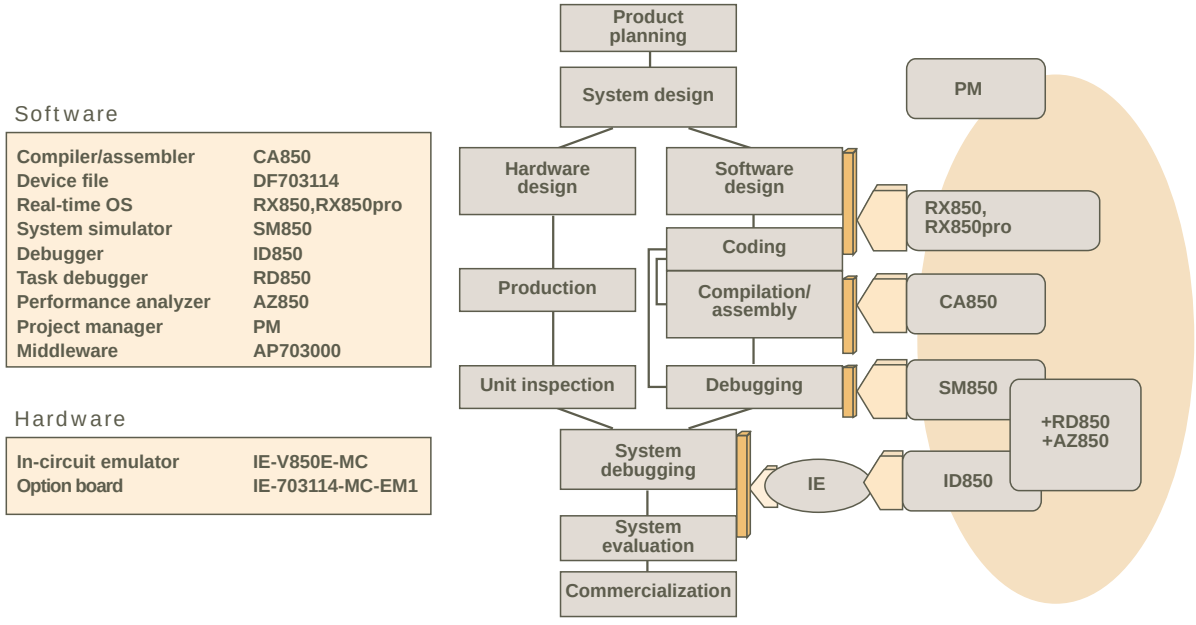

Fig. 3 Development Environment

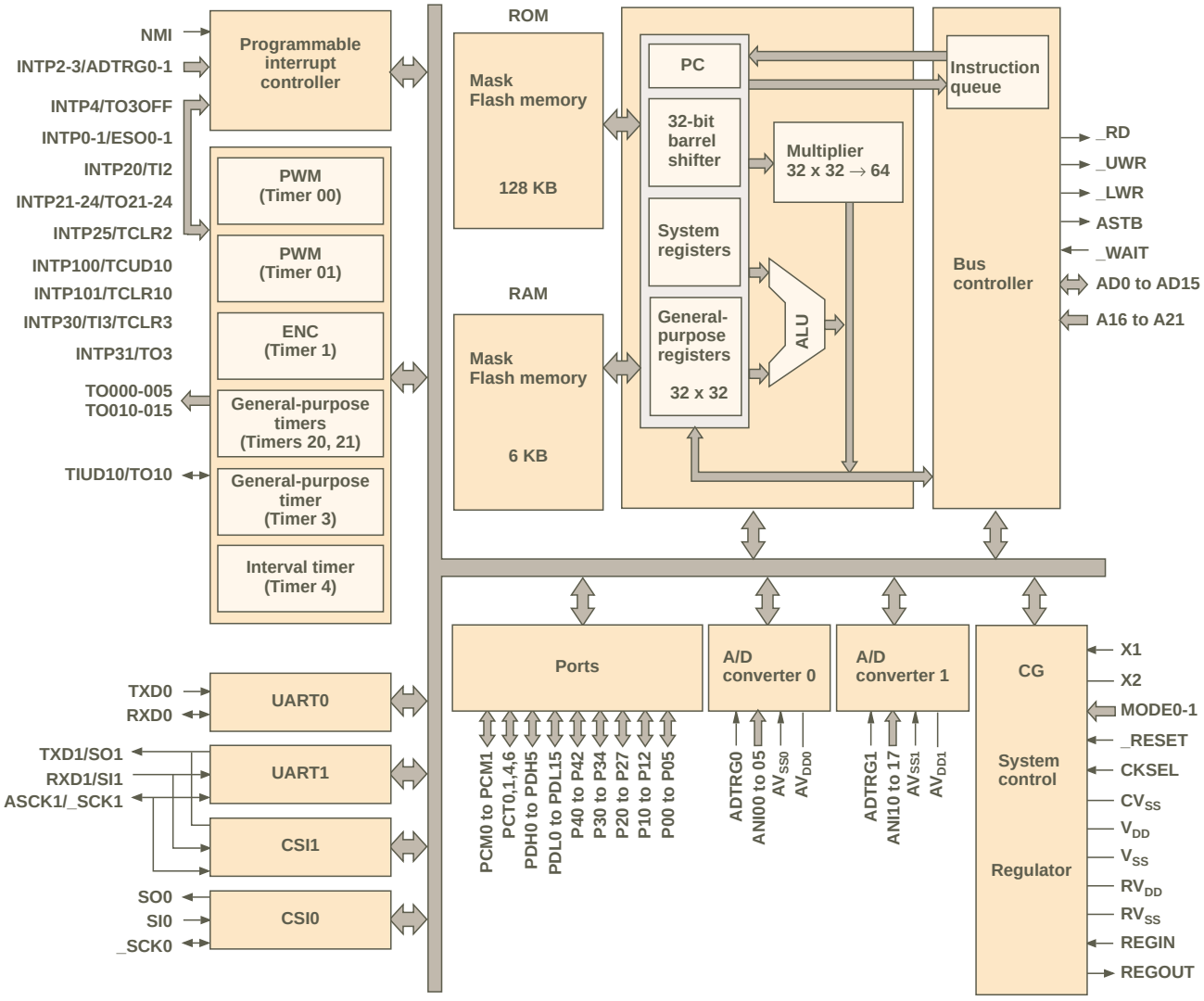

Fig. 4 V850E/IA2 Block Diagram

2-channel clocked serial interface (CSI), with 3 of the 4 serial interface channels assigned to separate pins. This independent configuration allows easy communication between system units that have different communication protocols and speeds and devices such as microcontrollers and EEPROM.

5. Provision of proven and enriched development environment

An optimized C compiler, simulator, in-circuit emulator, debugger, and other components of the integrated environment with a proven track record in the V800 Series, as well as a µITRON-compliant OS, task debugger, and performance analyzer will be supplied as an integrated development environment (Fig. 3). Moreover, by working in close partnership with toolmakers, NEC also pledges to provide proven-quality C compilers, real-time OSs, in-circuit emulators, and other development environments.

Peripheral Functions

In addition to the 32-bit RISC CPU core, the V850E/IA2 has all the peripheral functions essential for configuring an application system, including ROM, RAM, an external bus interface, a DMA controller, timer/counters, A/D converters, serial interfaces, a clock generator, an interrupt controller, and a regulator, packaged together in a 100-pin 14 mm x 14 mm LQFP. Figure 4 shows the internal block diagram of the V850E/IA2.

1. Internal ROM

The V850E/IA2 has both a mask ROM version, the µPD703114 (with 128 KB of mask ROM), and a flash memory version, the µPD70F3114 (with 128 KB of flash memory).

Because the instruction codes configured in the internal ROM can fetch instructions from the CPU in a 1-clock pitch, the effectiveness of CPU pipeline processing can be maximized. With the μPD70F3114, users can easily rewrite programs while the microcontroller is mounted on the target board.

2. Internal RAM

The μPD70F3114 and μPD70F3114 incorporate 6 KB of RAM. Data can be read/written in 1 clock, allowing the internal RAM to be used as a high-speed work memory or a stack memory.

3. External bus interface

The external bus interface consists of a multiplexed 22-bit address and 8-/16-bit data bus, and the total space is divided into 8 blocks, for each of which wait states can be set. These features enable compact external expansion even in systems with memories of differing types or access speeds, or mixed I/O.

4. DMA controller

An on-chip DMA controller with 4 channels is provided. DMA can be used to perform CPU-internal operations and data transfers at the same time as transfers to and from the memory. Transfers can be requested via software or interrupt, and data transfers between the internal RAM and the internal peripheral I/O are performed in two cycles.

5. Timer/counters

Seven channels are provided for the 4 types of timers available.

Timer 0 consists of two 16-bit up/down counter channels (timer 00 and timer 01) that output 6-phase inverter PWM sine waves corresponding to positive and negative phases. A dead-time timer is also provided to protect against short-circuiting of the positive and negative phases. Not only can the PWM waveforms be selected from 3 modes: symmetrical triangle, asymmetrical triangle, and sawtooth, but the output buffer can also be switched off (high-impedance state) by external input, A/D conversion result, or software processing, which is particularly effective when an overcurrent or other such abnormality has been detected. In the V850E/IA2, INTCM01m (m = 0 to 5), CM0nx, and BFCMnx (n = 0 or 1, x = 4 or 5) have been added. When not used for sine-wave PWM output, INTCM01m can be used as an interval timer, which added to INTCM0n3 and INTTM0n, raises the available channel number to 11. Also, because CM0nx and BFCMnx can also be used as A/D conversion start triggers, A/D conversion can be started both synchronously and asynchronously to sine-wave PWM output (Fig. 5).

Timer 1 is a 2-channel timer with alternative functions as a 16-bit up/down counter for counting the motor's encoder pulses and a general-purpose timer capable of PWM output. The encoder pulse input count can be selected from 4 modes based on the order of the 2-phase pulse edge or input phase, and the general-purpose timer is available for use as an interval timer and a free-running timer, as well as for PWM output.

Timer 2 consists of two general-purpose 16-bit timer/event counter channels (TM20 and TM21), which can be used as a 32-bit timer/event counter by connecting the two channels in cascade. Four PWM outputs are available via the 6-channel capture/compare register provided. Timer 2 can also be used as an up/down counter set via an external signal level.

Timer 3 consists of a 16-bit timer/event counter and 2 capture/compare registers, and can be used for PWM output, and as an external event counter. In the V850E/IA2, a function has been added to allow the timer's output buffer (TO3) to be set to high-impedance via an external input (INTP4).

Timer 4 consists of a 1-channel 16-bit timer counter and a compare register, and can be used as an interval timer.

6. A/D converter

The V850E/IA2 includes two 10-bit resolution A/D converters with a total of 14 analog input channels (6 in one and 8 in the other). These A/D converters are of the successive approximation type, and can convert analog variables into digital signals in no more than 6 μs, including sampling time. Because two converters are incorporated, two of the 3 current phases can be measured, and by using the encoder input, the current state of motor revolutions can be clearly ascertained. Furthermore, if the conversion value is greater than that set (i.e. an overcurrent has been detected), it is possible to switch off PWM output for motor driving and place the output buffer in a high-impedance state without the intervention of software.

7. Serial interfaces

Two types of serial interfaces, UART (asynchronous serial interface), and CSI (clocked serial interface) are provided, consisting of 2 channels each.

UART0 and UART1 have maximum transfer rates of 312.5 Kbps and 153.6 Kbps respectively, and can support transfer of 9-bit length data through the addition of bit extension. UART1 can also transfer data synchronously via an external clock.

CSI0 and CSI1 are capable of a high-speed transfer rate of up to 4 Mbps. Data can be transmitted and received in 8-bit or 16-bit units using half-duplex communication.

UART1 and CSI1 use the same alternate-function pin.

8. Clock generator

The V850E/IA2 can operate at a frequency selected as 1, 5, or 10 times that of the oscillation clock by means of an on-chip PLL circuit. Operation at 1/2 the frequency of an external clock is also possible. In addition, three types of power saving modes (software STOP, IDLE, and HALT) are supported, enabling sophisticated power control.

9. Interrupt controller

The interrupt controller provided in the V850E/IA2 can handle 16 sources of external interrupts input from pins (including NMIs (Non-Maskable Interrupts)), and 42 internal interrupt sources generated by peripheral hardware. Up to eight priority levels can be programmed for each interrupt. The interrupt handler of each interrupt source is activated by means of a vector (fixed) method.

10. I/O pins

There are 47 general-purpose I/O pins, which can be switched between input and output in 1-bit units, 6 input-only pins, and 12 PWM output pins for motor driving. Fourteen analog

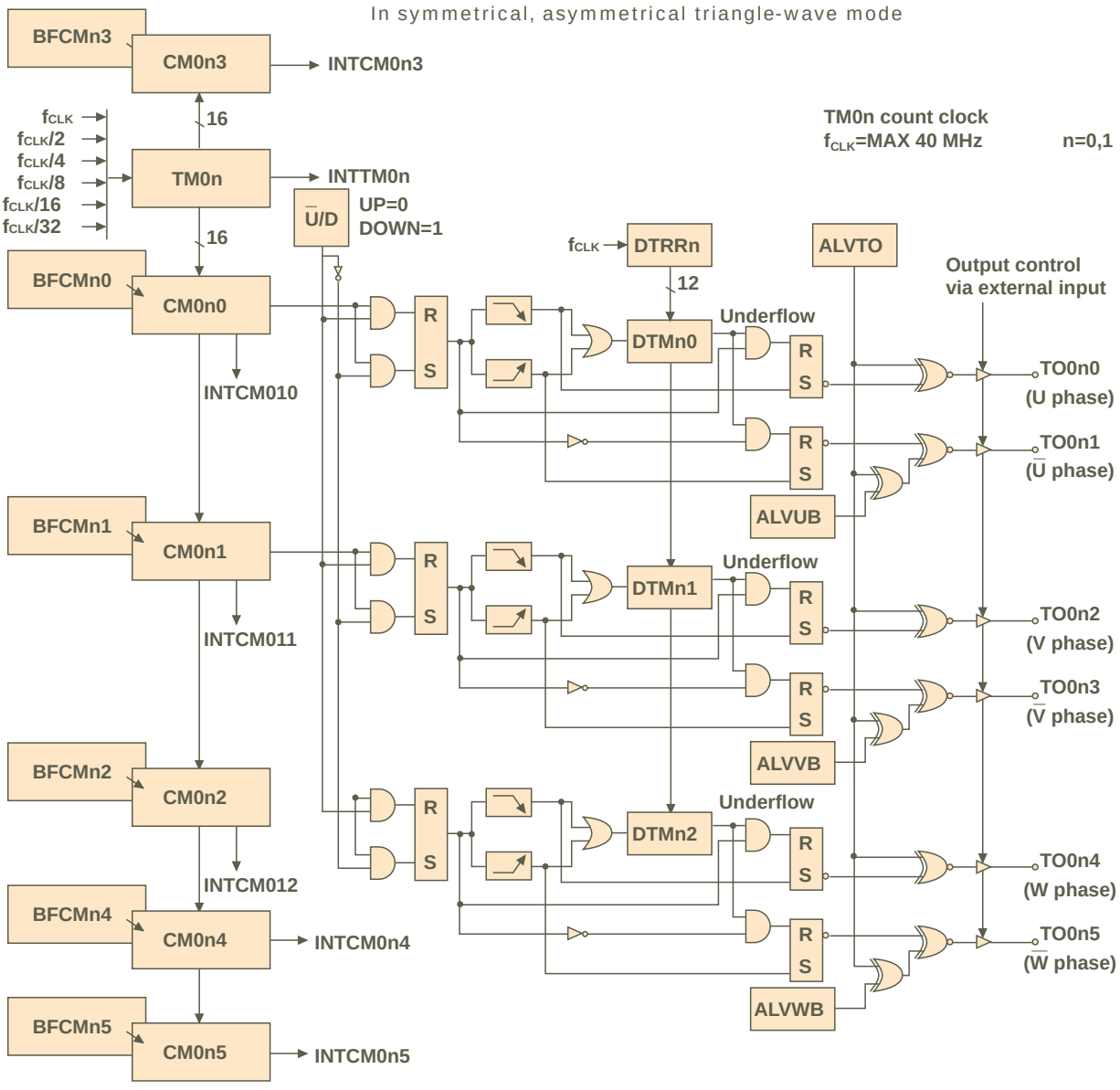

Fig. 5 3-Phase Sine-Wave PWM Timer (Timer 00, 01)

input pins are also provided for the A/D converter.

11. Regulator

The additional incorporation in the V850E/IA2 of a regulator makes it possible to configure 5 V single-power-supply systems simply by externally attaching a Pch power MOSFET.

With the V850E/IA2, NEC has achieved a 32-bit RISC microcontroller for inverter control that features a superior cost performance.

Future Development

NEC aims to increase the operating frequency and further reduce the power consumption of the V850E1 core employed by the second-iteration inverter control ASSP featured here, thus promoting even higher performance. In addition to the above, NEC pledges to continue its effort to provide solutions optimized to applications by expanding its product range through the development of ASSPs that support a wide range of fields related to motor control, including consumer appliances, industrial machines, and automotive electronics.