V63C31322048
64K X 32 CMOS SYNCHRONOUS BURST PIPELINED SRAM

Features

- High-speed clock access time: 5/6/7/8ns
- Single 3.3V power supply
- Synchronous operation
- Individual byte write control and global write
- Internal registers for address, data, and controls
- Output data registers
- Asynchronous Output Enable
- Supports snooze mode (low-power state)
- Internal burst counter supports interleaved or linear burst mode
- Available in 100-pin PQFP/TQFP

Functional Description

The V63C31322048 is a high-speed synchronous burst pipelined CMOS SRAM organized as 65,536 words by 32 bits that supports both i486/ Pentium™ Interleaved mode and 680X0/Power PC™ linear mode address pipelining. Control is achieved through the use of the $\overline{LBO}$ pin.

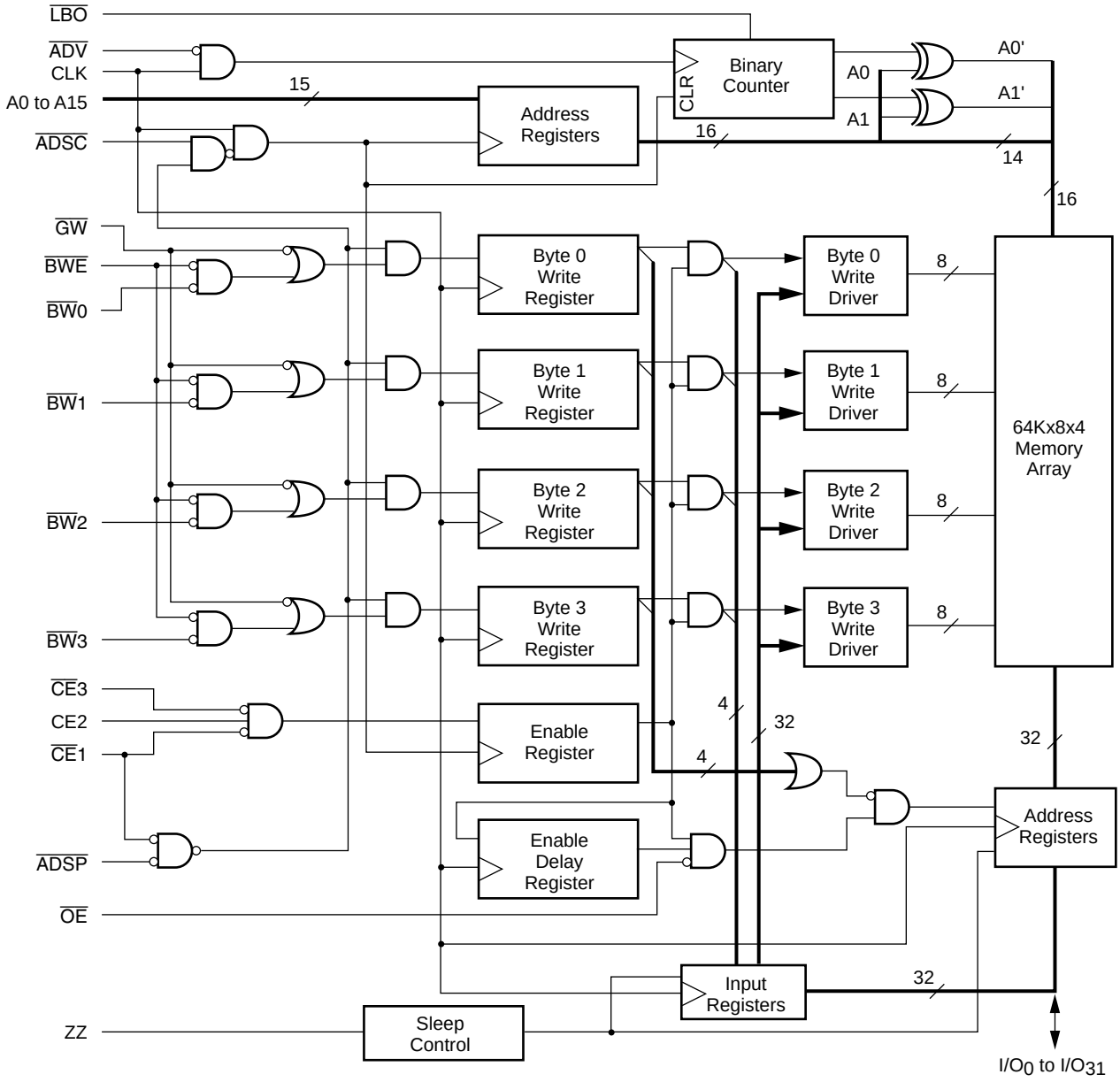
Burst operations can be initiated with either the address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) inputs. Subsequently burst addresses can be internally generated as controlled by the burst advance ($\overline{ADV}$) input.

The V63C31322048 operates on a single 3.3V power supply and is ideally suited for applications that require high-speed, low-power and wide-bit configuration in secondary cache designs.

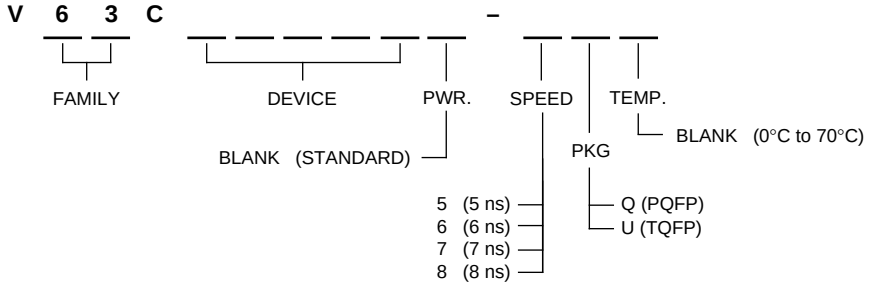
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	Q	U	5	6	7	8	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank

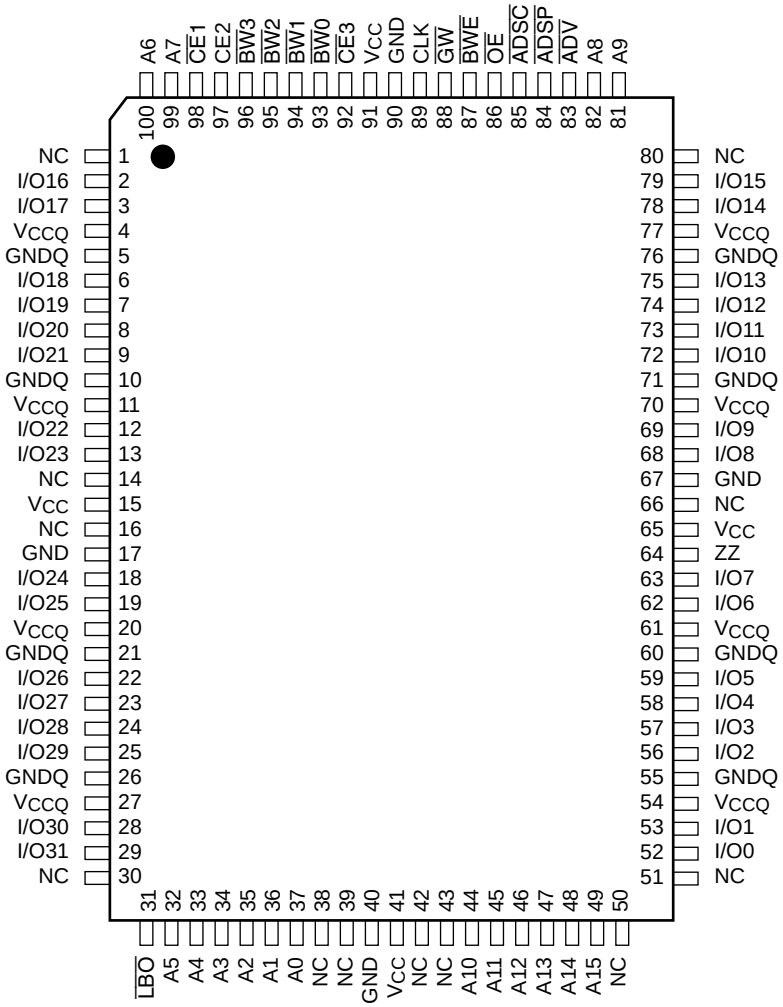
Block Diagram



Ordering Information



100-Pin QFP/TQFP PIN CONFIGURATION



Pin Names

Symbol	Type	Description
A0—A15	Input, Synchronous	Address
I/O_0-I/O_{31}	I/O, Synchronous	Data Inputs/Outputs
CLK	Input, Clock	Processor Host Bus Clock
$\overline{CE1}$, CE2, $\overline{CE3}$	Input, Synchronous	Chip Enables
$\overline{GW}$	Input, Synchronous	Global Write
$\overline{BWE}$	Input, Synchronous	Byte Write Enable from Cache Controller
$\overline{BW_0}$-$\overline{BW_3}$	Input, Synchronous	Host BusByte Enables Used with $\overline{BWE}$
$\overline{OE}$	Input, Asynchronous	Output Enable
$\overline{ADV}$	Input, Synchronous	Internal Burst Address Counter Advance
$\overline{ADSC}$	Input, Synchronous	Address Status from Controller
$\overline{ADSP}$	Input, Synchronous	Address Status from Processor
ZZ	Input, Asynchronous	Snooze Pin for Low-Power State
$\overline{LBO}$	Input, Static	This Mode Selects Burst Sequence; LOW for Linear, HIGH for interleaved
V_{CCQ}		I/O Power Supply
GNDQ		I/O Ground
V_{CC}		Power Supply
GND		Ground

Absolute Maximum Ratings*

Core Supply Voltage to GND..... –0.5 to +4.6V
I/O Supply Voltage to GND..... –0.5 to +4.6V
Input/Output to
GND Potential ..... GNDQ–0.5 to V_{CCQ}+0.5V
Allowable Power Dissipation 1.0W
Storage Temperature ..... –65 to +150°C
Operating Temperature ..... 0 to +70°C

Note: Exposure to conditions beyond those listed under *Absolute Maximum Ratings* may adversely affect the life and reliability of the device.

Capacitance

V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz

Symbol	Parameter*	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

* Note: These parameters are guaranteed by device characterization and are not production tested.

Truth Table

Cycle	Address Used	$\overline{CE}$1	CE2	$\overline{CE}$3	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	Data	Write(1)
Unselected	No	1	X	X	X	0	X	X	Hi-Z	X
Unselected	No	0	X	1	0	X	X	X	Hi-Z	X
Unselected	No	0	0	X	0	X	X	X	Hi-Z	X
Unselected	No	0	X	1	1	0	X	X	Hi-Z	X
Unselected	No	0	0	X	1	0	X	X	Hi-Z	X
Begin Read	External	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	X	X	X	1	1	0	0	D-OUT	Read
Continue Read	Next	1	X	X	X	1	0	1	Hi-Z	Read
Continue Read	Next	1	X	X	X	1	0	0	D-OUT	Read
Suspend Read	Current	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	X	X	X	1	1	1	0	D-Out	Read
Suspend Read	Current	1	X	X	X	1	1	1	Hi-Z	Read
Suspend Read	Current	1	X	X	X	1	1	0	D-OUT	Read
Begin Write	Current	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	1	X	X	X	1	1	X	Hi-Z	Write
Begin Write	External	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	1	X	X	X	1	0	X	Hi-Z	Write
Suspend Write	Current	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	1	X	X	X	1	1	X	Hi-Z	Write

Notes:

1. For a detailed definition of read/write, see the Write Table (next page).
2. A “X” means “don’t care,” “1” means logic HIGH, and “0” means logic LOW.
3. The $\overline{OE}$ pin enables the data output but is not synchronous with the clock. All signals of the SRAM are sampled synchronous to the bus clock except for the $\overline{OE}$ pin.
4. On a write cycle that follows a read cycle, $\overline{OE}$ must be inactive prior to the start of write cycle to allow write data to setup the SRAM. $\overline{OE}$ must also disable the output buffer prior to the finish of a write cycle to ensure the SRAM data hold timing are met.

Write Mode

The V63C31322048 support different kinds of write mode operations. The $\overline{BWE}$ and $\overline{BW}$ [3:0] support individual byte writes. The $\overline{BE}$ [7:0] signals can be directly connected to the SRAM $\overline{BW}$ [3:0]. The $\overline{GW}$ signal is used to override the byte enable signals and allows the cache controller to write all bytes to the SRAM, no matter what the byte write enable signals are. The various write modes are indicated in the Write Table, below. Note that in pipelined mode, the byte write enable signals are not latched by the SRAM with addresses but with data. In pipelined mode, the cache controller must ensure the SRAM latches both data and valid byte enable signals from the processor.

Write Table

Read/Write Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$	$\overline{BW0}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0, $I/O_0 – I/O_7$	1	0	1	1	1	0
Write Byte 1, $I/O_8 – I/O_{15}$	1	0	1	1	0	1
Write Byte 1, Byte 0	1	0	1	1	0	0
Write Byte 2, $I/O_{16} – I/O_{23}$	1	0	1	0	1	1
Write Byte 2, Byte 0	1	0	1	0	1	0
Write Byte 2, Byte 1	1	0	1	0	0	1
Write Byte 2, Byte 1, Byte 0	1	0	1	0	0	0
Write Byte 3, $I/O_{24} – I/O_{31}$	1	0	0	1	1	1
Write Byte 3, Byte 0	1	0	0	1	1	0
Write Byte 3, Byte 1	1	0	0	1	0	1
Write Byte 3, Byte 1, Byte 0	1	0	0	1	0	0
Write Byte 3, Byte 2	1	0	0	0	1	1
Write Byte 3, Byte 2, Byte 0	1	0	0	0	1	0
Write Byte 3, Byte 2, Byte 1	1	0	0	0	0	1
Write All Bytes, $I/O_0 – I/O_{31}$	1	0	0	0	0	0
Write All Bytes, $I/O_0 – I/O_{31}$	0	X	X	X	X	X

Burst Address Sequence

	Intel System ($\overline{LBO}$ = V_{CCQ})				Linear Mode ($\overline{LBO}$ = GNDQ)			
	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]	A[1:0]
External Start Address	00	01	10	11	00	01	10	11
Second Address	01	00	11	10	01	10	11	00
Third Address	10	11	00	01	10	11	00	01
Fourth Address	11	10	01	00	11	00	01	10

Snooze Mode

The ZZ state is a low-power state in which the device consumes less power than in the unselected mode. Enabling the ZZ pin for a fixed period of time will force the SRAM into the ZZ state. Pulling the ZZ pin LOW for a set period of time will wake up the SRAM again. While the SRAM is in ZZ mode, data retention is guaranteed, but the chip will not monitor any input signal except for the ZZ pin. In the unselected mode, the other hand, all the input signals are monitored.

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O Status
Read	L	L	Data Out
Read	L	H	High-Z
Write	L	X	High-Z, Data in
Deselect	L	X	High-Z
Power down (Snooze)	H	X	High-Z

Note: H means logic HIGH. L means logic LOW. X means H or L.

Operating Characteristics (V_{CC} = 3.3V ±5%, T_A = 0 to 70°C)

Parameter	Sym	Test Conditions	Min.	Typ.	Max.	Unit
Input Low Voltage	V_{IL}		–0.5	–	+0.8	V
Input High Votage	V_{IH}		2.0	–	V_{CC} +0.3	V
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CCQ}	–5	–	+5	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = GND to V_{CCQ}, & data I/O pins disabled	–5	–	+5	µA
Output Low Voltage	V_{OL}	V_{OL} = 8mA	–	–	0.4	V
Output High Voltage	V_{OH}	V_{OH} = -4mA	2.4	–	–	V
Operating Current	I_{DD}	$T_{CYC} \geq t_{KC}$ Min, I/O = 0 mA, V_{CC} = Max	–	–	300	mA
Standby Current	I_{SB}	V_{CC} = Max, Device deselected All inputs = V_{IL} or V_{IH} $T_{CYC} \geq t_{KC}$ Min	–	–	25	mA
ZZ Mode Current	I_{ZZ}	ZZ mode, $T_{CYC} \geq t_{KC}$ Min	–	–	5	mA

Note: V_{IL} Min = –2.0V undershoot for pulse width ≤ t_{CYC} Min/2.

AC Test Conditions

Parameter	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	2 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH} / I_{OL} = –4mA/8mA

AC Test Loads and Waveform

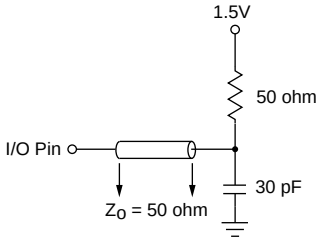


Figure 1

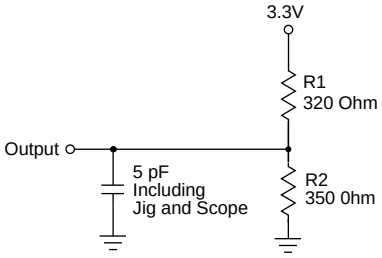
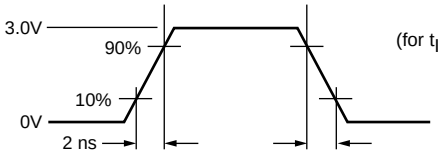


Figure 2



AC Timing Characteristics (V_{CC} = 3.3V ±5%, T_A = 0 to 70°C)

#	Sym	Parameter	5		6		7		8		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{AS}	Address Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
2	t_{AH}	Address Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
3	t_{DS}	Data Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
4	t_{DH}	Data Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
5	t_{ADVS}	$\overline{ADV}$ Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
6	t_{ADVH}	$\overline{ADV}$ Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
7	t_{ADSS}	$\overline{ADSP}$ Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
8	t_{ADSH}	$\overline{ADSP}$ Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
9	t_{ADCS}	$\overline{ADSC}$ Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
10	t_{ADCH}	ADSC Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
11	t_{CES}	$\overline{CE}$1, CE2, $\overline{CE}$3 Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
12	t_{CEH}	$\overline{CE}$1, CE2, $\overline{CE}$3 Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
13	t_{WS}	$\overline{GW}$, $\overline{BWE}$ X Setup Time	2.5	–	2.5	–	2.5	–	2.5	–	ns	
14	t_{WH}	$\overline{GW}$, $\overline{BWE}$ X Hold Time	0.5	–	0.5	–	0.5	–	0.5	–	ns	
15	t_{CYC}	Clock Cycle Time	10	–	12	–	15	–	20	–	ns	
16	t_{KH}	Clock High Pulse Width	4	–	4.5	–	5	–	6	–	ns	
17	t_{KL}	Clock Low Pulse Width	4	–	4.5	–	5	–	6	–	ns	
18	t_{KQ}	Clock to Output Valid	–	5	–	6	–	7	–	8	ns	
19	t_{KHZ}	Clock to Output High-Z	2	10	2	11.1	2	13.3	2	15	ns	1

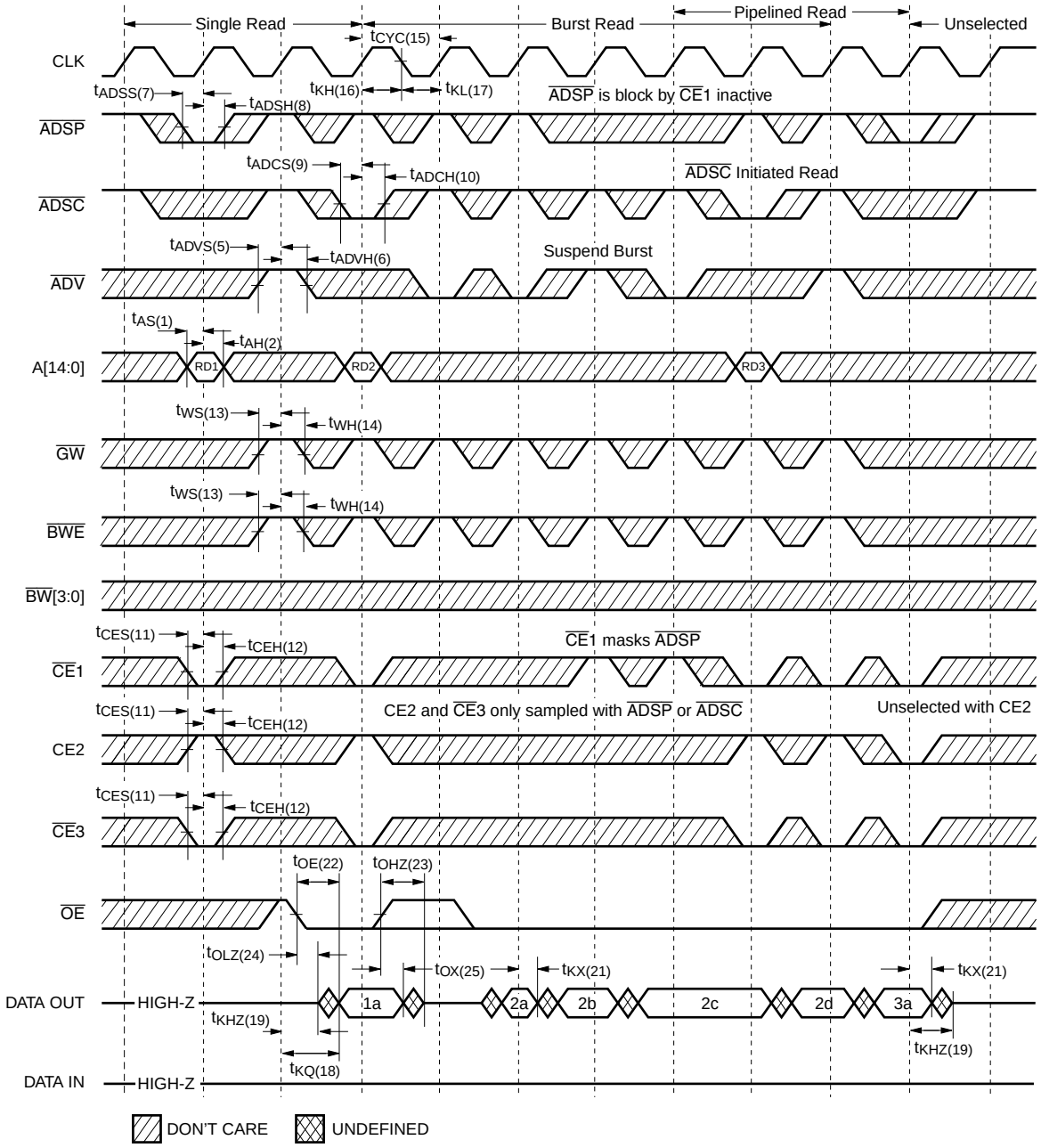
AC Characteristics (Cont'd)

#	Sym	Parameter	5		6		7		8		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
20	t_{KLZ}	Clock to Output Low-Z	4	–	5	–	5	–	5	–	ns	1
21	t_{KX}	Clock to Output Invalid	2	–	2	–	2	–	2	–	ns	1
22	t_{OE}	Output Enable to Output Valid	–	5	–	6	–	7	–	8	ns	
23	t_{OHZ}	Output Enable to Output High-Z	–	5	–	6	–	7	–	8	ns	1
24	t_{OLZ}	Output Enable to Output Low-Z	0	–	0	–	0	–	0	–	ns	1
26	t_{ZZS}	ZZ Standby Time	–	100	–	100	–	100	–	100	ns	2
27	t_{ZZR}	ZZ Recover Time	100	–	100	–	100	–	100	–	ns	3

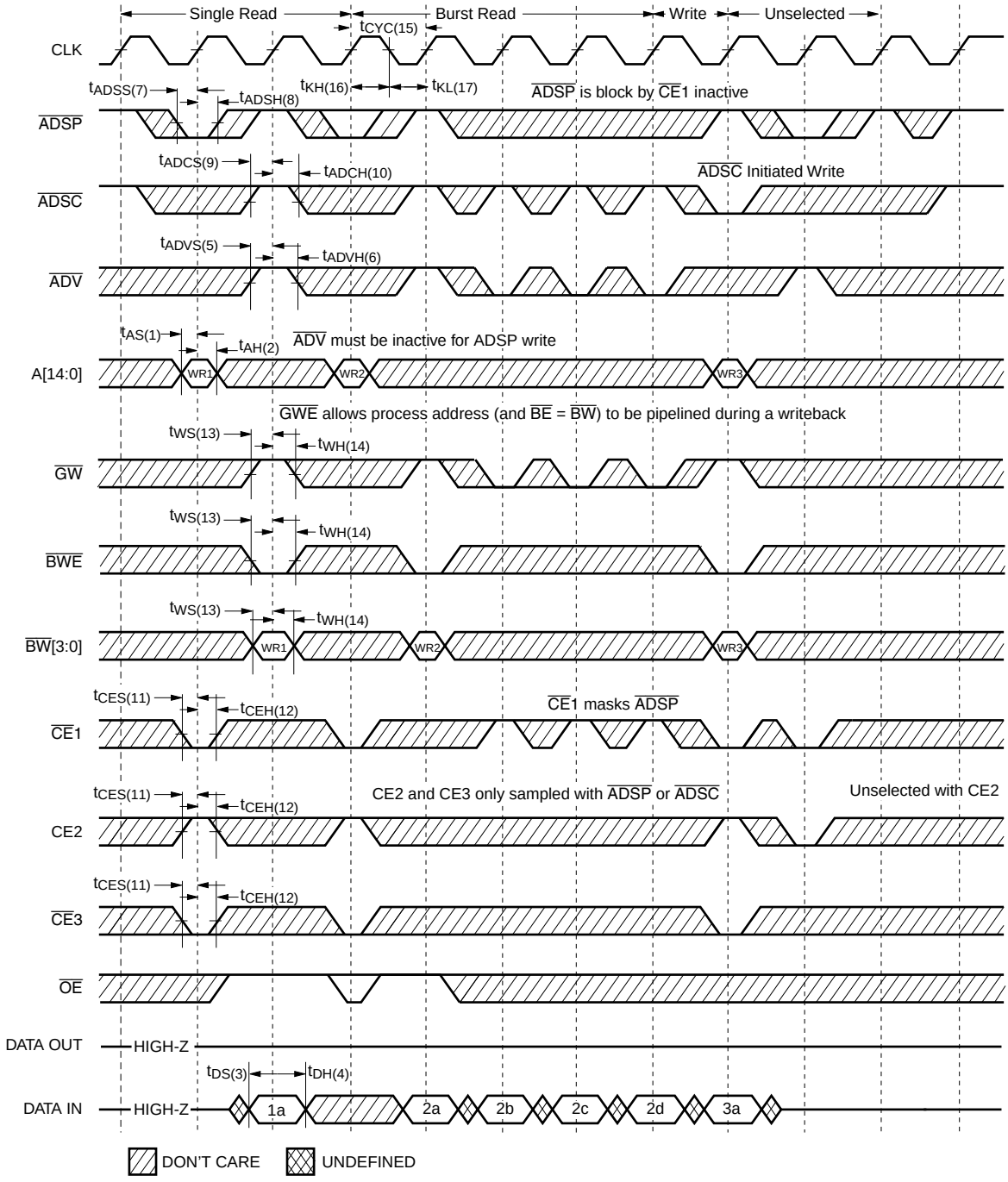
Notes:

1. These parameters are sampled but not 100% tested.
2. In the ZZ mode, the SRAM will enter a low-power state. In this mode, data retention is guaranteed and the clock is active.
3. $\overline{\text{ADSC}}$ and $\overline{\text{ADSP}}$ should not be accessed for at least 100 ns after chip leaves ZZ Mode.

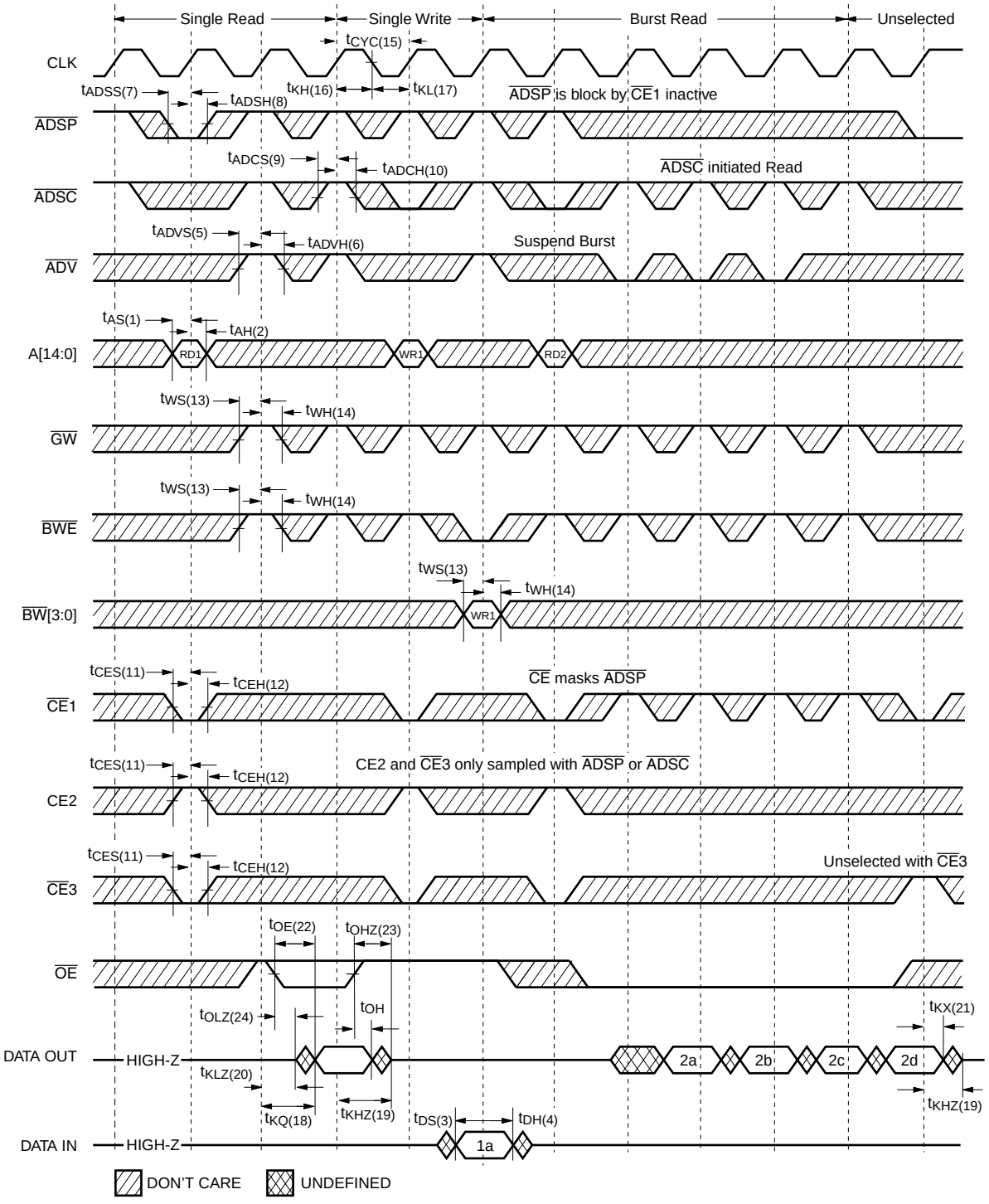
Waveforms of Read Cycle



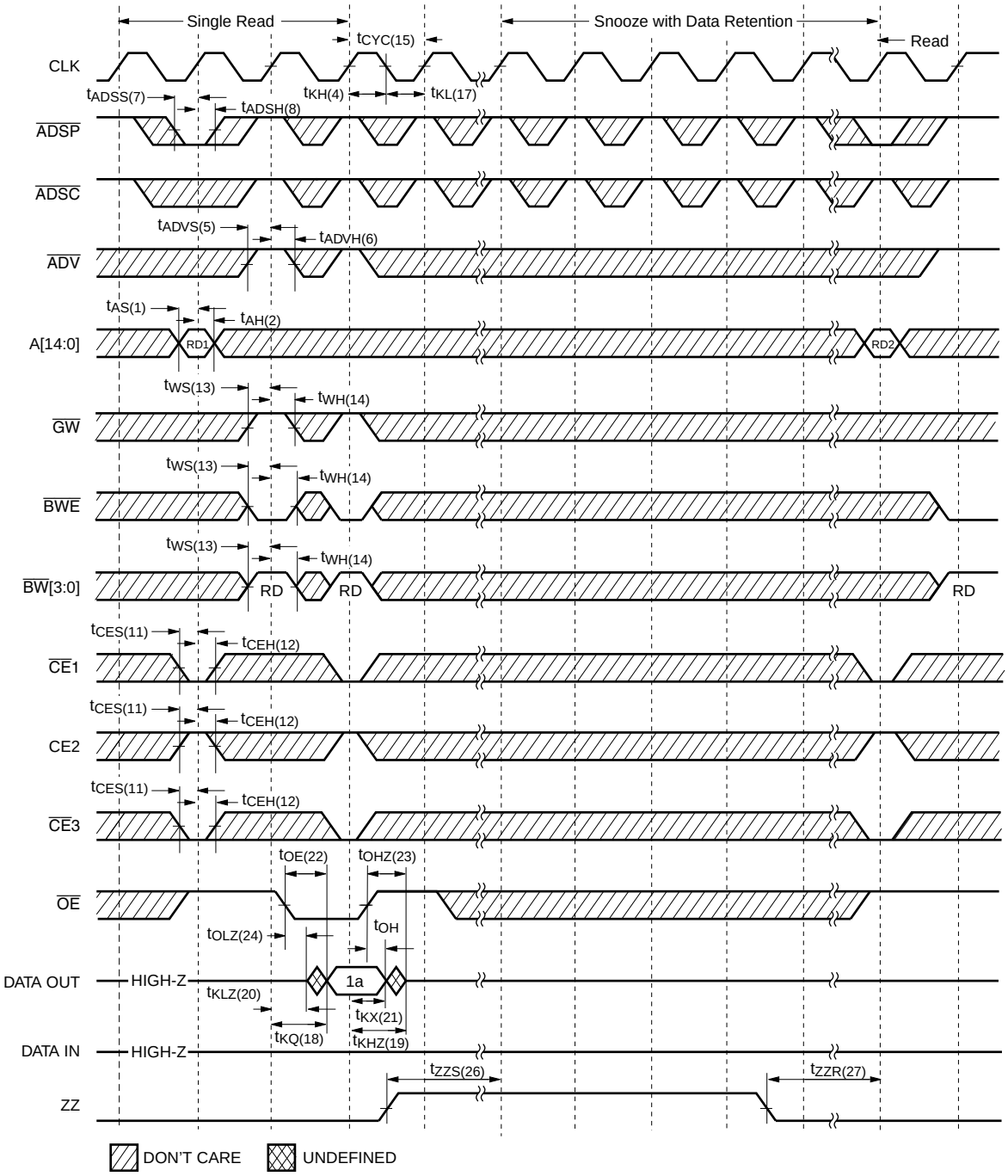
Waveforms of Write Cycle



Waveforms of Read/Write Cycle

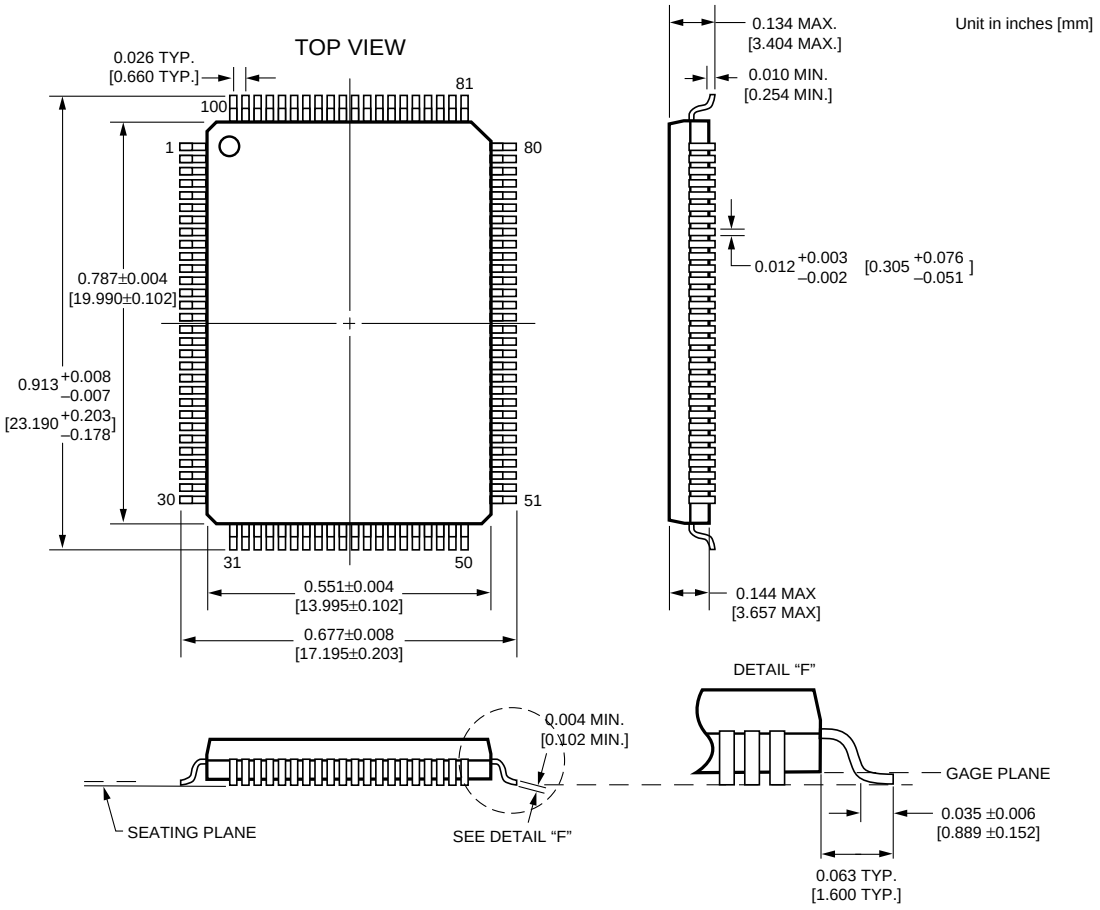


Waveforms of ZZ and RD Cycle

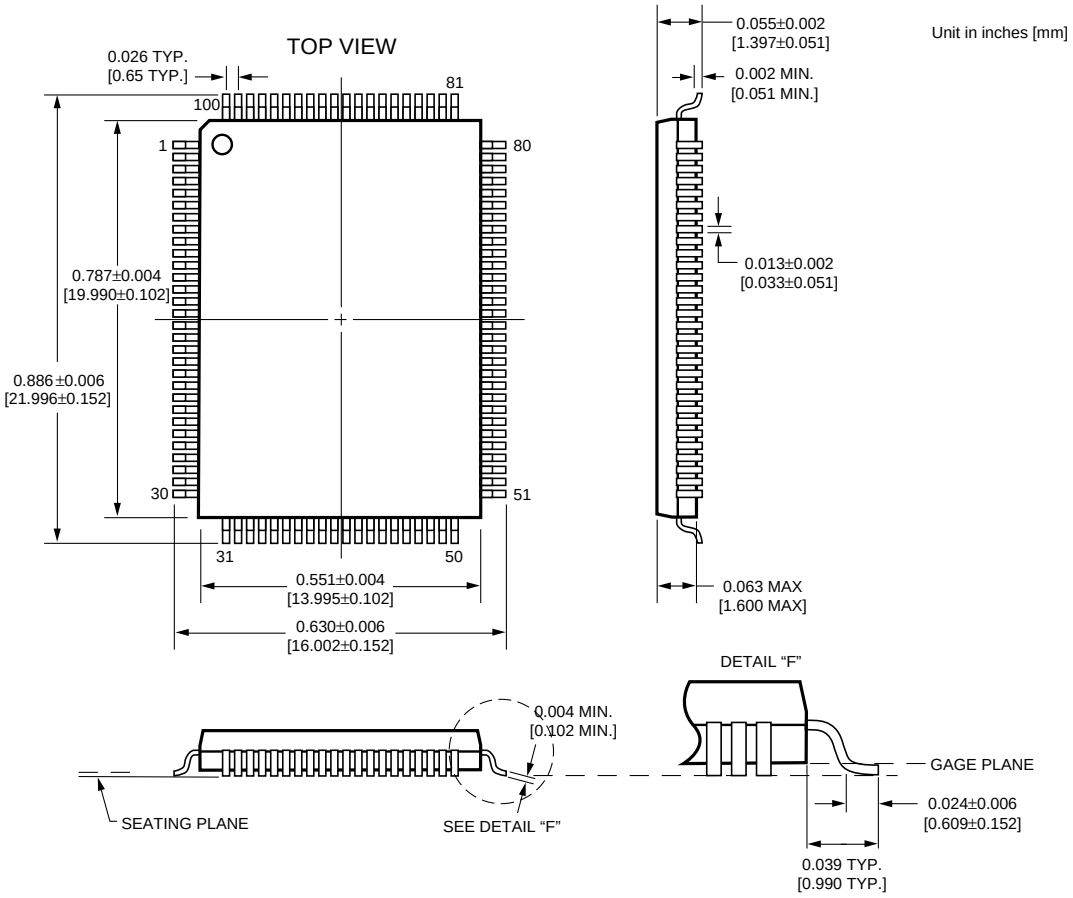


Package Diagram

100-pin PQFP (Q)



100-pin TQFP (TQ)



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