



VDSL Product Brief

The purpose of Metalink's Very High Bit Rate Digital Subscriber Line (VDSL) chipset solution is to supply the core technology required for the next generation telecom and datacom services. As users demand for high speed Internet, Intranet and other forms of access is escalating, their need for more bandwidth rises, and service providers are struggling to supply the demand.

Copper is the most prevalent infrastructure in the world and is the medium on which most high rate services will be carried. VDSL is the only technology capable of transmitting at very high speeds over copper wires. VDSL is currently being defined by the standards committees in Europe and in North America.

Metalink has been one of the most significant HDSL and SDSL chipset solution providers during the past five years. Metalink is expanding upon its proven technology and expertise in the area of digital communication over copper infrastructure to provide a VDSL chipset solution. The VDSL chipset solution will provide the core technology for future Full Service Access Networks (FSAN). Relying on its past experience with HDSL, Metalink will provide a complete solution including chipsets, software, hardware reference design and excellent system integration.

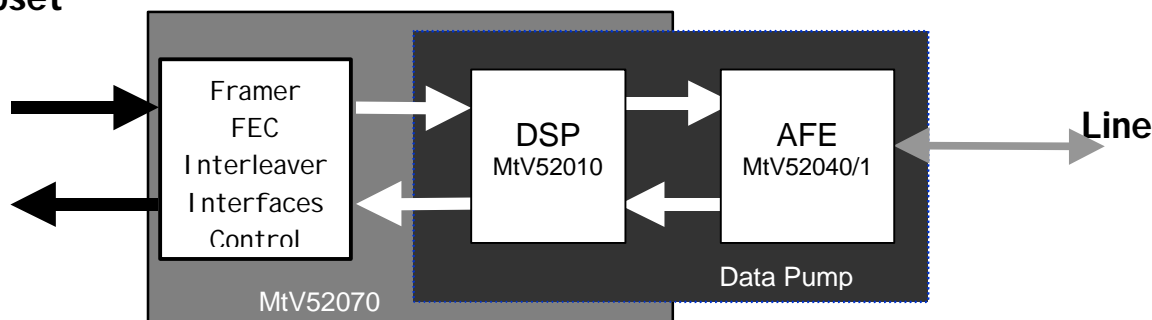
Metalink VDSL total solution concept includes:

1. Chipset
2. Hardware reference design
3. Recommended peripherals
4. Evaluation board
5. Software – (a) Customer interface functions
(b) Detailed software manual

Product Description

Line Code	QAM (CAP compatible receiver)	
Duplexing method	Frequency Division Duplexing (FDD)	
Rates	Symmetric	1.5 Mbps – 26Mbps
	Asymmetric	1.5 Mbps – 6.5Mbps U/S
		6.0 Mbps – 52Mbps D/S

Chipset



Product Features

- QAM line code (CAP compatible)
- Symmetric and asymmetric transmissions
- Asymmetric rates:
1.5 Mbps – 6.5 Mbps U/S
6 Mbps – 52 Mbps D/S
- Symmetric rates:
2.3Mbps – 26Mbps
- ANSI and ETSI compliant
- Flexible carrier frequencies
- Supports dual carrier (bands) for U/S and D/S
- Programmable band allocation for U/S and D/S
- Programmable output power level and power backoff mechanism
- Reed Solomon FEC
- Interleaver
- Loopbacks
- Rate adaptive functionality
- RFI egress/ RFI ingress immunity implementing patented Metalink technology
- Constant delay
- Line distortion detection
- SNR measurement
- Enhanced monitoring functions and capabilities
- Digital POTS and ISDN provisioning
- ATM, Ethernet and Synchronous interfaces

Chipset Components:

MtV52010 – Digital Signal Processor. Includes a QAM transmitter and receiver. Performs all the digital operations of the transceiver: bit mapping, shaping filters, AGC, equalization, timing recovery, clock generation, modulation and demodulation.

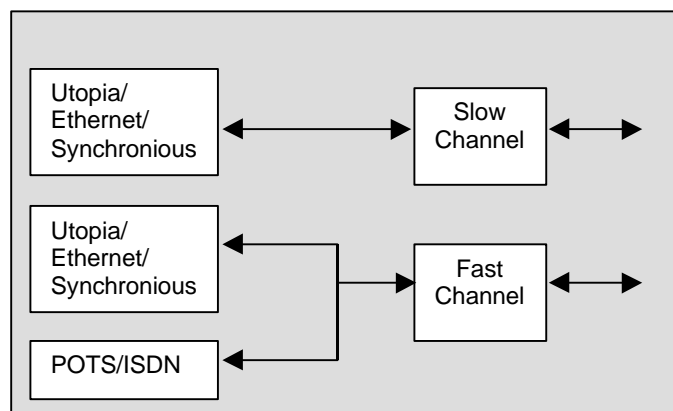
MtV52040 – AFE, based on discrete components. Performs all the analog operations of the chipset: D/A and A/D, filtering, AGC, line driving.

MtV52070 – Digital VDSL Processor – Performs all the tasks of the MtV52010 with additional: framing/deframing, FEC encoding and decoding, Interleaving/deinterleaving, application interfaces.

MtV52041 – Monolithic Analog Front End

MtV52070 Application's Interfaces

The application's interfaces include two parallel channels that may be operated. Each channel is characterized by its latency. For the low latency (fast channel) one out of five interfaces may be selected: Utopia, Ethernet, Synchronous, ISND or POTS. The high latency channel (slow channel) is chosen out of three interfaces: Utopia, Ethernet or synchronous.



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