Preliminary

Product Summary

2.5 — 3.125 Gbps Four-Lane CMOS SerDes (Serializer / Deserializer)

GENERAL DESCRIPTION

The Velio VC1013 is a 4-lane Serializer / Deserializer IC, which operates from 2.5 – 3.125 Gbps, (and half these rates). The device is designed for flexibility; it has multiple configuration options, allowing the operation to be tailored to specific system environments. The 4 transmitters can accept parallel data in several formats and speeds, depending upon the configuration. The 4 receivers accept serial data, recover the clock and data, and then deserialize the data into one of several formats, depending upon the configuration.

Table 1: VC1013 Features and Benefits

FEATURES	BENEFITS
Four 2.5 – 3.125 Gbps (and half-rate) SERDES Lanes	Integration conserves board space, reduces power
1.8 V Core Voltage Supply	Low Voltage Core reduces power consumption
1.1 W Typical Power	Reduces overall system power requirements
CML High-Speed Serial I/O with Programmable Output Voltage Swing	Serial Output Signal can be tailored to specific system conditions
SSTL_2 ASIC-side I/O	Popular I/O standard for flexible ASIC design
Adjustable Pre-Emphasis on Serial Outputs	Reduces Inter-Symbol-Interference, enables serial transmission over longer distances
Typical Receiver Sensitivity as low as 50 mV	Reduces BER on noisy or lossy signals
Compensated On-Chip Termination Resistors for Serial Outputs and Inputs	Internal compensation ensures matched impedances, reducing transmission reflections
8b/10 encoder/decoder (and bypass mode)	Performs 8b/10b encode and decode
User-selectable 8 or 10 bit/Lane ASIC Interface	Multiple bit/Lane modes support 8b/10b and SONET data streams
Self-Test with PRBS Generation	Enables in-system testing and diagnostics
17 mm x 17 mm PBGA	Space-saving, thermally enhanced package

APPLICATIONS

- 10 Gigabit Ethernet
- SONET Backplanes
- Infiniband
- Backplane applications
- Optical Transceiver Interface

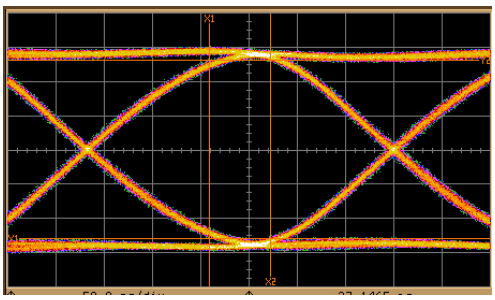

Figure 1: VC1013 Transmit Signal at 3.125 Gbps

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REVISION 1.2

FUNCTIONAL OVERVIEW

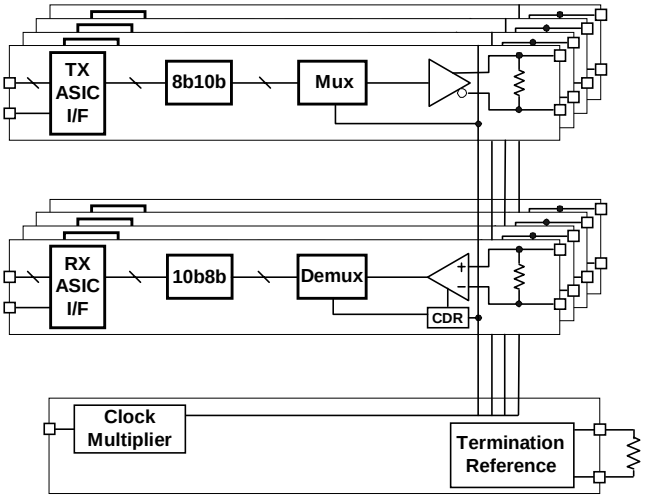

Figure 2: VC1013 Block Diagram

Configurable Serial Outputs for Signal Integrity

The VC1013 utilizes a programmable SERializer and DESerializer core for high-speed serial I/O signals. The user-selectable features uniquely address Inter-Symbol Interference (ISI), and help ensure signal integrity at multi-gigabit speeds.

Programmable Pre-Emphasis

To counteract the effects of ISI, the VC1013 serial output signal has an optional pre-emphasis component. This results in a detectable data signal over longer trace lengths.

Internal Termination Resistors

Termination resistors are provided on the serial input, as well as the serial output. Input termination resistors are common at these speeds, but the internal output termination deserves special mention. It absorbs reflections from impedance discontinuities, increasing the available signal margin. The value of each of the internal termination resistors is closely matched to that of a single external resistor placed across the RREF+ and RREF- pins.

PRE-EMPHASIS EFFECTS ON SIGNAL INTEGRITY

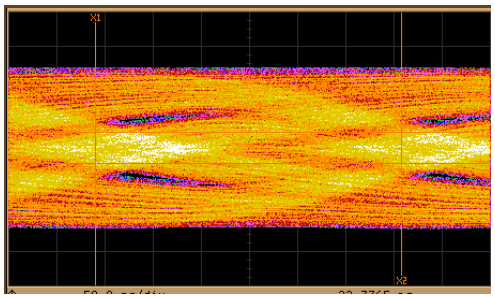

Figure 3: 3.125 Gbps Signal Sent Over a One-Meter FR4 Backplane Plus Two Connectors (Pre-Emphasis Turned OFF)

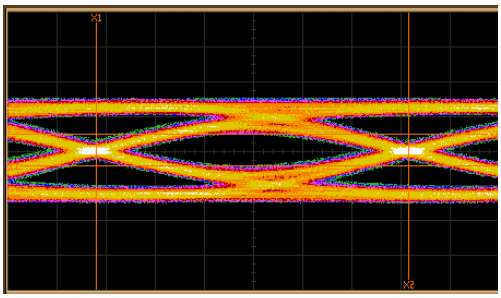

Figure 4: 3.125 Gbps Signal Sent Over a One-Meter FR4 Backplane Plus Two Connectors (Pre-Emphasis Turned ON)