V96SSC Rev. B1

HIGH-INTEGRATION SYSTEM CONTROLLER FOR i960®Sx/Jx AND PowerPC™ 401Gx PROCESSORS

- Direct interface to i960Sx/Jx and PPC401Gx processors
- High-performance burst DRAM controller
- Two-channel fly-by DMA controller
- Serial communications unit
- Programmable chip-select/strobe generation
- Support for 8/16-bit boot PROMs
- Two 32-bit general purpose timers
- Pulse width modulation capability
- System watchdog and heartbeat timers
- 16 general purpose I/O bits
- Eight input ports and eight output ports
- Interrupt control unit
- Local bus speeds up to 33MHz
- Low cost 100-pin EIAJ PQFP package
- Fastest time to market for i960Sx and i960Jx based designs

The V96SSC High-Integration System Controller is a single-chip device that simplifies the design of systems based on i960Sx, i960Jx or PPC401Gx embedded microprocessors. The V96SSC replaces many lower integration components with a single, high-integration device.

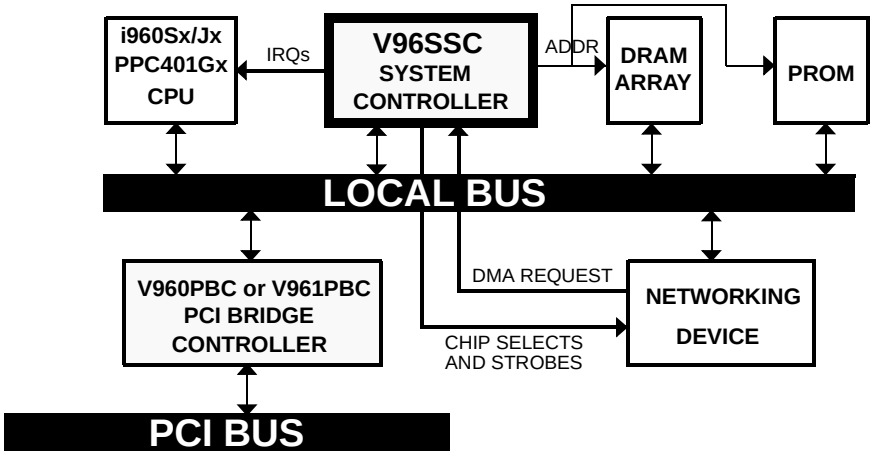
Nearly all i960 or PowerPC processor based systems will require DRAM for code and data storage. The V96SSC includes a high-performance DRAM controller which is programmable to accommodate a wide range of DRAM speeds and architectures.

The eight chip-select/strobes further simplify peripheral/memory connection. Each select has programmable timing and a total of four wait-state generators are provided.

Beyond simplifying memory and peripheral control, the V96SSC also includes many of the peripherals needed to build a high-performance i960 or PPC401Gx based system: DMA channels, synchronous/asynchronous serial port, general purpose and system heartbeat timers, bit I/O ports, and an interrupt controller.

In addition, the V96SSC includes special features to enhance system integrity. The bus watch timer prevents system hangs on access to unpopulated memory. A watchdog timer is also included to recover from software upsets.

Due to its small footprint, and glueless interface, the V96SSC provides the best features of an integrated processor without any performance compromises!



This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V96SSC. Detailed functional information is contained in the User's Manual.

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1.0 Product Codes

Table 1: Product Codes

Product Code	Processor	Bus Type	Package	Frequency
V96SSC-33LP	i960SA/SB i960JA/JD/JF PPC401GF	16-bit multiplexed 32-bit multiplexed 32-bit multiplexed	100-pin EIAJ PQFP	33MHz

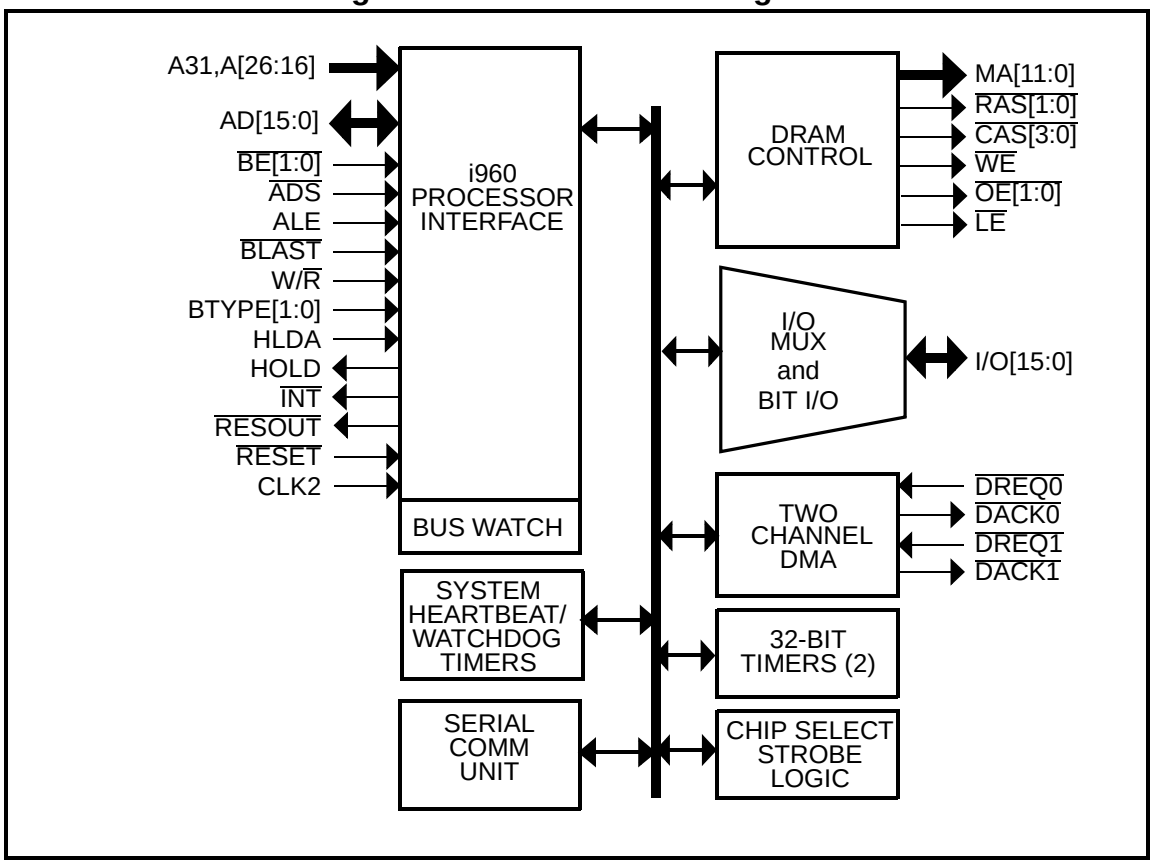
2.0 Functional Description

The V96SSC consists of the following functional units:

- Direct i960 and PPC401Gx Processors Bus Interface Unit
- Burst DRAM Controller
- DMA Controller
- Serial Communications Unit
- Chip Select/Strobe Unit
- General Purpose Timer/Counters
- System Watchdog and System Heartbeat Timers
- Interrupt Control Unit
- I/O Control Unit and Internal Signal Multiplexer

A block diagram of the V96SSC is shown in Figure 1. Each of the functional units is described briefly in the sections below. The V96SSC Data Sheet provides information regarding AC and DC specifications, pinout, and packaging. Detailed information regarding hardware and software interfacing can be found in the V96SSC User's Manual.

Figure 1: V96SSC Block Diagram



2.1 Direct i960 Sx/Jx and PPC401Gx Processors Bus Interface Units

The V96SSC is designed to connect directly to i960Sx/Jx and PPC401Gx processors. No “glue logic” is required. Care was taken during the design of the V96SSC to insure full AC timing compatibility with these processors running with bus speeds up to 33MHz. Even the pinout of the V96SSC has been designed with ease of connection in mind.

At the beginning of each processor bus cycle the V96SSC samples the BTYPE[1:0] pins. As it’s shown in the following table, these pins indicate what type of bus cycle is being run. Because the bus type is dynamically detected, the V96SSC may be used in systems using both 16-bit and 32-bit masters.

Table 2: BTYPE[1:0] Pin Decoding

BTYPE[1:0]	CPU Mode	Boot Address	Description
00	i960SA/SB	A[31, 26:24]=”0000”	16-bit data bus, $\overline{BE[1:0]}$ valid for current cycle, both processor and V96SSC use 2x clock
01	PPC401Gx	A[31, 26:24]=”1111”	32-bit data bus, $\overline{BE[3:0]}$ valid for current cycle, processor uses 1X clock and V96SSC uses 2X clock

Table 2: BTYPE[1:0] Pin Decoding

BTYPE[1:0]	CPU Mode	Boot Address	Description
10	i960Jx (32 bit bus)	A[31, 26:24]=”1110”	32-bit data bus, $\overline{BE[3:0]}$ valid for current cycle, processor uses 1X clock and V96SSC uses 2X clock
11	i960Jx (16 bit bus)	A[31, 26:24]=”1110”	32-bit data bus, $\overline{BE3}$ and $\overline{BE0}$ valid for current cycle, processor uses 1X clock and V96SSC uses 2X clock

In i960Sx systems, the low order address signals are latched internally from the AD[15:0] bus upon assertion of ALE. The high-order address lines are demultiplexed on the i960Sx processor, and are routed directly to the V96SSC’s high order address inputs. The i960Jx processor uses a 32-bit multiplexed address/data bus, therefore for i960Jx bus accesses, the V96SSC latches the high order address signals internally on the assertion of ALE.

All accesses to V96SSC’s internal registers are performed via the AD[15:0] lines. In 32-bit i960Jx systems, the internal registers are typically accessed in a 32 bit region where access to the internal registers is done by software 16 bits at a time (BTYPE="10"). Alternately, it can be mapped into a 16 bit region using BTYPE="11". While the V96SSC is internally a 16-bit device, it is capable of supporting 32-bit memory and peripheral devices.

V96SSC also supports direct interface to PPC401Gx. When BTYPE=”01” then the boot address matches that of the PPC401Gx. In this mode a cycle can be initiated with either an ALE or $\overline{ADS}$ pulse. Since the PPC401Gx has only an ALE output and lacks an $\overline{ADS}$ ($\overline{AS}$) pin, $\overline{ADS}$ on the V96SSC can be tied high by a pull-up resistor.

2.2 Burst DRAM Controller

The V96SSC’s DRAM controller provides the following features:

- Support for fast page mode, extended data out, and Ramtron’s enhanced DRAM architectures
- Two DRAM banks of up to 64MByte each (128MBytes total)
- Programmable DRAM bank address base and size
- Programmable row/column multiplexing mode
- Programmable $\overline{RASx}$ and $\overline{CASx}$ timings
- Support for 16-bit and 32-bit DRAM arrays
- Support for extended burst cycles up to 256 bytes transactions in length
- Programmable page caching to eliminate RAS cycles for subsequent accesses to the same DRAM page
- Programmable refresh counter
- 1-0-0-0 read and 0-0-0-0 write performance at 33MHz

The burst DRAM controller is designed to support traditional fast page mode DRAMs (FPM), the new extended data out page mode DRAMs (EDO), and Ramtron’s ultra high-performance enhanced DRAM (Ramtron EDRAM) devices. A wide variety of DRAM speeds and organizations may be

accommodated due to the V96SSC's flexibility.

Two DRAM banks are provided. Each bank has its own programmable address base and size. The mapping of memory address lines to row and column addresses is also programmable for each bank. The twelve mixed address lines (MA[11:0]) are shared by both banks. Each bank may be independently enabled and/or write protected. Both banks share a common DRAM signal timing generator that controls all DRAM timing parameters. DRAM array width can be set to either 16-bit or 32-bits; the V96SSC controls lane steering logic in mixed width systems.

FPM, EDO, and Ramtron EDRAMs are a natural fit for burst bus processors such as i960 or PPC401Gx family. The V96SSC takes advantage of fast page mode accesses for every burst transaction, insuring the highest transfer rate possible. The V96SSC also supports extended burst peripherals, such as networking controllers, up to a maximum length of 64Byte data cycles.

The DRAM controller also includes page cache management logic. This logic detects subsequent burst accesses within the same DRAM page, and eliminates the RAS precharge time and row address cycles for these accesses. Removing these cycles can reduce the average wait-state profile for many applications. The "aggressiveness" of the caching algorithm is programmable, and page caching can be completely disabled. The page size is programmable from 512 to 8192 bytes.

2.3 DMA Controller

Two independent DMA Channels are provided in the V96SSC. The DMA Controller generates fly-by cycles to transfer data directly from the DRAM to the selected peripheral, or vice-versa. Each channel includes a request input ($\overline{\text{DREQx}}$), an acknowledge output ($\overline{\text{DACKx}}$), and an end-of-process output ($\overline{\text{EOPx}}$, accessible via the I/O Multiplexer). Each channel can also be assigned to a chip select/strobe channel to provide the necessary strobing signals to the DMA target/source peripheral.

The DMA buffer start and stop addresses are programmable, as is the direction of transfer (read or write). Transfers may be initiated either via the $\overline{\text{DREQx}}$ pins or through software.

The DMA Controller's programmable throttle count allows long transfers to be periodically interrupted to allow the processor access to the bus for code fetches, etc.

2.4 Serial Communications Unit (SCU)

The V96SSC's Serial Communications Unit offers both synchronous and asynchronous modes. In asynchronous mode, the Serial Communications Unit functions as an industry standard, full duplex UART. Transmission and reception are double buffered to help prevent data overruns. Interrupts are generated on receiver buffer full, transmit buffer empty, buffer overrun error, and framing error.

In synchronous (SPI) mode, data is moved into, or out of, the SCU's buffers on transitions of the serial clock output pin (SCLK). Data word length is programmable from 1 to 16 bits. An interrupt is generated upon completion of an SPI transfer. SPI mode is ideal for connecting to serial interface peripherals such as A/D converters.

The clock reference for the Serial Communications Unit can be either the independent baud rate generator or general purpose timer 1.

2.5 Chip Select/Strobe Unit

The Chip Select/Strobe Unit provides all the logic necessary to interface a wide array of peripherals and memory components to the i960Sx/Jx processor. Address decoding, wait-state generation, chip-select, and read/write strobe generation are handled completely by the V96SSC; no glue logic is

needed. Eight output strobes/selects are available as output pins from the I/O Multiplexer.

There are eight memory decode registers, each with the following options:

- Base address and size (minimum granularity 64K)
- Region data width
- Read/Write enable

Each memory decode register has an associated Region Timing Control register. This register assigns timings for synchronous mode strobes as well as for wait-state generation. The following timings are programmable for each region:

- Strobe assert from bus cycle start
- Strobe de-assert from bus cycle start
- $\overline{\text{READY}}$ delay from cycle start (wait-states)
- Back-to-Back cycle delay

Each of the 8 chip select/strobe output pins is assigned to one of four programmable memory ranges. These strobe signals can be used as asynchronous chip-selects, or combined with the timing values for the region to create read and write strobes. Each strobe has the following programmable options:

- Address match register assignment
- Access type: read, write, both
- Timing: asynchronous, synchronous
- Sub-decode: finer granularity decoding

The chip select/strobe unit is also tied to the DMA Controller. Each DMA channel can be assigned to a particular decode region and its associated timing.

2.6 General Purpose Timers (GPT)

Two identical 32-bit general purpose timers are integrated in the V96SSC. These timers may be used for a number of applications including: periodic interrupt generation, event counting, and pulse width modulation.

The timers decrement every clock cycle, from a 32-bit preload value until a terminal count of zero is reached. A maskable interrupt is generated on terminal count. The timer may be programmed to halt on terminal count, or to reload and restart counting.

Each timer has an external input (TIx) and external output pin (TOx). The TIx pin can be used as an edge or level sensitive start trigger. The TOx pin has the following modes:

- Latched low
- Short and long pulse low on terminal count
- Toggle on terminal count
- Pulse width modulation
- One shot

2.7 Watchdog and System Heartbeat Timers

The V96SSC's watchdog timer is used to recover a system that has crashed due to a software upset. If the watchdog timer is not periodically reset by "trusted" system software, the V96SSC assumes that a software crash has occurred and resets the processor by driving the $\overline{\text{RSTOUT}}$ pin low. The V96SSC's "system heartbeat" is a fixed-delay periodic interrupt to the processor that is used as a time reference by real-time operating systems.

2.8 Bus Watch Timer (BWT)

Additional system security is provided by the Bus Watch Timer. When enabled, the BWT monitors the $\overline{\text{READY}}$ pin (and, optionally, the $\overline{\text{PREADY}}$ pin) for every bus access initiated by an external master. If $\overline{\text{READY}}$ is not asserted within a programmable window (between 1 and 255 clocks), then the V96SSC will assert $\overline{\text{READY}}$ to end the cycle and generate an interrupt. For burst accesses, the BWT reloads its time-out count on each $\overline{\text{READY}}$ and returns to idle on $\overline{\text{BLAST}}$.

2.9 Interrupt Control Unit

The Interrupt Control Unit manages interrupts for all off the V96SSC's on-chip interrupts, as well as providing interrupt control for up to 8 external requests. Each pending request is latched in the Interrupt Status Register. The Interrupt Mask Register allows independent masking of all interrupt sources.

External interrupts may be routed to the Interrupt Control Unit via the I/O Multiplexer through the I/O port unit.

2.10 I/O Port Unit

The I/O Port Unit provides 8 independent single bit input or output ports. Each bit may be configured as an input port or an output port. As input ports, the unlatched inverted state of the associated pin is read from the Input Port Register. In addition, the input port bits are connected to the Interrupt Control Unit to provide external interrupt requests ($\overline{\text{IO}}$[7:0] pins). When configured as an output port, the state of the associated pin is set by writing to the Output Port Register.

The mapping of I/O Port bits to IOx pins is controlled via the I/O Multiplexer.

2.11 I/O Multiplexer

To allow the V96SSC to fit into a compact and economical 100-pin PQFP package, some non-essential I/O signals are multiplexed onto the IO[15:0] pins. Many internal signals have several options as to which IO pins they connect to. The multiplexing options for each IO pin are described in Table 4. Programming of the I/O Multiplexer is described in the *V96SSC User's Manual.*

2.12 Boot ROM Support

The V96SSC provides special support for boot ROM devices. When an access within the processor's boot range is detected on the A31, A[26:24] pins, the V96SSC outputs a latched low order address on the MA[11:0] pins (normally the muxed address lines for DRAM) and asserts $\overline{\text{IOC0}}$. The V96SSC automatically detects boot ranges specific to each processor: 0x0000.0000 for the i960Sx, 0xFEFF.0000 for the i960Jx and 0xFFFF.0000 for PPC401Gx.

For i960Sx systems using 8-bit boot ROMs, the V96SSC will automatically steer the byte data to the proper half of the AD bus (i960Jx processors handle byte assembly internally).

3.0 Pin Description and Pinout

Table 3 below lists the pin types found on the V96SSC. Table 4 describes the function of each pin on the V96SSC. Table 5 lists the pins by pin number. Figure 2 shows the pinout for the 100-pin EIAJ PQFP package and Figure 3 shows the mechanical dimensions of the package.

Table 3: Pin Types

Pin Type	Description
I	Input pin
I_S	Schmidt trigger input pin
O	Output pin with 4mA drive
O_{12}	Output pin with 12mA drive
I/O	I/O pin with 4mA output drive
I_{SU}	Schmidt trigger input with internal pull-up resistor

Table 4: Signal Descriptions

Processor Interface Signals			
Signal	**Type**	**R[a]**	**Description**
A31,A[26:16]	I		High-order address lines from i960 processor. These signals are latched internally by the V96SSC on the falling edge of ALE. Processor signals A[30:27] are optional and may be routed to the V96SSC through the I/O port pins (see below).
AD[15:0]	I/O	Z	Multiplexed address/data bus. For i960Jx based systems, the V96SSC only uses the lower 16-bits of the AD[31:0] bus.
ALE	I		Address latch enable is connected to the i960 processor's ALE pin. This signal is connected to the internal address latches.
$\overline{ADS}$	I		Address status is connected to the $\overline{AS}$ pin on the i960Sx and to $\overline{ADS}$ on the i960Jx processors.
$\overline{BE[1:0]}$	I/O	Z	Low order byte enables. The $\overline{BE[1:0]}$ pins are inputs for accesses from external masters; they become outputs when the V96SSC is the bus master. $\overline{BE[3:2]}$ are available through the I/O port pins for i960Jx systems (see below).
$\overline{BLAST}$	I		End of burst indication from i960 processor.
W/$\overline{R}$	I/O	Z	Write/Read indication from the i960 processor. W/$\overline{R}$ is driven during V96SSC DMA operations to indicate the direction of the transfer.
HOLD	O	L	Hold request from the V96SSC DMA Controller to the i960 processor.
HLDA	I		Hold acknowledge from the i960 processor. This signal informs the V96SSC that it is now the local bus master.
$\overline{INT}$	O	H	Interrupt request output from the V96SSC interrupt controller.
$\overline{READY}$	I/O	H	Data READY indication. The V96SSC returns $\overline{READY}$ to the i960 processor when data is read/written to memory addresses under the V96SSC's control. The V96SSC also monitors the $\overline{READY}$ signal for all bus accesses when the bus watch timer is enabled.
BTYPE[1:0]	I		Bus transaction type. These signals are examined during the assertion of $\overline{AS}$, $\overline{ADS}$ or $\overline{ALE}$ to determine the type of external master initiating the bus cycle. BTYPE[1:0] Master 00 i960SA/SB 01 PPC401Gx 10 i960JA/JD/JF (32-bit bus) 11 i960JA/JD/JF (16-bit bus)

Table 4: Signal Descriptions (cont'd)

DMA and DRAM Controller Signals			
Signal	**Type**	**R**	**Description**
$\overline{\text{DREQ[1:0]}}$	I		DMA request inputs.
$\overline{\text{DACK[1:0]}}$	O	H[b]	DMA acknowledge outputs.
MA[11:0]	O_{12}	X[b]	DRAM multiplexed memory address lines.
$\overline{\text{RAS[1:0]}}$	O_{12}	H[b]	DRAM row address strobes.
$\overline{\text{CAS[3:0]}}$ or $\overline{\text{CAL[3:0]}}$	O_{12}	H[b]	Column address strobes. In EDRAM mode, the $\overline{\text{CAS[3:0]}}$ signals become $\overline{\text{CAL[3:0]}}$.
$\overline{\text{WE}}$	O_{12}	H[b]	Memory write enable.
$\overline{\text{LE}}$	O_{12}	H[b]	Latch enable.
$\overline{\text{OE[1:0]}}$	O_{12}	H[b]	Memory output enables.

Multimode I/O Signals Each of these pins has two or more alternate functions. Pin function is controlled via the I/O multiplexer			
Signal	**Type**	**R**	**Description**
IO0	I/O	Z	Functions: Input port 0, Output port 0, I/O strobe 0.
IO1	I/O	Z	Functions: Input port 1, Output port 1, I/O strobe 1, serial clock for serial communications unit in SPI mode.
IO2	I/O	Z	Functions: Input port 2, Output port 2, I/O strobe 2, serial data output (TxD in UART mode, SDO in SPI mode).
IO3	I/O	Z	Functions: Input port 3, Output port 3, I/O strobe 3, serial data input (RxD in UART mode, SDI in SPI mode).
IO4	I/O	Z	Functions: Input port 4, Output port 4, I/O strobe 4, refresh cycle indication from DRAM controller.
IO5	I/O	Z	Functions: Input port 5, Output port 5, I/O strobe 5, $\overline{\text{PREADY}}$.
IO6	I/O	Z	Functions: Input port 6, Output port 6, I/O strobe 6, general purpose timer 0 input.
IO7	I/O	Z	Functions: Input port 7, Output port 7, I/O strobe 7, general purpose timer 1 input.
IO8	I/O	Z	Functions: Input port 0, Output port 0, general purpose timer 0 output.
IO9	I/O	Z	Functions: Input port 1, Output port 1, general purpose timer 1 output.

Table 4: Signal Descriptions (cont'd)

Signal	Type	R	Description
$\overline{BE2}$/IO10	I/O	Z	Functions: Input port 2, Output port 2, byte enable 2 input/output (for use w/32-bit masters), end-of-process indication for DMA channel 0.
$\overline{BE3}$/IO11	I/O	Z	Functions: Input port 3, Output port 3, byte enable 3 input/output (for use w/32-bit masters), end-of-process indication for DMA channel 1.
A27/IO12	I/O	Z	Functions: Input port 4, Output port 4, A27 input pin, general purpose timer 0 output.
A28/IO13	I/O	Z	Functions: Input port 5, Output port 5, A28 input pin, general purpose timer 1 output.
A29/IO14	I/O	Z	Functions: Input port 6, Output port 6, A29 input pin, end-of-process indication for DMA channel 0.
A30/IO15	I/O	Z	Functions: Input port 7, Output port 7, A30 input pin, end-of-process indication for DMA channel 1.

Clock, Reset and Configuration Signals			
Signal	**Type**	**R**	**Description**
CLK2	I		2X clock input (in i960Jx/PPC401Gx systems, this signal is 2X the processor frequency).
$\overline{RESET}$	I_S		RESET input.
$\overline{RSTOUT}$	O	L	RESET output from watchdog timer.
EN5V[c]	I_{SU}	H	Selects 5V (driven high) or 3.3V (driven low) DRAM memory interface. An internal weak pull-up is provided for backward compatibility.

Power and Ground Signals			
Signal	**Type**	**R**	**Description**
V_{CC}	-		POWER leads for CPU I/O and internal core logic. Connect to a 5V board plane.
$V_{CC}3$	-		POWER leads for DRAM interface signals. Connect to either a 5V or 3.3V board plane as determined by EN5V (5V only prior to revision B1).
GND	-		GROUND leads intended for external connection to a GND board plane.

a. **R** indicates state during reset.
b. Reset state is 'Z' when 3.3V memory interface is selected via EN5V driven low. This feature can be used to float the DRAM signals for board testing.
c. This signal was a no-connect prior to revision B1

Table 5: Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	$\overline{\text{READY}}$	26	$\overline{\text{BE0}}$	51	A27/IO12	76	MA6
2	ALE	27	$\overline{\text{BE1}}$	52	$\overline{\text{BE3}}$/IO11	77	MA7
3	A22	28	AD0	53	$\overline{\text{BE2}}$/IO10	78	$\overline{\text{RAS1}}$
4	A21	29	V_{CC}	54	IO9	79	$\overline{\text{CAS1}}$
5	$\overline{\text{ADS}}$	30	GND	55	IO8	80	$V_{CC}3$
6	$\overline{\text{RESET}}$	31	AD1	56	IO7	81	GND3
7	$\overline{\text{DREQ0}}$	32	AD2	57	IO6	82	MA8
8	$\overline{\text{DREQ1}}$	33	AD3	58	IO5	83	MA9
9	BTYPE0	34	AD4	59	IO4	84	MA10
10	BTYPE1	35	AD5	60	IO3	85	$\overline{\text{WE}}$
11	$\overline{\text{BLAST}}$	36	AD6	61	IO2	86	$\overline{\text{OE0}}$
12	V_{CC}	37	AD7	62	IO1	87	$\overline{\text{CAS2}}$
13	GND	38	AD8	63	IO0	88	$\overline{\text{LE}}$
14	W/$\overline{\text{R}}$	39	AD9	64	$V_{CC}3$	89	$V_{CC}3$
15	HOLD	40	AD10	65	GND3	90	GND3
16	A20	41	AD11	66	MA0	91	MA11
17	A19	42	AD12	67	MA1	92	$\overline{\text{CAS3}}$
18	HLDA	43	AD13	68	MA2	93	$\overline{\text{OE1}}$
19	$\overline{\text{INT}}$	44	AD14	69	MA3	94	$\overline{\text{DACK0}}$
20	A18	45	AD15	70	$\overline{\text{RAS0}}$	95	$\overline{\text{DACK1}}$
21	A17	46	V_{CC}	71	$\overline{\text{CAS0}}$	96	A23
22	A16	47	GND	72	$V_{CC}3$	97	A24
23	$\overline{\text{RSTOUT}}$	48	A30/IO15	73	GND3	98	A25
24	CLK2	49	A29/IO14	74	MA4	99	A26
25	EN5V	50	A28/IO13	75	MA5	100	A31

Figure 2: Pinout for 100-pin EIAJ PQFP (top view)

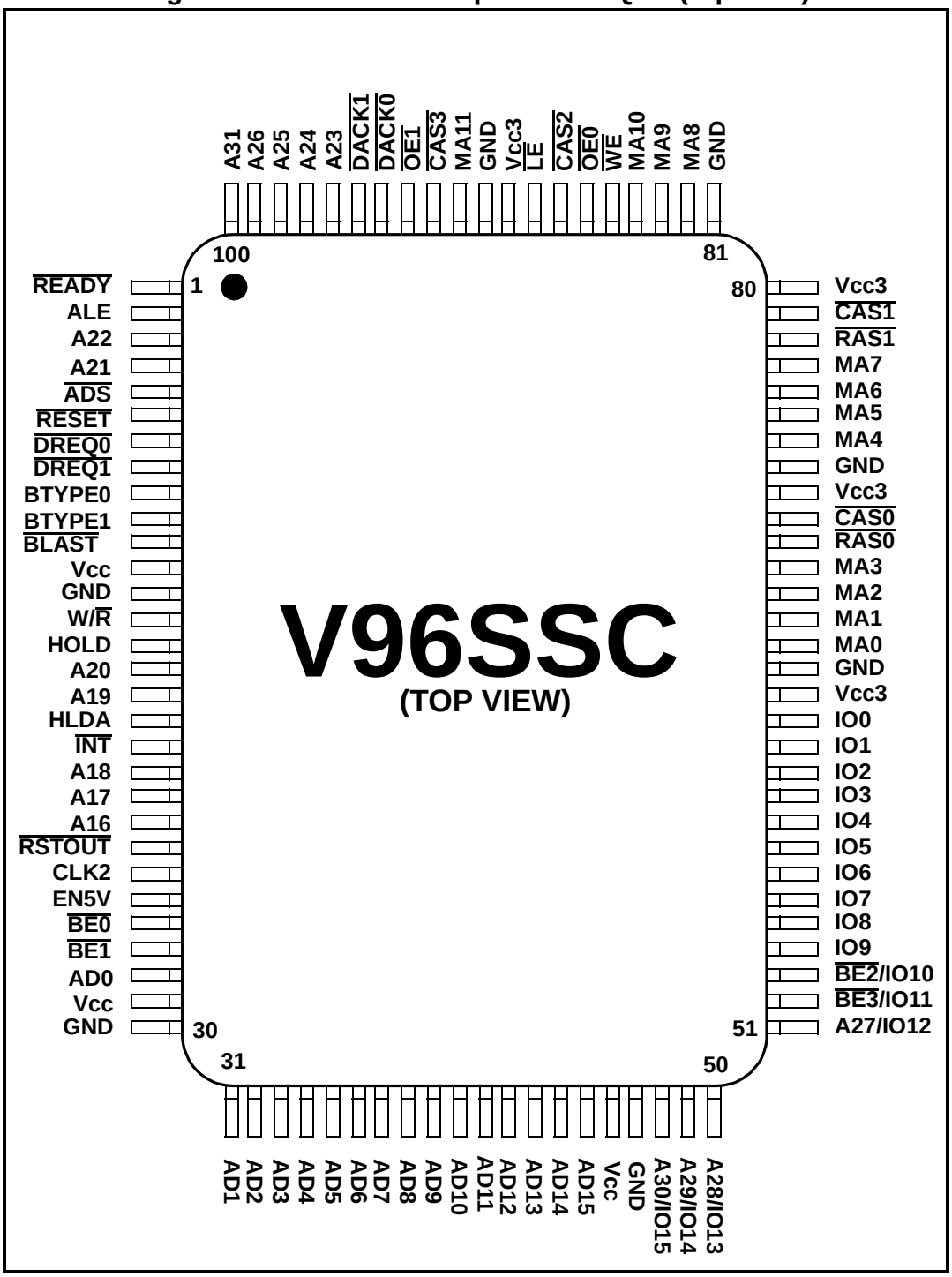
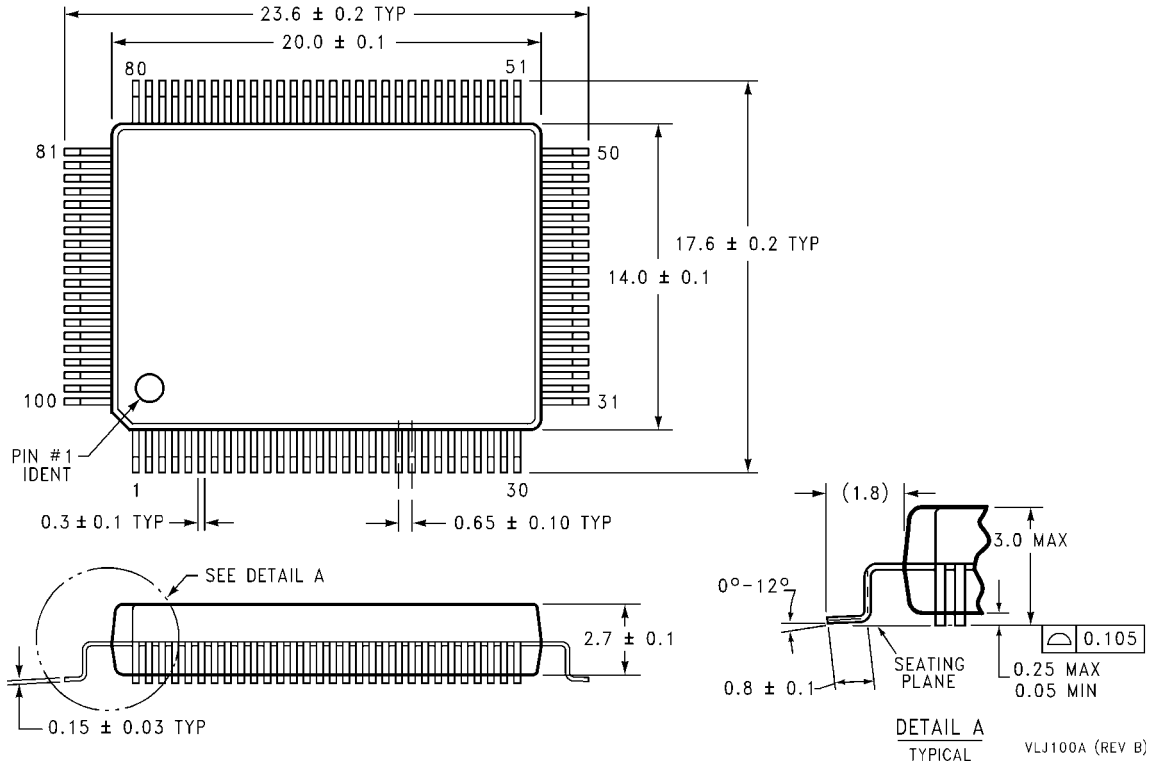


Figure 3: 100-pin EIAJ PQFP mechanical details



Unit of Measurement = millimeters

4.0 DC Specifications

The following DC specifications are based on B1 stepping silicon.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	DC input voltage	-0.3 to V_{CC}+0.3	V
I_{IN}	DC source or sink current	-50 to +50	mA
T_{STG}	Storage temperature range	-65 to 150	°C

Table 7: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	-40 to 85	°C

Table 8: DC Operating Specifications

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage	V_{CC} = 4.75V		0.8	V
V_{IH}	High level input voltage	V_{CC} = 5.25V	2.0		V
I_{IL}	Low level input current	V_{IN}=GND, V_{IN}=5.25V		-10	µA
I_{IH}	High level input current	V_{IN}=V_{IN}=5.25V		10	µA
V_{OL4}	Low level output voltage for 4mA outputs and I/O pins	I_{OL} = 4mA		0.4	V
V_{OH4}	High level output voltage for 4mA outputs and I/O pins	I_{OH} = -4mA	3.7		V
V_{OL12}	Low level output voltage for 12mA outputs and I/O pins	I_{OL} = 12mA		0.4	V
V_{OH12}	High level output voltage for 12mA outputs and I/O pins	I_{OH} = -12mA	3.7		V
I_{OZL}	Low level float input leakage	V_{IN} = GND		-10	µA
I_{OZH}	High level float input leakage	V_{IN} = V_{CC}		10	µA
I_{CC} (max)	Maximum supply current	V_{CC} = 5.5V Frequency = 20MHz		71	mA
I_{CC} (typ)	Typical supply current	V_{CC} = 5.0V Frequency = 20MHz		65	mA
C_{IO}	Input and output capacitance			20	pF

5.0 AC Specifications

The following AC specifications are based on A-0 stepping silicon.

Table 9: AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage	4.75 to 5.25	V
V_{IN}	Input low and high voltages	0.8 and 2.4	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 10: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Derating
4mA	0.11ns/pF for loads > 50pF
12mA	0.04ns/pF for loads > 50pF

Figure 4: Clock and Synchronous Signals

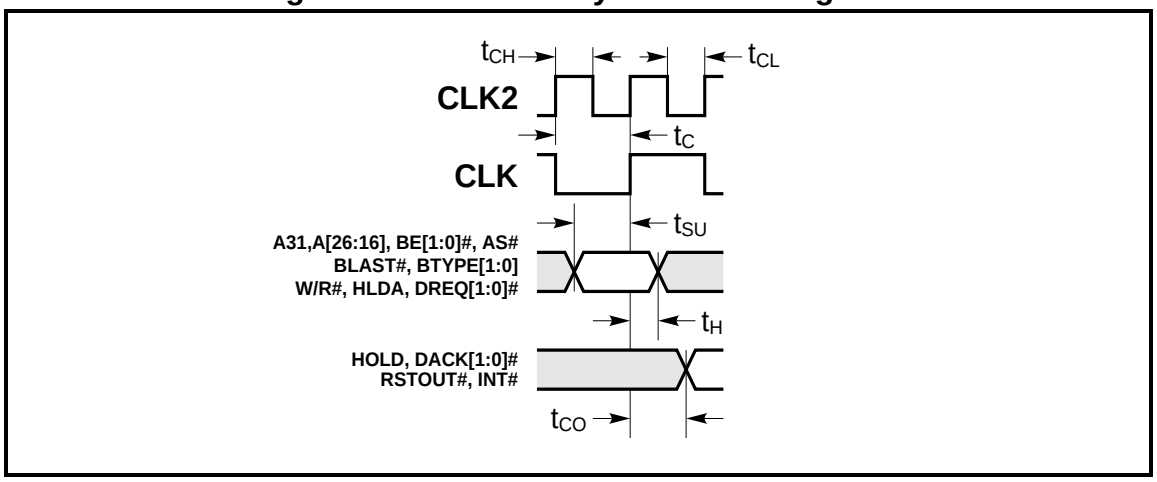


Figure 5: ALE Signal

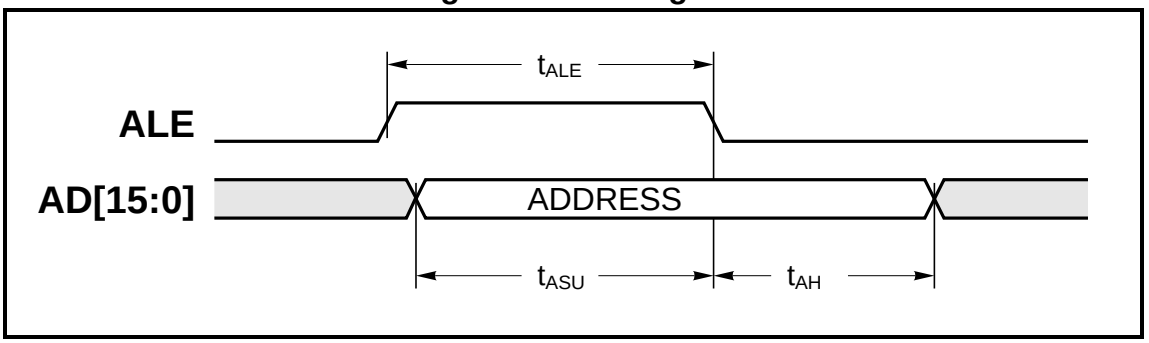


Table 11: Clock, ALE, Synchronous Inputs and Outputs

				33 MHz		
#	Symbol	Description	Notes	Min	Max	Units
1	t_C	CLK2 period		15		ns
2	t_{CH}	CLK2 high time		6		ns
3	t_{CL}	CLK2 low time		6		ns
4	t_{SU}	Synchronous input setup		10		ns
5	t_H	Synchronous input hold			3	ns
6	t_{CO}	CLK2 to synchronous output delay	1		12	ns
7	t_{ALE}	ALE pulse width		t_C-7		ns
8	t_{ASU}	Address setup to ALE falling		3		ns
9	t_{AH}	Address hold from ALE falling		1		ns

Notes:
1. t_{CO} is for signals $\overline{\text{RSTOUT}}$, HOLD, $\overline{\text{DACKx}}$, and $\overline{\text{INT}}$.

Figure 6: Internal Register Read/Write Waveforms

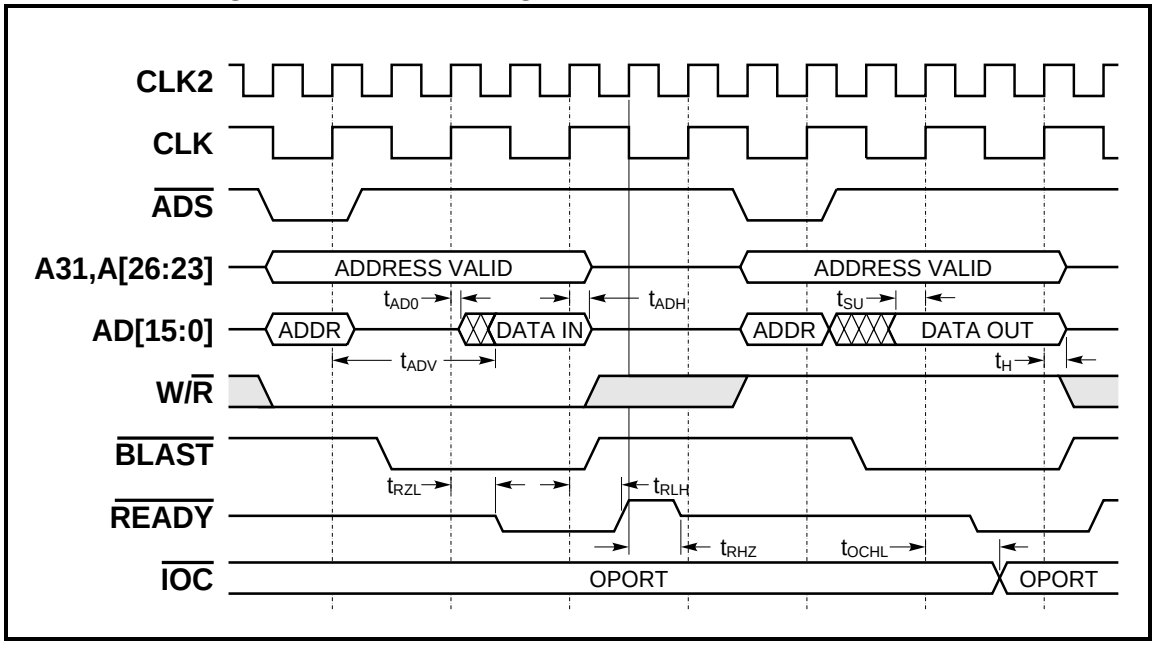


Table 12: Timing Relationships for Internal Register Read/Write

#	Sym-bol	Description	Notes	33 MHz Min	33 MHz Max	Units
1	t_{ADO}	CLK2 to Data Output driving delay	1	4	12	ns
2	t_{ADV}	CLK2+$\overline{ADS}$ to internal register data valid, read access time	1		49	ns
3	t_{ADH}	Data hold after CLK2	1	3		ns
4	t_{PD}	IO asynchronous chip-select output delay	2		19	ns
5	t_{OC}	IO synchronous strobe output delay from CLK2	3		18	ns
6	t_{RZL}	$\overline{READY}$ float to driving low from CLK2		3	12	ns
7	t_{RLH}	$\overline{READY}$ low to high delay from CLK2			11	ns
8	t_{RHZ}	$\overline{READY}$ high to float delay from CLK2			12	ns
9	t_{RFV}	$\overline{REFRESH}$ (synchronous) output delay			14	ns

Notes:
1. For V96SSC internal register read.
2. Delays are measured from address valid and ALE asserted.
3. In IOC mode, delays are measured from CLK2 when CLK is high and $\overline{ADS}$ is asserted. In OPORT mode, delays are measured from CLK2 when CLK is high during Td cycle.

Figure 7: Memory Timing Waveforms

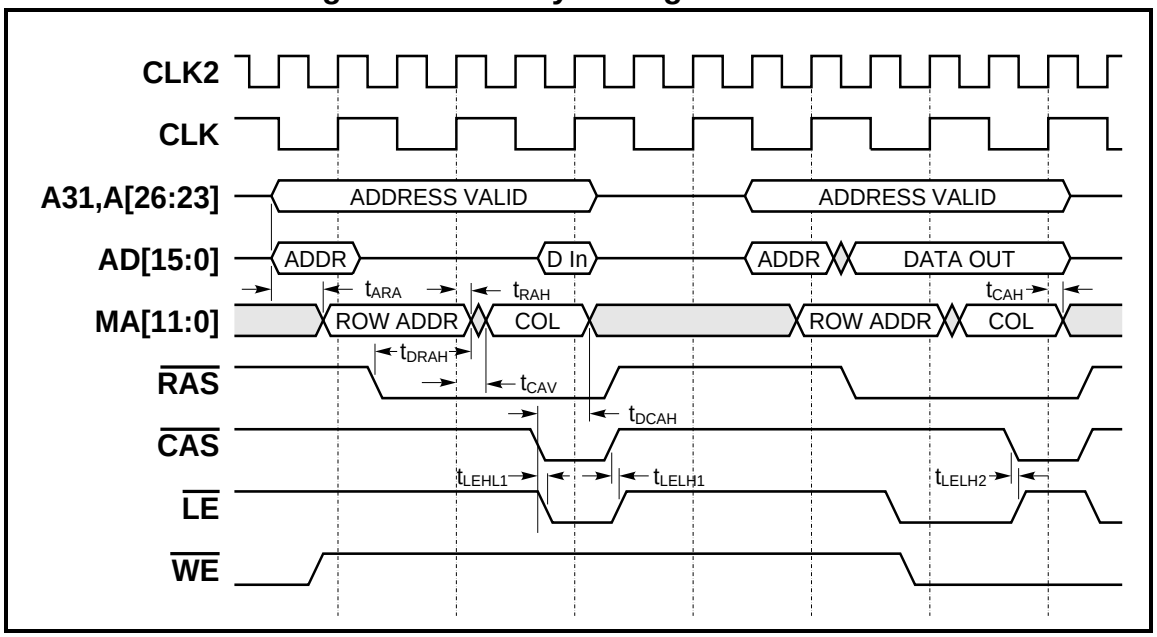


Table 13: Memory Interface Signals

				33 MHz		
#	Sym-bol	Description	Notes	Min	Max	Units
1	t_{ARA}	Address input valid to row address valid on MA[11:0]	1		13	ns
2	t_{RAH}	Row address hold after CLK2		3		ns
3	t_{CAV}	CLK2 to column address valid	1		12	ns
4	t_{CAH}	Column address hold after CLK2 or $\overline{CLK2}$	1,2	4		ns
5	t_{BCAH}	Column address hold after CLK2 or $\overline{CLK2}$ during burst operation	1,2	4		ns
6	t_{BCAV}	CLK2 or $\overline{CLK2}$ to column address valid during burst operation	1,2		14	ns
7	t_{DRAH}	DRAM row address hold	3	tM+1		ns
8	t_{DCAH}	DRAM column address hold	4	tN+1		ns
9	t_{RSHL}	CLK2 to $\overline{RAS}$ asserted delay	1		9	ns
10	t_{RSLH}	CLK2 to $\overline{RAS}$ de-asserted delay	1		9	ns
11	t_{CHL1}	CLK2 to CAS asserted delay	1		11	ns
12	t_{CLH1}	CLK2 to CAS de-asserted delay	1		10	ns
13	t_{CHL2}	$\overline{CLK2}$ to CAS asserted delay	1,5		10	ns
14	t_{CLH2}	$\overline{CLK2}$ to CAS de-asserted delay	1,6		10	ns
15	t_{OEHL}	CLK2 to OE asserted delay	1		10	ns
16	t_{OELH}	CLK2 to OE de-asserted delay	1		9	ns
17	t_{WEHL}	CLK2 to WE asserted delay	1		10	ns
18	t_{WELH}	CLK2 to $\overline{WE}$ de-asserted delay	1		10	ns
19	t_{LEHL1}	$\overline{CAS}$ asserted to LE asserted delay (read)	1		1	ns
20	t_{LELH1}	$\overline{CAS}$ de-asserted to LE de-asserted (read)	1		1	ns
21	t_{LEHL2}	$\overline{CAS}$ asserted to LE de-asserted delay (write)	1,7		1	ns
22	t_{LELH2}	$\overline{CAS}$ de-asserted to LE asserted (write)	1,7		1	ns

Note:
1. The delay is from CPU Address valid or ALE if it comes first.
Derate given delays by 0.058 ns per pF of load in excess of 50pF.
2. Relative to $\overline{CLK2}$ only when T_CACA_RD or T_CACA_WR equals 0.
3. tM = (1 CLK2 period) * (T_RACA+1).
4. tN = (1/2 CLK2 period) * (T_CACA_RD + 1) for Read or (1/2 CLK2 period)*(T_CACA_WR+1) for 0-wait states write.
5. For Read Mode 2 and Write Mode 1 only.
6. For Write Mode 1 only.
7. For CAS Write Mode 0 and 1.

6.0 Revision History

Table 14: Revision History

Revision Number	Date	Comments and Changes
2.3	11/97	First release of RevB1 data sheet.
2.2	10/96	Data Book revision.
2.1	08/96	Updated timing specification.
2.01	11/95	Fixed incorrect polarity on some ALE and $\overline{RESOUT}$ signals. Fixed W/$\overline{R}$ description.
2.0	11/95	Final Data Sheet. All specifications guaranteed from actual silicon. DC input levels changed to TTL compatible. Removed 16MHz and 20MHz timing specification.
1.2	03/95	First released version of the data sheet. Some changes to AC and DC specifications and to waveforms. All future changes to the data sheet will be documented in detail in this section.
1.0	01/95	First pre-silicon revision of preliminary data sheet. Sent only to a limited number of customers.

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