V300PSC Rev A0

PCI Bus Target Interface

Datasheet

Revision 1.1

V300PSC Rev. A0

PCI BUS TARGET INTERFACE

- A general purpose PCI bus target interface
- Multiplexed and de-multiplexed 32-, 16-, or 8-bit local bus interface
- Fully compliant with PCI 2.1 specification
- Large, 288-byte FIFOs using V3's unique *DYNAMIC BANDWIDTH ALLOCATION™* architecture
- On-the-fly byte order (endian) conversion including automatic endian detection
- Address space remapping
- Mailboxes w/doorbell interrupts
- Flexible PCI and local interrupt management
- Serial EEPROM configuration interface
- 33MHz local bus with independent PCI bus operation up to 33MHz
- Low cost 160-pin EIAJ PQFP package

The V300PSC provides the highest performance, most flexible, and most economical method to connect a general purpose 32-, 16-, 8-bit local bus to the PCI bus. V3 Semiconductor's simple to use local bus interface makes the V300PSC the fastest route to adding PCI to your system. The V300PSC may be used in systems without a CPU for a generic PCI target interface.

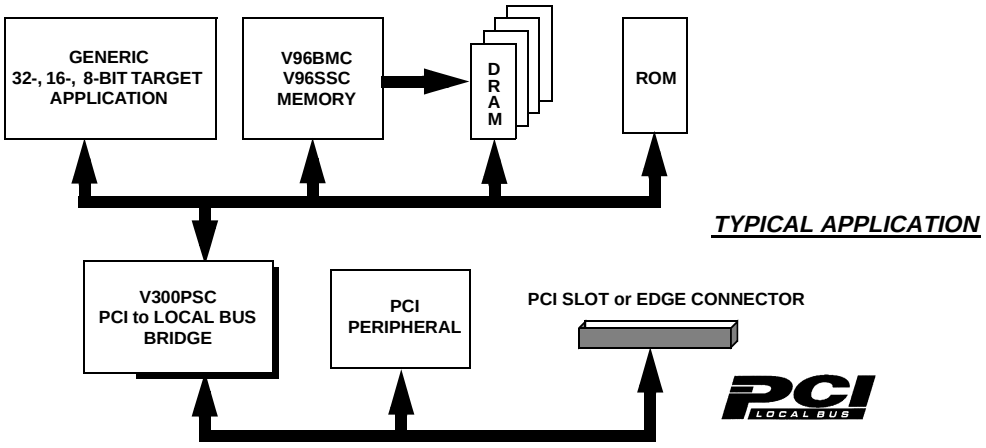
The V300PSC supports independent interface speeds allowing the PCI bus to run at the full 33MHz frequency, regardless of local bus clock rate. The V300PSC uses the unique *DYNAMIC BANDWIDTH ALLOCATION™* FIFOs to decouple the local and PCI bus, while dramatically improving the overall throughput of the system.

A PCI master can gain access to the local bus through two programmable address apertures with address remapping capabilities, and on-the-fly byte order conversion.

To support existing DOS I/O devices a special decoder mode allows up to 3 I/O regions (and one memory region below 1MB) to be decoded.

The V300PSC's interrupt control mechanism is very flexible and allows interrupts from multiple sources on the local bus to share a single PCI interrupt.

The V300PSC operates up to 33MHz, and is packaged in a low cost, 160-pin EIAJ Plastic Quad Flat Pack (PQFP) package.



TYPICAL APPLICATION

This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V300PSC. Detailed functional information is contained in the V300PSC User's Manual.

V3 Semiconductor retains the rights to change documentation, specifications, or device functionality at any time without notice. Please verify that you have the latest copy of all documents before finalizing a design.

1.0 Product Codes

Table 1: Product Codes

Product Code	Local Bus Type	Package	Frequency
V300PSC-33 REV A0	32-,16-,8- bit multiplexed / demultiplexed	160-pin EIAJ PQFP	33MHz

2.0 Pin Description and Pinout

Table 2 below lists the pin types found on the V300PSC. Table 3 and 4 describe modes and function of each pin on the V300PSC. Table 5 and Table 6 list the pins by pin number. Figure 1 and Figure 2 show the pinout for the 160-pin EIAJ PQFP package and Figure 3 shows the mechanical dimensions of the package.

Table 2: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/O_D	PCI input with open drain output.
I/O_4	TTL I/O pin with 4mA output drive.
I	TTL input only pin.
O_4	TTL output pin with 4mA output drive.

Table 3: RESET State for Configuration and Test Mode Pins

PIN#	**134** (ALE)	**135** ($\overline{\text{BTERM}}$)	**153**
Connection for de-multiplexed bus	Pull-Up	Pull-Up	Pull-Up
Connection for multiplexed bus	Pull-Down	Pull-Up	Pull-Down

Table 4: Signal Descriptions

PCI Bus Interface			
Signal	**Type**	**R[a]**	**Description**
AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
C/$\overline{\text{BE}}$[3:0]	PCI I	Z	Bus Command and Byte Enables, multiplexed on the same pins.
PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and C/$\overline{\text{BE}}$[3:0].
$\overline{\text{FRAME}}$	PCI I	Z	Cycle Frame indicates the beginning and burst length of an access.
$\overline{\text{IRDY}}$	PCI I	Z	Initiator Ready indicates the master agent is ready to complete the current data phase of the transaction.
$\overline{\text{TRDY}}$	PCI O	Z	Target Ready indicates the target agent's (V300PSC) ability to complete the current data phase of the transaction.
$\overline{\text{STOP}}$	PCI O	Z	Stop indicates the V300PSC is requesting the master to stop the current transaction (retry or disconnect).
$\overline{\text{DEVSEL}}$	PCI O	Z	Device Select, indicates the V300PSC device has decoded its address as the target of the current access.
IDSEL	PCI I	Z	Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
PCLK	PCI I	Z	PCLK provides timing for all transactions on the PCI bus.
$\overline{\text{PRST}}$	PCI I	Z	Asserted low to bring all internal operations to a reset state.
$\overline{\text{PERR}}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERR}}$	PCI I/O_D	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{\text{INT}}$[A:D]	PCI I/O_D	Z	Level-sensitive interrupt requests may be received or generated.

Serial EEPROM Interface			
Signal	**Type**	**R**	**Description**
SCL/$\overline{\text{LPERR}}$	O_4	X	EEPROM clock. Local parity error.
SDA	I/O_4	X	EEPROM data.

Table 4: Signal Descriptions (cont'd)

Local Bus Interface			
Signal	**Type**	**R**	**Description**
LAD[31:0]	I/O_4	Z	Local address and multiplexed data bus (multiplexed mode).
LA[5:2]	O_4	Z	Lower local address bus. Generated during local bus master cycles and incremented during a burst (multiplexed mode).
LD[31:0]	I/O_4	Z	Local data bus (de-multiplexed mode).
LA[31:2]	I/O_4	Z	Local address bus (de-multiplexed mode).
$\overline{BE[3:0]}$	I/O_4	Z	Local bus byte enables.
W/$\overline{R}$	I/O_4	Z	Write/$\overline{Read}$.
ALE	I/O_4	Z	Address Latch Enable: used to latch the address during the address phase (multiplexed mode).
$\overline{ADS}$	I/O_4	Z	Asserted low to indicate the beginning of a bus cycle.
$\overline{RDYRCV}$ $\overline{READY}$	I/O_4	Z	Local Bus data ready.
HOLD	O_4	L	Local bus hold request: asserted by the P3PSC to initiate a local bus master cycle.
HOLDA	I		Local bus hold acknowledge.
LPAR[3:0]	I/O_4	Z	Local bus parity.
$\overline{BLAST}$	I/O_4	Z	Burst last.
$\overline{BTERM}$	I/O_4	Z	Bus Time-out. Burst terminate.
LINT	O_4	H	Local interrupt request.
$\overline{LRST}$	I/O_4	L/Z	Local bus RESET signal.
LCLK	I		Local bus clock.

Power and Ground Signals			
Signal	**Type**	**R**	**Description**
V_{CC}	-		POWER pins for connection to the board's V_{CC} plane.
GND	-		GROUND pins for connection to the board's GND plane.

a. **R** indicates state during reset.

Table 5: Pin Assignments (multiplexed bus)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{INTD}$	42	AD14	82	NC	122	NC
3	$\overline{PRST}$	43	AD13	83	LAD8	123	LAD25
4	PCLK	44	AD12	84	NC	124	LA5
5	’1’	45	AD11	85	LAD9	125	LAD26
6	NC	46	AD10	86	NC	126	LA4
7	AD31	47	AD9	87	LAD10	127	LAD27
8	AD30	48	AD8	88	NC	128	LA3
9	AD29	49	C/$\overline{BE0}$	89	LAD11	129	LAD28
10	AD28	50	V_{CC}	90	NC	130	LA2
11	GND	51	GND	91	LAD12	131	LAD29
12	AD27	52	AD7	92	NC	132	LAD30
13	AD26	53	AD6	93	LAD13	133	LAD31
14	AD25	54	AD5	94	NC	134	ALE
15	AD24	55	AD4	95	LAD14	135	$\overline{BTERM}$
16	C/$\overline{BE3}$	56	AD3	96	NC	136	$\overline{RDYRCV}$
17	IDSEL	57	AD2	97	LAD15	137	HOLD
18	AD23	58	AD1	98	NC	138	HOLDA
19	AD22	59	AD0	99	LAD16	139	$\overline{ADS}$
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LAD0	102	NC	142	LCLK
23	AD20	63	NC	103	LAD17	143	GND
24	AD19	64	LAD1	104	NC	144	V_{CC}
25	AD18	65	NC	105	LAD18	145	$\overline{BE3}$
26	AD17	66	LAD2	106	NC	146	$\overline{BE2}$

Table 5: Pin Assignments (multiplexed bus) (cont'd)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
27	AD16	67	NC	107	LAD19	147	$\overline{BE1}$
28	C/$\overline{BE2}$	68	LAD3	108	NC	148	$\overline{BE0}$
29	$\overline{FRAME}$	69	NC	109	LAD20	149	$\overline{BLAST}$
30	GND	70	LAD4	110	NC	150	W/$\overline{R}$
31	$\overline{IRDY}$	71	NC	111	LAD21	151	'1'
32	$\overline{TRDY}$	72	LAD5	112	NC	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	NC	113	LAD22	153	'0'
34	$\overline{STOP}$	74	LAD6	114	NC	154	$\overline{LINT}$
35	$\overline{PERR}$	75	NC	115	LAD23	155	SDA
36	$\overline{SERR}$	76	LAD7	116	NC	156	SCL/ $\overline{LPERR}$
37	PAR	77	NC	117	LPAR2	157	$\overline{INTA}$
38	C/$\overline{BE1}$	78	LPAR0	118	LPAR3	158	$\overline{INTB}$
39	AD15	79	LPAR1	119	LAD24	159	$\overline{INTC}$
40	GND	80	GND	120	GND	160	GND

Table 6: Pin Assignments (de-multiplexed bus)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{INTD}$	42	AD14	82	LA23	122	LA6
3	$\overline{PRST}$	43	AD13	83	LD8	123	LD25
4	PCLK	44	AD12	84	LA22	124	LA5
5	'1'	45	AD11	85	LD9	125	LD26
6	NC	46	AD10	86	LA21	126	LA4
7	AD31	47	AD9	87	LD10	127	LD27
8	AD30	48	AD8	88	LA20	128	LA3

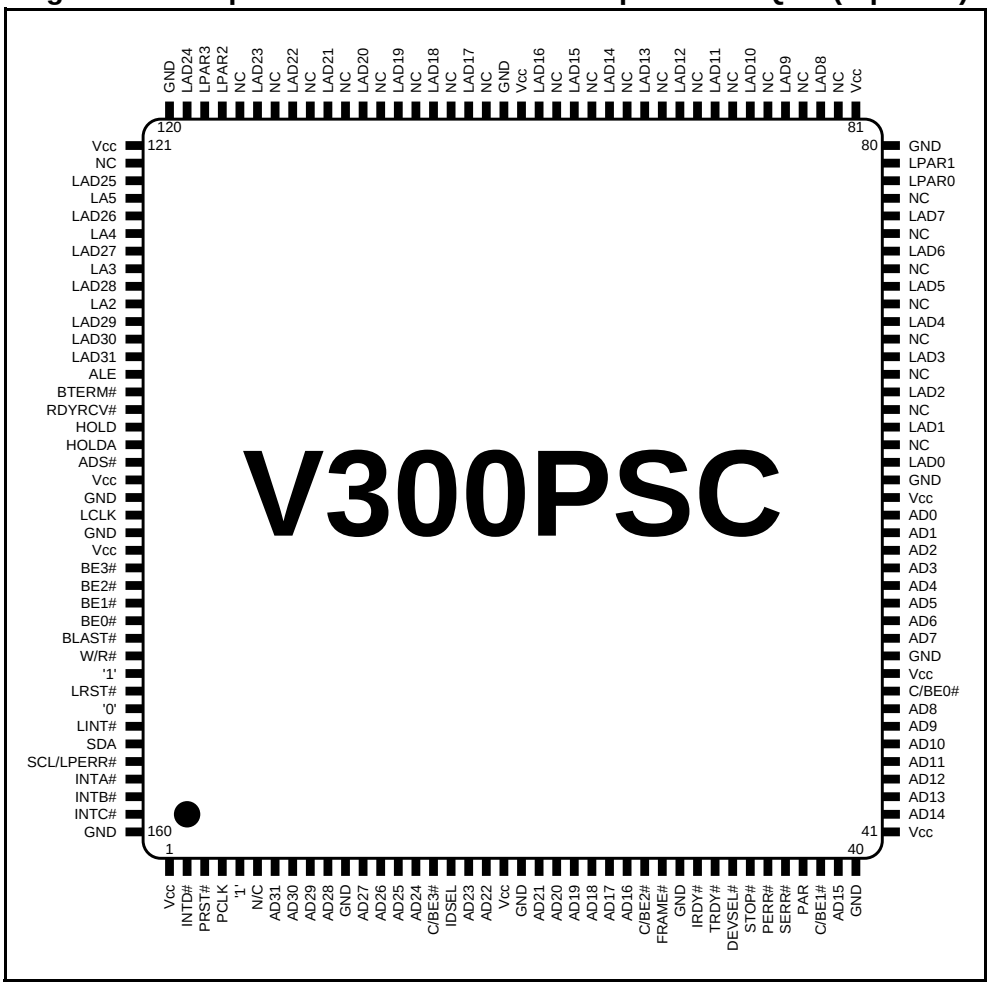
Table 6: Pin Assignments (de-multiplexed bus) (cont'd)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
9	AD29	49	C/$\overline{BE0}$	89	LD11	129	LD28
10	AD28	50	V_{CC}	90	LA19	130	LA2
11	GND	51	GND	91	LD12	131	LD29
12	AD27	52	AD7	92	LA18	132	LD30
13	AD26	53	AD6	93	LD13	133	LD31
14	AD25	54	AD5	94	LA17	134	'1'
15	AD24	55	AD4	95	LD14	135	$\overline{BTERM}$
16	C/$\overline{BE3}$	56	AD3	96	LA16	136	$\overline{READY}$
17	IDSEL	57	AD2	97	LD15	137	HOLD
18	AD23	58	AD1	98	LA15	138	HOLDA
19	AD22	59	AD0	99	LD16	139	$\overline{ADS}$
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LD0	102	LA14	142	LCLK
23	AD20	63	LA31	103	LD17	143	GND
24	AD19	64	LD1	104	LA13	144	V_{CC}
25	AD18	65	LA30	105	LD18	145	$\overline{BE3}$
26	AD17	66	LD2	106	LA12	146	$\overline{BE2}$
27	AD16	67	LA29	107	LD19	147	$\overline{BE1}$
28	C/$\overline{BE2}$	68	LD3	108	LA11	148	$\overline{BE0}$
29	$\overline{FRAME}$	69	LA28	109	LD20	149	$\overline{BLAST}$
30	GND	70	LD4	110	LA10	150	W/$\overline{R}$
31	$\overline{IRDY}$	71	LA27	111	LD21	151	'1'
32	$\overline{TRDY}$	72	LD5	112	LA9	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	LA26	113	LD22	153	'1'
34	$\overline{STOP}$	74	LD6	114	LA8	154	$\overline{LINT}$
35	$\overline{PERR}$	75	LA25	115	LD23	155	SDA

Table 6: Pin Assignments (de-multiplexed bus) (cont'd)

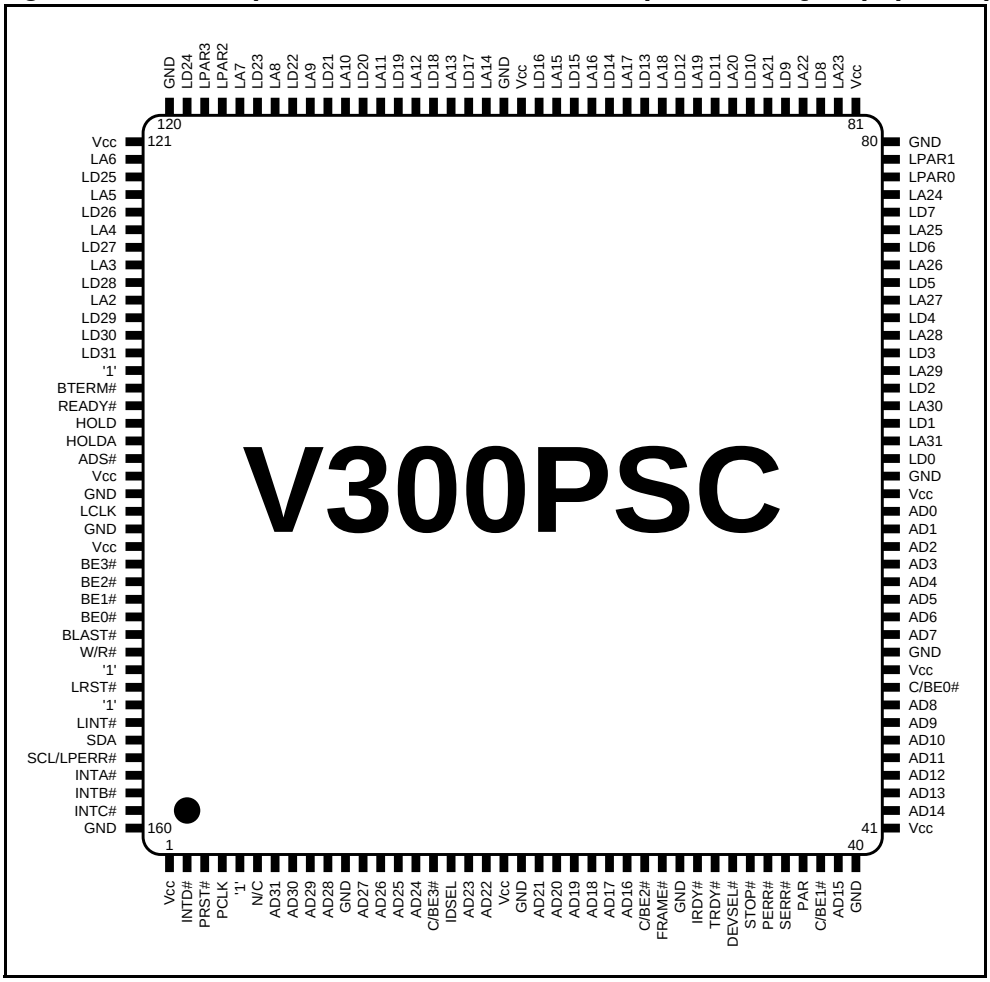
PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
36	$\overline{\text{SERR}}$	76	LD7	116	LA7	156	SCL/ $\overline{\text{LPERR}}$
37	PAR	77	LA24	117	LPAR2	157	$\overline{\text{INTA}}$
38	C/$\overline{\text{BE1}}$	78	LPAR0	118	LPAR3	158	$\overline{\text{INTB}}$
39	AD15	79	LPAR1	119	LD24	159	$\overline{\text{INTC}}$
40	GND	80	GND	120	GND	160	GND

Figure 1: Multiplexed Mode Pinout for 160-pin EIAJ PQFP (top view)



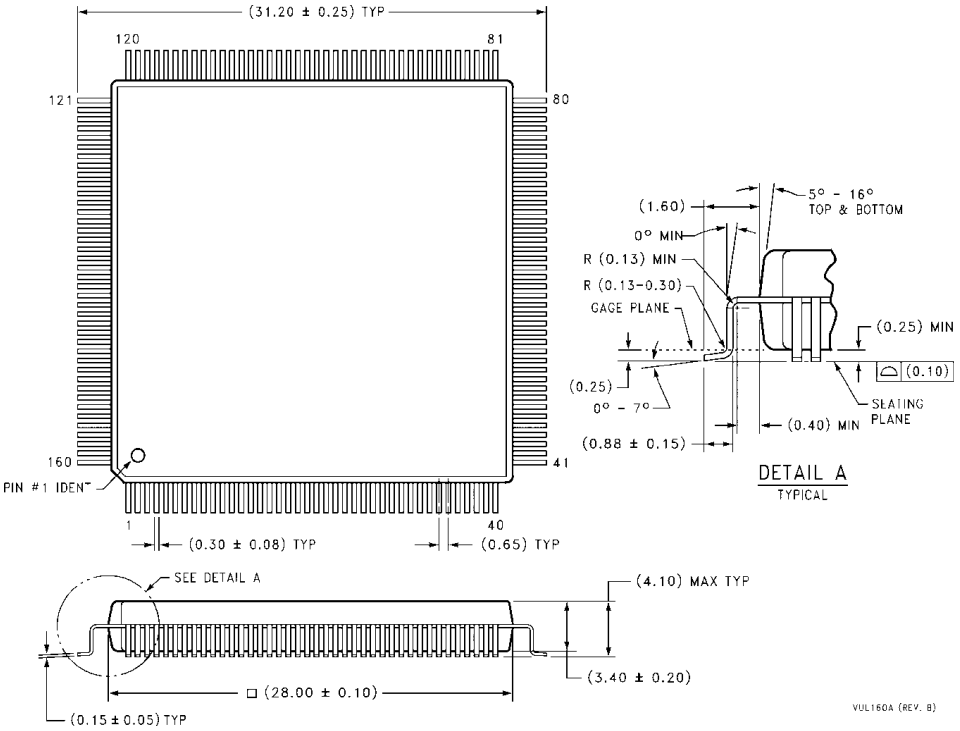
V300PSC require pull-down resistor on ALE and pull-up resistor on $\overline{\text{BTERM}}$ to ensure proper multiplexed mode operation.

Figure 2: De-Multiplexed Mode Pinout for 160-pin EIAJ PQFP (top view)



V300PSC require pull-up resistors on ALE and $\overline{\text{BTERM}}$ to ensure proper de-multiplexed mode operation.

Figure 3: 160-pin EIAJ PQFP mechanical details



Unit of Measurement = millimeters

3.0 DC Specifications

The DC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.1. For more information on the PCI DC specifications, see the PCI Specification.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	-0.3 to +7	V
V_{IN}	DC input voltage	-0.3 to V_{CC}+0.3	V
I_{IN}	DC input current	± 10	mA
T_{STG}	Storage temperature range	-40 to +125	°C

Table 8: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	4.75 to 5.25	V
T_A	Ambient temperature range	0 to 70	°C

3.1 PCI Bus DC Specifications

Table 9: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input high voltage		2.0	V_{CC}+0.5	V	
V_{IL}	Input low voltage		-0.5	0.8	V	
I_{IH}	Input high leakage current	V_{IN} = 2.7V		70	µA	1
I_{IL}	Input low leakage current	V_{IN} = 0.5V		-70	µA	1
V_{OH}	Output high voltage	I_{OUT} = -2mA	2.4		V	
V_{OL}	Output low voltage	I_{OUT} = 3mA, 6mA		0.55	V	2
C_{IN}	Input pin capacitance			10	pF	3
C_{CLK}	PCLK pin capacitance		5	12	pF	
C_{IDSEL}	IDSEL pin capacitance			8	pF	4
L_{PIN}	Pin inductance			20	nH	

Notes:
1. Input leakage currents include high impedance output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pullup resistors have greater than 3mA low output current. Signals requiring pull resistors have greater than 6mA output current. The latter include $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, $\overline{SERR}$, $\overline{PERR}$.
3. Absolute maximum pin capacitance for a PCI unit is 10pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

3.2 Local Bus DC Specifications

Table 10: Local Bus Signals DC Operating Specifications

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage	V_{CC} = 4.75V		0.8	V
V_{IH}	High level input voltage	V_{CC} = 5.25V	2.0		V
I_{IL}	Low level input current	V_{IN}=GND, V_{CC}=5.25V	-10		µA
I_{IH}	High level input current	V_{IN} = V_{CC} = 5.25V		10	µA
V_{OL4}	Low level output voltage for 4 mA outputs and I/O pins	I_{OL} = -4 mA		0.4	V
V_{OH4}	High level output voltage for 4 mA outputs and I/O pins	I_{OH} = 4 mA	2.4		V
I_{OZL}	Low level float input leakage	V_{IN} = GND	-10		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{CC}		10	µA
I_{CC} (max)	Maximum supply current	V_{CC} = 5.25V PCLK = LCLK = 33MHz		150	mA
I_{CC} (typ)	Typical supply current	V_{CC} = 5.0V PCLK = LCLK = 33MHz		120	mA
C_{IO}	Input and output capacitance			10	pF

4.0 AC Specifications

The AC specifications for the PCI bus signals match exactly those given in the PCI Specification, Rev. 2.1, Section 4.2.1.2. For more information on the PCI AC specifications, including the V/I curves for 5V signalling, see section 4.2.1.2 of Rev 2.1 PCI Specification.

4.1 PCI Bus Timings

Table 11: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
$I_{OH(AC)}$	Switching current high	$0V<V_{OUT}\leq 1.4V$	-44		mA	1
		$1.4V<V_{OUT}<2.4V$	$-44+(V_{OUT}-1.4)/0.024$	Equation A	mA	1, 2, 3
	(Test point)	$V_{OUT}=3.1V$		-142	mA	3
$I_{OL(AC)}$	Switching current low	$V_{OUT}\geq 2.2V$	95		mA	1
		$2.2V>V_{OUT}>0.55$	$V_{OUT}/0.023$	Equation B	mA	1, 3
	(Test point)	$V_{OUT}=0.71$		206	mA	3
I_{CL}	Low clamp current	$-5<V_{IN}\leq -1$	$-25+(V_{IN}+1)/0.015$		mA	
t_R	Unloaded output rise time	0.4V to 2.4V	1	5	V/ns	4
t_F	Unloaded output fall time	2.4V to 0.4V	1	5	V/ns	4

Notes:
1. Refer to the V/I curves in Section 4.2.1 of the PCI Specification. This specification does not apply to CLK and $\overline{RST}$ which are system outputs. “Switching Current High” specifications are not relevant to open drain outputs such as $\overline{SERR}$ and $\overline{INTA}$-$\overline{INTD}$.
2. Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as it does in the pull-down curve). This difference is intended to allow for an optional N-channel pullup.
3. Maximum current requirements are met as drivers pull beyond the first step voltage (AC drive point). Equations defining these maximums (A and B) are provided with the respective V/I curves given in the PCI Spec. The equation defined maxima is met by design.
4. The minimum slew rate (slowest signal edge) is met by the PCI drivers. The maximum slew rate (fastest signal edge) is a guideline. Motherboard designers must bear in mind that rise and fall times faster than this maximum guideline could occur, and should ensure that signal integrity modeling accounts for this.

Equation A: $I_{OH} = 11.9\cdot(V_{OUT} - 5.25V)\cdot(V_{OUT} + 2.45V)$ for $V_{CC} > V_{OUT} > 3.1V$

Equation B: $I_{OL} = 78.5\cdot V_{OUT}(4.4V - V_{OUT})$ for $0V < V_{OUT} < 0.71V$

4.2 Local Bus Timings

Table 12: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage	4.75 to 5.25	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 13: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Derating
4mA	0.058 ns/pF for loads > 50pF

Figure 4: Clock and Synchronous Signals

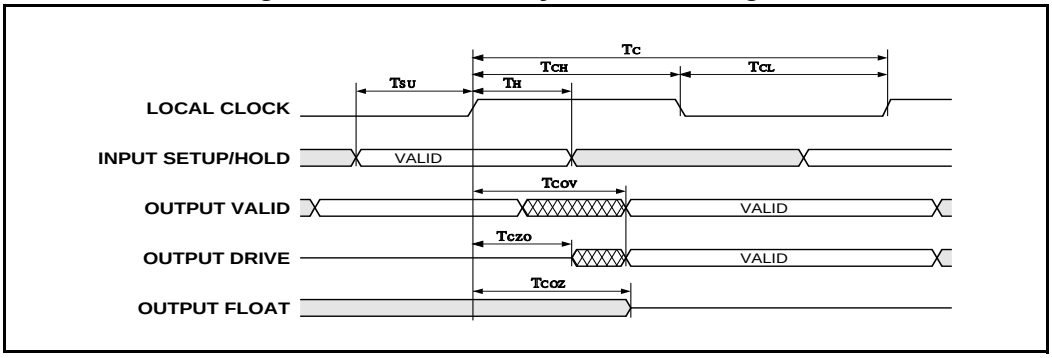


Figure 5: ALE Signal

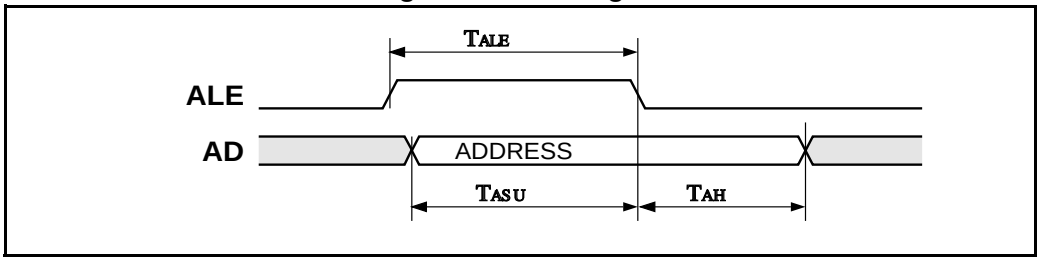


Table 14: Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		
#	Symbol	Description	Notes	Min	Max	Units
1	T_C	LCLK period		30		ns
2	T_{CH}	LCLK high time	1	12		ns
3	T_{CL}	LCLK low time	1	12		ns
4	T_{SU}	Synchronous input setup	2	7		ns
4a	T_{SU}	Synchronous input setup ($\overline{BTERM}$)		4		ns
4b	T_{SU}	Synchronous input setup (data)		5		ns
5	T_H	Synchronous input hold			2	ns
6	T_{COV}	LCLK to output valid delay	3	3	14	ns
6a	T_{COV}	LCLK to output valid delay (address, data, byte enable, parity)		3	15	ns
7	T_{CZO}	LCLK to output driving delay		3	15	ns
8	T_{COZ}	LCLK to high impedance delay	4	3	15	ns

Notes:
1. Measured at 1.5V.
2. All local bus signals except those in 4a, 4b, 4c.
3. All local bus signals except those in 6a.
4. $\overline{READY}$, $\overline{BLAST}$, $\overline{ADS}$ are driven to high impedance at the falling edge of LCLK.

Table 15: ALE Timing Parameters for Vcc = 5 Volts +/- 5%

			33MHz		
#	Symbol	Description	Min	Max	Units
1	T_{ALE}	ALE Pulse Width	T_{CH}-4		ns
2	T_{ASU}	Address setup to ALE falling (ALE as output)	T_{CH}-5		ns
3	T_{AH}	Address hold from ALE falling (ALE as output)	T_{CL}-5		ns

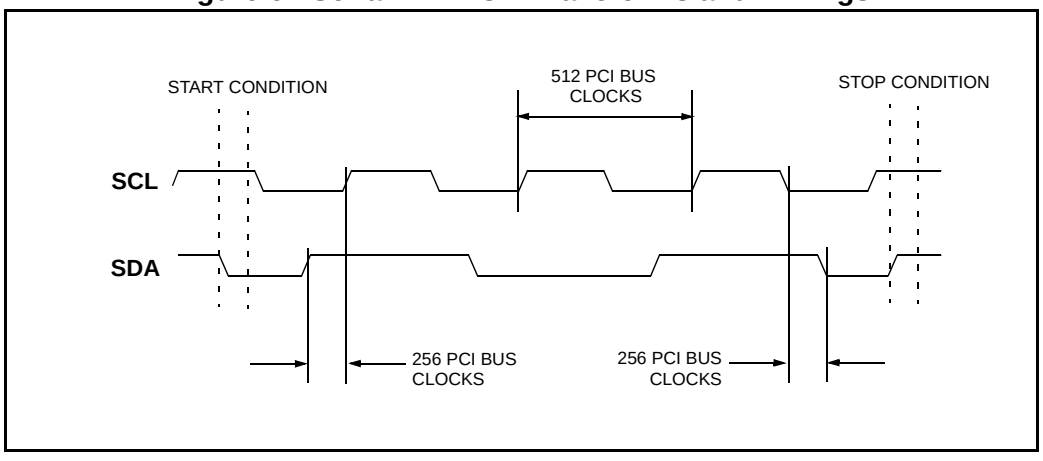
Table 16: PCI Bus Timing Parameters for Vcc = 5 Volts +/- 5%

#	Symbol	Description	Notes	Min	Max	Units
1	T_C	PCLK period		30		ns
2	T_{SU}	Synchronous input setup to PCLK	1	7		ns
3	T_H	Synchronous input hold from PCLK		0		ns
4	T_{COV}	PCLK to output valid delay	2	3	11	ns
5	T_{CZO}	PCLK to output driving delay		4	11	ns
6	T_{COZ}	PCLK to high impedance delay		5	18	ns
7	T_{RST}	Reset period		$16 \cdot T_C$		

4.3 Serial EEPROM Port TImings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in Figure 6.

Figure 6: Serial EEPROM Waveforms and Timings



5.0 Revision History

Table 17: Revision History

Revision Number	Date	Comments and Changes
1.1	4/97	Second revision. Updated signal names and product codes.
1.0	3/97	Preliminary data sheet. DC and AC specs TBD. Sent only to a limited number of customers.

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