N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-92	Die†
400V	35Ω	250mA	VN0540N3	VN0540ND

† MIL visual screening available

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

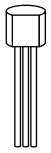
These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor controls
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Package Options



S G D

TO-92

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	100mA	400mA	1.0W	125	170	100mA	400mA

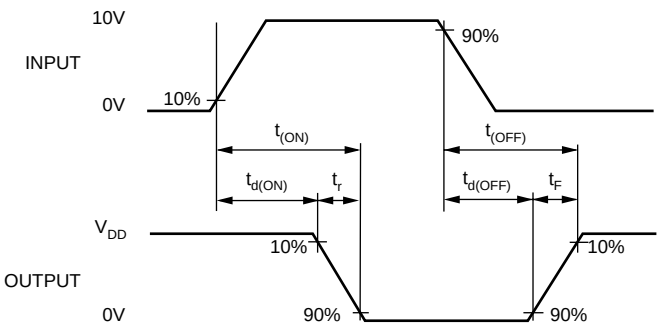
* I_D (continuous) is limited by max rated T_j.

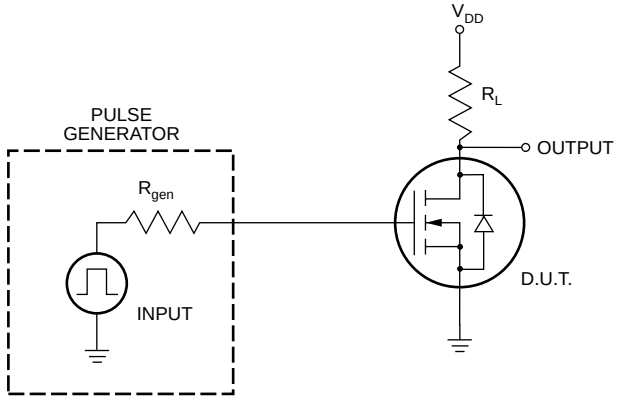
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	400			V	V_{GS} = 0V, I_D = 1mA
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	V_{GS} = V_{DS} , I_D = 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.5	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	V_{GS} = 0V, V_{DS} = Max Rating
				500		V_{GS} = 0V, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		300		mA	V_{GS} = 5V, V_{DS} = 25V
		250	340			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		30		Ω	V_{GS} = 5V, I_D = 20mA
			25	35		V_{GS} = 10V, I_D = 0.1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.9	1.5	%/°C	V_{GS} = 10V, I_D = 0.1A
G_{FS}	Forward Transconductance	100	180		m℧	V_{DS} = 25V, I_D = 0.1A
C_{ISS}	Input Capacitance		45	55	pF	V_{GS} = 0V, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance		8	10		
C_{RSS}	Reverse Transfer Capacitance		2	5		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = 25V, I_D = 250mA R_{GEN} = 25Ω
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			10		
t_f	Fall Time			10		
V_{SD}	Diode Forward Voltage Drop		0.8		V	V_{GS} = 0V, I_{SD} = 0.5A
t_{rr}	Reverse Recovery Time		400		ns	V_{GS} = 0V, I_{SD} = 0.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

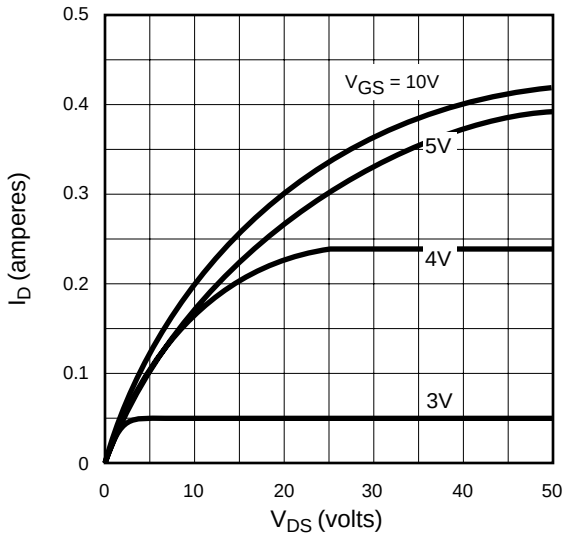
Switching Waveforms and Test Circuit



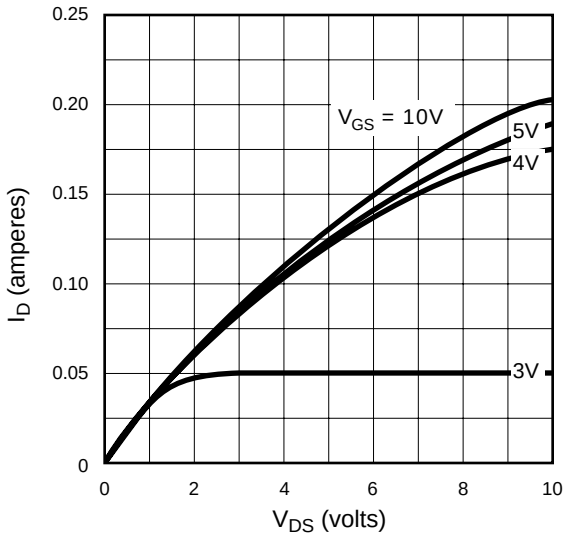


Typical Performance Curves

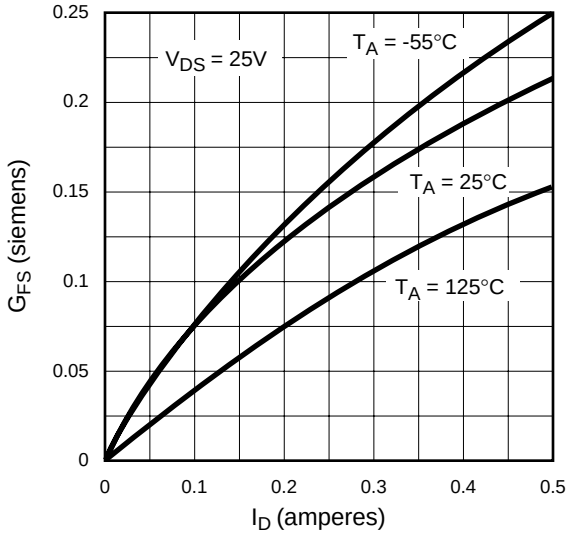
Output Characteristics



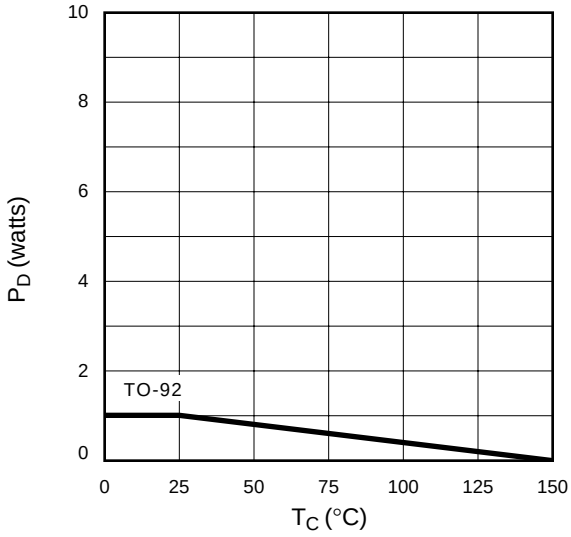
Saturation Characteristics



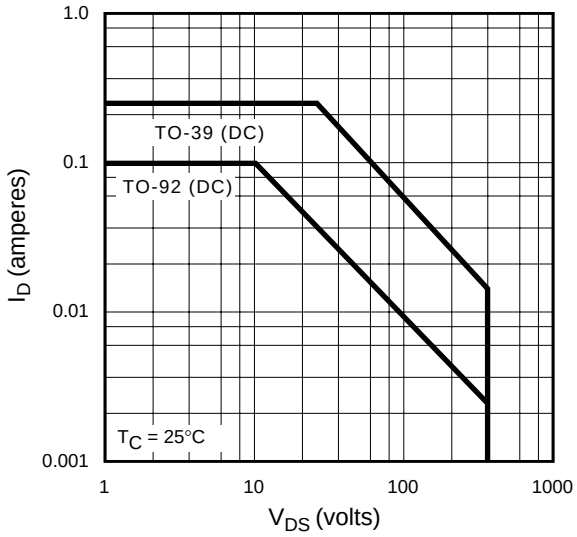
Transconductance vs. Drain Current



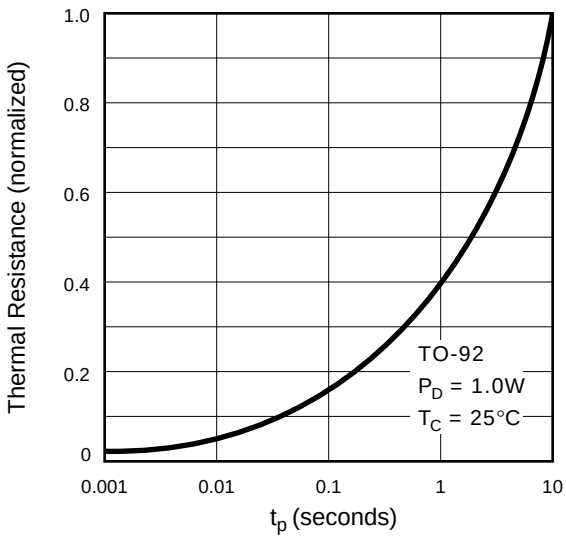
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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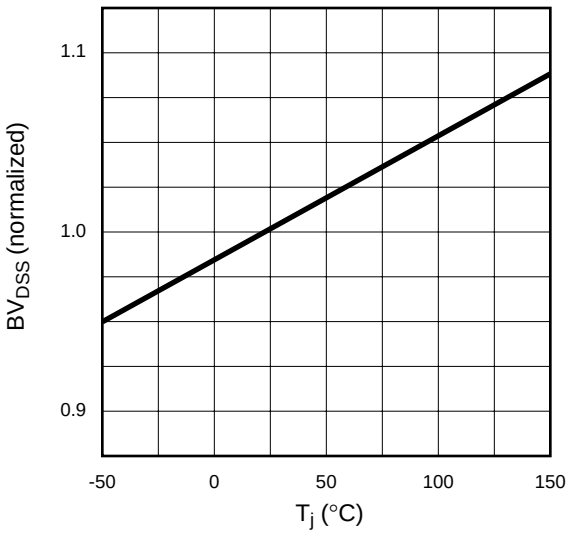
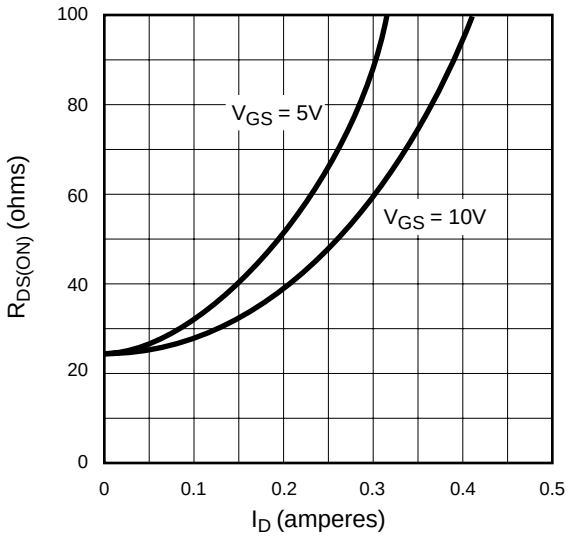
Typical Performance Curves

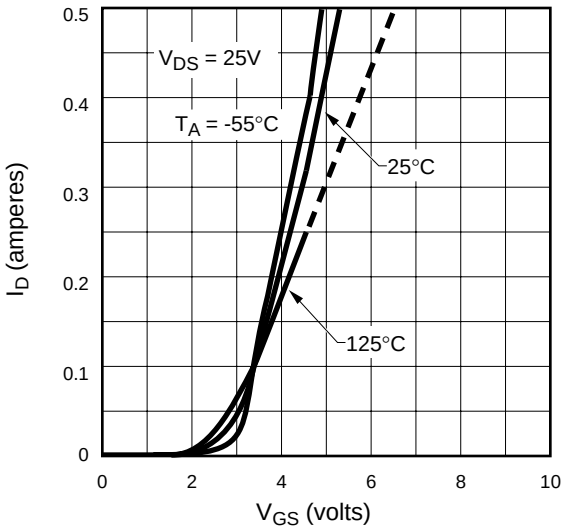
BV$_{DSS}$ Variation with Temperature



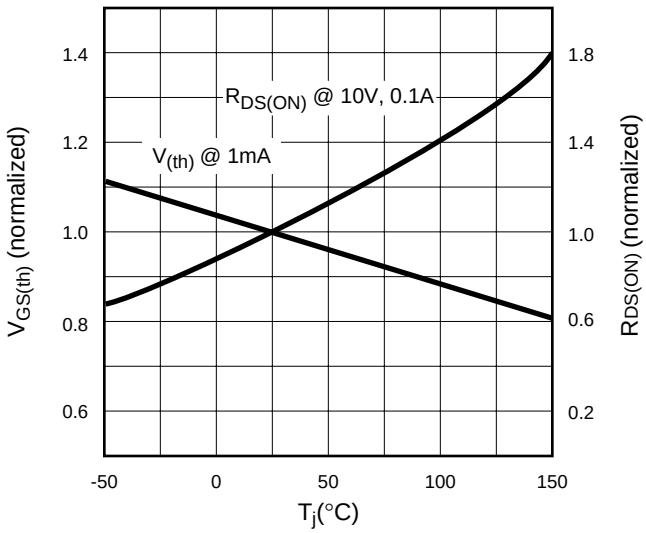
On-Resistance vs. Drain Current



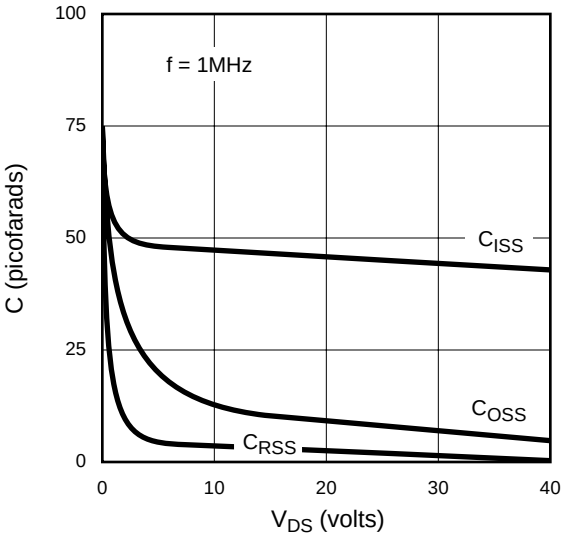
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics