

HIGH PERFORMANCE**2.5 VOLT 4M X 16 DDR SDRAM****4 BANKS X 1Mbit X 16**

| | 6 | 7 | 8 |
|----------------------------------|---------|---------|---------|
| System Frequency (f_{CK}) | 166 MHz | 143 MHz | 125 MHz |
| Clock Cycle Time (t_{CK3}) | 6 ns | 7 ns | 8 ns |
| Clock Cycle Time ($t_{CK2.5}$) | 6.5 ns | 7.5 ns | 9 ns |
| Clock Cycle Time (t_{CK2}) | 7ns | 8ns | 10ns |

Features

- 4 banks x 1Mbit x 16 organization
- High speed data transfer rates with system frequency up to 166 MHz
- Data Mask for Write Control (DM)
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2, 2.5, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
2, 4, 8 for Sequential Type
2, 4, 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Suspend Mode and Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 66-pin 400 mil TSOP-II
- SSTL-2 Compatible I/Os
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQs) for input and output data, active on both edges
- On-Chip DLL aligns DQ and DQs transitions with CLK transitions
- Differential clock inputs CLK and \overline{CLK}
- Power supply 2.5V \pm 0.2V

Description

The V58C265164S is a four bank DDR DRAM organized as 4 banks x 1Mbit x 16. The V58C265164S achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

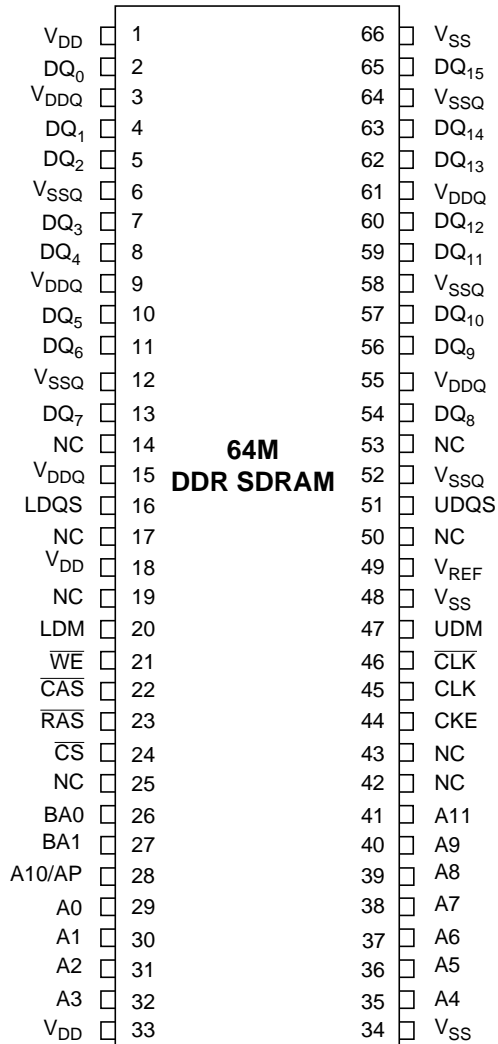
All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are possible on both edges of DQS.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Device Usage Chart

| Operating Temperature Range | Package Outline | CLK Cycle Time (ns) | | | Power | | Temperature Mark |
|-----------------------------|-----------------|---------------------|----|----|-------|---|------------------|
| | JEDEC 66 TSOPII | -6 | -7 | -8 | Std. | L | |
| 0°C to 70 °C | • | • | • | • | • | • | Blank |

66 Pin Plastic TSOP-II
PIN CONFIGURATION
Top View



Pin Names

| | |
|-----------------------------------|------------------------------|
| CLK, CLK | Differential Clock Input |
| CKE | Clock Enable |
| CS | Chip Select |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WE | Write Enable |
| UDQS, LDQS | Data Strobe (Bidirectional) |
| A ₀ –A ₁₁ | Address Inputs |
| BA0, BA1 | Bank Select |
| DQ ₀ –DQ ₁₅ | Data Input/Output |
| UDM, LDM | Data Mask |
| V _{DD} | Power (+2.5V) |
| V _{SS} | Ground |
| V _{DDQ} | Power for I/O's (+2.5V) |
| V _{SSQ} | Ground for I/O's |
| NC | Not connected |
| V _{REF} | Reference Voltage for Inputs |

Capacitance*
 $T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $f = 1 \text{ Mhz}$

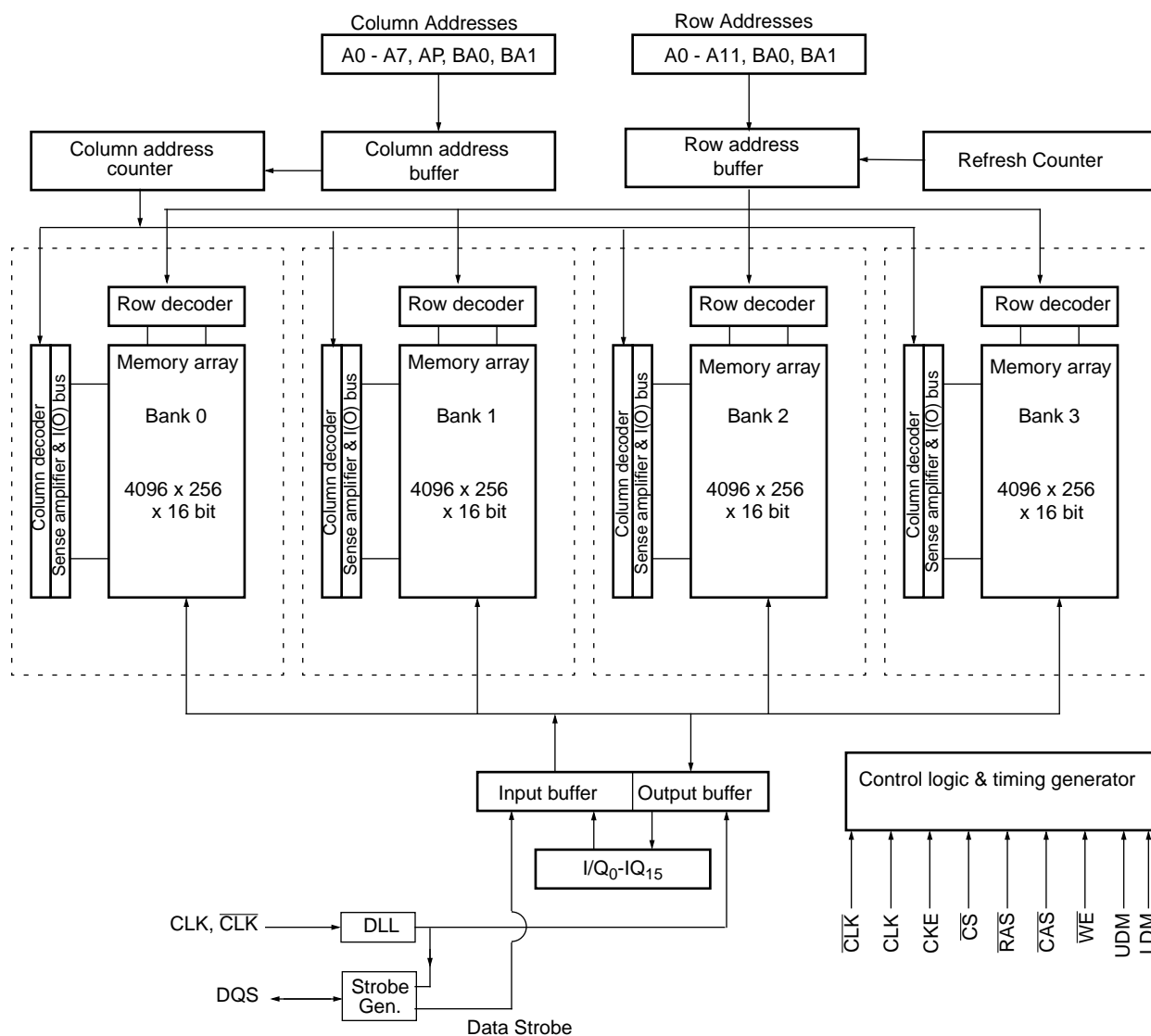
| Symbol | Parameter | Max. | Unit |
|------------------|--|------|------|
| C _{I1} | Input Capacitance (A0 to A11) | 5 | pF |
| C _{I2} | Input Capacitance RAS, CAS, WE, CS, CKE | 5 | pF |
| C _{IO} | Output Capacitance (DQ) | 6.5 | pF |
| C _{CLK} | Input Capacitance (CCLK, CLK) | 4 | pF |

*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Operating temperature range 0 to 70 °C
 Storage temperature range -55 to 150 °C
 Input/output voltage -0.3 to ($V_{CC}+0.3$) V
 Power supply voltage -0.3 to 4.6 V
 Power dissipation 1.6 W
 Data out current (short circuit) 50 mA

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram


Signal Pin Description

| Pin | Type | Signal | Polarity | Function |
|---|------------------|--------|---------------|--|
| CLK $\overline{\text{CLK}}$ | Input | Pulse | Positive Edge | The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CLK. |
| CKE | Input | Level | Active High | Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode. |
| $\overline{\text{CS}}$ | Input | Pulse | Active Low | $\overline{\text{CS}}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the command to be executed by the SDRAM. |
| DQS | Input/ Output | Pulse | Active High | Active on both edges for data input and output. Center aligned to input data Edge aligned to output data |
| A0 - A11 | Input | Level | — | During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organization: 8M x 8 SDRAM CAn = CA8 (Page Length = 512 bits) In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0 and BA1. |
| BA0, BA1 | Input | Level | — | Selects which bank is to be active. |
| DQx | Input/ Output | Level | — | Data Input/Output pins operate in the same manner as on conventional DRAMs. |
| DM | Input | Pulse | Active High | In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if is high. |
| VDD, VSS | Supply | | | Power and ground for the input buffers and the core logic. |
| VDDQ VSSQ | Supply | — | — | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| VREF | Input | Level | — | SSTL Reference Voltage for Inputs |

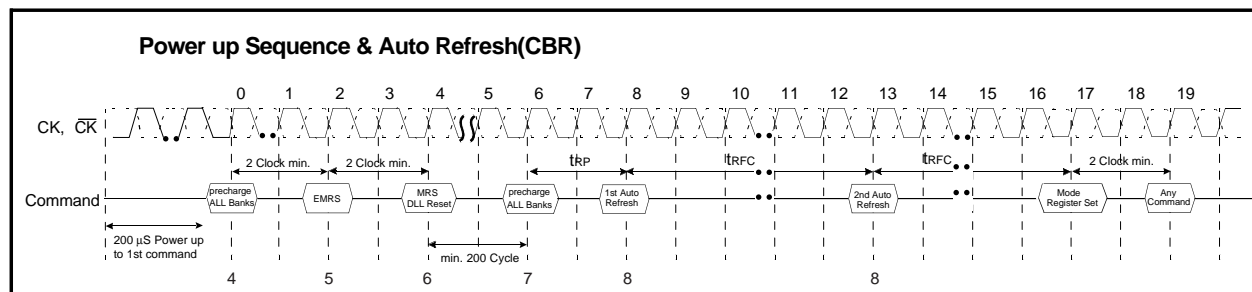
Functional Description

■ Power-Up Sequence

The following sequence is required for POWER UP.

1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
 - Apply VDD before or at the same time as VDDQ.
 - Apply VDDQ before or at the same time as VTT & Vref.
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock (CLK, $\overline{\text{CLK}}$), apply NOP & take CKE high.
4. Precharge all banks.
5. Issue EMRS to enable DLL.(To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide "High" to A8 and "Low" to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command to initialize device operation.

Note1 Every "DLL enable" command resets DLL. Therefore sequence 6 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.



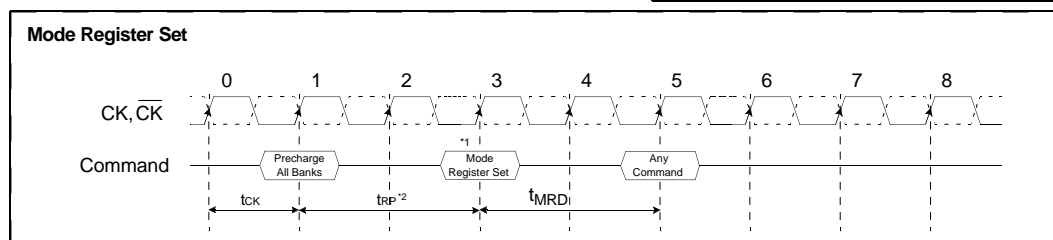
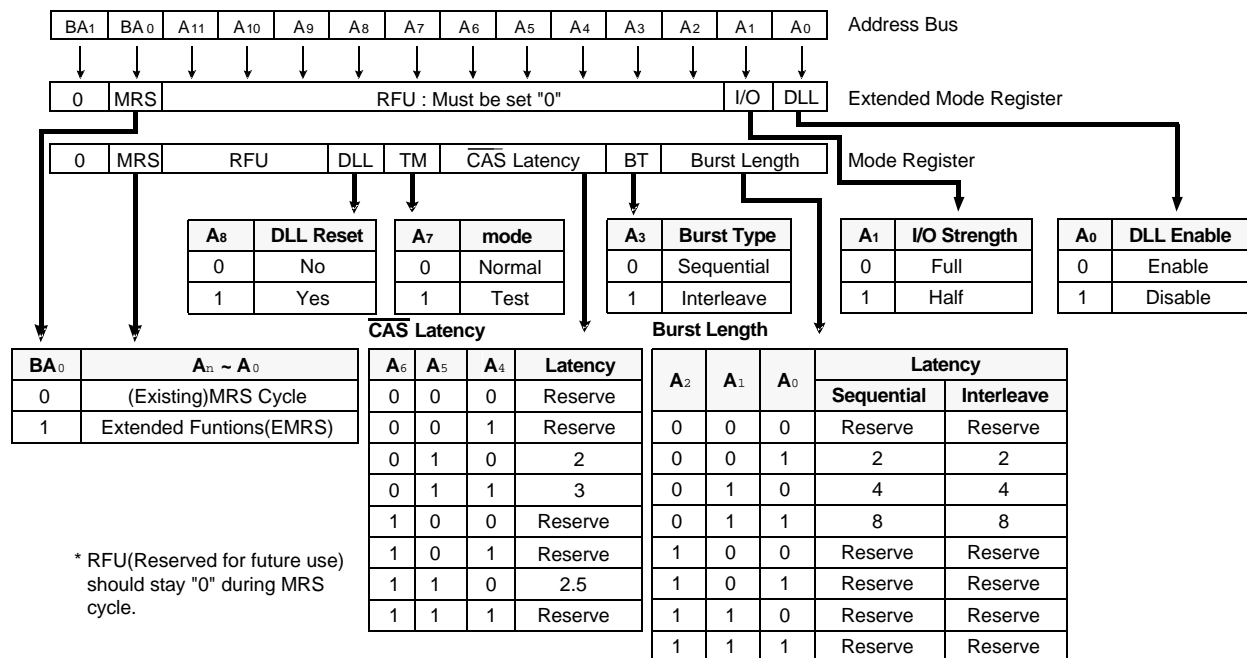
Extended Mode Register Set (EMRS)

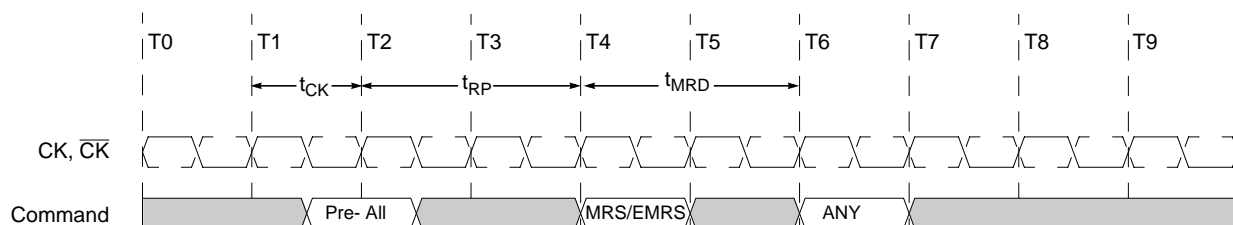
The extended mode register stores the data for enabling or disabling DLL. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{\text{CS}}$, RAS, CAS, WE and high on BA₀ (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A₀ ~ A₁₁ and BA₁ in the same cycle as $\overline{\text{CS}}$, RAS, CAS and WE low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A₀ is used for DLL enable or disable. "High" on BA₀ is used for EMRS. All the other address pins except A₀ and BA₀ must be set to low for proper EMRS operation. A₁ is used at EMRS to indicate I/O strength A₁ = 0 full strength, A₁ = 1 half strength. Refer to the table for specific codes.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for a variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} and BA_0 (The DDR SDRAM should be in all bank precharge with \overline{CKE} already high prior to writing into the mode register). The state of address pins $A_0 \sim A_{11}$ in the same cycle as \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} and BA_0 low is written in the mode register. Two clock cycles are required to meet t_{MRD} spec. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses $A_0 \sim A_2$, addressing mode uses A_3 , CAS latency (read latency from column address) uses $A_4 \sim A_6$. A_7 is a Mosel Vitelic specific test mode during production test. A_8 is used for DLL reset. A_7 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.

1. MRS can be issued only at all banks precharge state.
2. Minimum t_{RP} is required to issue MRS command.



Mode Register Set Timing

Mode Register set (MRS) or Extended Mode Register Set (EMRS) can be issued only when all banks are in the idle state.

If a MRS command is issued to reset the DLL, then an additional 200 clocks must occur prior to issuing any new command to allow time for the DLL to lock onto the clock.

Burst Mode Operation

Burst Mode Operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). Two parameters define how the burst mode will operate: burst sequence and burst length. These parameters are programmable and are determined by address bits A_0 — A_3 during the Mode Register Set command. Burst type defines the sequence in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequence are supported: sequential and interleave. The burst length controls the number of bits that will be output after a Read command, or the number of bits to be input after a Write command. The burst length can be programmed to values of 2, 4, or 8. See the Burst Length and Sequence table below for programming information.

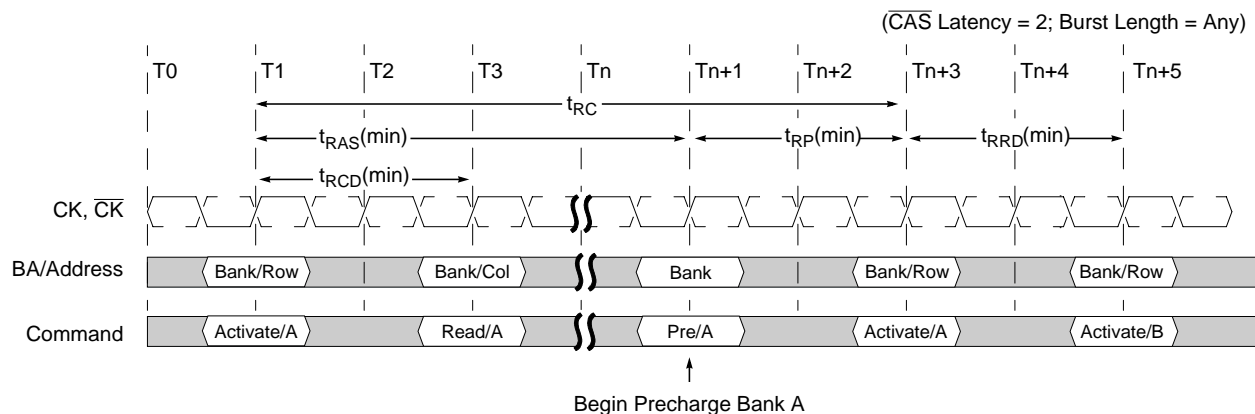
Burst Length and Sequence

| Burst Length | Starting Length (A_2, A_1, A_0) | Sequential Mode | Interleave Mode |
|--------------|-------------------------------------|---------------------------|------------------------|
| 2 | xx0 | 0, 1 | 0, 1 |
| | xx1 | 1, 0 | 1, 0 |
| 4 | x00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 000 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 001 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 010 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 011 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 100 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 101 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 110 | 6, 7, 0, 1, 2, 3, 4, 5, 6 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 111 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |

Bank Activate Command

The Bank Activate command is issued by holding $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ high with $\overline{\text{CS}}$ and $\overline{\text{RAS}}$ low at the rising edge of the clock. The DDR SDRAM has four independent banks, so two Bank Select addresses (BA_0 and BA_1) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum RAS to $\overline{\text{CAS}}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Activation Timing



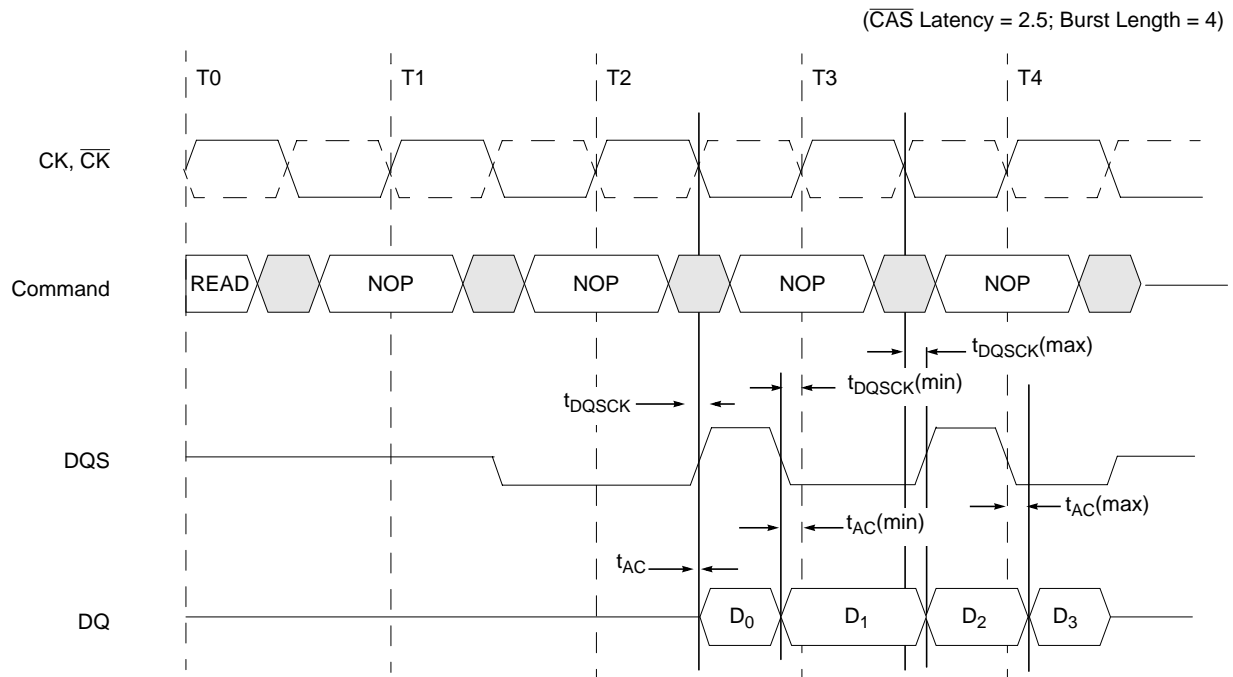
Read Operation

With the DLL enabled, all devices operating at the same frequency within a system are ensured to have the same timing relationship between DQ and DQS relative to the CK input regardless of device density, process variation, or technology generation.

The data strobe signal (DQS) is driven off chip simultaneously with the output data (DQ) during each read cycle. The same internal clock phase is used to drive both the output data and data strobe signal off chip to minimize skew between data strobe and output data. This internal clock phase is nominally aligned to the input differential clock (CK, $\overline{\text{CK}}$) by the on-chip DLL. Therefore, when the DLL is enabled and the clock frequency is within the specified range for proper DLL operation, the data strobe (DQS), output data (DQ), and the system clock (CK) are all nominally aligned.

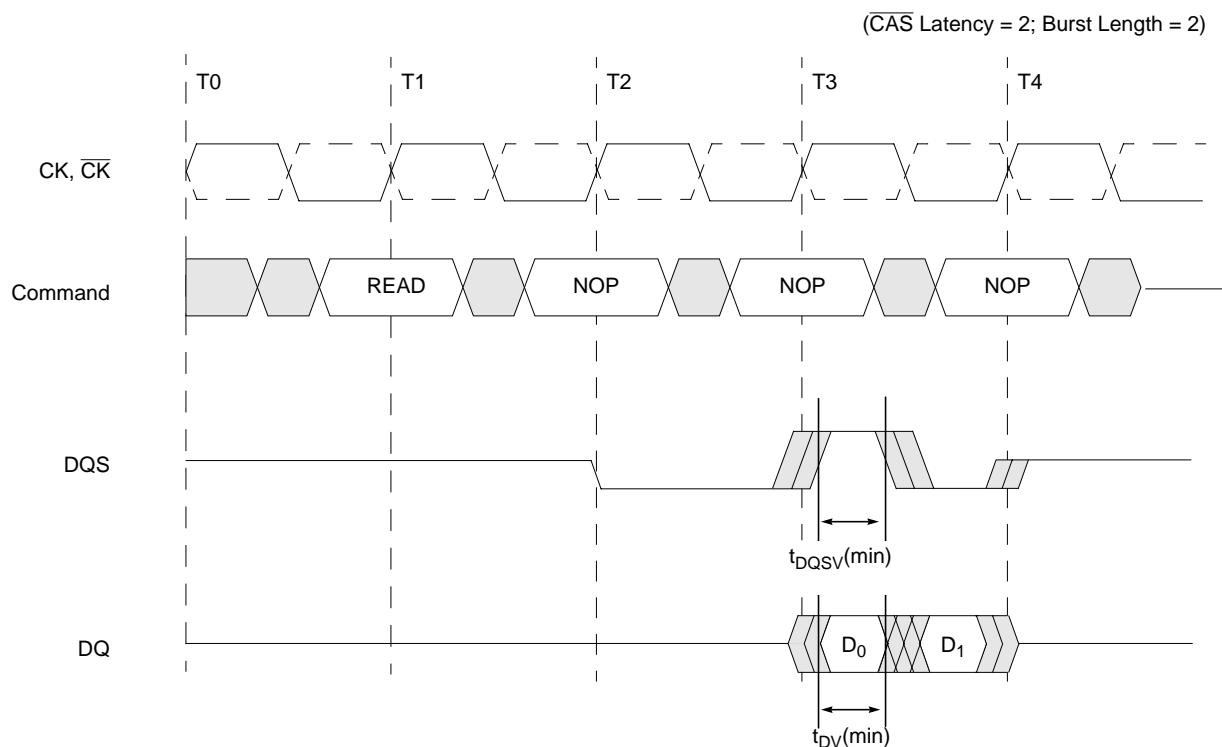
Since the data strobe and output data are tightly coupled in the system, the data strobe signal may be delayed and used to latch the output data into the receiving device. The tolerance for skew between DQS and DQ (t_{DQSQ}) is tighter than that possible for CK to DQ (t_{AC}) or DQS to CK (t_{DQSCK}).

**Output Data (DQ) and Data Strobe (DQS) Timing Relative to the Clock (CK)
During Read Cycles**



The minimum time during which the output data (DQ) is valid is critical for the receiving device (i.e., a memory controller device). This also applies to the data strobe during the read cycle since it is tightly coupled to the output data. The minimum data output valid time (t_{DV}) and minimum data strobe valid time (t_{DQSV}) are derived from the minimum clock high/low time minus a margin for variation in data access and hold time due to DLL jitter and power supply noise.

Output Data and Data Strobe Valid Window for DDR Read Cycles



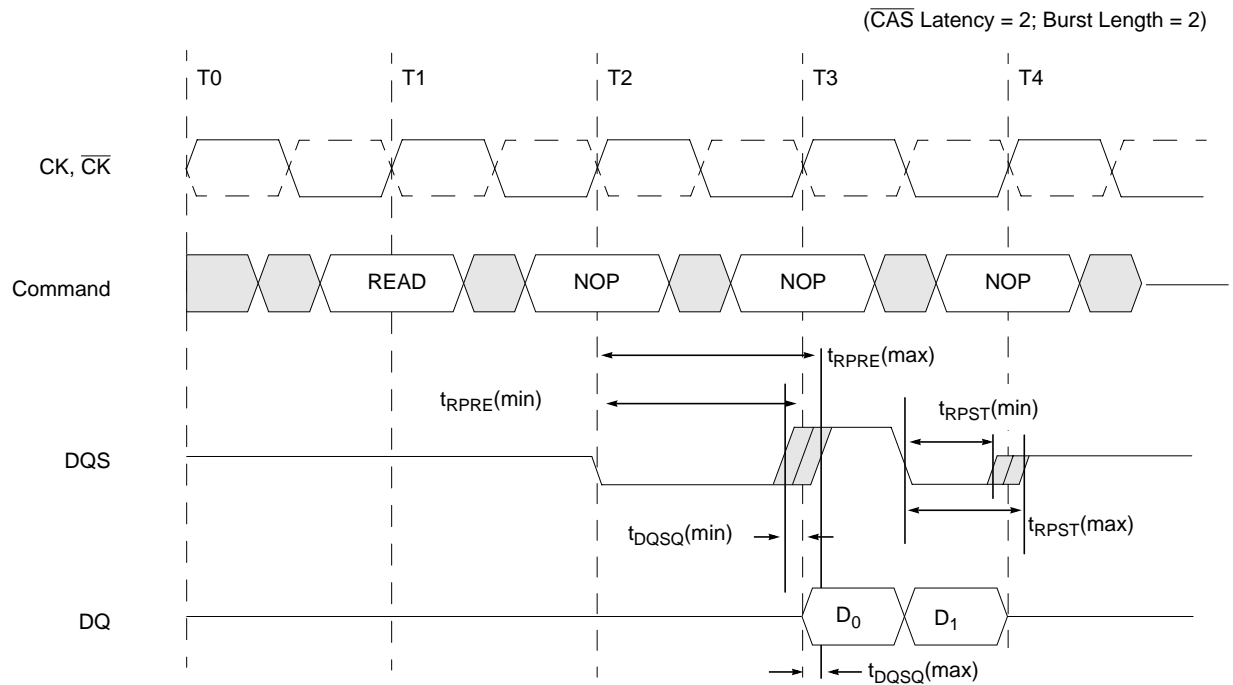
Read Preamble and Postamble Operation

Prior to a burst of read data and given that the controller is not currently in burst read mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. This is referred to as the data strobe “read preamble” (t_{RPRE}). This transition from Hi-Z to logic low nominally happens one clock cycle prior to the first edge of valid data.

Once the burst of read data is concluded and given that no subsequent burst read operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “read postamble” (t_{RPST}). This transition happens nominally one-half clock period after the last edge of valid data.

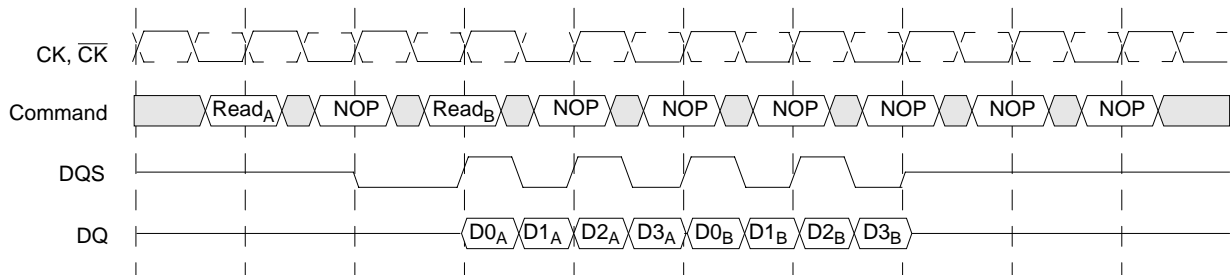
Consecutive or “gapless” burst read operations are possible from the same DDR SDRAM device with no requirement for a data strobe “read” preamble or postamble in between the groups of burst data. The data strobe read preamble is required before the DDR device drives the first output data off chip. Similarly, the data strobe postamble is initiated when the device stops driving DQ data at the termination of read burst cycles.

Data Strobe Preamble and Postamble Timings for DDR Read Cycles

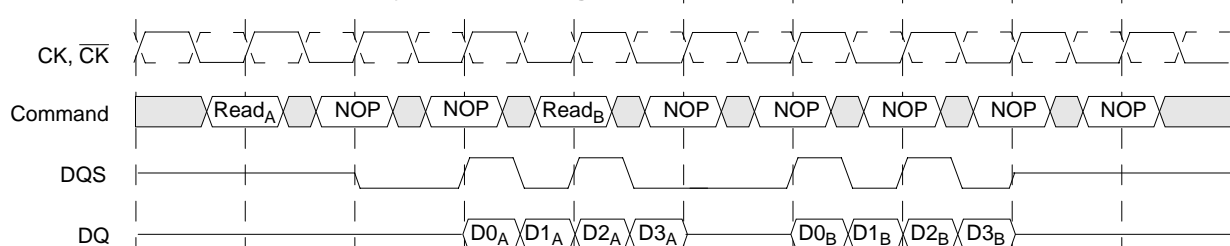


Consecutive Burst Read Operation and Effects on the Data Strobe Preamble and Postamble

Burst Read Operation (CAS Latency = 2; Burst Length = 4)



Burst Read Operation (CAS Latency = 2; Burst Length = 4)



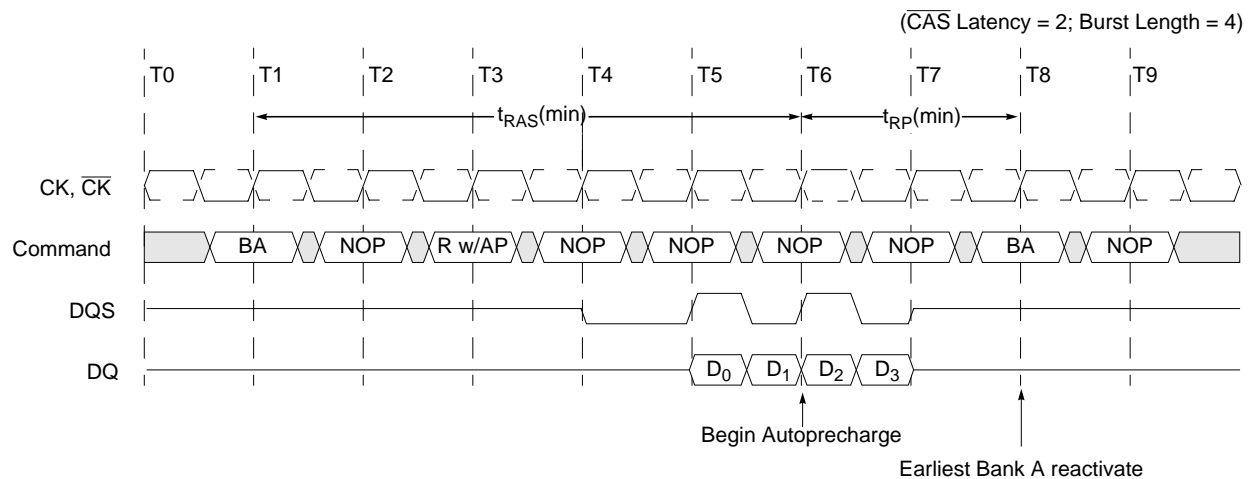
Auto Precharge Operation

The Auto Precharge operation can be issued by having column address A_{10} high when a Read or Write command is issued. If A_{10} is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once $t_{RAS(min)}$ is satisfied.

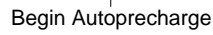
Read with Auto Precharge

If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the \overline{CAS} latency programmed into the device. If a Read with autoprecharge command is issued before $t_{RAS(min)}$ is satisfied, the precharge operation will be delayed until that time when $t_{RAS(min)}$ is met. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time (t_{RP}) has been satisfied.

Read with Autoprecharge Timing



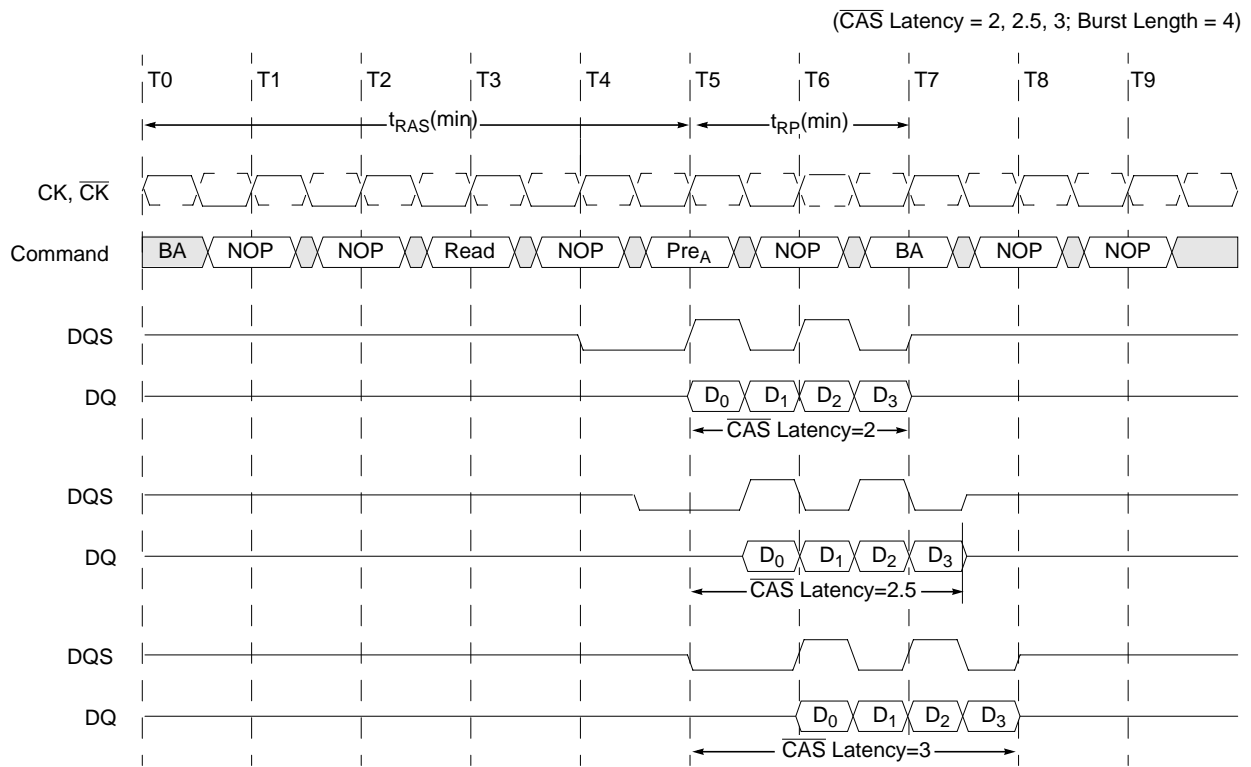
(CAS Latency = 2, 2.5, 3; Burst Length = 4)



Precharge Timing During Read Operation

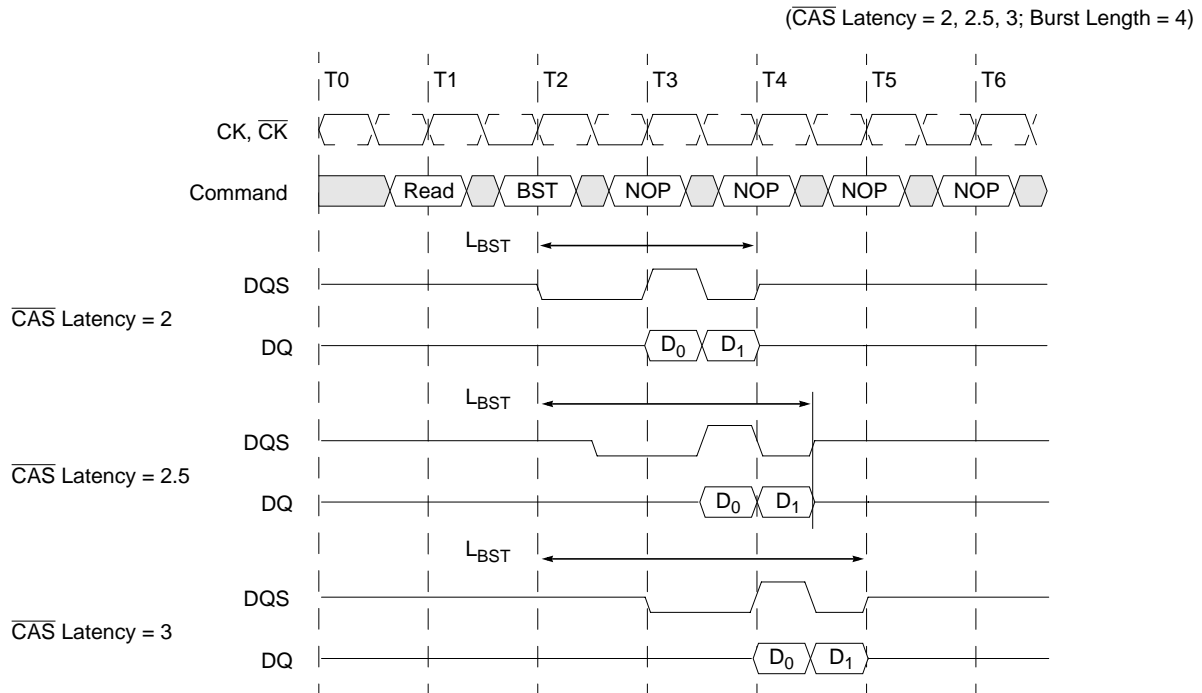
For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be issued on the rising clock edge which is $\overline{\text{CAS}}$ latency (CL) clock cycles before the end of the Read burst. A new Bank Activate (BA) command may be issued to the same bank after the $\overline{\text{RAS}}$ precharge time (t_{RP}). A Precharge command can not be issued until $t_{\text{RAS}}(\text{min})$ is satisfied.

Read with Precharge Timing as a Function of $\overline{\text{CAS}}$ Latency



Burst Stop Command

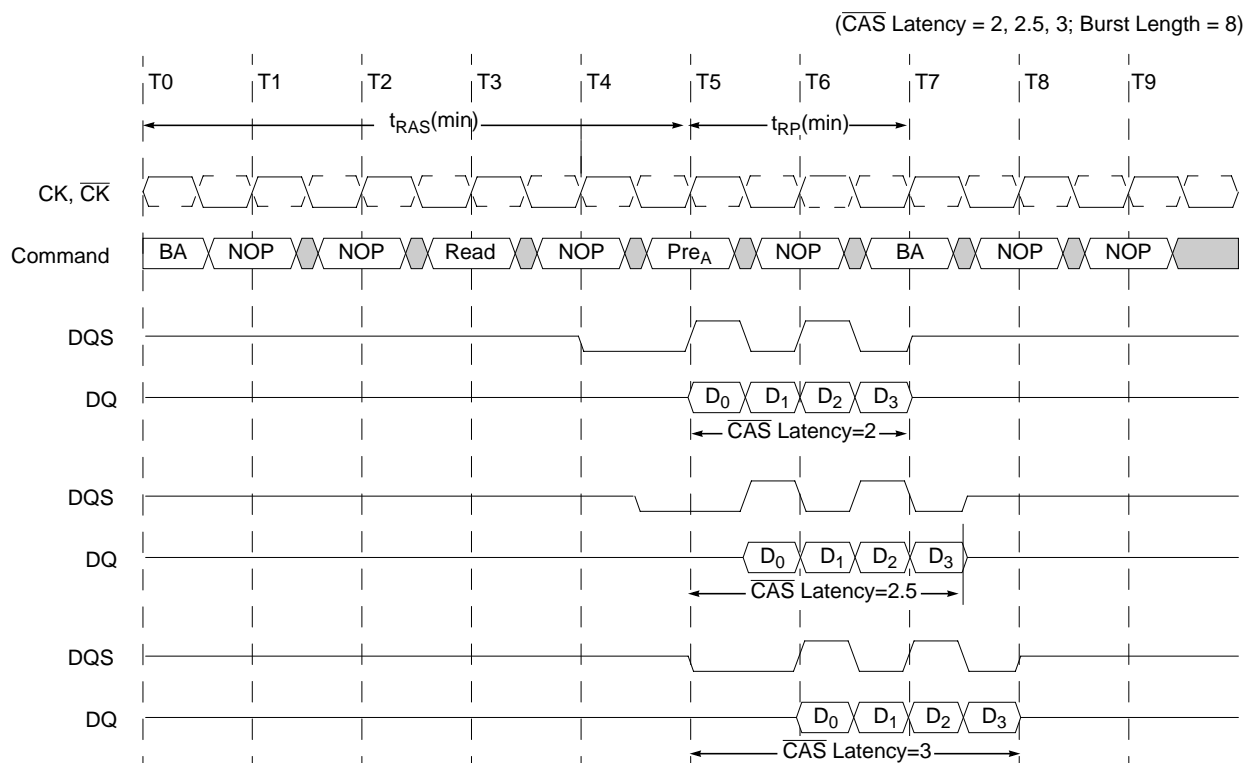
The Burst Stop command is valid only during burst read cycles and is initiated by having $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high with $\overline{\text{CS}}$ and $\overline{\text{WE}}$ low at the rising edge of the clock. When the Burst Stop command is issued during a burst Read cycle, both the output data (DQ) and data strobe (DQS) go to a high impedance state after a delay (L_{BST}) equal to the $\overline{\text{CAS}}$ latency programmed into the device. If the Burst Stop command is issued during a burst Write cycle, the command will be treated as a NOP command.

Read Terminated by Burst Stop Command Timing

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by a precharge of the same bank. The Precharge command to Output Disable latency is equivalent to the $\overline{\text{CAS}}$ latency.

Read Interrupted by a Precharge Timing



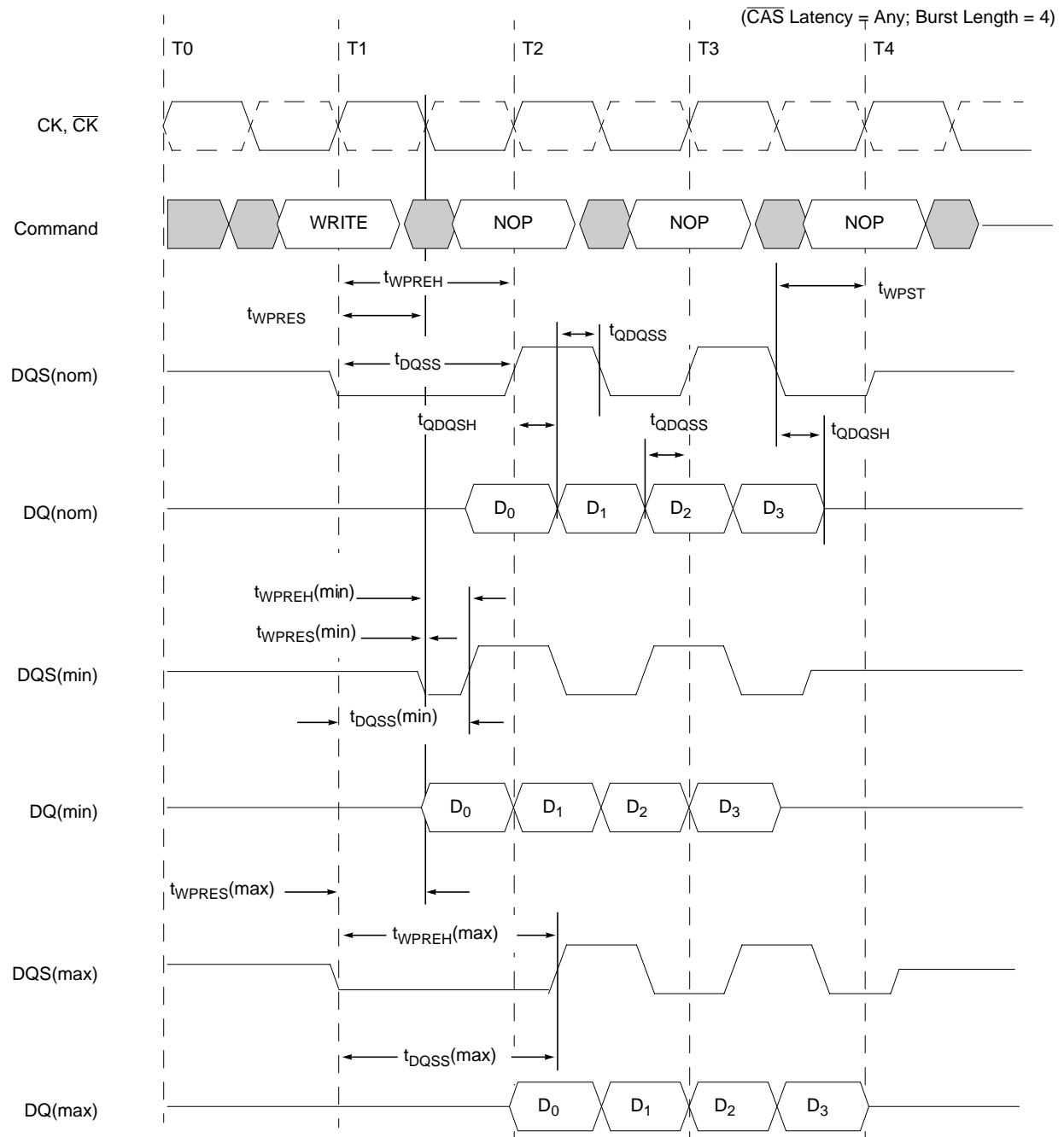
Burst Write Operation

The Burst Write command is issued by having $\overline{\text{CS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ low while holding $\overline{\text{RAS}}$ high at the rising edge of the clock. The address inputs determine the starting column address. The memory controller is required to provide an input data strobe (DQS) to the DDR SDRAM to strobe or latch the input data (DQ) and data mask (DM) into the device. During Write cycles, the data strobe applied to the DDR SDRAM is required to be nominally centered within the data (DQ) and data mask (DM) valid windows. The data strobe must be driven high nominally one clock after the write command has been registered. Timing parameters $t_{\text{DQSS}}(\text{min})$ and $t_{\text{DQSS}}(\text{max})$ define the allowable window when the data strobe must be driven high.

Input data for the first Burst Write cycle must be applied one clock cycle after the Write command is registered into the device ($\text{WL}=1$). The input data valid window is nominally centered around the midpoint of the data strobe signal. The data window is defined by DQ to DQS setup time ($t_{\text{DQDQS}}(\text{min})$) and DQ to DQS hold time ($t_{\text{DQDQSH}}(\text{min})$). All data inputs must be supplied on each rising and falling edge of the data strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

Write Preamble and Postamble Operation

Prior to a burst of write data and given that the controller is not currently in burst write mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. This is referred to as the data strobe "write preamble". This transition from Hi-Z to logic low nominally happens on the falling edge of the clock after the write command has been registered by the device. The preamble is explicitly defined by a setup time ($t_{\text{WPRES}}(\text{min})$) and hold time ($t_{\text{WPREH}}(\text{min})$) referenced to the first falling edge of CK after the write command.

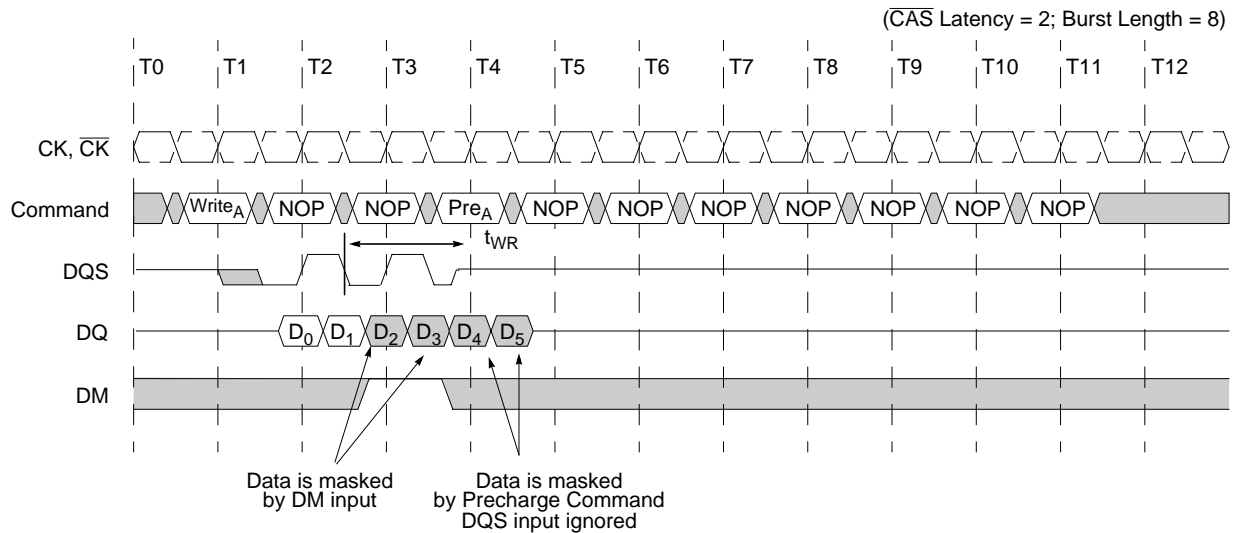
Burst Write Timing

Once the burst of write data is concluded and given that no subsequent burst write operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “write postamble”. This transition happens nominally one-half clock period after the last data of the burst cycle is latched into the device.

Write Interrupted by a Precharge

A Burst Write can be interrupted before completion of the burst by a Precharge command, with the only restriction being that the interval that separates the commands be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

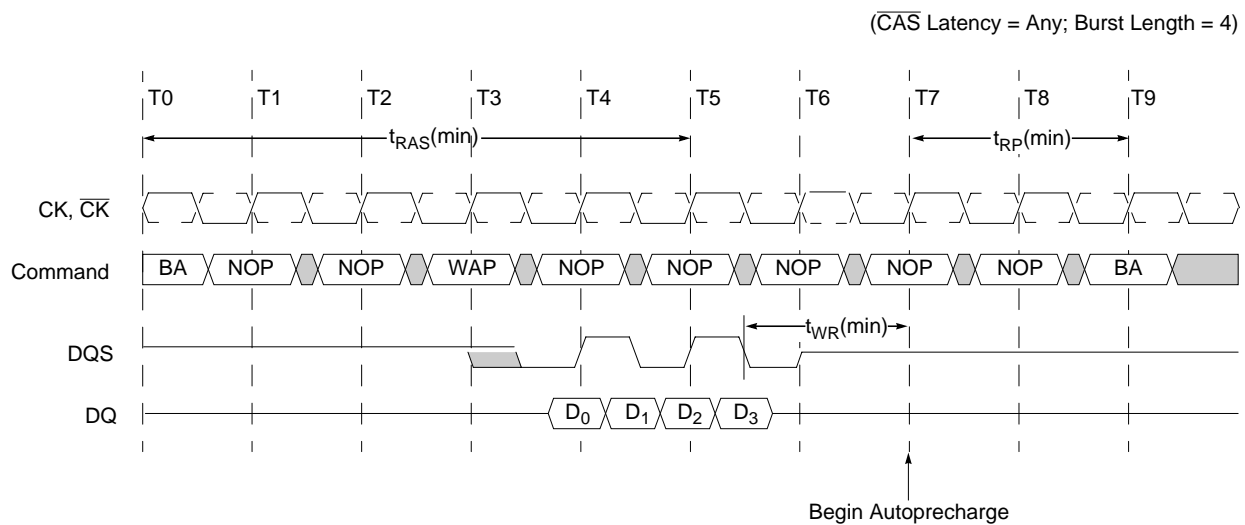
Write Interrupted by a Precharge Timing



Write with Auto Precharge

If A₁₀ is high when a Write command is issued, the Write with auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping t_{WR} (min.).

Write with Auto Precharge Timing



Precharge Timing During Write Operation

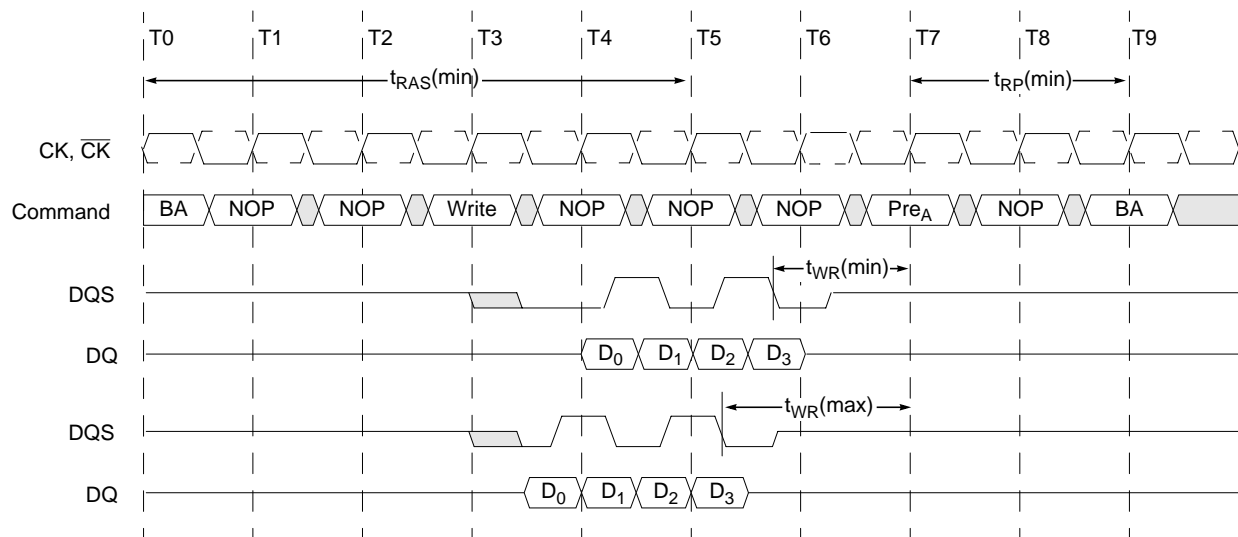
Precharge timing for Write operations in DRAMs requires enough time to satisfy the write recovery requirement. This is the time required by a DRAM sense amp to fully store the voltage level. For DDR SDRAMs, a timing parameter (t_{WR}) is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The “write recovery” operation begins on the rising clock edge after the last DQS edge that is used to strobe in the last valid write data. “Write recovery” is complete on the next rising clock edge that is used to strobe in the Precharge command.

For the earliest possible Precharge command following a Write burst without interrupting the burst, the minimum time for “write recovery” is 1.25 clock cycles. Maximum “write recovery” time is 1.75 clock cycles.

Write with Precharge Timing

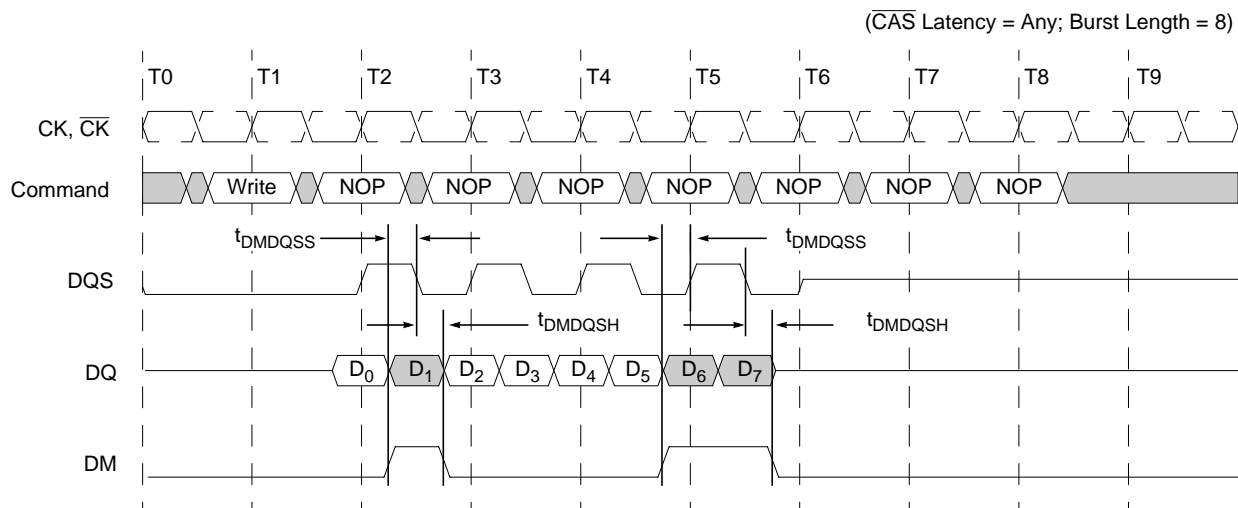
($\overline{\text{CAS}}$ Latency = Any; Burst Length = 4)



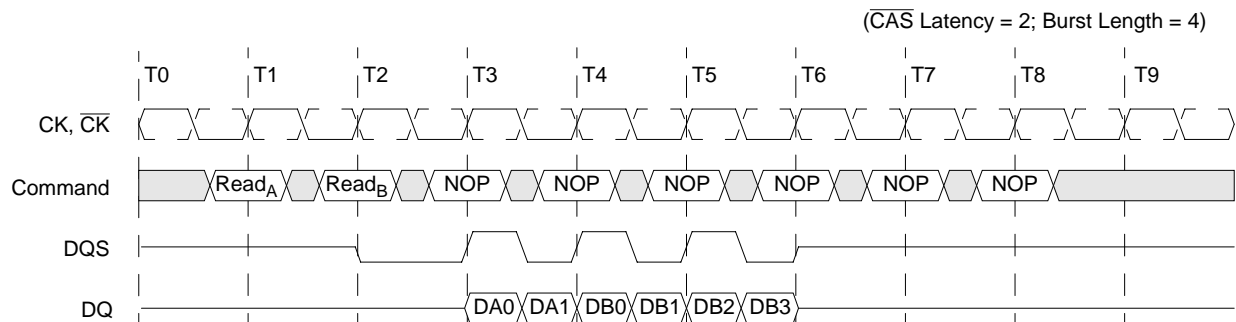
Data Mask Function

The DDR SDRAM has a Data Mask function that is used in conjunction with the Write cycle, but not the Read cycle. When the Data Mask is activated (DM high) during a Write operation, the Write is blocked (Mask to Data Latency = 0).

When issued, the Data Mask must be referenced to both the rising and falling edges of Data Strobe.

Data Mask Timing**Burst Interruption****Read Interrupted by a Read**

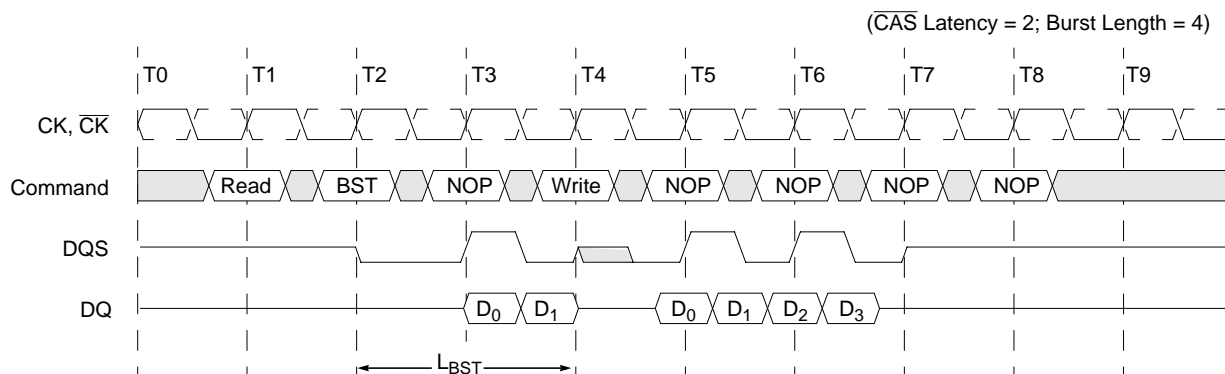
A Burst Read can be interrupted before completion of the burst by issuing a new Read command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Read command continues to appear on the outputs until the $\overline{\text{CAS}}$ latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears on the bus. Read commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Read with autoprecharge command with a Read command.

Read Interrupted by a Read Command Timing

Read Interrupted by a Write

To interrupt a Burst Read with a Write command, a Burst Stop command must be asserted to stop the burst read operation and 3-state the DQ bus. Additionally, control of the DQS bus must be turned around to allow the memory controller to drive the data strobe signal (DQS) into the DDR SDRAM for the write cycles. Once the Burst Stop command has been issued, a Write command can not be issued until a minimum delay or latency (L_{BST}) has been satisfied. This latency is measured from the Burst Stop command and is equivalent to the \overline{CAS} latency programmed into the mode register. In instances where \overline{CAS} latency is measured in half clock cycles, the minimum delay (L_{BST}) is rounded up to the next full clock cycle (i.e., if $CL=2$ then $L_{BST}=2$, if $CL=2.5$ then $L_{BST}=3$). It is illegal to interrupt a Read with autoprecharge command with a Write command.

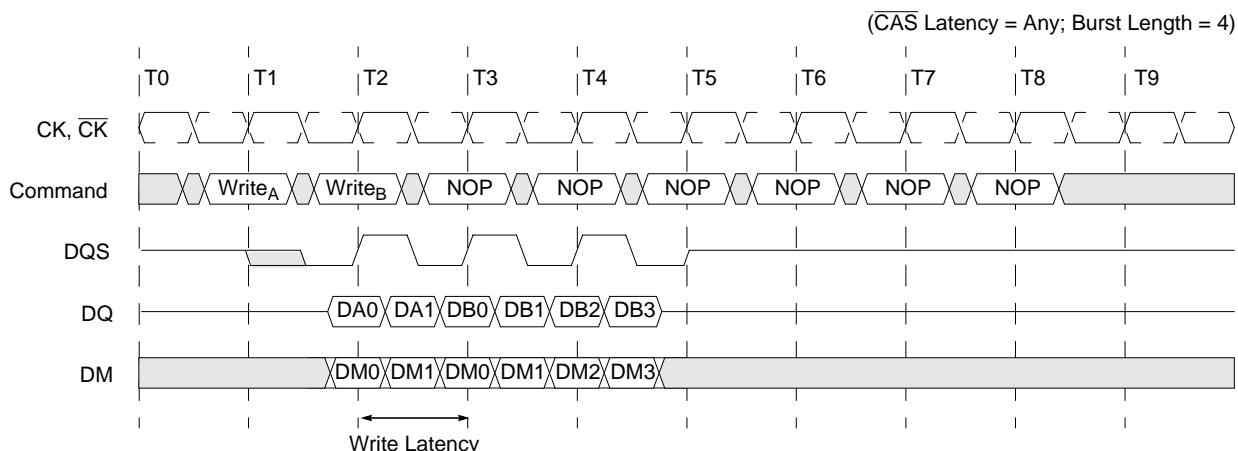
Read Interrupted by Burst Stop Command Followed by a Write Command Timing



Write Interrupted by a Write

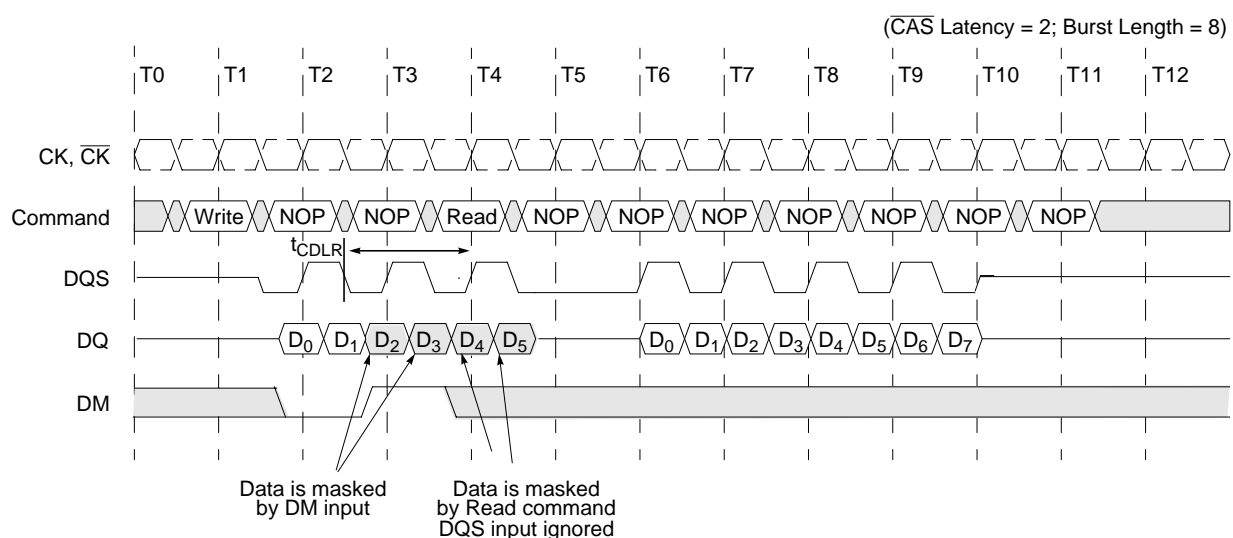
A Burst Write can be interrupted before completion by a new Write command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Write command continues to be input into the device until the Write Latency of the interrupting Write command is satisfied ($WL=1$). At this point, the data from the interrupting Write command is input into the device. Write commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Write with autoprecharge command with a Write command.

Write Interrupted by a Write Command Timing

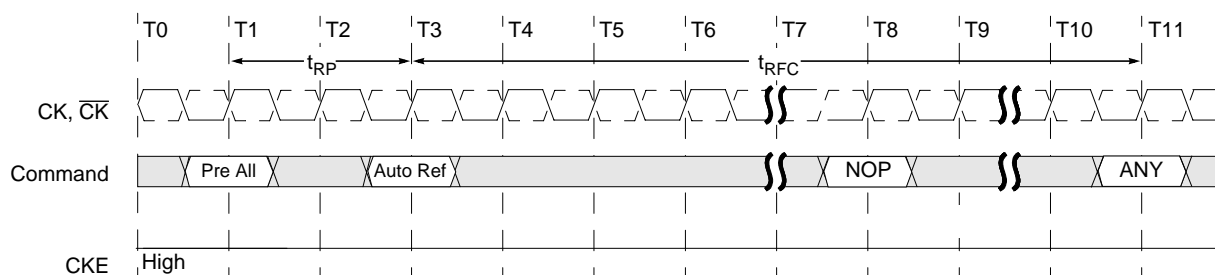


Write Interrupted by a Read

A Burst Write can be interrupted by a Read command to any bank. If a burst write operation is interrupted prior to the end of the burst operation, then the last two pieces of input data prior to the Read command must be masked off with the data mask (DM) input pin to prevent invalid data from being written into the memory array. Any data that is present on the DQ pins coincident with or following the Read command will be masked off by the Read command and will not be written to the array. The memory controller must give up control of both the DQ bus and the DQS bus at least one clock cycle before the read data appears on the outputs in order to avoid contention. In order to avoid data contention within the device, a delay is required (t_{CDLR}) from the last valid data input before a Read command can be issued to the device. It is illegal to interrupt a Write with autoprecharge command with a Read command.

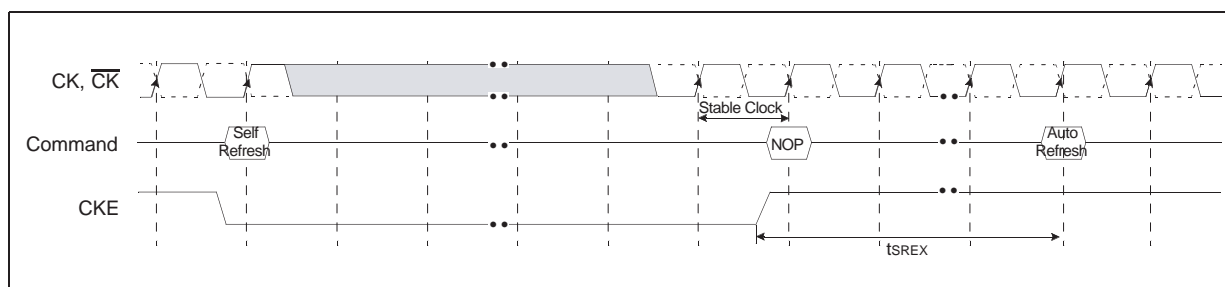
Write Interrupted by a Read Command Timing**Auto Refresh**

The Auto Refresh command is issued by having $\overline{\text{CS}}$, $\overline{\text{RAS}}$, and $\overline{\text{CAS}}$ held low with CKE and $\overline{\text{WE}}$ high at the rising edge of the clock. All banks must be precharged and idle for a $t_{RP}(\text{min})$ before the Auto Refresh command is applied. No control of the address pins is required once this cycle has started because of the internal address counter. When the Auto Refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate command or subsequent Auto Refresh command must be greater than or equal to the $t_{RFC}(\text{min})$. Commands may not be issued to the device once an Auto Refresh cycle has begun. $\overline{\text{CS}}$ input must remain high during the refresh period or NOP commands must be registered on each rising edge of the CK input until the refresh period is satisfied.

Auto Refresh Timing

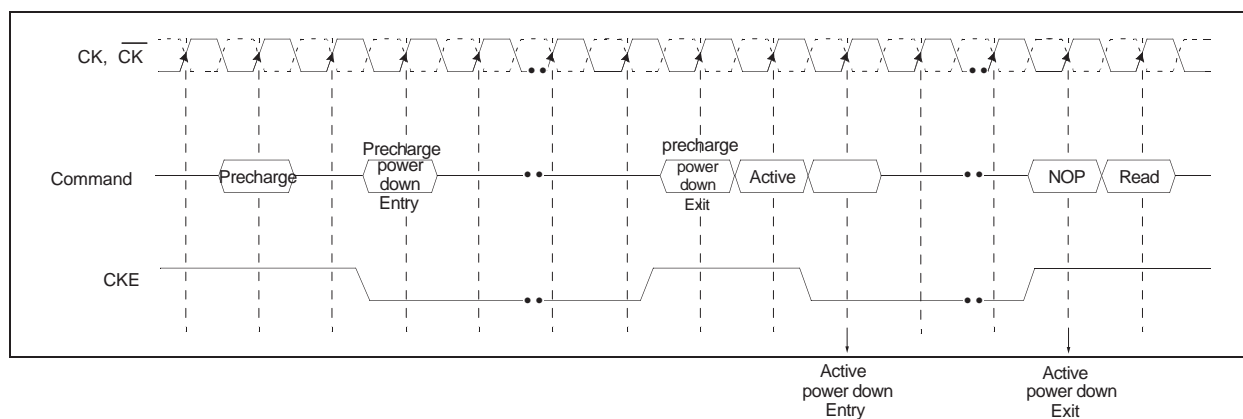
Self Refresh

A self refresh command is defined by having \overline{CS} , \overline{RAS} , \overline{CAS} and \overline{CKE} held low with \overline{WE} high at the rising edge of the clock (CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than t_{SREX} for locking of DLL. The auto refresh is required before self refresh entry and after self refresh exit.



Power Down Mode

The power down mode is entered when CKE is low and exited when CKE is high. Once the power down mode is initiated, all of the receiver circuits except clock, CKE and DLL circuit tree are gated off to reduce power consumption. The both banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least $1t_{CK} + t_{IS}$ prior to row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period (t_{REF}) of the device.



SSTL_2 Input AC/DC Logic Levels

| Symbol | Parameter | Min | Max | Units | Notes |
|---------------|---------------------|----------------|----------------|-------|-------|
| V_{IH} (DC) | DC Input Logic High | $V_{REF}+0.18$ | $V_{DDQ}+0.3$ | V | 1 |
| V_{IH} (AC) | AC Input Logic High | $V_{REF}+0.35$ | — | V | |
| V_{IL} (DC) | DC Input Logic Low | -0.30 | $V_{REF}-0.18$ | V | |
| V_{IL} (AC) | AC Input Logic Low | — | $V_{REF}-0.35$ | V | |

Note: 1. The relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of V_{IH} (max) (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that supports SSTL_2 inputs but has no SSTL_2 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0V (High corner $V_{DDQ}+300mV$.)

SSTL_2 AC Test Conditions

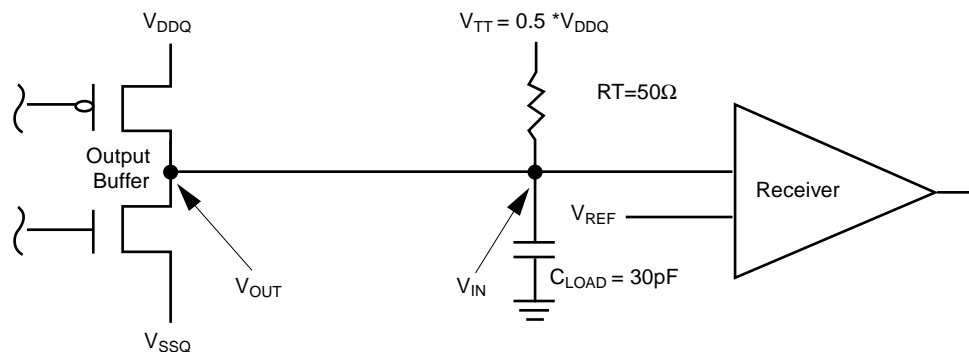
| Symbol | Parameter | Value | Units | Notes |
|-------------------|---|---------------------|-------|-------|
| V_{REF} | Input Reference Voltage | $0.5 \cdot V_{DDQ}$ | V | 1 |
| V_{SWING} (max) | Input Signal Maximum Peak to Peak Swing | 1.5 | V | 1, 2 |
| SLEW | Input Signal Minimum Slew Rate | 1.0 | V/ns | 3 |

Notes: 1. Input waveform timing is referenced to the input signal crossing the V_{REF} level applied to the device.
 2. Compliant devices must still meet the V_{IH} (AC) and V_{IL} (AC) specifications under actual use conditions.
 3. The 1 V/ns input signal minimum slew rate is to be maintained in the V_{IL} max (AC) to V_{IL} min (AC) range of the input signal swing.

SSTL_2 Output Buffers

The input voltage provided to the receiver depends on three parameters:

- V_{DDQ} and current drive capabilities of the output buffer
- Termination voltage
- Termination resistance
- $V_{DDQ} \leq V_{DD}$

Class II SSTL_2 Output Buffer (Driver)

DC CHARACTERISTICSRecommended operating conditions Unless Otherwise Noted, $T_A=0$ to 70°C

| Parameter | Symbol | Test Condition | $\overline{\text{CAS}}$ Latency | Version | | | Unit |
|---|------------|---|------------------------------------|---------|-----|-----|------|
| | | | | -6 | -7 | -8 | |
| Operating Current (One Bank Active) | I_{CC1} | Burst Length=2 $t_{RC}=t_{RC}(\text{min})$ $I_{OL}=0\text{mA}$ | | 130 | 120 | 110 | mA |
| Precharge Standby Current in Power-Down Mode | I_{CC2P} | $\text{CKE}=V_{IL}(\text{max})$, $t_{CC}=10\text{ns}$ | | 20 | | | mA |
| Precharge Standby Current in Non Power-Down Mode | I_{CC2N} | $\text{CKE}=V_{IH}(\text{min})$, $\text{CS}-V_{IH}(\text{min})$, $t_{CC}=10\text{ns}$ Input signals are changed once during 20ns | | 45 | | | mA |
| Active Standby Current in Power-Down Mode | I_{CC3P} | $\text{CKE}=V_{IL}(\text{max})$, $t_{CC}=10\text{ns}$ | | 30 | | | mA |
| Active Standby Current in Non- Power-Down Mode | I_{CC3N} | $\text{CKE}=V_{IH}(\text{min})$, $\text{CS}-V_{IH}(\text{min})$, $t_{CC}=10\text{ns}$ Input signals are changed once during 20ns | | 60 | | | mA |
| Operating Current (Burst Mode) | I_{CC4} | $I_{OL}=0\text{mA}$ Page Burst All Banks activated $t_{CCD}=2\text{CKs}$ | 2 | 140 | 130 | 120 | mA |
| Refresh Current | I_{CC5} | $t_{RC}=t_{RFC}(\text{min})$ | | 200 | | | mA |
| Self Refresh Current | I_{CC6} | $\text{CKE}=0.2\text{V}$ | | 2 | | | mA |

AC Characteristics ($T_A=0$ to $+70^{\circ}\text{C}$, $V_{CC}=2.5 \pm 0.2\text{V}$)

| Symbol | Parameter | | −8 | | −7 | | −6 | | Unit |
|------------------------|-----------------------------|----------|--------|-------|--------|-------|--------|-------|-----------------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock Cycle | | | | | | | | | |
| t _{CK} | Clock Cycle | CL = 2.0 | 10 | 15 | 8 | 15 | 7 | 15 | ns |
| | | CL = 2.5 | 9 | 15 | 7.5 | 15 | 6.5 | 15 | ns |
| | | CL = 3.0 | 8 | 15 | 7 | 15 | 6 | 15 | ns |
| t _{CH} | Clock Duty Cycle | | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | % |
| t _{CL} | | | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | % |
| Command Cycle | | | | | | | | | |
| t _{RAS} | Row Active Time (ACT->PRE) | | 56 | - | 49 | - | 42 | - | ns |
| t _{RP} | Row Precharge (PRE->ACT) | | 24 | - | 21 | - | 18 | - | ns |
| t _{RC} | Row Cycle (ACT->ACT) | | 80 | - | 70 | - | 60 | - | ns |
| t _{RCD} | RAS->CAS Delay (ACT->WR/RD) | | 24 | - | 21 | - | 18 | - | ns |
| t _{RRD} | RAS->RAS Delay (ACTa->ACTb) | | 16 | - | 14 | - | 12 | - | ns |
| t _{RFC} | Auto-Refresh (REF->REF/ACT) | | 88 | - | 77 | - | 66 | - | ns |
| t _{REF} | Refresh Cycle | | - | 64 | - | 64 | - | 64 | ms |
| t _{SREX(DLL)} | Self-Refresh Exit Delay | | 200 | - | 200 | - | 200 | - | cycles |
| t _{SREX} | | | 1 | - | 1 | - | 1 | - | t _{RC} |
| t _{IS} | CMD, ADDR->CLK Setup | | 0.15 | - | 0.15 | - | 0.15 | - | t _{CK} |
| t _{IH} | CMD, ADDR->CLK Hold | | 0.15 | - | 0.15 | - | 0.15 | - | t _{CK} |
| t _{CCD} | CAS->CAS Delay (Cola->Colb) | | 1 | | 1 | | 1 | | t _{CK} |
| t _{MRD} | Mode Register Set Delay | | 2 | | 2 | | 2 | | t _{CK} |
| t _{PDENT} | Power Down Entry Delay | | 1 | | 1 | | 1 | | t _{CK} |
| t _{PDEX(DLL)} | Power Down Exit Delay | | 1 | | 1 | | 1 | | t _{CK} |
| t _{PDEX} | | | 1 | | 1 | | 1 | | t _{CK} |
| Read Cycle | | | | | | | | | |
| t _{AC} | CLK->DQ Skew | | -0.1 | 0.1 | -0.1 | 0.1 | -0.1 | 0.1 | t _{CK} |
| t _{DQSK} | CLK->DQS Skew | | -0.1 | 0.1 | -0.1 | 0.1 | -0.1 | 0.1 | t _{CK} |
| t _{DQSQ} | DQS->DQ Skew | | -0.075 | 0.075 | -0.075 | 0.075 | -0.075 | 0.075 | t _{CK} |
| t _{DV} | DQ/DQS Valid Window | | 0.3 | - | 0.3 | - | 0.3 | - | t _{CK} |
| t _{RPRE} | Read DQS Preamble | | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t _{CK} |
| t _{RPST} | Read DQS Postamble | | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} |

AC Characteristics (Continued) ($T_A=0$ to $+70^{\circ}\text{C}$, $V_{CC}=2.5 \pm 0.2\text{V}$)

| Symbol | Parameter | −8 | | −7 | | −6 | | Unit |
|-------------|--------------------------------------|-------|------|-------|------|-------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Cycle | | | | | | | | |
| tWPRES | Write Preamble DQS Setup | 0 | 0.5 | 0 | 0.5 | 0 | 0.5 | tCK |
| tWPREH | Write Preamble DQS Hold | 0.25 | 1.25 | 0.25 | 1.25 | 0.25 | 1.25 | tCK |
| tDQSS | Write Preamble CLK->DQS (first) | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | tCK |
| tDSH | Write DQS High Width | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| tDSL | Write DQS Low Width | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| tWPST | Write Postamble DQS (last) -> Hi-Z | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| tDQSR | Write (last DIN) -> READ Command | 1.25 | 1.75 | 1.25 | 1.75 | 1.25 | 1.75 | tCK |
| tWR | Write (last DIN) -> PRE Command | 1.25 | 1.75 | 1.25 | 1.75 | 1.25 | 1.75 | tCK |
| tDS | DQ/DM -> DQS Setup (Data Setup) | 0.075 | - | 0.075 | - | 0.075 | - | tCK |
| tDH | DQ/DM -> DQS Hold (Data Hold) | 0.075 | - | 0.075 | - | 0.075 | - | tCK |
| tDQSS | Date Input to Data Strobe Setup Time | 0.075 | - | 0.075 | - | 0.075 | - | tCK |
| tDQSH | Date Input to Data Strobe Hold Time | 0.075 | - | 0.075 | - | 0.075 | - | tCK |
| tDMDSQS | Date Mask to Data Strobe Setup Time | 0.075 | - | 0.075 | - | 0.075 | - | tCK |
| tDMDQSH | Date Mask to Data Strobe Hold Time | 0.075 | - | 0.075 | - | 0.075 | - | tCK |

Complete List of Operation Commands
DDR SDRAM Function Truth Table

| CURRENT STATE ¹ | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | \overline{BS} | Addr | ACTION |
|----------------------------|-----------------|------------------|------------------|-----------------|-----------------|-------|--|
| Idle | H | X | X | X | X | X | NOP or Power Down |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BS | X | ILLEGAL ² |
| | L | H | L | X | BS | X | ILLEGAL ² |
| | L | L | H | H | BS | RA | Row (&Bank) Active; Latch Row Address |
| | L | L | H | L | BS | AP | NOP ⁴ |
| | L | L | L | H | X | X | Auto-Refresh or Self-Refresh ⁵ |
| | L | L | L | L | Op- | Code | Mode reg. Access ⁵ |
| Row Active | H | X | X | X | X | X | NOP |
| | L | H | H | X | X | X | NOP |
| | L | H | L | H | BS | CA,AP | Begin Read; Latch CA; DetermineAP |
| | L | H | L | L | BS | CA,AP | Begin Write; Latch CA; DetermineAP |
| | L | L | H | H | BS | X | ILLEGAL ² |
| | L | L | H | L | BS | AP | Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Read | H | X | X | X | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | L | BS | X | ILLEGAL |
| | L | H | L | H | BS | CA,AP | Term Burst, New Read, DetermineAP ³ |
| | L | H | L | L | BS | CA,AP | Term Burst, Start Write, DetermineAP ³ |
| | L | L | H | H | BS | X | ILLEGAL to Same Bank, other Bank OK if tRRD is Satisfied |
| | L | L | H | L | BS | AP | Term Burst, Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Write | H | X | X | X | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | L | BS | X | ILLEGAL |
| | L | H | L | H | BS | CA,AP | Term Burst, Start Read, DetermineAP ³ |
| | L | H | L | L | BS | CA,AP | Term Burst, New Write, DetermineAP ³ |
| | L | L | H | H | BS | X | ILLEGAL ² |
| | L | L | H | L | BS | AP | Term Burst, Precharge ³ |
| | L | L | L | X | X | X | ILLEGAL |
| Read with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | L | BS | X | ILLEGAL ² |
| | L | H | L | H | BS | X | ILLEGAL ² |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | H | BS | X | ILLEGAL ² |
| | L | L | H | L | BS | AP | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |

DDR SDRAM Function Truth Table (continued)

| CURRENT STATE ¹ | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | \overline{BS} | Addr | ACTION |
|----------------------------|-----------------|------------------|------------------|-----------------|-----------------|------|--|
| Write with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | L | BS | X | ILLEGAL ² |
| | L | H | L | H | BS | X | ILLEGAL ² |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | H | BS | X | ILLEGAL ² |
| | L | L | H | L | BS | AP | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |
| Precharging | H | X | X | X | X | X | NOP;> Idle after tRP |
| | L | H | H | H | X | X | NOP;> Idle after tRP |
| | L | H | H | L | BS | X | ILLEGAL ² |
| | L | H | L | X | BS | X | ILLEGAL ² |
| | L | L | H | H | BS | X | (0K Provided tRP Satisfied) ACT |
| | L | L | H | L | BS | AP | NOP ⁴ |
| | L | L | L | X | X | X | ILLEGAL |
| Row Activating | H | X | X | X | X | X | NOP;> Row Active after tRCD |
| | L | H | H | H | X | X | NOP;> Row Active after tRCD |
| | L | H | H | L | BS | X | ILLEGAL ² |
| | L | H | L | X | BS | X | (0K if tRCD satisfied) Read/Write |
| | L | L | H | H | BS | X | (0K to other Bank if tRRD Satisfied) ACT |
| | L | L | H | L | BS | AP | Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Write Recovering | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BS | X | ILLEGAL ² |
| | L | H | L | X | BS | X | ILLEGAL ² |
| | L | L | H | H | BS | X | ILLEGAL ² |
| | L | L | H | L | BS | AP | ILLEGAL ² |
| | L | L | L | X | X | X | ILLEGAL |
| Refreshing | H | X | X | X | X | X | NOP;> Idle after tRC |
| | L | H | H | X | X | X | NOP;> Idle after tRC |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | H | X | X | X | ILLEGAL |
| | L | L | L | X | X | X | ILLEGAL |
| Mode Register Accessing | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | X | X | ILLEGAL |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | ILLEGAL |

Clock Enable (CKE) Truth Table

| STATE(n) | CKE n-1 | CKE n | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Addr | ACTION |
|---|------------|----------|-----------------|------------------|------------------|-----------------|------|--|
| Self-Refresh ⁶ | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | EXIT Self-Refresh, Idle after tRC |
| | L | H | L | H | H | H | X | EXIT Self-Refresh, Idle after tRC |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Self-Refresh) |
| Power-Down | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | EXIT Power-Down, > Idle. |
| | L | H | L | H | H | H | X | EXIT Power-Down, > Idle. |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Low-Power Mode) |
| All. Banks Idle ⁷ | H | H | X | X | X | X | X | Refer to the function truth table |
| | H | L | H | X | X | X | X | Enter Power- Down |
| | H | L | L | H | H | H | X | Enter Power- Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | H | X | X | ILLEGAL |
| | H | L | L | L | L | H | X | Enter Self-Refresh |
| | H | L | L | L | L | L | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP |
| Any State other than listed above | H | H | X | X | X | X | X | Refer to the function truth table |
| | H | L | X | X | X | X | X | Begin Clock Suspend next cycle ⁸ |
| | L | H | X | X | X | X | X | Exit Clock Suspend next cycle ⁸ . |
| | L | L | X | X | X | X | X | Maintain Clock Suspend. |

Abbreviations:

RA = Row Address

BS = Bank Select Address

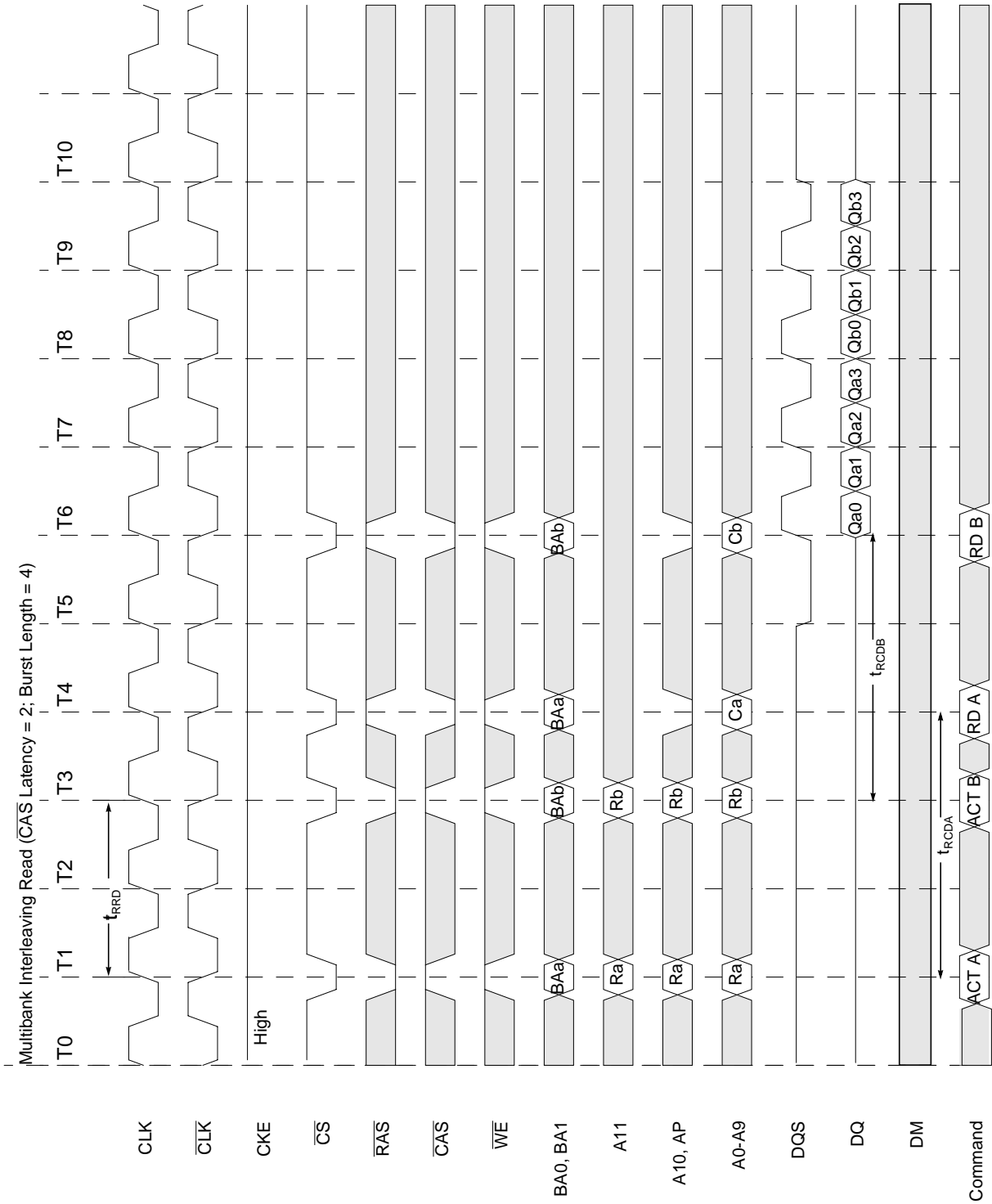
CA = Column Address

AP = Auto Precharge

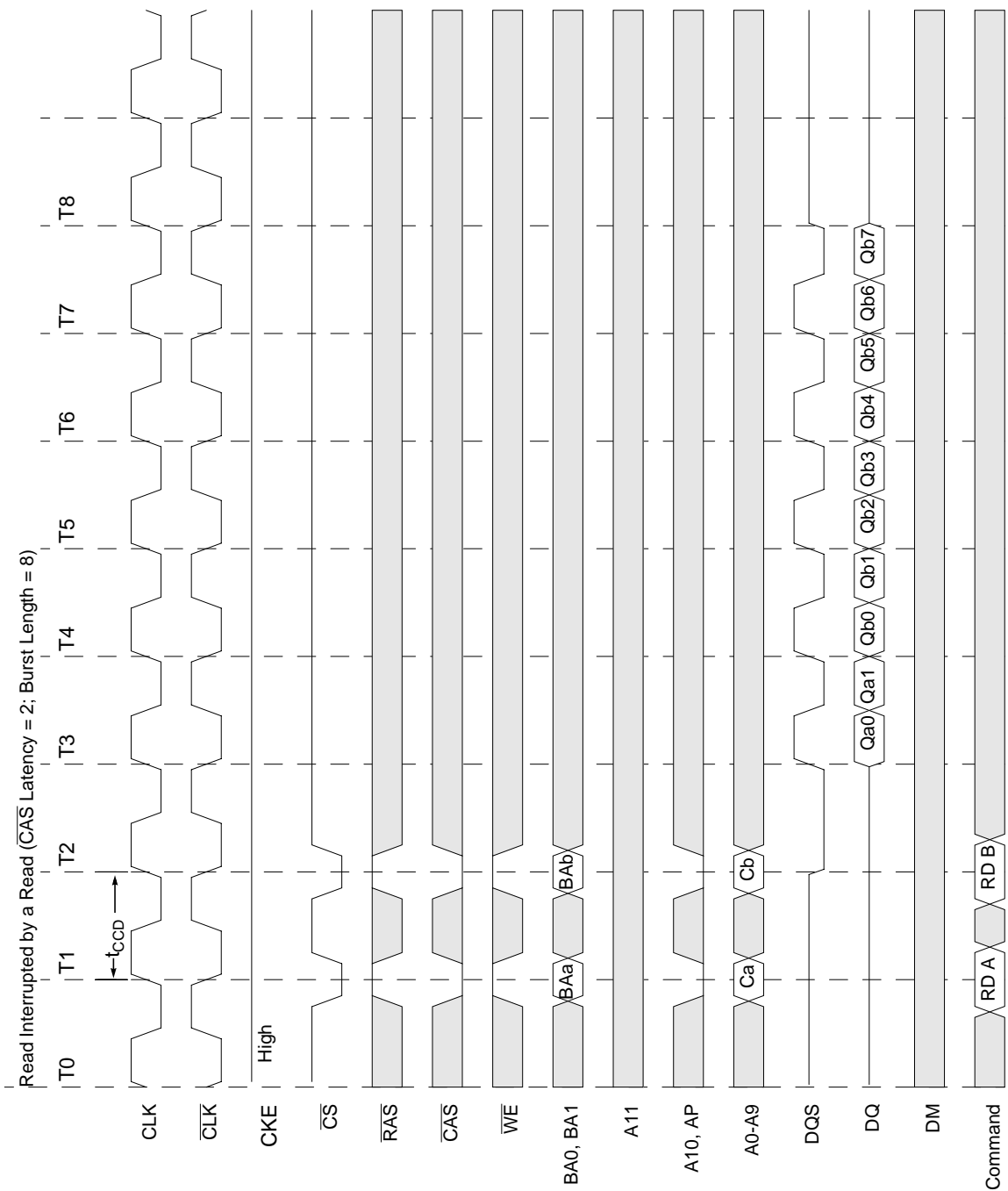
Notes for SDRAM function truth table:

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. The precharge bank(s) indicated by BS and AP.
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

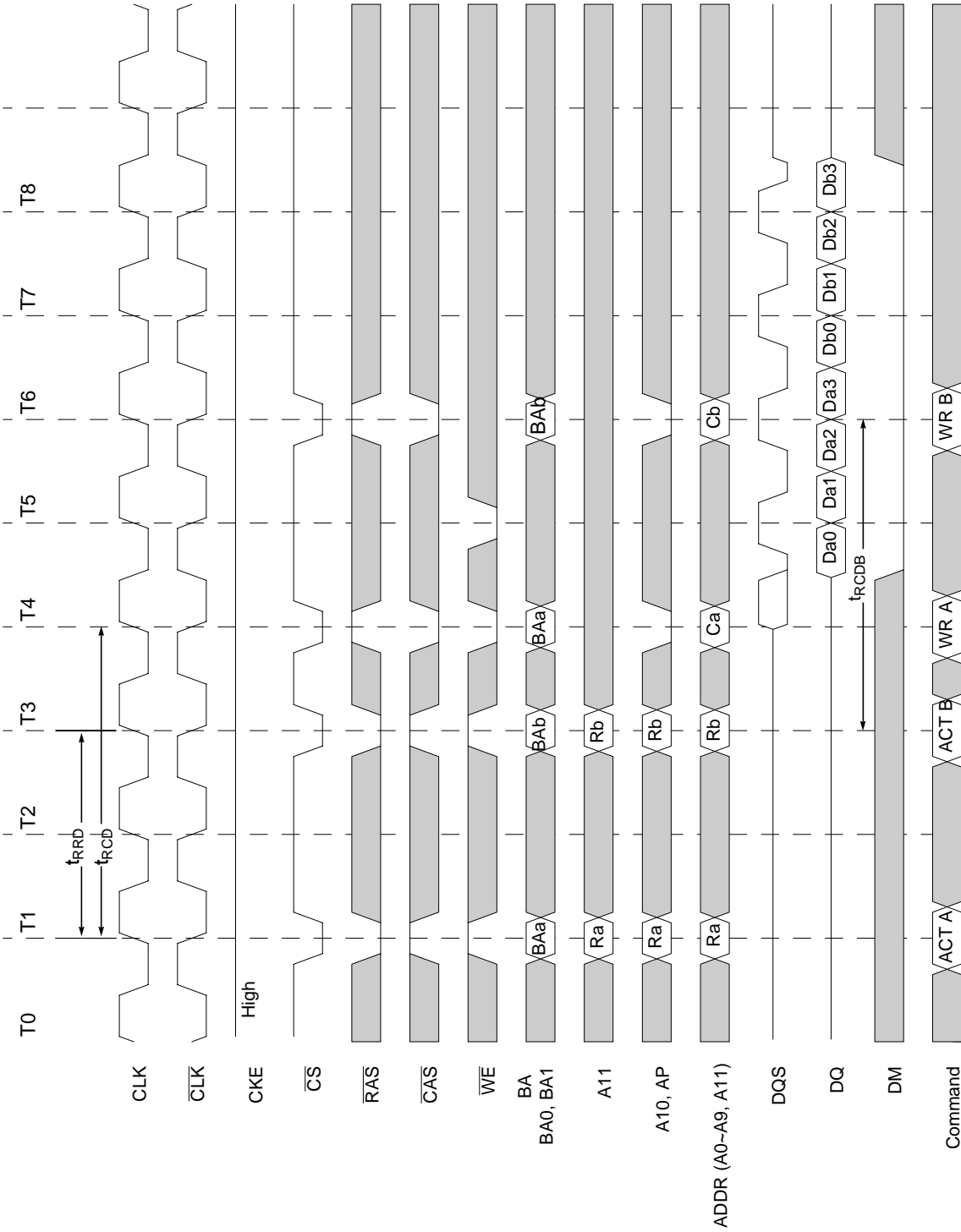
Multibank Interleaving Read



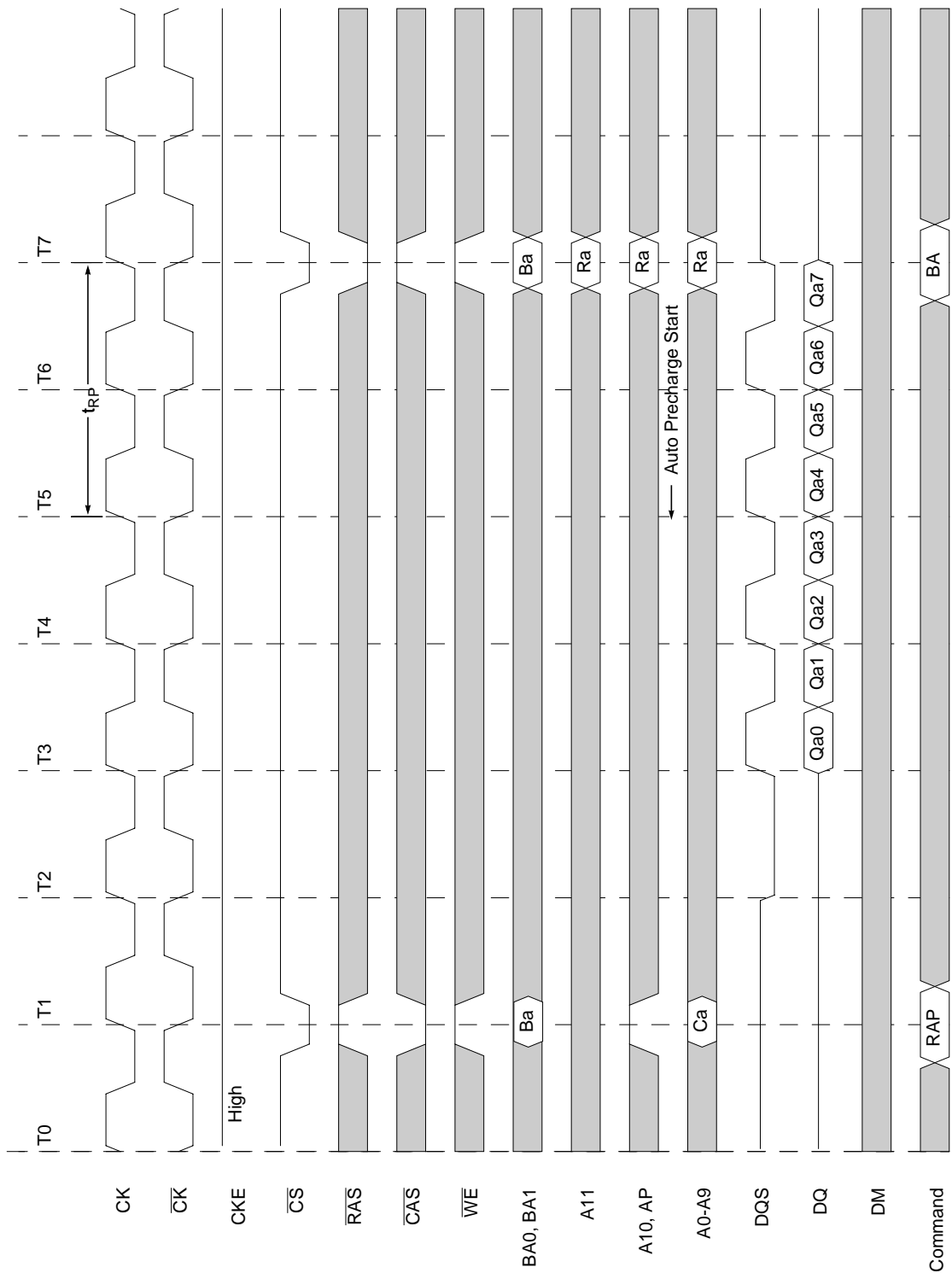
Read Interrupted by a Read



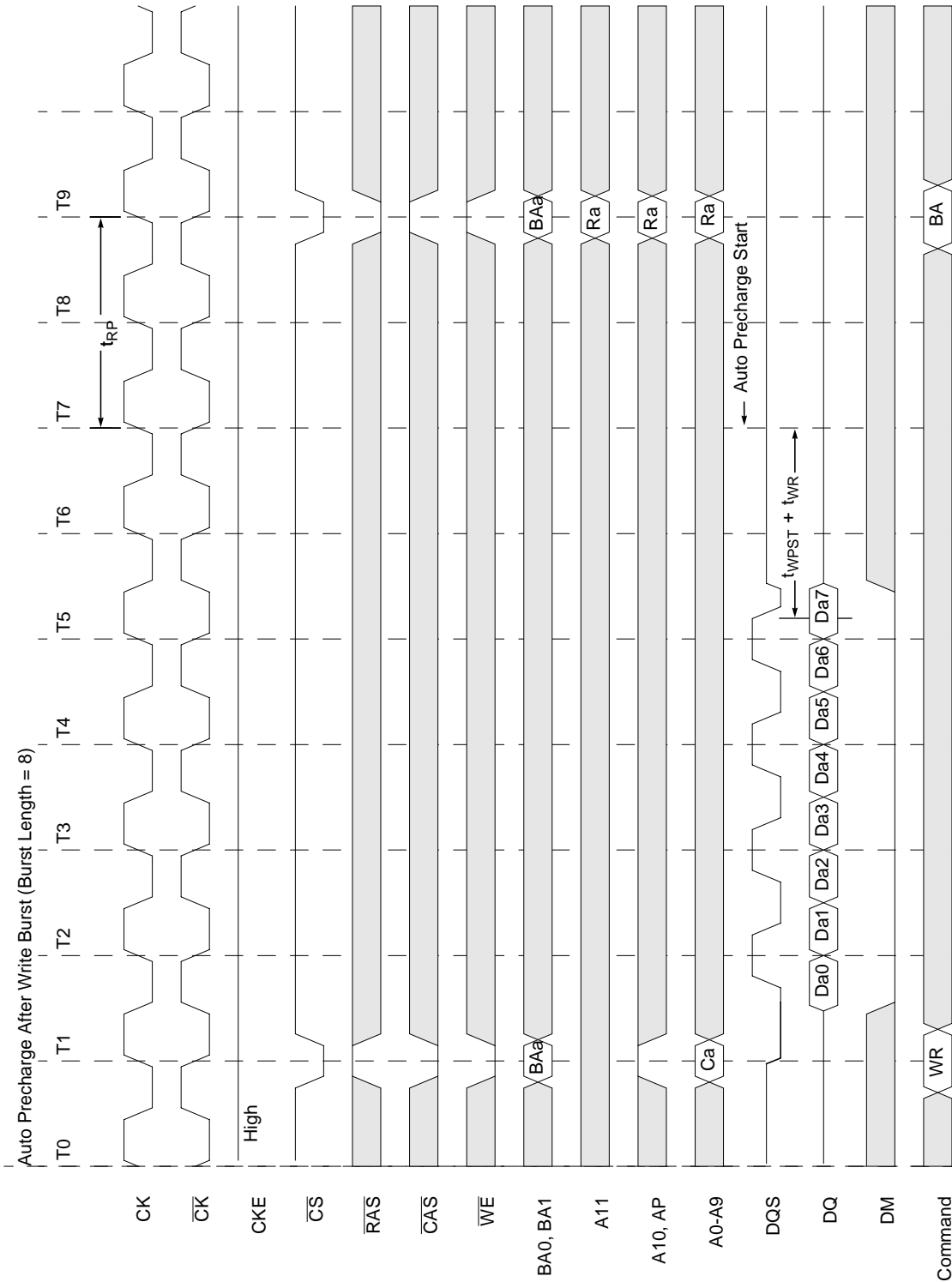
Multi Bank Interleaving Write (@ BL = 4)



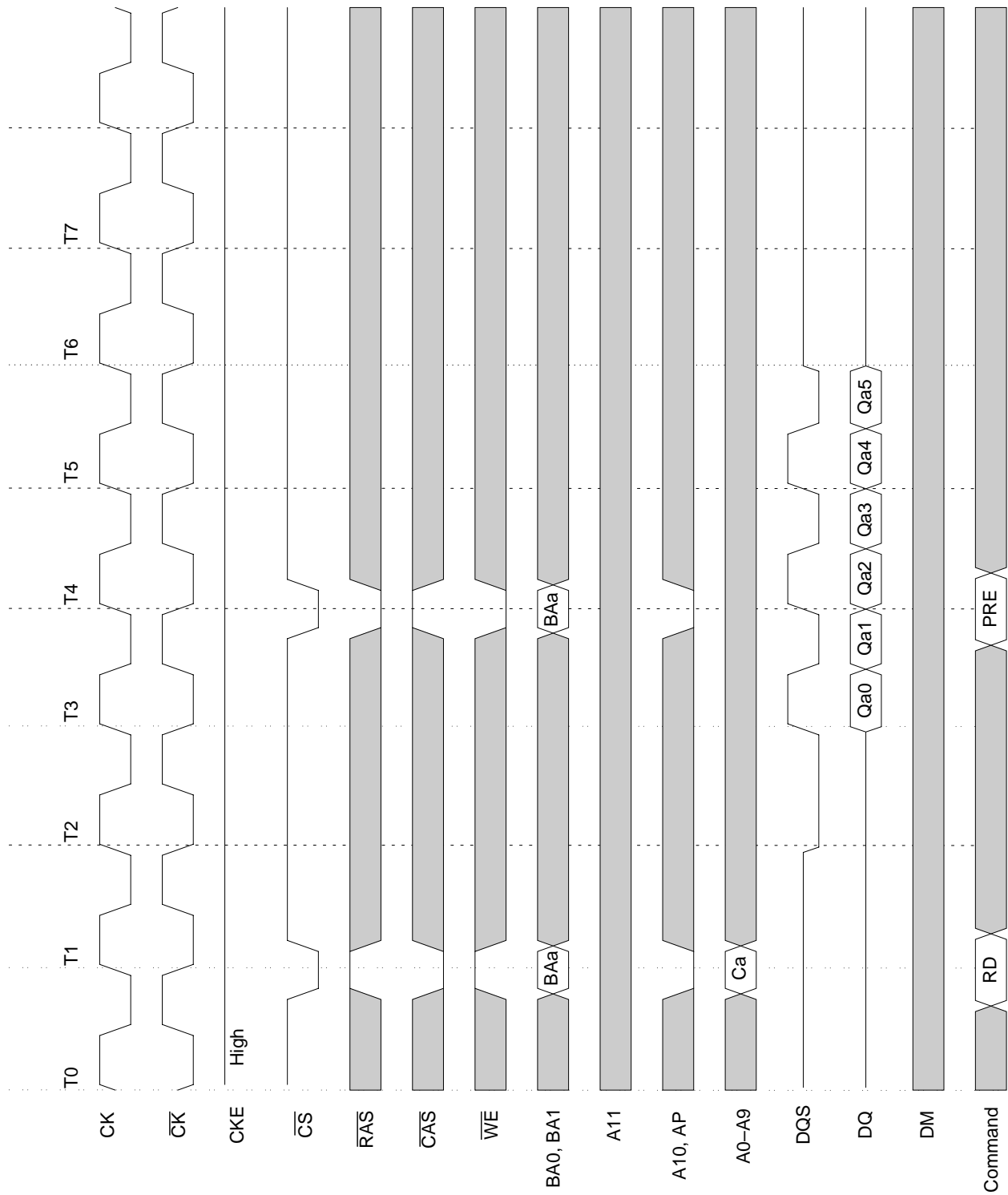
Auto Precharge After Read Burst (@ BL = 8, CL = 2)



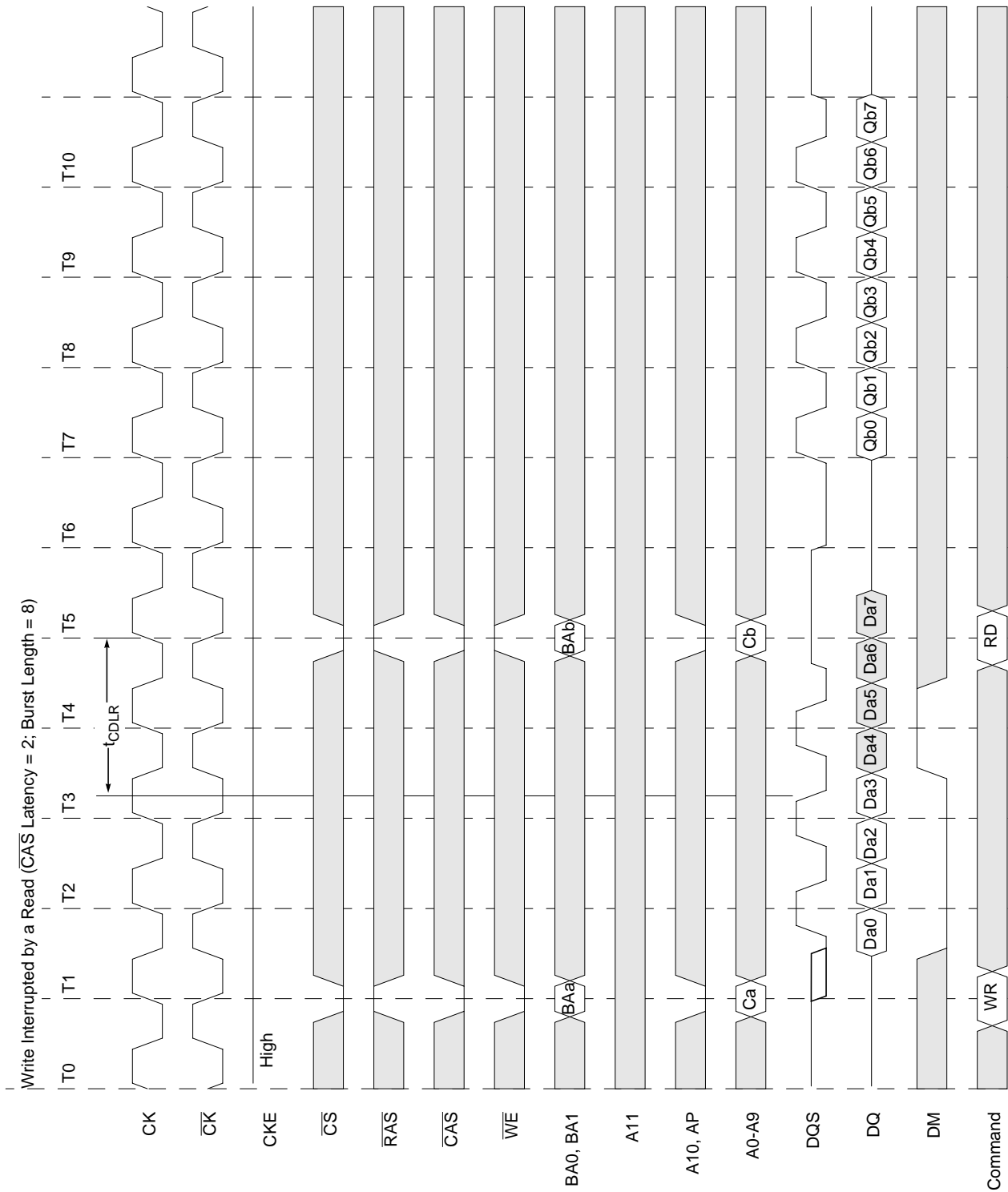
Auto Precharge After Write Burst (@ BL=8)



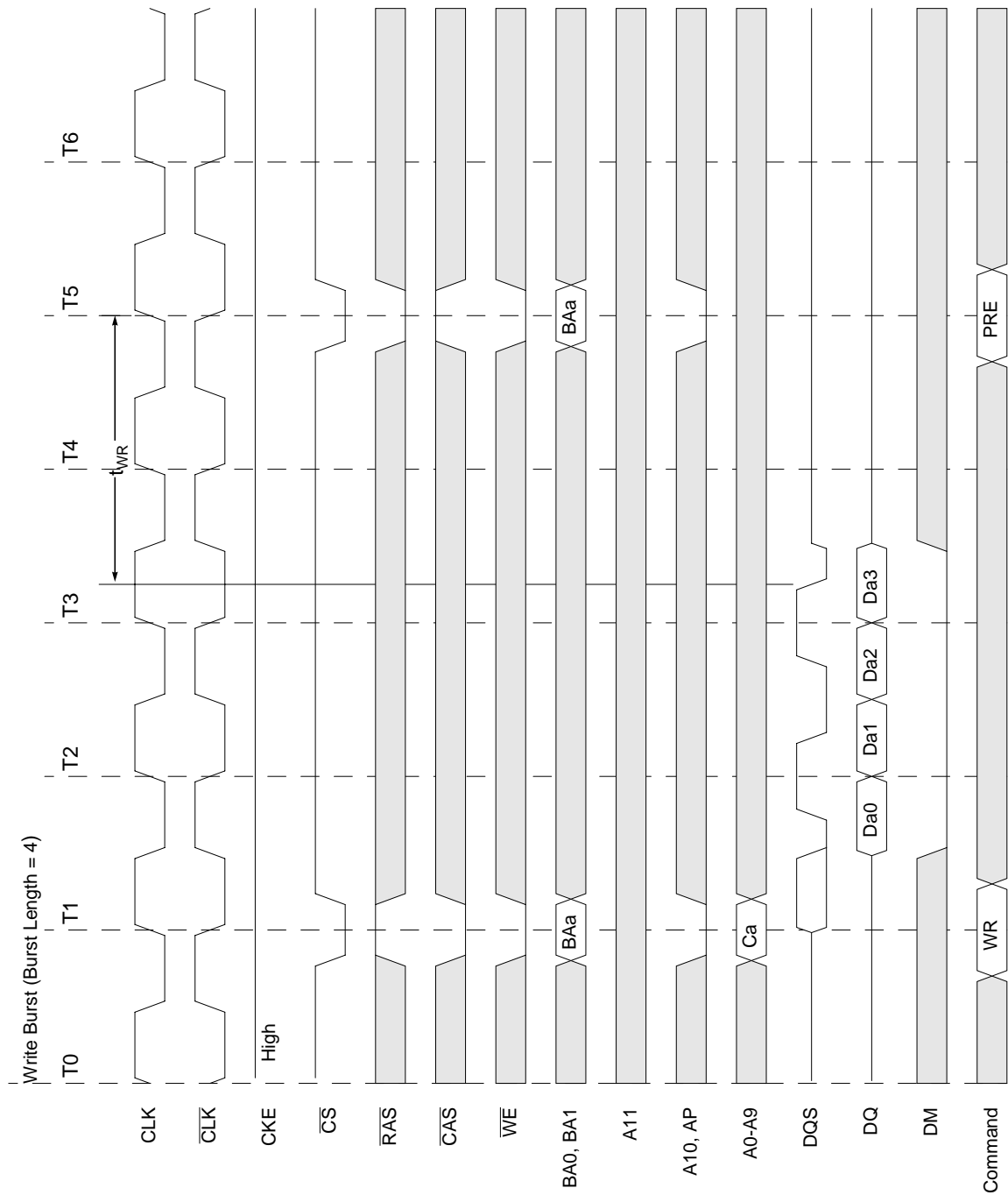
Read Interrupted by Precharge (@BL = 8, CL = 2)



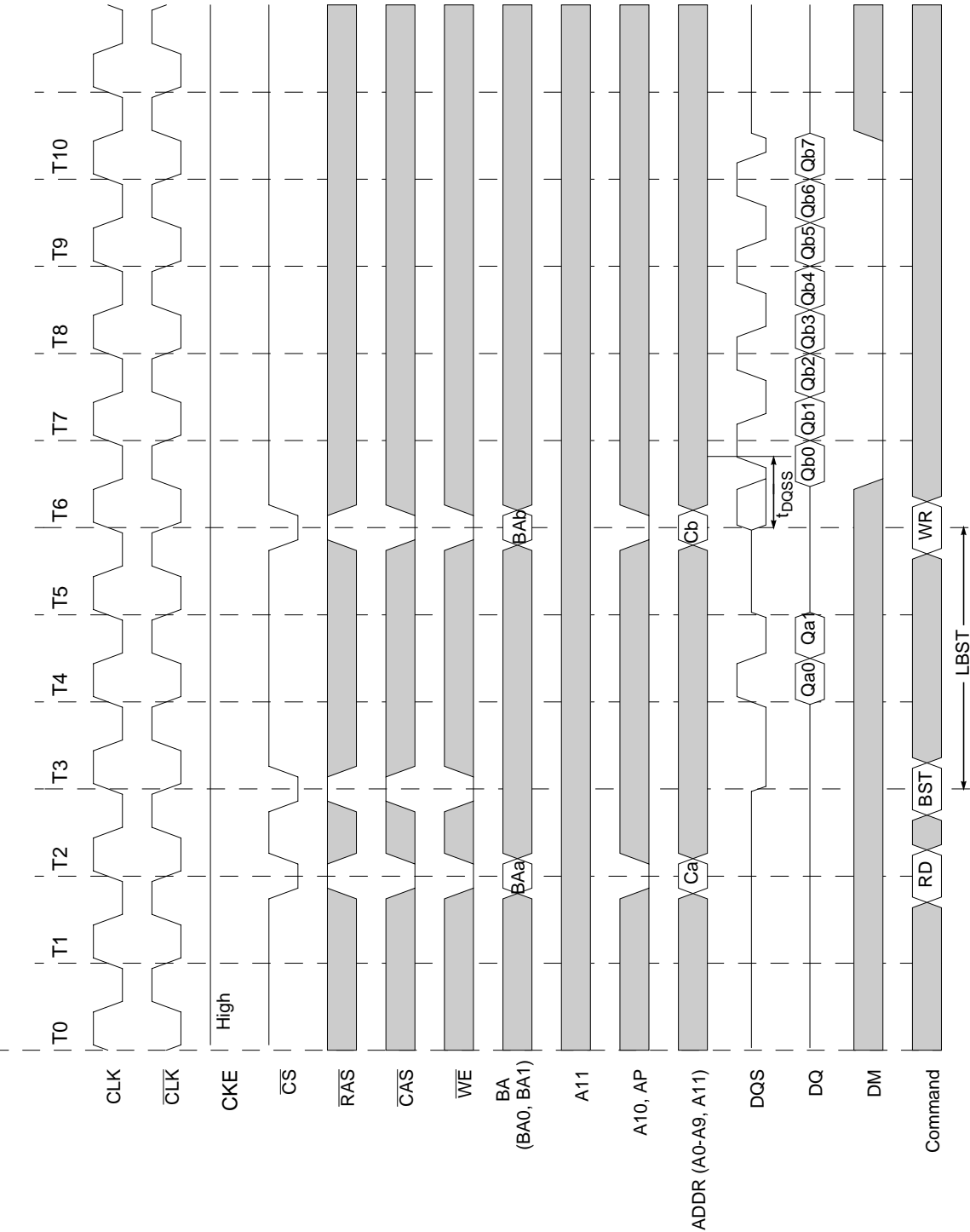
Write Interrupted by a Read (@BL=8, CL=2)



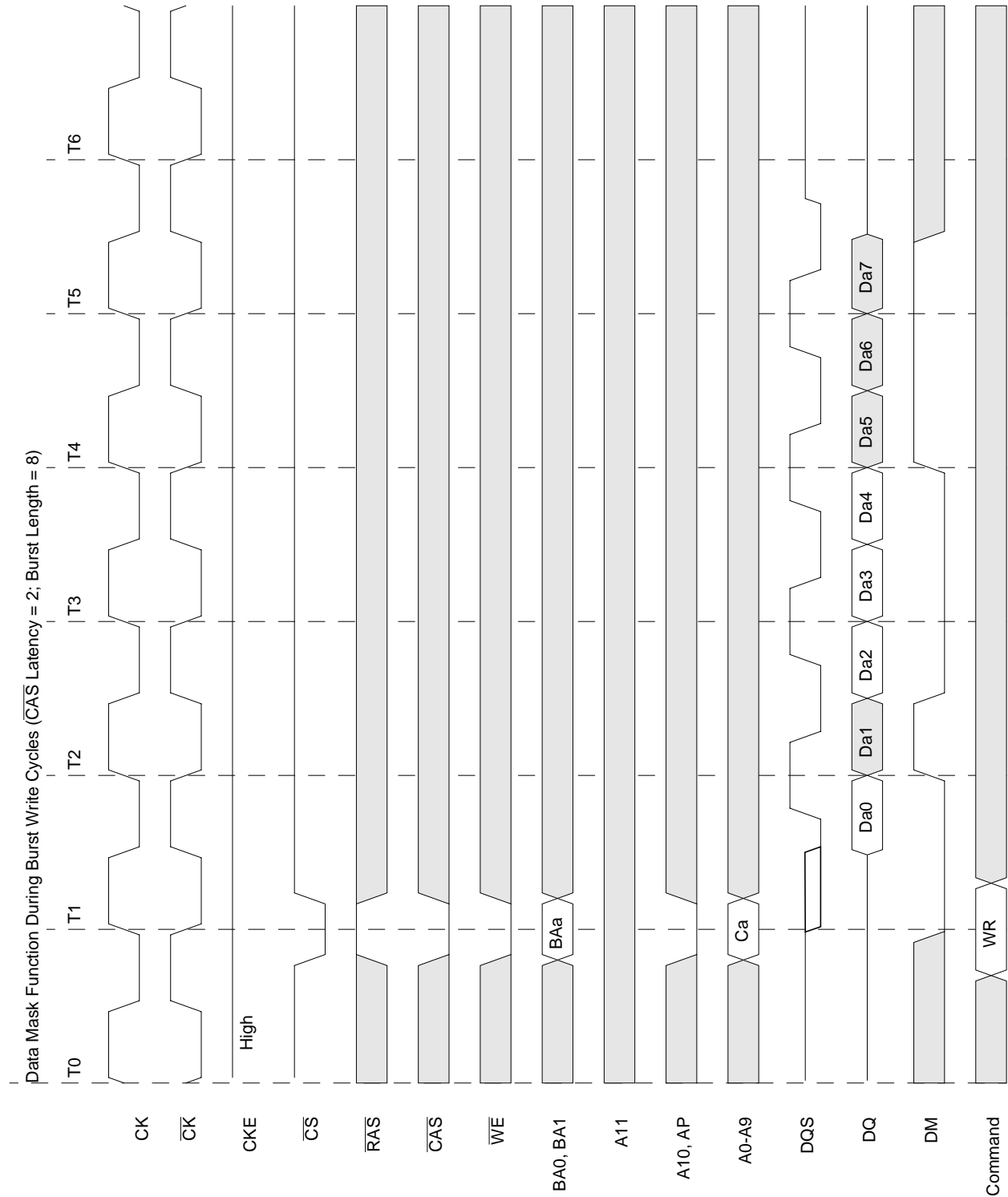
Write Burst



Read Interrupted by a Write and Burst Stop



Data Mask Function (@BL=8) Only for Write



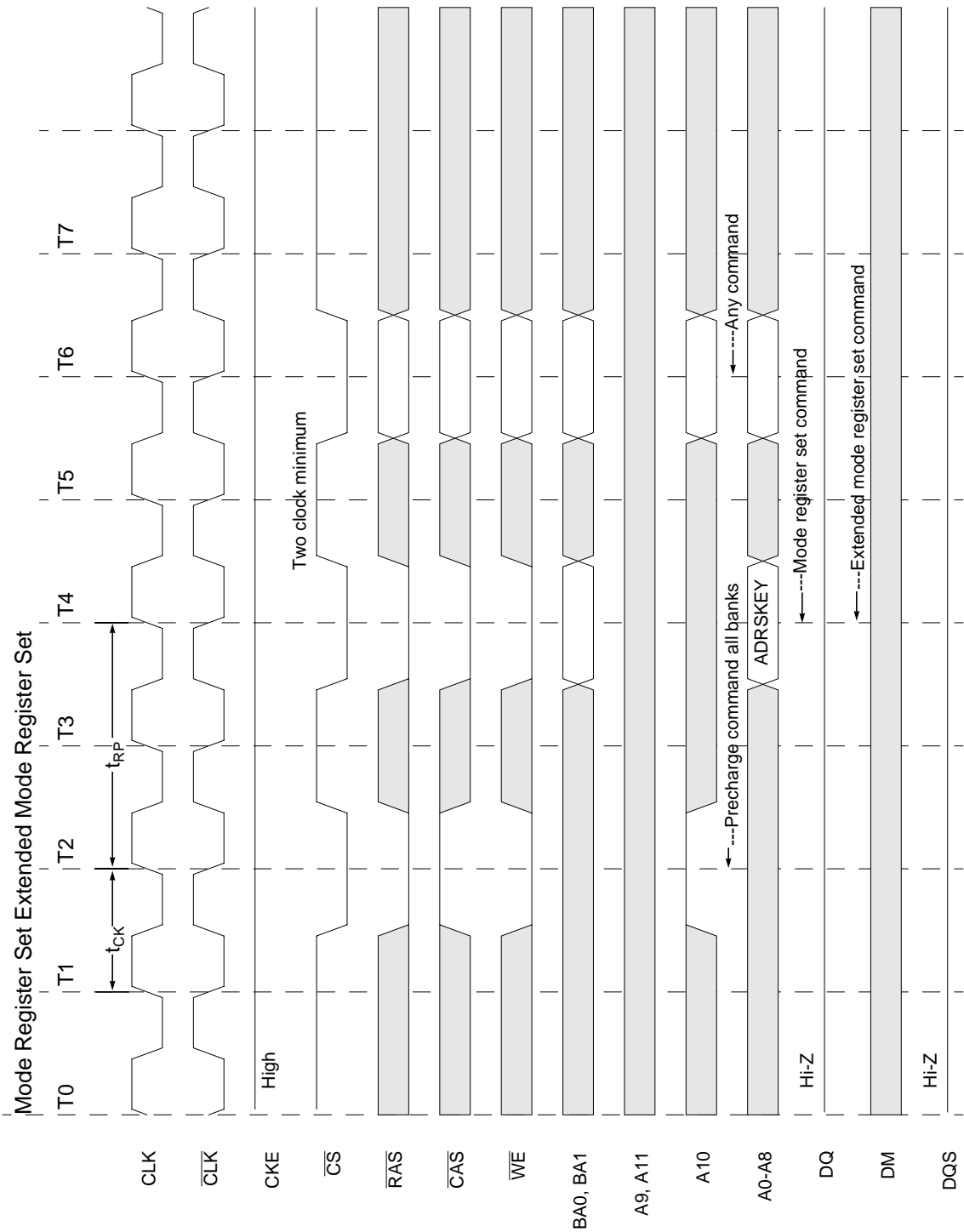
The diagram illustrates the timing sequence for power-up and auto refresh. Key signals and their timing requirements are as follows:

- CLK**: Clock signal. A period of 200 clock minimum is indicated between T0 and T1.
- CLK**: Clock signal. A period of 200 clock minimum is indicated between T1 and T2.
- CKE**: Clock Enable. High level is required from T0 to T1.
- CS**: Chip Select. Minimum of two refresh cycles is required from T0 to T1.
- RAS**: Row Address Strobe. Two clock minimum is indicated between T0 and T1.
- CAS**: Column Address Strobe. Two clock minimum is indicated between T0 and T1.
- WE**: Write Enable. Two clock minimum is indicated between T0 and T1.
- BA0, BA1, A0, A1-A6, A7, A8, A9, A11**: Address signals. Two clock minimum is indicated between T0 and T1.
- A10**: Address signal. Two clock minimum is indicated between T0 and T1.
- DQ, DM, DQS**: Data signals. Two clock minimum is indicated between T0 and T1.

Additional annotations include:

- High level is required**: Indicated for CKE from T0 to T1.
- Minimum of two refresh cycles is required**: Indicated for CS from T0 to T1.
- Two clock minimum**: Indicated for RAS, CAS, WE, BA0, BA1, A0, A1-A6, A7, A8, A9, A11, and A10 from T0 to T1.
- Precharge all**: Indicated for DQ, DM, and DQS from T0 to T1.

Mode Register/Extended Mode Register Set



Units : Millimeters



U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

HONG KONG

19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 852-2666-3307
FAX: 852-2770-8011

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
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FAX: 886-2-2545-1209

NO 19 LI HSIN RD.
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-579-5888
FAX: 886-3-566-5888

SINGAPORE

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INTERNATIONAL PLAZA
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PHONE: 65-3231801
FAX: 65-3237013

JAPAN

WBG MARIVE WEST 25F
6, NAKASE 2-CHOME
MIHAMA-KU, CHIBA-SHI
CHIBA 261-7125
PHONE: 81-43-299-6000
FAX: 81-43-299-6555

UK & IRELAND

SUITE 50, GROVEWOOD
BUSINESS CENTRE
STRATHCLYDE BUSINESS
PARK
BELLSHILL, LANARKSHIRE,
SCOTLAND, ML4 3NQ
PHONE: 01698-748515
FAX: 01698-748516

**GERMANY
(CONTINENTAL
EUROPE & ISRAEL)**

71083 HERRENBERG
BENZSTR. 32
GERMANY
PHONE: +49 7032 2796-0
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U.S. SALES OFFICES**NORTHWESTERN**

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