## MOSEL VITELIC

### V54C365804VD(L)
### HIGH PERFORMANCE 143/133/125 MHz
### 3.3 VOLT 8M X 8 SYNCHRONOUS DRAM
### 4 BANKS X 2Mbit X 8

*PRELIMINARY*

|  | 7 | 75 | 8PC | 8 |
|---|---|---|---|---|
| System Frequency ($f_{CK}$) | 143MHz | 133MHz | 125 MHz | 125 MHz |
| Clock Cycle Time ($t_{CK3}$) | 7 ns | 7.5 ns | 8 ns | 8 ns |
| Clock Access Time ($t_{AC3}$) $\overline{CAS}$ Latency = 3 | 5.4 ns | 5.4 ns | 6 ns | 7 ns |
| Clock Access Time ($t_{AC2}$) CAS Latency = 2 | 5.5 ns | 6 ns | 6 ns | 7 ns |

### Features

- 4 banks x 2Mbit x 8 organization
- High speed data transfer rates up to 143 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed $\overline{RAS}$ Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page for Sequential Type
  1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Suspend Mode and Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 54 Pin 400 mil TSOP-II
- LVTTL Interface
- Single +3.3 V ±0.3 V Power Supply

### Description

The V54C365804VD(L) is a four bank Synchronous DRAM organized as 4 banks x 2Mbit x 8. The V54C365804VD(L) achieves high speed data transfer rates up to 143 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock

All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 143 MHz is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

### Device Usage Chart

| Operating Temperature Range | Package Outline | Access Time (ns) | | | | Power | | Temperature Mark |
|---|---|---|---|---|---|---|---|---|
| | T | 7 | 75 | 8PC | 8 | Std. | L | |
| 0°C to 70°C | • | • | • | • | • | • | • | Blank |

| Description | Pkg. | Pin Count |
|-------------|------|-----------|
| TSOP-II | T | 54 |

## 54 Pin Plastic TSOP-II
## PIN CONFIGURATION
## Top View

| Left | | | Right |
|------|--|--|-------|
| $V_{CC}$ | 1 | 54 | $V_{SS}$ |
| $I/O_1$ | 2 | 53 | $I/O_8$ |
| $V_{CCQ}$ | 3 | 52 | $V_{SSQ}$ |
| NC | 4 | 51 | NC |
| $I/O_2$ | 5 | 50 | $I/O_7$ |
| $V_{SSQ}$ | 6 | 49 | $V_{CCQ}$ |
| NC | 7 | 48 | NC |
| $I/O_3$ | 8 | 47 | $I/O_6$ |
| $V_{CCQ}$ | 9 | 46 | $V_{SSQ}$ |
| NC | 10 | 45 | NC |
| $I/O_4$ | 11 | 44 | $I/O_5$ |
| $V_{SSQ}$ | 12 | 43 | $V_{CCQ}$ |
| NC | 13 | 42 | NC |
| $V_{CC}$ | 14 | 41 | $V_{SS}$ |
| NC | 15 | 40 | NC |
| $\overline{WE}$ | 16 | 39 | DQM |
| $\overline{CAS}$ | 17 | 38 | CLK |
| $\overline{RAS}$ | 18 | 37 | CKE |
| $\overline{CS}$ | 19 | 36 | NC |
| BA0 | 20 | 35 | $A_{11}$ |
| BA1 | 21 | 34 | $A_9$ |
| $A_{10}$ | 22 | 33 | $A_8$ |
| $A_0$ | 23 | 32 | $A_7$ |
| $A_1$ | 24 | 31 | $A_6$ |
| $A_2$ | 25 | 30 | $A_5$ |
| $A_3$ | 26 | 29 | $A_4$ |
| $V_{CC}$ | 27 | 28 | $V_{SS}$ |

365804VA 01

## Pin Names

| | |
|--|--|
| CLK | Clock Input |
| CKE | Clock Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $A_0$–$A_{11}$ | Address Inputs |
| BA0, BA1 | Bank Select |
| $I/O_1$–$I/O_8$ | Data Input/Output |
| DQM | Data Mask |
| $V_{CC}$ | Power (+3.3V) |
| $V_{SS}$ | Ground |
| $V_{CCQ}$ | Power for I/O's (+3.3V) |
| $V_{SSQ}$ | Ground for I/O's |
| NC | Not connected |

# MOSEL VITELIC

*V54C365804VD(L)*

## *Capacitance\**

$T_A = 0$ to $70°C$, $V_{CC} = 3.3$ V $\pm$ 0.3 V, f = 1 Mhz

| Symbol | Parameter | Max. | Unit |
|--------|-----------|------|------|
| $C_{I1}$ | Input Capacitance (A0 to A11) | 5 | pF |
| $C_{I2}$ | Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE, DQM | 5 | pF |
| $C_{IO}$ | Output Capacitance (I/O) | 6.5 | pF |
| $C_{CLK}$ | Input Capacitance (CLK) | 4 | pF |

*\*Note:*Capacitance is sampled and not 100% tested.

## *Block Diagram*
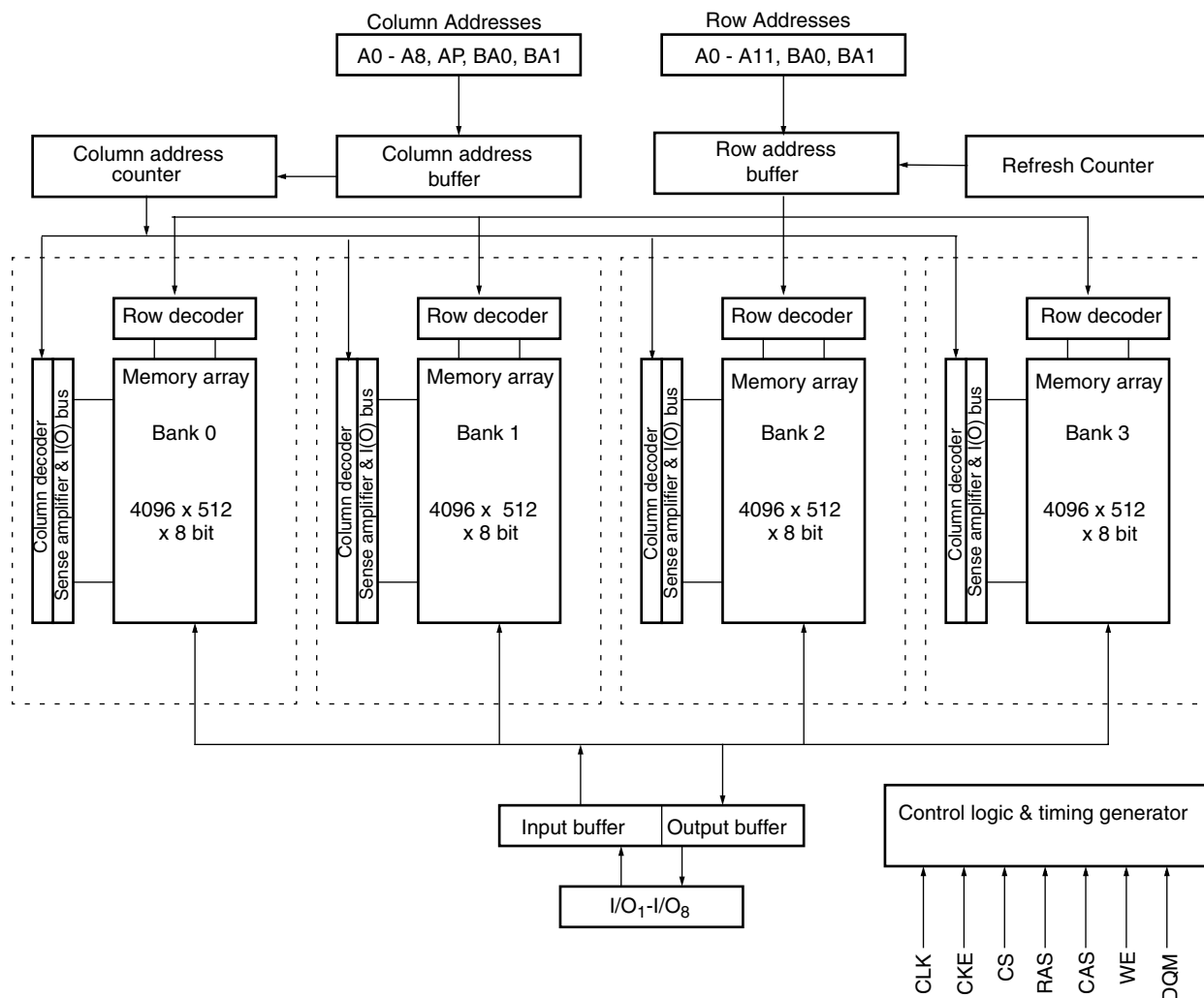
## *Signal Pin Description*

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| CLK | Input | Pulse | Positive Edge | The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock. |
| CKE | Input | Level | Active High | Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode. |
| $\overline{CS}$ | Input | Pulse | Active Low | $\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}, \overline{CAS}$ $\overline{WE}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM. |
| A0 - A11 | Input | Level | — | During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organization: 8M x 8 SDRAM  CA0–CA8    (Page Length = 512 bits)<br><br>In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge. |
| BA0, BA1 | Input | Level | — | Selects which bank is to be active. |
| DQx | Input Output | Level | — | Data Input/Output pins operate in the same manner as on conventional DRAMs. |
| DQM | Input | Pulse | Active High | The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. One DQM input is present in x4 and x8 DRAMs. |
| VCC, VSS | Supply | | | Power and ground for the input buffers and the core logic. |
| VCCQ VSSQ | Supply | — | — | Isolated power supply and ground for the output buffers to provide improved noise immunity. |

## *Operation Definition*

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the thruth table for the operation commands.

| Operation | Device State | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | A0-9, A11 | A10 | BS0 BS1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Row Activate | Idle[3] | H | X | L | L | H | H | X | V | V | V |
| Read | Active[3] | H | X | L | H | L | H | X | V | L | V |
| Read w/Autoprecharge | Active[3] | H | X | L | H | L | H | X | V | H | V |
| Write | Active[3] | H | X | L | H | L | L | X | V | L | V |
| Write with Autoprecharge | Active[3] | H | X | L | H | L | L | X | V | H | V |
| Row Precharge | Any | H | X | L | L | H | L | X | X | L | V |
| Precharge All | Any | H | X | L | L | H | L | X | X | H | X |
| Mode Register Set | Idle | H | X | L | L | L | L | X | V | V | V |
| No Operation | Any | H | X | L | H | H | H | X | X | X | X |
| Device Deselect | Any | H | X | H | X | X | X | X | X | X | X |
| Auto Refresh | Idle | H | H | L | L | L | H | X | X | X | X |
| Self Refresh Entry | Idle | H | L | L | L | L | H | X | X | X | X |
| Self Refresh Exit | Idle (Self Refr.) | L | H | H | X | X | X | X | X | X | X |
| | | | | L | H | H | X | | | | |
| Power Down Entry | Idle Active[5] | H | L | H | X | X | X | X | X | X | X |
| | | | | L | H | H | X | | | | |
| Power Down Exit | Any (Power Down) | L | H | H | X | X | X | X | X | X | X |
| | | | | L | H | H | L | | | | |
| Data Write/Output Enable | Active | H | X | X | X | X | X | L | X | X | X |
| Data Write/Output Disable | Active | H | X | X | X | X | X | H | X | X | X |

**Notes:**
1.  V = Valid , x = Don't Care,  L = Low Level, H = High Level
2.  CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3.  These are state of bank designated by BS0, BS1 signals.
4.  Device state is Full Page Burst operation
5.  Power Down Mode can not entry in the burst cycle. When this command assert in the burst mode cycle device is clock suspend mode.

### Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VCC and VCCQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed VCC+0.3V on any of the input pins or VCC supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 μs is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

### Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS **Latency** Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at l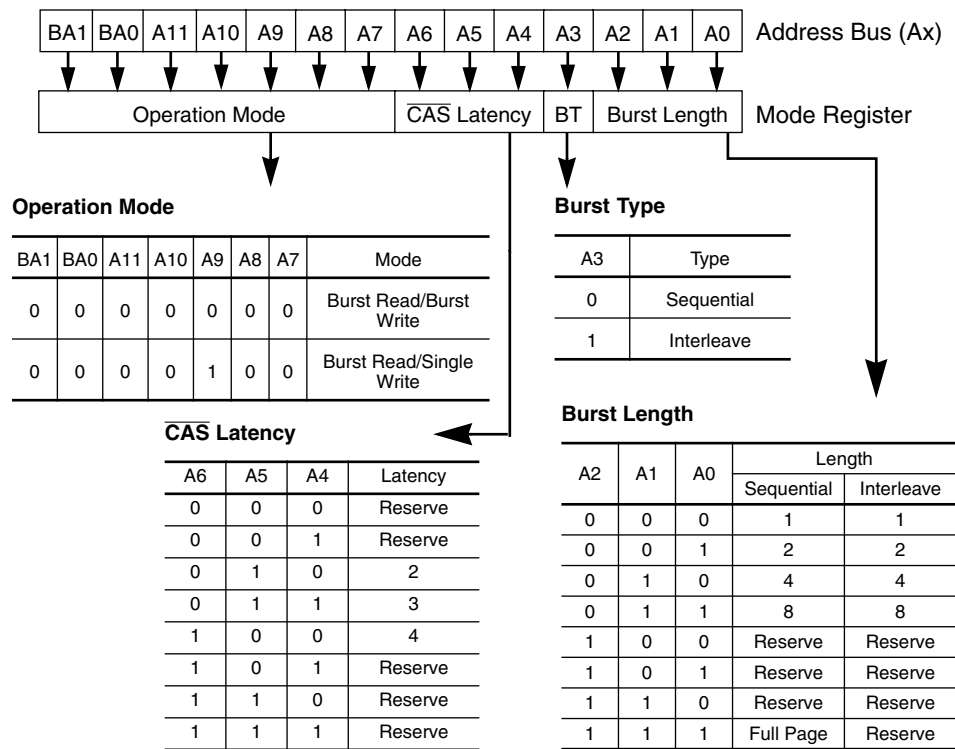east one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

### Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, $t_{RCD}$, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 143 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 3 or 8, full page burst continues until it is terminated using another command.

### Address Input for Mode Set (Mode Register Operation)

| BA1 | BA0 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address Bus (Ax) |

| Operation Mode | | | $\overline{CAS}$ Latency | BT | Burst Length | Mode Register |

**Operation Mode**

| BA1 | BA0 | A11 | A10 | A9 | A8 | A7 | Mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Burst Read/Burst Write |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | Burst Read/Single Write |

**Burst Type**

| A3 | Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

**$\overline{CAS}$ Latency**

| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserve |
| 0 | 0 | 1 | Reserve |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | Reserve |
| 1 | 1 | 0 | Reserve |
| 1 | 1 | 1 | Reserve |

**Burst Length**

| A2 | A1 | A0 | Length | |
|---|---|---|---|---|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserve | Reserve |
| 1 | 0 | 1 | Reserve | Reserve |
| 1 | 1 | 0 | Reserve | Reserve |
| 1 | 1 | 1 | Full Page | Reserve |

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum $t_{RAS}$ or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

## Burst Length and Sequence:

| Burst Length | Starting Address (A2 A1 A0) | Sequential Burst Addressing (decimal) | Interleave Burst Addressing (decimal) |
|---|---|---|---|
| 2 | xx0<br>xx1 | 0, 1<br>1, 0 | 0, 1<br>1, 0 |
| 4 | x00<br>x01<br>x10<br>x11 | 0, 1, 2, 3<br>1, 2, 3, 0<br>2, 3, 0, 1<br>3, 0, 1, 2 | 0, 1, 2, 3<br>1, 0, 3, 2<br>2, 3, 0, 1<br>3, 2, 1, 0 |
| 8 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | 0 1 2 3 4 5 6 7<br>1 2 3 4 5 6 7 0<br>2 3 4 5 6 7 0 1<br>3 4 5 6 7 0 1 2<br>4 5 6 7 0 1 2 3<br>5 6 7 0 1 2 3 4<br>6 7 0 1 2 3 4 5<br>7 0 1 2 3 4 5 6 | 0 1 2 3 4 5 6 7<br>1 0 3 2 5 4 7 6<br>2 3 0 1 6 7 4 5<br>3 2 1 0 7 6 5 4<br>4 5 6 7 0 1 2 3<br>5 4 7 6 1 0 3 2<br>6 7 4 5 2 3 0 1<br>7 6 5 4 3 2 1 0 |
| Full Page | nnn | Cn, Cn+1, Cn+2,..... | not supported |

### Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one $t_{RC}$ delay is required prior to any access command.

### DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to "high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency $t_{DQZ}$ ). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency $t_{DQW}$ = zero clocks).

### Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency $t_{CSL}$).

### Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE "high". One clock delay is required for mode entry and exit.

### Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the

operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, two clocks for $\overline{CAS}$ latencies 3 and three clocks for CAS latencies 4. If CAS10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to $t_{WR}$ (Write recovery time) after the last data in.

### *Precharge Command*

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2, two clocks before the last data out for CAS latency = 3 and three clocks before the last data out for CAS latency = 4. Writes require a time delay twr from the last data out to apply the precharge command.

Bank Selection by Address Bits:

| A10 | BA0 | BA1 | |
|-----|-----|-----|-----------|
| 0 | 0 | 0 | Bank 0 |
| 0 | 0 | 1 | Bank 1 |
| 0 | 1 | 0 | Bank 2 |
| 0 | 1 | 1 | Bank 3 |
| 1 | X | X | all Banks |

### *Burst Termination*

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory.

## MOSEL VITELIC

<div align="right"><em>V54C365804VD(L)</em></div>

### Absolute Maximum Ratings*

Operating temperature range ..................0 to 70 °C
Storage temperature range ............... -55 to 150 °C
Input/output voltage .................. -0.3 to ($V_{CC}$+0.3) V
Power supply voltage .......................... -0.3 to 4.6 V
Power dissipation ............................................ 1 W
Data out current (short circuit) ...................... 50 mA

**\*Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Recommended Operation and Characteristics for LV-TTL

$T_A$ = 0 to 70 °C; $V_{SS}$ = 0 V; $V_{CC}$, $V_{CCQ}$ = 3.3 V $\pm$ 0.3 V

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Input high voltage | $V_{IH}$ | 2.0 | Vcc+0.3 | V | 1, 2 |
| Input low voltage | $V_{IL}$ | − 0.3 | 0.8 | V | 1, 2 |
| Output high voltage ($I_{OUT}$ = − 2.0 mA) | $V_{OH}$ | 2.4 | – | V | |
| Output low voltage ($I_{OUT}$ = 2.0 mA) | $V_{OL}$ | – | 0.4 | V | |
| Input leakage current, any input (0 V < $V_{IN}$ < 3.6 V, all other inputs = 0 V) | $I_{I(L)}$ | − 5 | 5 | µA | |
| Output leakage current (DQ is disabled, 0 V < $V_{OUT}$ < $V_{CC}$) | $I_{O(L)}$ | − 5 | 5 | µA | |

**Note:**
1.   All voltages are referenced to $V_{SS}$.
2.   $V_{IH}$ may overshoot to $V_{CC}$ + 2.0 V for pulse width of < 4ns with 3.3V. $V_{IL}$ may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

**Operating Currents** ($T_A$ = 0 to 70°C, $V_{CC}$ = 3.3V ± 0.3V)
(Recommended Operating Conditions unless otherwise noted)

| Symbol | Parameter & Test Condition | | Max. | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | -7 | -75 | -8PC | -8 | | |
| ICC1 | Operating Current $t_{RC}$ = $t_{RCMIN.}$, $t_{RC}$ = $t_{CKMIN.}$ Active-precharge command cycling, without Burst Operation | 1 bank operation | 150 | 140 | 130 | 130 | mA | 7 |
| ICC2P | Precharge Standby Current in Power Down Mode $\overline{CS}$ =$V_{IH}$, CKE≤ $V_{IL(max)}$ | $t_{CK}$ = min. | 2 | 2 | 2 | 2 | mA | 7 |
| ICC2PS | | $t_{CK}$ = Infinity | 1 | 1 | 1 | 1 | mA | 7 |
| ICC2N | Precharge Standby Current in Non-Power Down Mode $\overline{CS}$ =$V_{IH}$, CKE≥ $V_{IL(max)}$ | $t_{CK}$ = min. | 45 | 40 | 35 | 35 | mA | |
| ICC2NS | | $t_{CK}$ = Infinity | 5 | 5 | 5 | 5 | mA | |
| ICC3 | No Operating Current $t_{CK}$ = min, $\overline{CS}$ = $V_{IH(min)}$ bank ; active state ( 4 banks) | CKE ≥ $V_{IH(MIN.)}$ | 55 | 50 | 45 | 45 | mA | |
| ICC3P | | CKE ≥ $V_{IL(MAX.)}$ (Power down mode) | 8 | 8 | 8 | 8 | mA | |
| ICC4 | Burst Operating Current $t_{CK}$ = min Read/Write command cycling | | 120 | 120 | 110 | 110 | mA | 7,8 |
| ICC5 | Auto Refresh Current $t_{CK}$ = min Auto Refresh command cycling | | 150 | 140 | 130 | 130 | mA | 7 |
| ICC6 | Self Refresh Current Self Refresh Mode, CKE=0.2V | | 1 | 1 | 1 | 1 | mA | |
| | | L-version | 500 | 500 | 500 | 500 | μA | |

**Notes:**

7.  These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of $t_{CK}$ and $t_{RC}$. Input signals are changed one time during $t_{CK}$.
8.  These parameter depend on output loading. Specified values are obtained with output open.

*AC Characteristics* [1,2,3]

$T_A$ = 0 to 70 °C; $V_{SS}$ = 0 V; $V_{DD}$ = 3.3 V ± 0.3 V, $t_T$ = 1 ns

| # | Symbol | Parameter | Limit Values | | | | | | | | Unit | Note |
|---|--------|-----------|------|------|------|------|------|------|------|------|------|------|
| | | | -7 | | -75 | | -8PC | | -8 | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| **Clock and Clock Enable** | | | | | | | | | | | | |
| 1 | $t_{CK}$ | Clock Cycle Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2 | 7 10 | – – | 7.5 10 | – – | 8 10 | – – | 8 12 | – – | s ns ns | |
| 2 | $t_{CK}$ | Clock Frequency $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2 | – – | 143 100 | – – | 133 100 | – – | 125 100 | – – | 125 83 | MHz MHz | |
| 3 | $t_{AC}$ | Access Time from Clock $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2 | – _ | 5.4 5.5 | _ _ | 5.4 6 | _ _ | 6 6 | _ _ | 7 7 | ns ns | 2, 4 |
| 4 | $t_{CH}$ | Clock High Pulse Width | 2.5 | – | 2.5 | – | 3 | – | 3 | – | ns | |
| 5 | $t_{CL}$ | Clock Low Pulse Width | 2.5 | – | 2.5 | – | 3 | – | 3 | – | ns | |
| 6 | $t_T$ | Transition Tim | 0.3 | 1.2 | 0.3 | 1.2 | 0.5 | 10 | 0.5 | 10 | ns | |
| **Setup and Hold Times** | | | | | | | | | | | | |
| 7 | $t_{IS}$ | Input Setup Time | 1.5 | – | 1.5 | – | 2 | – | 2.5 | – | ns | 5 |
| 8 | $t_{IH}$ | Input Hold Time | 0.8 | – | 0.8 | – | 1 | – | 1 | – | ns | 5 |
| 9 | $t_{CKS}$ | CKE Setup Time | 1.5 | – | 1.5 | – | 2 | – | 2.5 | – | ns | 5 |
| 10 | $t_{CKH}$ | CKE Hold Time | 0.8 | – | 0.8 | – | 1 | – | 1 | – | ns | 5 |
| 11 | $t_{RSC}$ | Mode Register Set-up Time | 14 | – | 15 | – | 16 | – | 16 | – | ns | |
| 12 | $t_{SB}$ | Power Down Mode Entry Time | 0 | 7 | 0 | 7.5 | 0 | 8 | 0 | 8 | ns | |
| **Common Parameters** | | | | | | | | | | | | |
| 13 | $t_{RCD}$ | Row to Column Delay Time | 20 | – | 20 | – | 20 | – | 24 | – | ns | 6 |
| 14 | $t_{RP}$ | Row Precharge Time | 20 | – | 20 | – | 20 | – | 24 | – | ns | 6 |
| 15 | $t_{RAS}$ | Row Active Time | 42 | 100K | 45 | 100K | 45 | 100k | 48 | 100k | ns | 6 |
| 16 | $t_{RC}$ | Row Cycle Time | 60 | – | 60 | – | 60 | – | 72 | – | ns | 6 |
| 17 | $t_{RRD}$ | Activate(a) to Activate(b) Command Period | 14 | – | 15 | – | 16 | – | 20 | – | ns | 6 |
| 18 | $t_{CCD}$ | $\overline{\text{CAS}}$(a) to $\overline{\text{CAS}}$(b) Command Period | 1 | – | 1 | – | 1 | – | 1 | – | CLK | |
| **Refresh Cycle** | | | | | | | | | | | | |
| 19 | $t_{REF}$ | Refresh Period (4096 cycles) | — | 64 | — | 64 | — | 64 | — | 64 | ms | |
| 20 | $t_{SREX}$ | Self Refresh Exit Time | 10 | | 10 | | 10 | | 12 | | ns | |

## AC Characteristics (Cont'd)

| # | Symbol | Parameter | -7 Min. | -7 Max. | -75 Min. | -75 Max. | -8PC Min. | -8PC Max. | -8 Min. | -8 Max. | Unit | Note |
|---|--------|-----------|---------|---------|----------|----------|-----------|-----------|---------|---------|------|------|
| **Read Cycle** | | | | | | | | | | | | |
| 21 | $t_{OH}$ | Data Out Hold Time | 2.7 | – | 2.7 | – | 3 | – | 3 | – | ns | 2 |
| 22 | $t_{LZ}$ | Data Out to Low Impedance Time | 1 | – | 1 | – | 0 | – | 0 | – | ns | |
| 23 | $t_{HZ}$ | Data Out to High Impedance Time | – | 5.4 | – | 5.4 | 3 | 8 | 3 | 8 | ns | 7 |
| 24 | $t_{DQZ}$ | DQM Data Out Disable Latency | – | 2 | – | 2 | – | 2 | – | 2 | CLK | |
| **Write Cycle** | | | | | | | | | | | | |
| 25 | $t_{WR}$ | Write Recovery Time | 2 | – | 2 | – | 2 | – | 2 | – | CLK | |
| 26 | $t_{DQW}$ | DQM Write Mask Latency | 0 | – | 0 | – | 0 | – | – | – | CLK | |

### Notes for AC Parameters:

1. For proper power-up see the operation section of this data sheet.

2. AC timing tests have $V_{IL} = 0.8V$ and $V_{IH} = 2.0V$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between $V_{IH}$ and $V_{IL}$. All AC measurements assume $t_T$ = 1ns with the AC output load circuit shown in Figure 1.
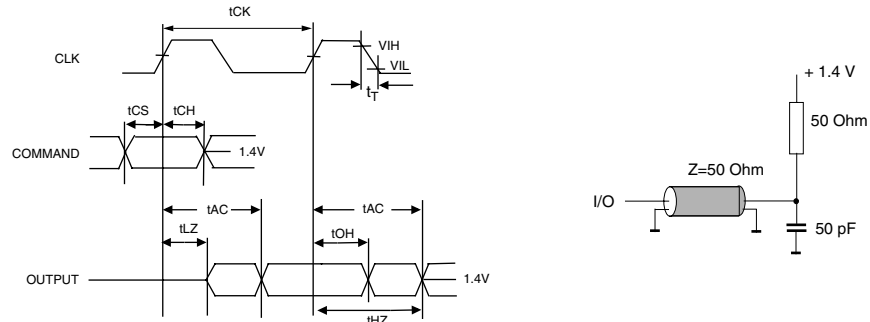


**Figure 1.**

4. If clock rising time is longer than 1 ns, a time $(t_T/2 - 0.5)$ ns has to be added to this parameter.

5. If $t_T$ is longer than 1 ns, a time $(t_T - 1)$ ns has to be added to this parameter.

6. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

   *the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*

   Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.

7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels

*Timing Diagrams*

***Timing Diagrams*** (Cont'd)

16. Random Column Read ( Page within same Bank)

       16.1 $\overline{\text{CAS}}$ Latency = 2

       16.2 $\overline{\text{CAS}}$ Latency = 3

17. Random Column Write ( Page within same Bank)

       17.1 $\overline{\text{CAS}}$ Latency = 2

       17.2 $\overline{\text{CAS}}$ Latency = 3

18. Random Row Read ( Interleaving Banks) with Precharge

       18.1 $\overline{\text{CAS}}$ Latency = 2

       18.2 $\overline{\text{CAS}}$ Latency = 3

19. Random Row Write ( Interleaving Banks) with Precharge

       19.1 $\overline{\text{CAS}}$ Latency = 2

       19.2 $\overline{\text{CAS}}$ Latency = 3

20. Full Page Read Cycle

       20.1 $\overline{\text{CAS}}$ Latency = 2

       20.2 $\overline{\text{CAS}}$ Latency = 3

21. Full Page Write Cycle

       21.1 $\overline{\text{CAS}}$ Latency = 2

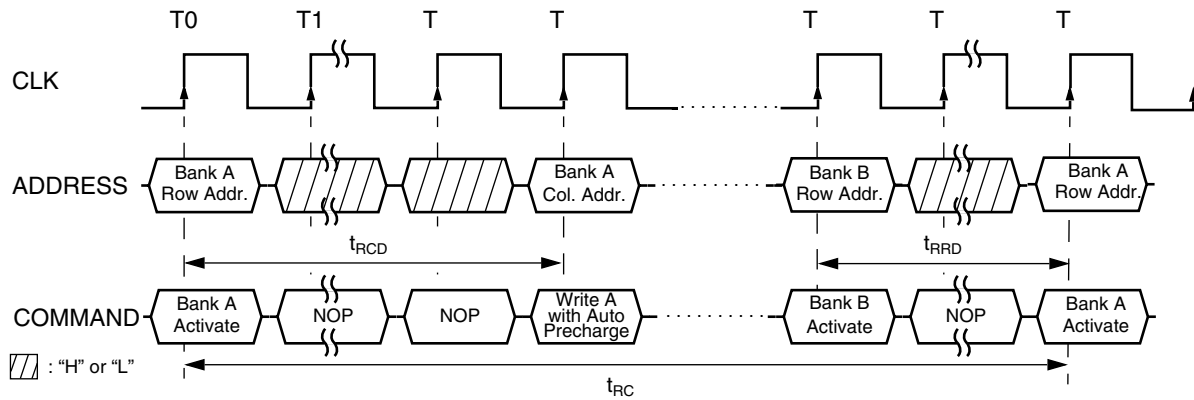       21.2 $\overline{\text{CAS}}$ Latency = 3

22. Precharge Termination of a Burst

       22.1 $\overline{\text{CAS}}$ Latency = 2

       22.2 $\overline{\text{CAS}}$ Latency = 3

## 1. Bank Activate Command Cycle

## ($\overline{CAS}$ latency = 3)



## 2. Burst Read Operation

## (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4)

### 3. Read Interrupted by a Read

**(Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4)**

T0   T1   T2   T3   T4   T5   T6   T7   T8

CLK

COMMAND: READ A | READ B | NOP | NOP | NOP | NOP | NOP | NOP | NOP

$\overline{CAS}$ latency = 2
$t_{CK2}$, I/O's: DOUT A$_0$ | DOUT B$_0$ | DOUT B$_1$ | DOUT B$_2$ | DOUT B$_3$

$\overline{CAS}$ latency = 3
$t_{CK3}$, I/O's: DOUT A$_0$ | DOUT B$_0$ | DOUT B$_1$ | DOUT B$_2$ | DOUT B$_3$

$\overline{CAS}$ latency = 4
$t_{CK4}$, I/O's: DOUT A$_0$ | DOUT B$_0$ | DOUT B$_1$ | DOUT B$_2$ | DOUT B$_3$

### 4.1 Read to Write Interval

**(Burst Length = 4, $\overline{CAS}$ latency = 3)**

T0   T1   T2   T3   T4   T5   T6   T7   T8

CLK

DQM

Minimum delay between the Read and Write Commands = 4+1 = 5 cycles

$t_{DQW}$

$t_{DQZ}$

COMMAND: NOP | READ A | NOP | NOP | NOP | NOP | WRITE B | NOP | NOP

I/O's: DOUT A$_0$ | DIN B$_0$ | DIN B$_1$ | DIN B$_2$

Must be Hi-Z before
the Write Command

: "H" or "L"

### 4.2 Minimum Read to Write Interval

### (Burst Length = 4, $\overline{CAS}$ latency = 2)

|  | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 |
|---|---|---|---|---|---|---|---|---|---|

CLK

DQM — $t_{DQZ}$ — $t_{DQW}$ — 1 Clk Interval

COMMAND: NOP, NOP, BANK A ACTIVATE, NOP, READ A, WRITE A, NOP, NOP, NOP

Must be Hi-Z before the Write Command

$\overline{CAS}$ latency = 2
$t_{CK2}$, I/O's: DIN A$_0$, DIN A$_1$, DIN A$_2$, DIN A$_3$

⬚ : "H" or "L"

### 4.3 Non-Minimum Read to Write Interval

### (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4

|  | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 |
|---|---|---|---|---|---|---|---|---|---|

CLK

DQM — $t_{DQZ}$ — $t_{DQW}$

COMMAND: NOP, READ A, NOP, NOP, READ A, NOP, WRITE B, NOP, NOP

$\overline{CAS}$ latency = 2
$t_{CK1}$, I/O's: DOUT A$_0$, DOUT A$_1$, DIN B$_0$, DIN B$_1$, - DIN B$_2$

Must be Hi-Z before the Write Command

$\overline{CAS}$ latency = 3
$t_{CK2}$, I/O's: DOUT A$_0$, DIN B$_0$, DIN B$_1$, - DIN B$_2$

$\overline{CAS}$ latency = 4
$t_{CK3}$, I/O's: DIN B$_0$, DIN B$_1$, DIN B$_2$

⬚ : "H" or "L"

## 5. Burst Write Operation

### (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, or 4)

|  | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 |

CLK

COMMAND: NOP — WRITE A — NOP — NOP — NOP — NOP — NOP — NOP — NOP

I/O's: DIN $A_0$ — DIN $A_1$ — DIN $A_2$ — DIN $A_3$ — don't care

The first data element and the Write are registered on the same clock edge.

Extra data is ignored after termination of a Burst.
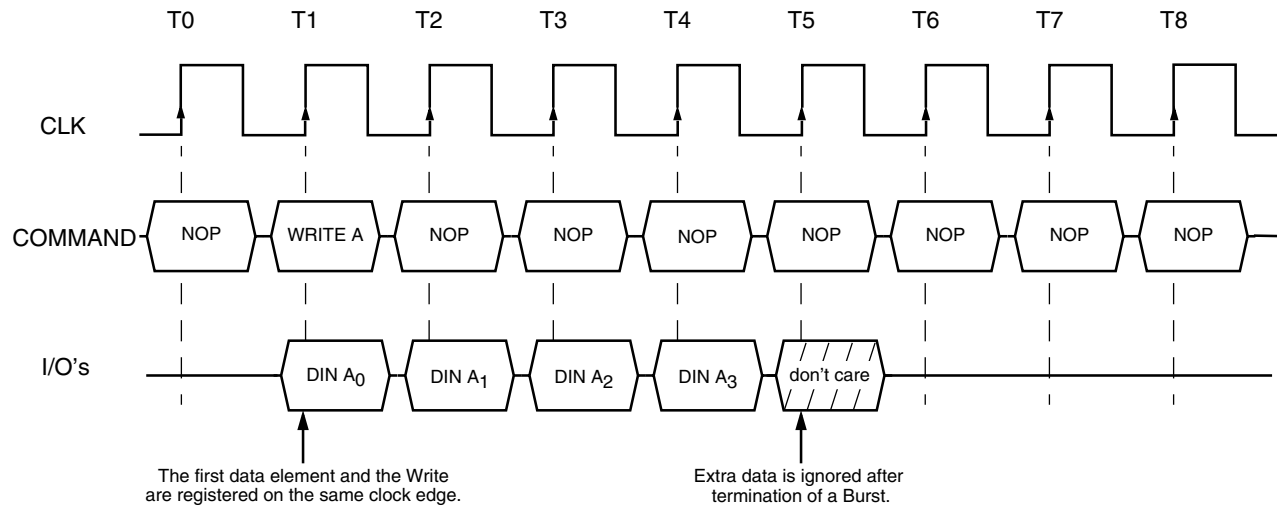
## 6.1 Write Interrupted by a Write

### (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, or 4)

|  | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 |

CLK

COMMAND: NOP — WRITE A — WRITE B — NOP — NOP — NOP — NOP — NOP — NOP

1 Clk Interval

I/O's: DIN $A_0$ — DIN $B_0$ — DIN $B_1$ — DIN $B_2$ — DIN $B_3$

## 6.2 Write Interrupted by a Read

### (Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4)



Input data for the Write is ignored.

Input data must be removed from the I/O's at least one clock cycle before the Read dataAPpears on the outputs to avoid data contention.
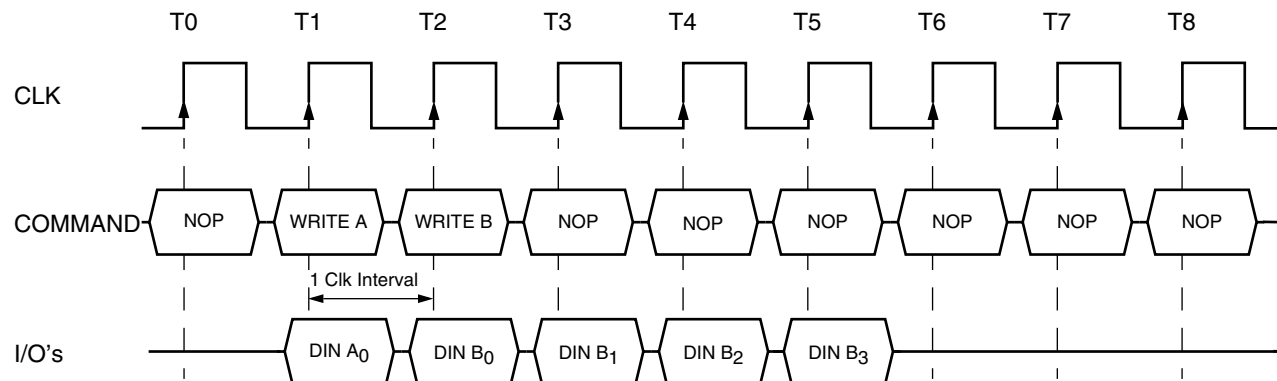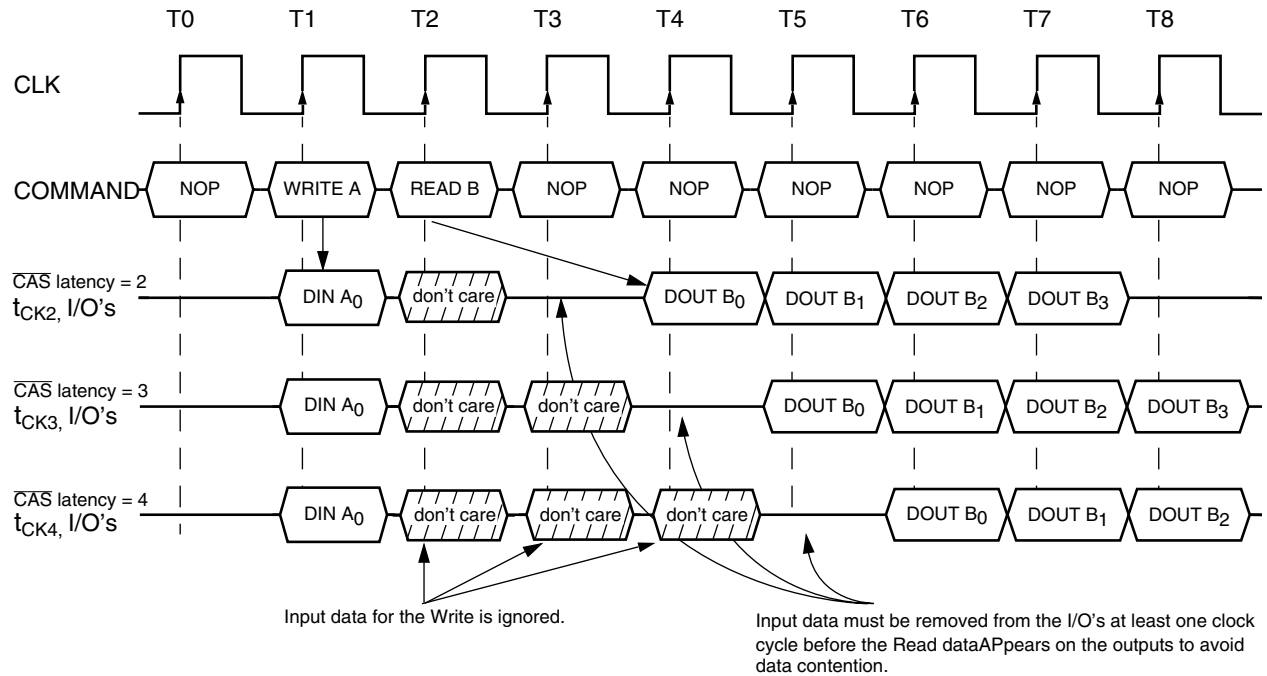
## 7. Burst Write with Auto-Precharge

### Burst Length = 2, $\overline{CAS}$ latency = 2, 3, 4)



★ Begin Autoprecharge

Bank can be reactivated after trp
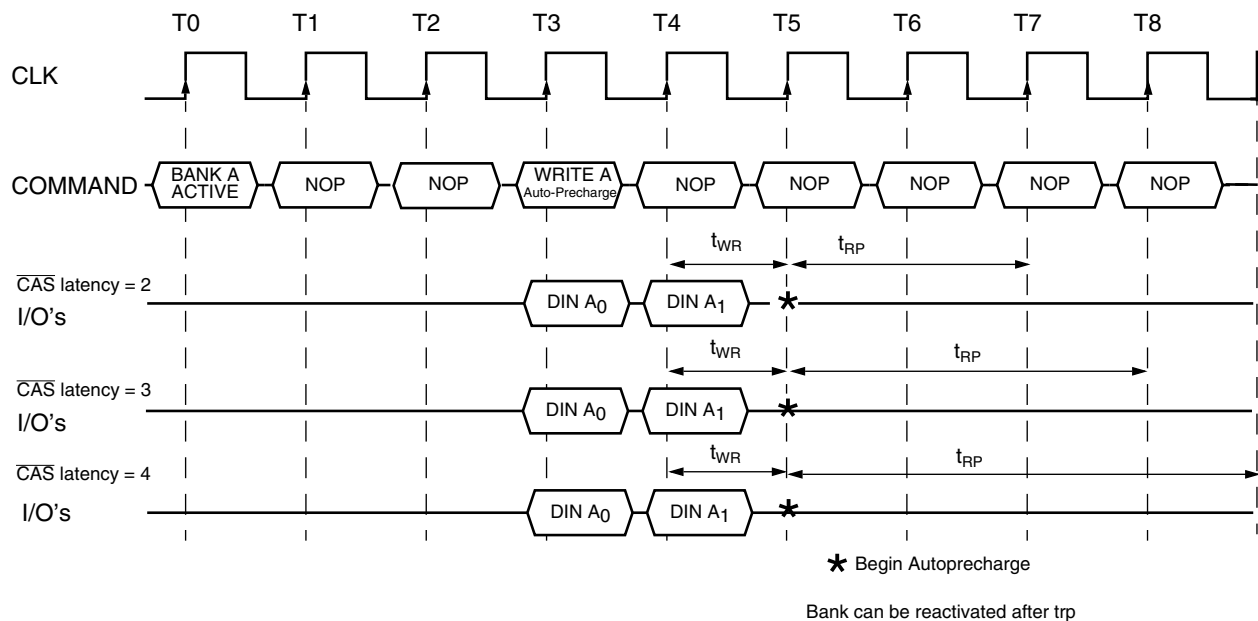
### 7.2 Burst Read with Auto-Precharge

### Burst Length = 4, $\overline{CAS}$ latency = 2, 3, 4)



★ Begin Autoprecharge

Bank can be reactivated after $t_{RP}$
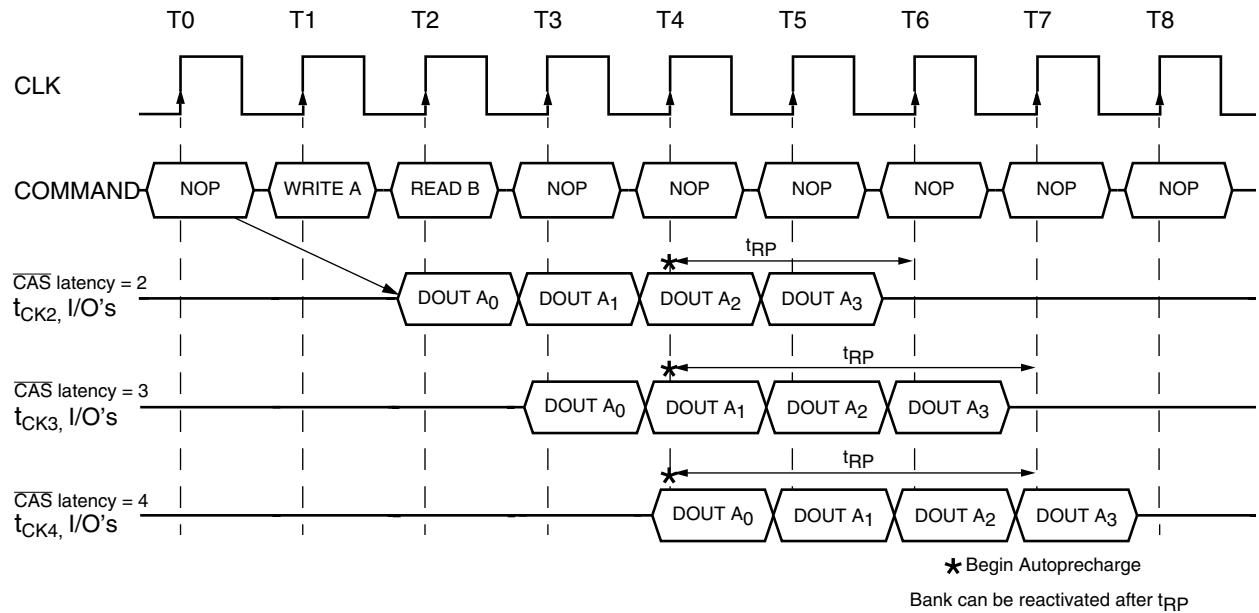
## 8.1 Termination of a Full Page Burst Read Operation

### ($\overline{CAS}$ latency = 2, 3, 4)



The burst ends after a delay equal to the $\overline{CAS}$ latency.
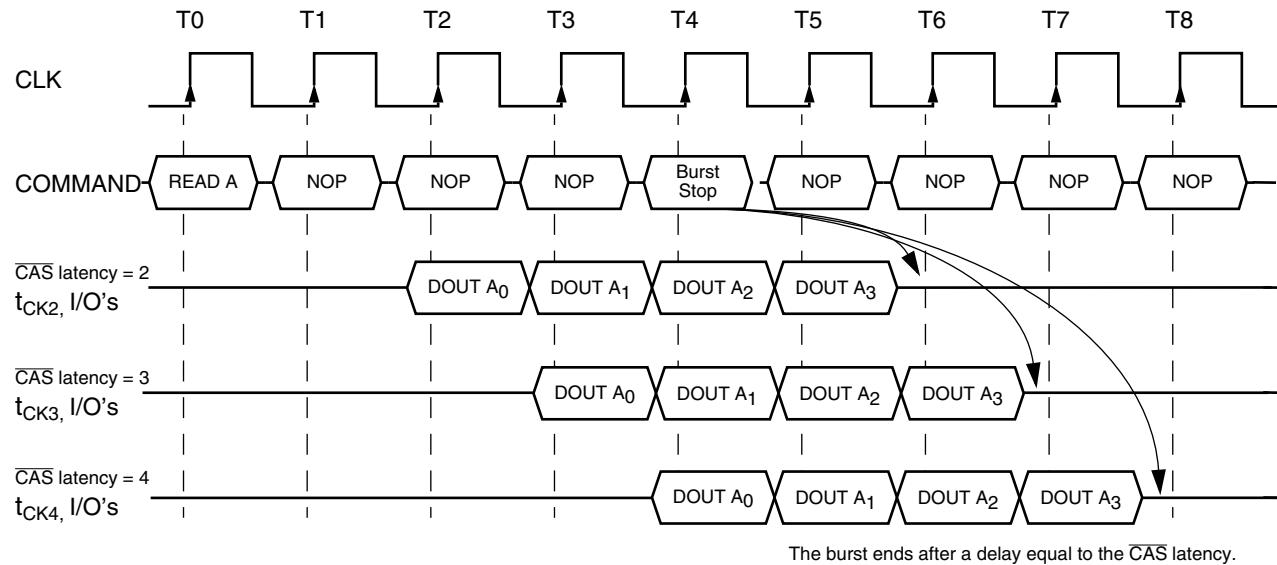
## 8.2 Termination of a Full Page Burst Write Operation

### ($\overline{CAS}$ latency = 2, 3, 4)



Input data for the Write is masked.

## 9.1 AC Parameters for Write Timing
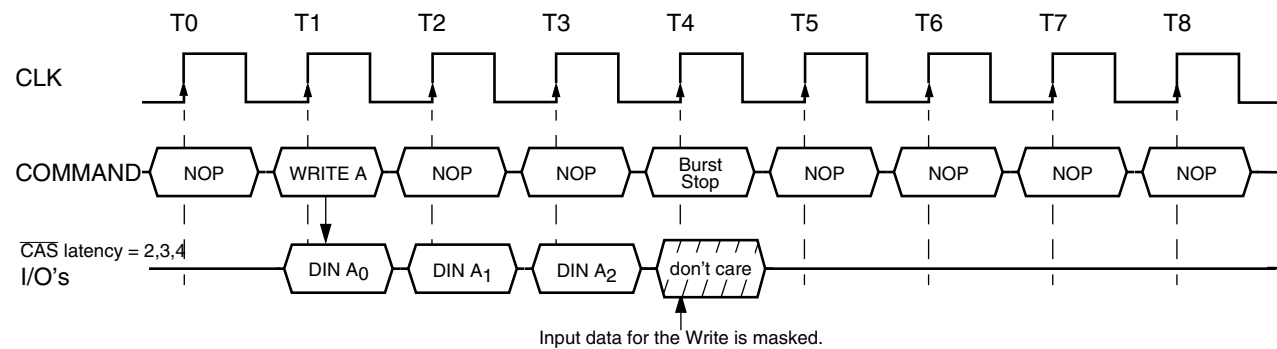
Burst Length = 4, $\overline{CAS}$ Latency = 2
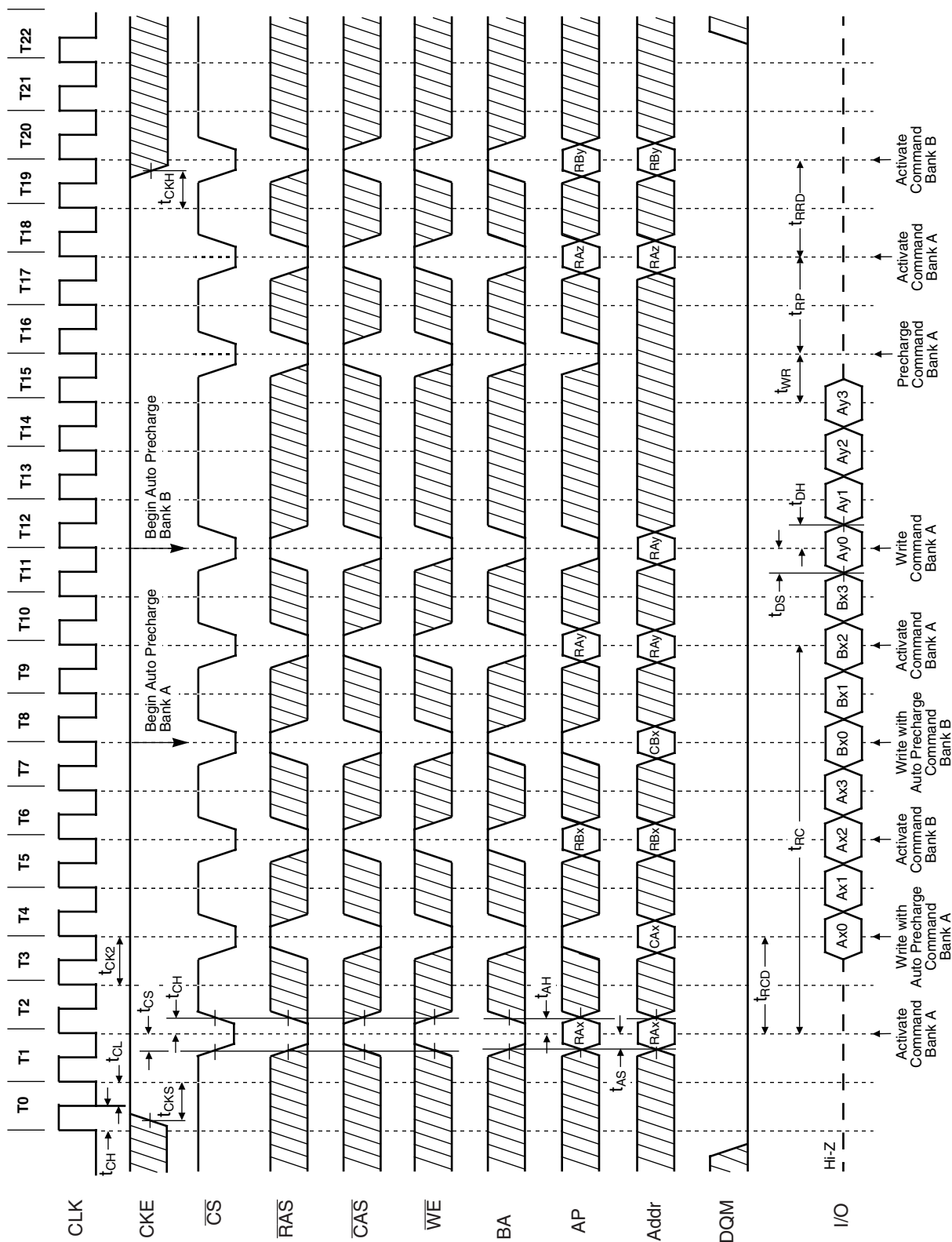
## 9.2 AC Parameters for Read Timing

Burst Length = 2, $\overline{CAS}$ Latency = 2

CLK　CKE　$\overline{CS}$　$\overline{RAS}$　$\overline{CAS}$　$\overline{WE}$　BA　AP　Addr　DQM　I/O

T0　T1　T2　T3　T4　T5　T6　T7　T8　T9　T10　T11　T12　T13

$t_{CL}$　$t_{CH}$　$t_{CKS}$　$t_{CK2}$　$t_{CS}$　$t_{CH}$　$t_{AS}$　$t_{AH}$　$t_{CKH}$

Begin Auto Precharge Bank B

RAx　RAx　RBx　RBx　CAx　RBx　RAy　RAy　Bx0　Bx1

Hi-Z　Ax0　Ax1

$t_{LZ}$　$t_{AC2}$　$t_{OH}$　$t_{AC2}$　$t_{HZ}$　$t_{HZ}$

$t_{RCD}$　$t_{RRD}$　$t_{RAS}$　$t_{RC}$　$t_{RP}$

Activate Command Bank A
Read Command Bank A
Activate Command Bank B
Read with Auto Precharge Command Bank B
Precharge Command Bank A
Activate Command Bank A

## 10. Mode Register Set
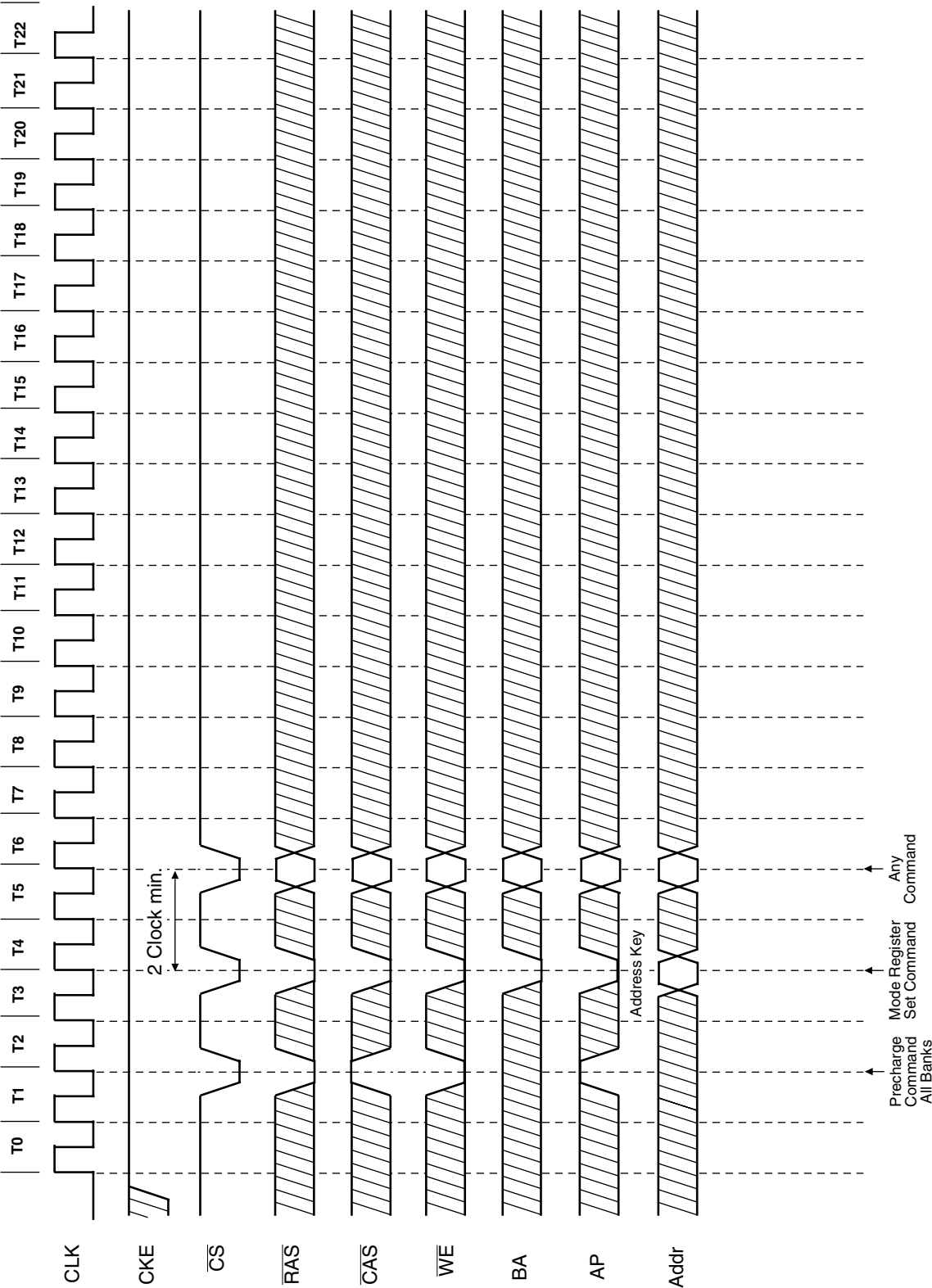
## 11. Power on Sequence and Auto Refresh (CBR)

CLK

CKE — High level is required

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

$\overline{WE}$

BA

AP

Addr

DQM

I/O — Hi-Z

T0

2 Clock min.

Minimum of 2 Refresh Cycles are required

Address Key

Inputs must be stable for 200µs

Precharge Command All Banks

$t_{RP}$

1st Auto Refresh Command

2nd Auto Refresh Command

$t_{RC}$

Mode Register Set Command

Any Command
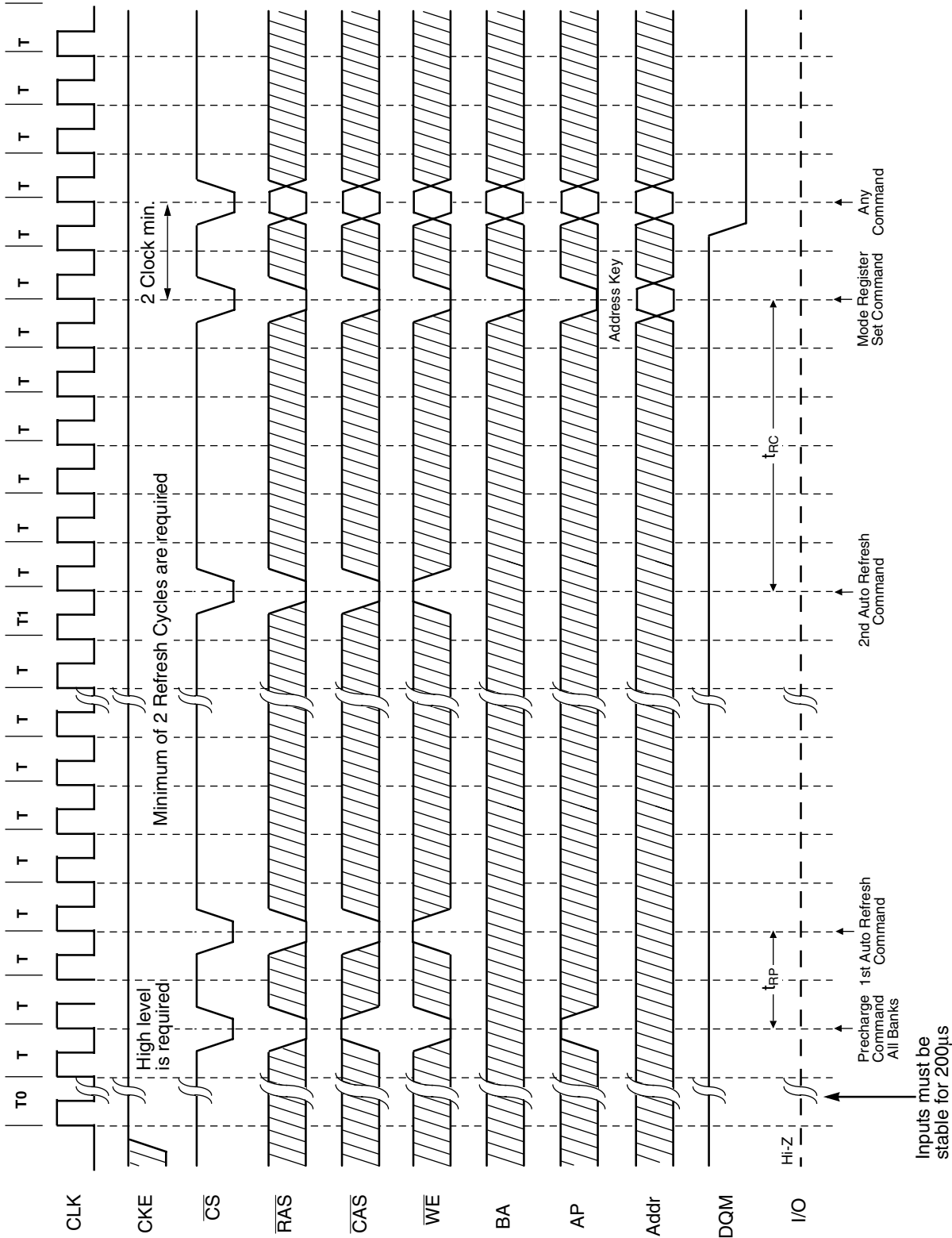
## 12.1 Clock Suspension During Burst Read (Using CKE) (1 of 3)

Burst Length = 4, $\overline{CAS}$ Latency = 1
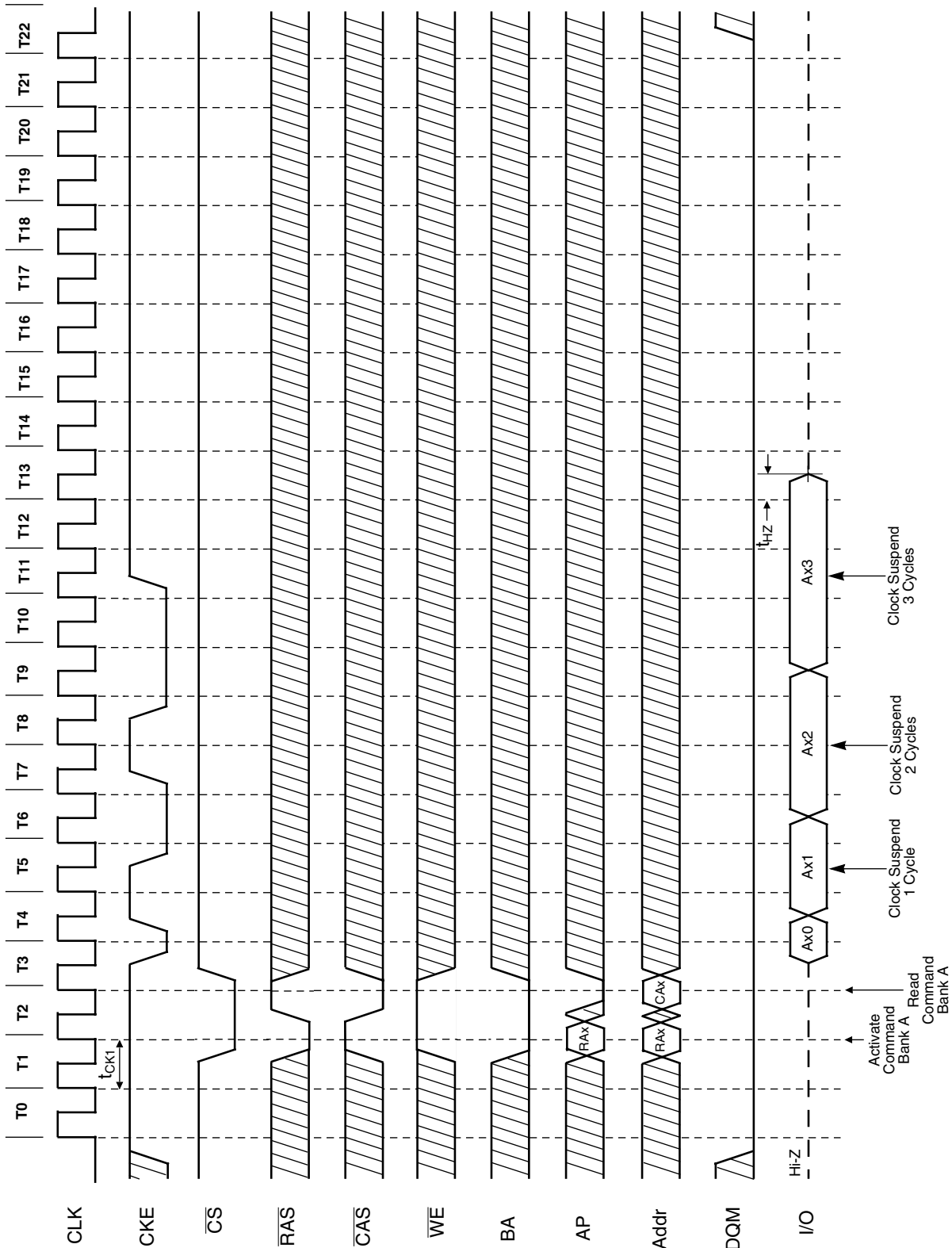
## 12.2 Clock Suspension During Burst Read (Using CKE) (2 of 3)

Burst Length = 4, CAS Latency = 2

## 12.3 Clock Suspension During Burst Read (Using CKE) (3 of 3)
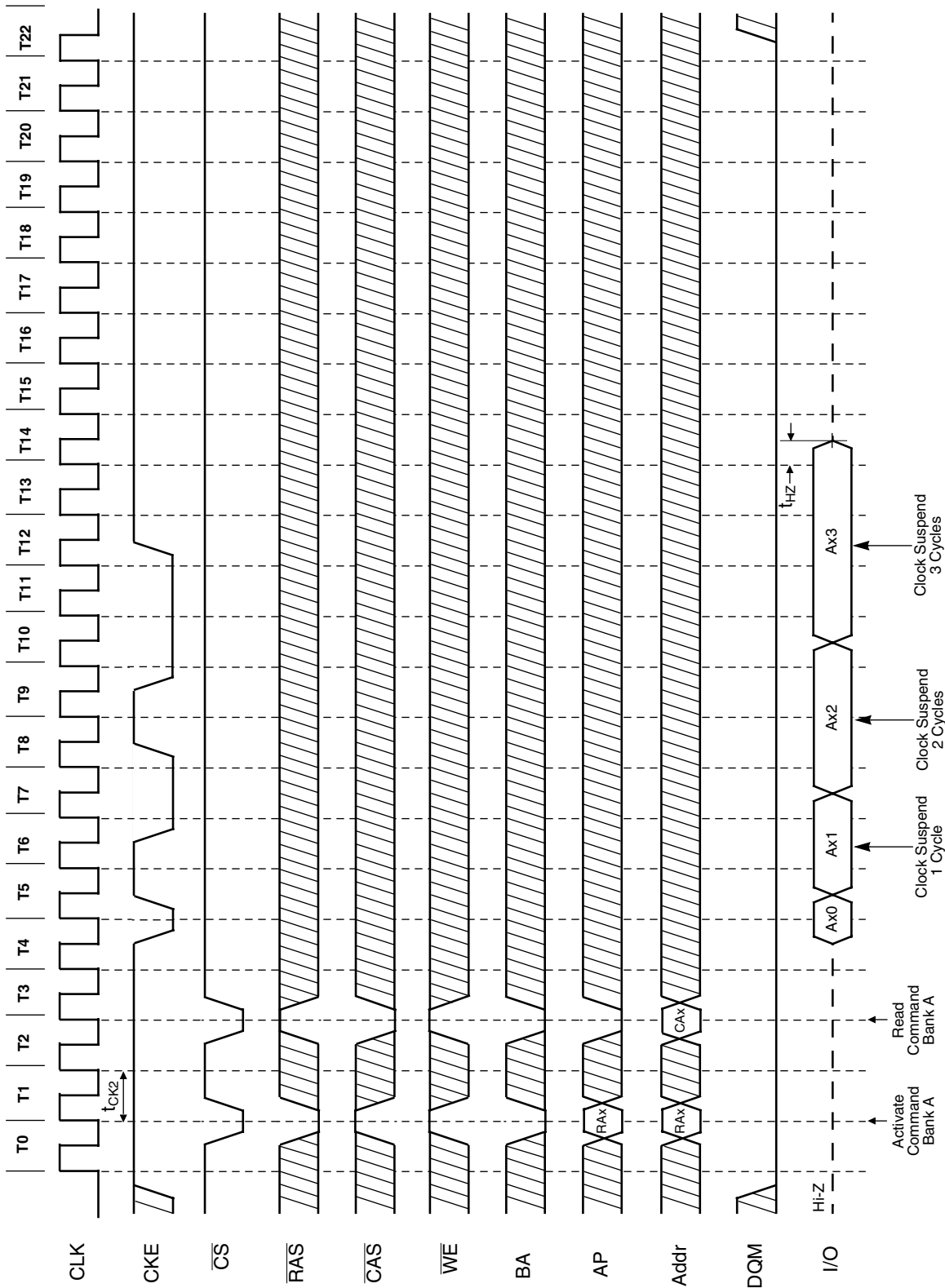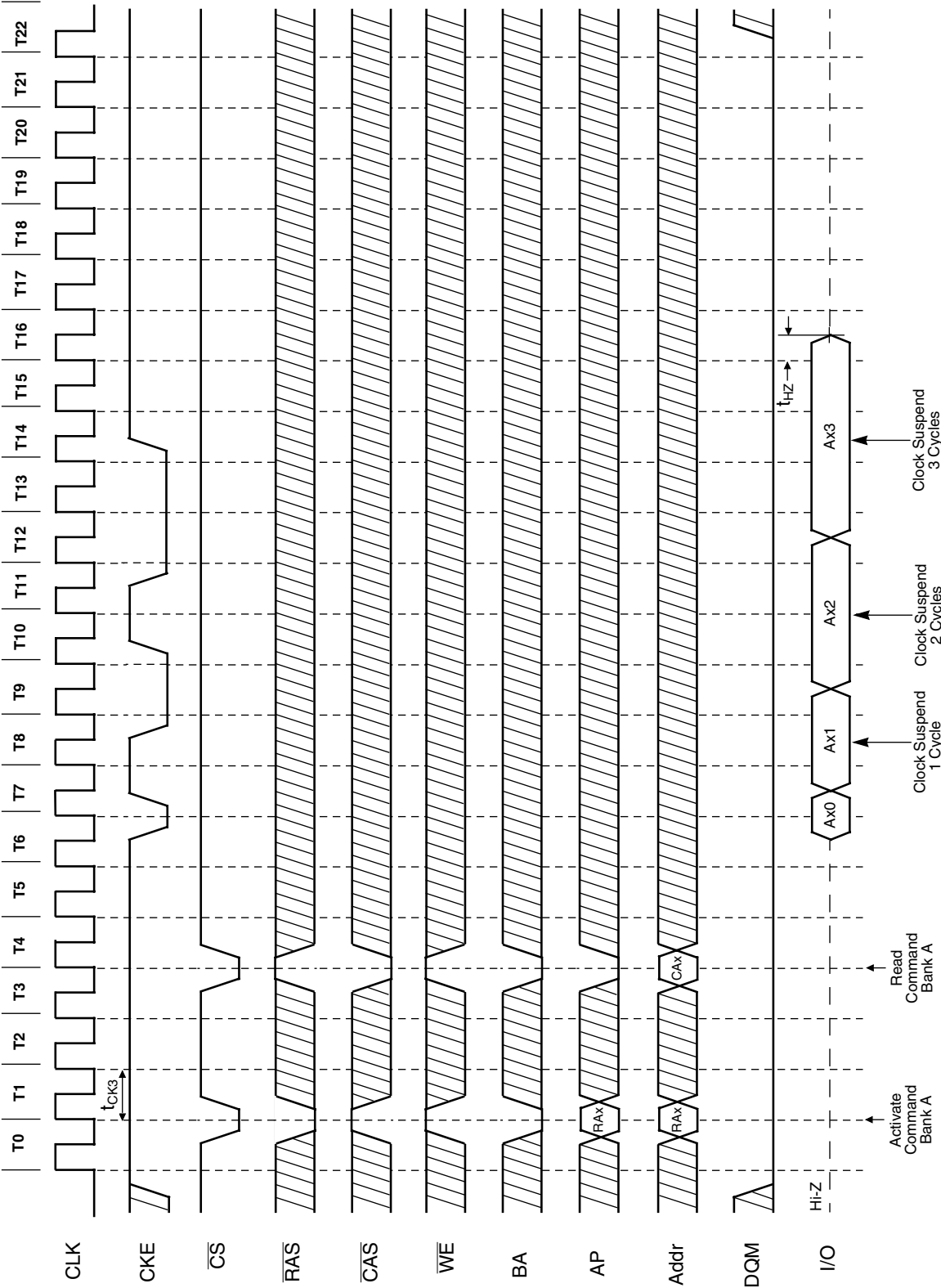
Burst Length = 4, $\overline{CAS}$ Latency = 3

## 12.4 Clip Suspension During Burst Write (Using CKE) (1 of 3)
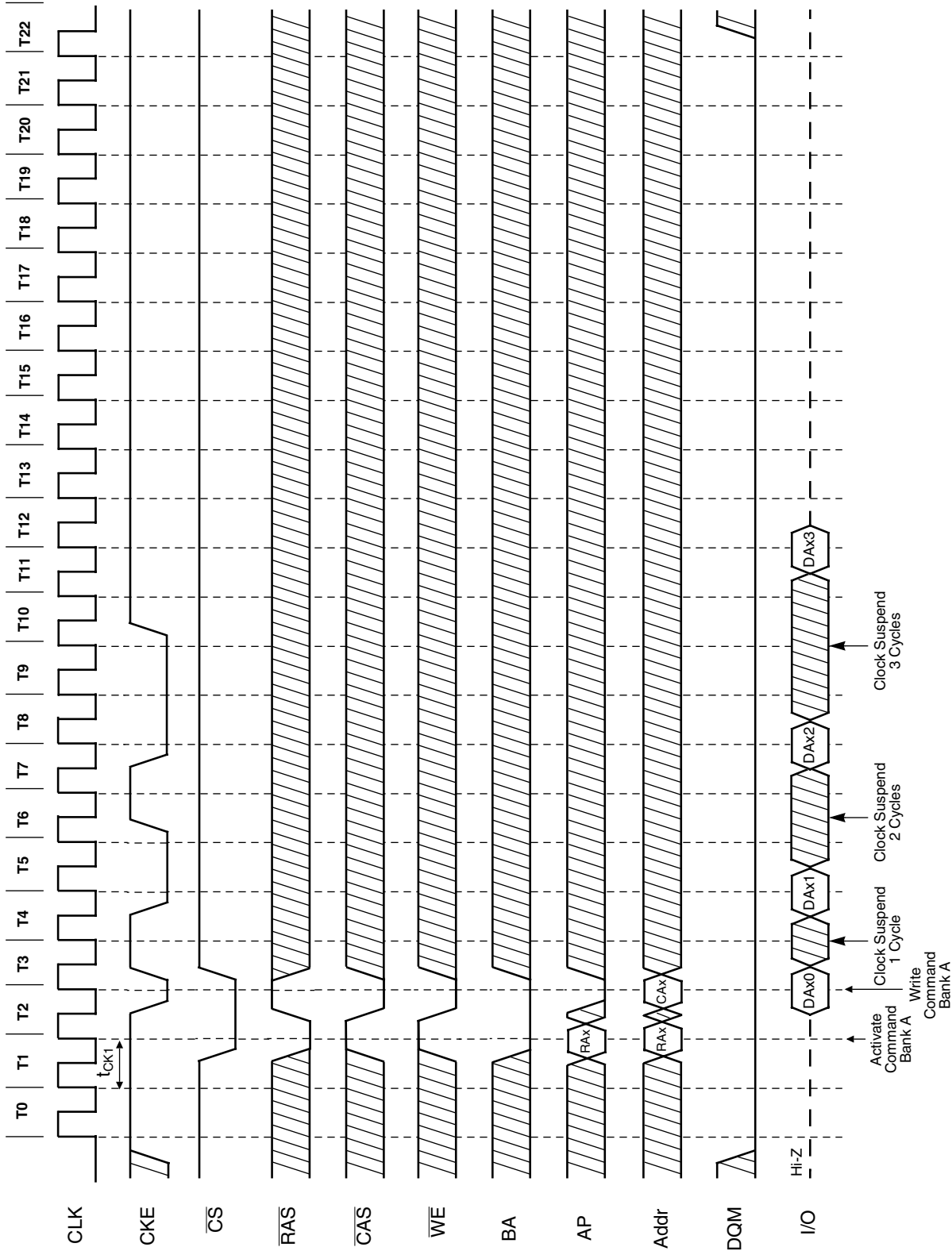
Burst Length = 4, $\overline{CAS}$ Latency = 1

## 13. Power Down Mode and Clock Suspend

Burst Length = 4, $\overline{CAS}$ Latency = 2
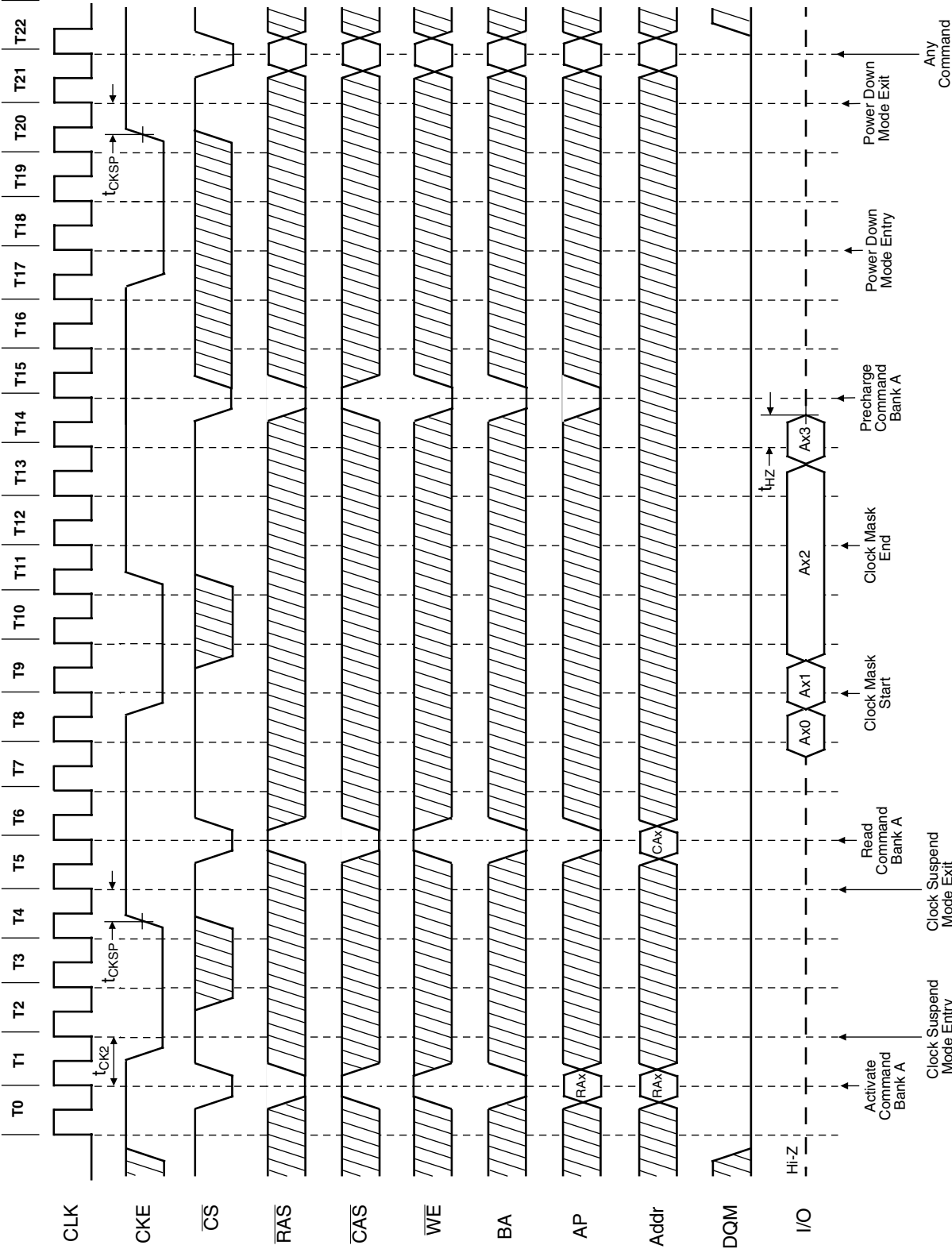
## 14. Self Refresh (Entry and Exit)
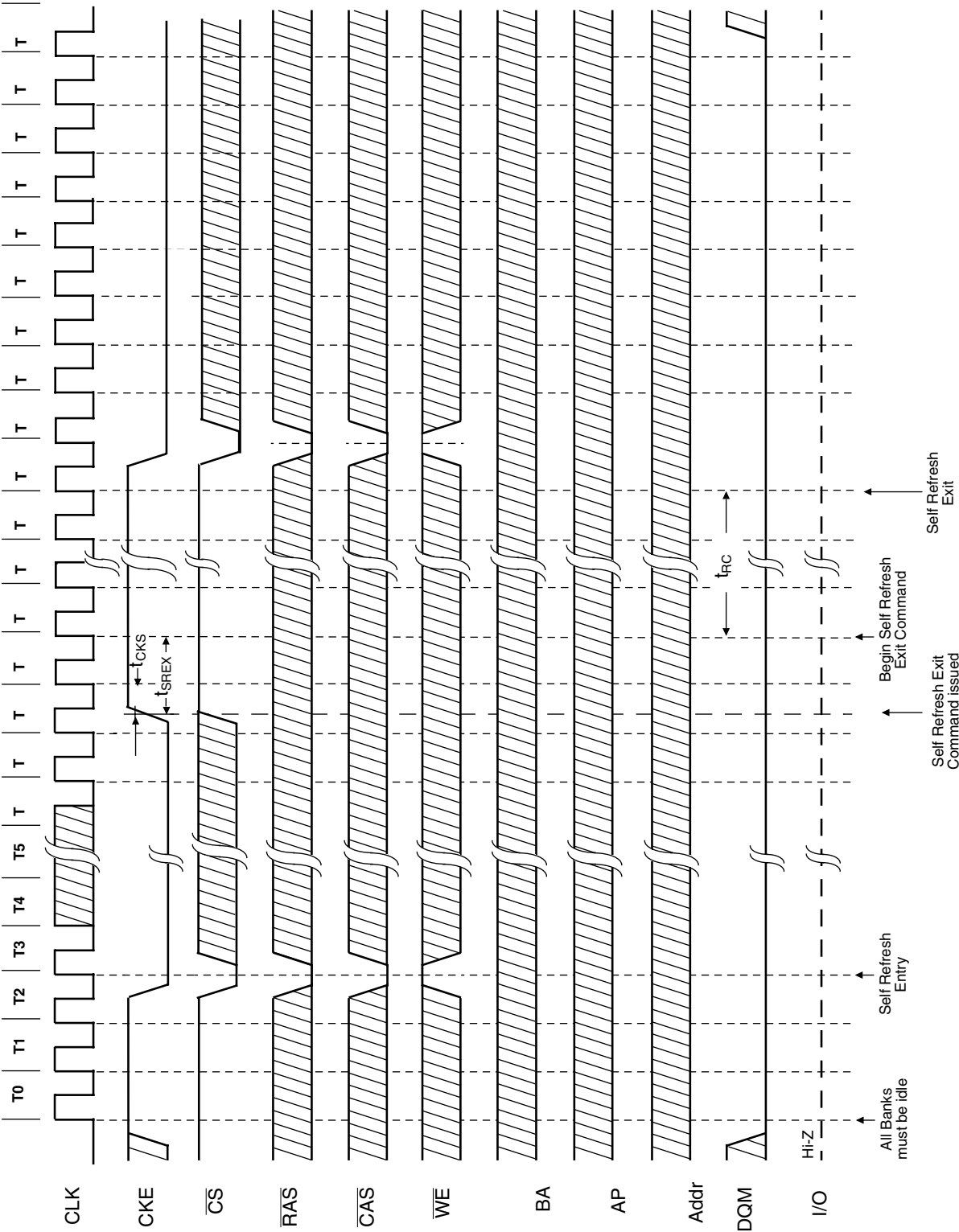
## 15. Auto Refresh (CBR)

Burst Length = 4, $\overline{CAS}$ Latency = 2

## 16.1 Random Column Read (Page within same Bank) (1 of 2)
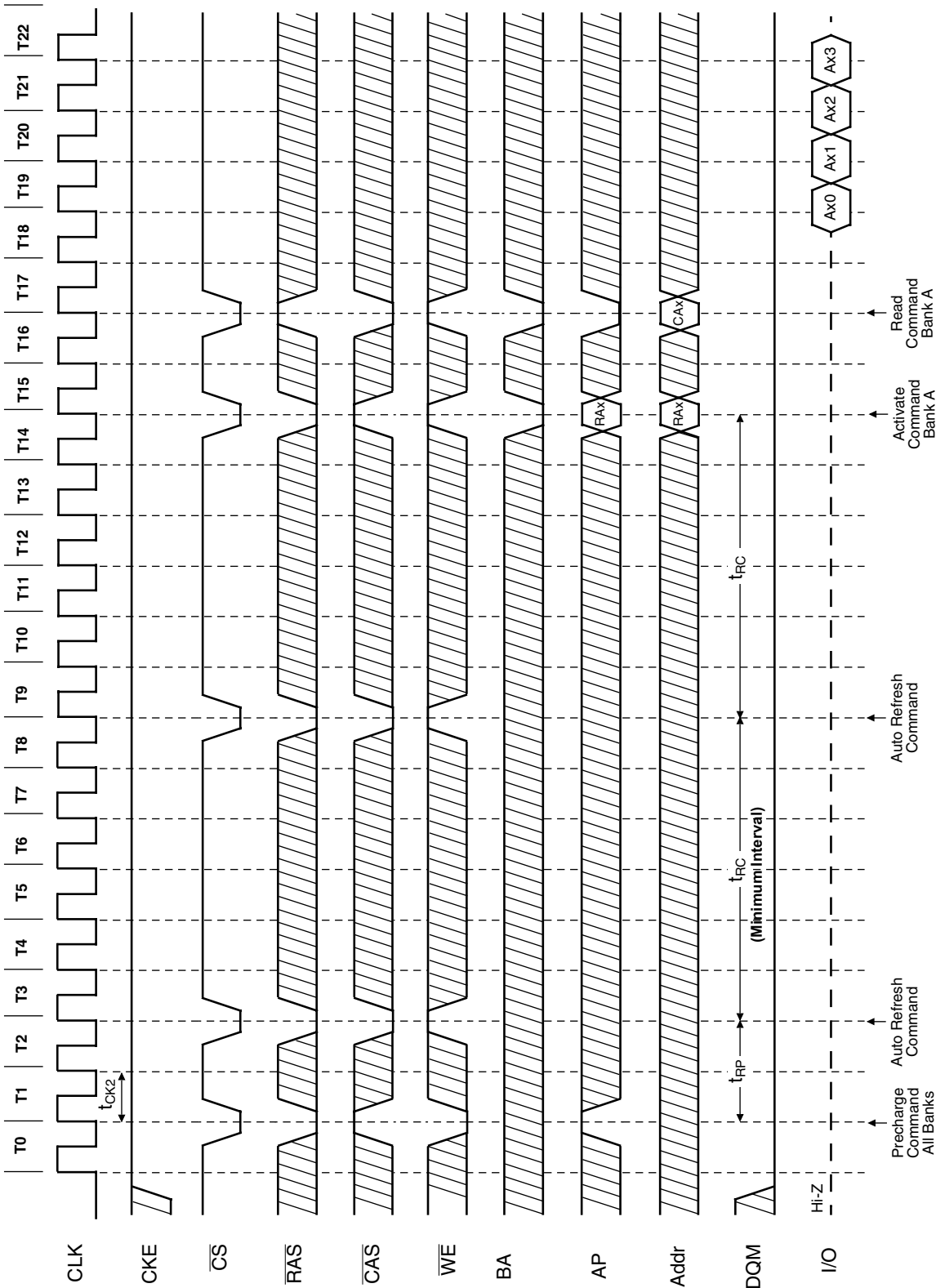
Burst Length = 4, $\overline{CAS}$ Latency = 2

## 16.2 Random Column Read (Page within same Bank) (2 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 3

## 17.1 Random Column Write (Page within same Bank) (1 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 2

CLK

CKE

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

$\overline{WE}$

BA

AP

Addr

DQM

I/O

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22

$t_{CK2}$

RBz, CBz, CBx, CBy, RBz, CBz

RBz, RBz

Hi-Z

DBw0 DBw1 DBw2 DBw3 DBx0 DBx1 DBy0 DBy1 DBy2 DBy3 DBz0 DBz1 DBz2 DBz3

Activate Command Bank B
Write Command Bank B
Write Command Bank B
Write Command Bank B
Write Command Bank B
Precharge Command Bank B
Activate Command Bank B
Write Command Bank B

## 17.2 Random Column Write (Page within same Bank) (2 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 3

Signals: CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA, AP, Addr, DQM, I/O

Time points: T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22

$t_{CK3}$

Activate Command Bank B

Write Command Bank B

Write Command Bank B

Write Command Bank B

Precharge Command Bank B

Activate Command Bank B

Write Command Bank B

Addr: RBz, CBz, CBx, CBy, RBz, CBz

I/O: Hi-Z, DBw0, DBw1, DBw2, DBw3, DBx0, DBx1, DBy0, DBy1, DBy2, DBy3, DBz0, DBz1

**18.1 Random Row Read (Interleaving Banks) (1 of 2)**

Burst Length = 8, $\overline{CAS}$ Latency = 2

CLK
CKE — High
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
A11(BS)
A10
A0 – A9
DQM — Hi-Z
I/O

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22

$t_{CK2}$

RBx RBx CBx RAx RAx CAx RBy RBy CBy Ax7

Bx0 Bx1 Bx2 Bx3 Bx4 Bx5 Bx6 Bx7 Ax0 Ax1 Ax2 Ax3 Ax4 Ax5 Ax6 Ax7 By0 By1

$t_{RCD}$ $t_{AC2}$ $t_{RP}$

Activate Command Bank B
Read Command Bank B
Activate Command Bank A
Read Command Bank A
Precharge Command Bank B
Activate Command Bank B
Read Command Bank B

*18. 2 Random Row Read (Interleaving Banks) (2 of 2)*

Burst Length = 8, $\overline{CAS}$ Latency = 3

| | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 | T8 | T9 | T10 | T11 | T12 | T13 | T14 | T15 | T16 | T17 | T18 | T19 | T20 | T21 | T22 |

CLK

CKE   High

$\overline{CS}$

$\overline{RAS}$

$\overline{CAS}$

$\overline{WE}$

A11(BS)

A10   RBx   RBy   RBy

A0 - A9   RBx   CBx   RAx   CAx   RBy   CBy

DQM

I/O   Hi-Z   Bx0   Bx1   Bx2   Bx3   Bx4   Bx5   Bx6   Bx7   Ax0   Ax1   Ax2   Ax3   Ax4   Ax5   Ax6   Ax7   By0

$t_{CK3}$   $t_{RCD}$   $t_{AC3}$   $t_{RP}$

Activate Command Bank B

Read Command Bank B

Activate Command Bank A

Read Command Bank A

Precharge Command Bank B

Activate Command Bank B

Read Command Bank B

Precharge Command Bank A

## 19.1 Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 2

| Signal | Waveform |
|---|---|
| CLK | |
| CKE | High |
| $\overline{CS}$ | |
| $\overline{RAS}$ | |
| $\overline{CAS}$ | |
| $\overline{WE}$ | |
| A11(BS) | |
| A10 | RAx, RBx, RAy, CAy |
| A0 - A9 | RAx, CAX, RBx, CBx, RAy, CAy |
| DQM | Hi-Z |
| I/O | DAx0 DAx1 DAx2 DAx3 DAx4 DAx5 DAx6 DAx7 DBx0 DBx1 DBx2 DBx3 DBx4 DBx5 DBx6 DBx7 DAy0 DAy1 DAy2 DAy3 DAy4 |

Timing clock labels: T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22

Timing parameters: $t_{CK2}$, $t_{RCD}$, $t_{DPL}$, $t_{RP}$

Command annotations:
- Activate Command Bank A
- Write Command Bank A
- Activate Command Bank B
- Write Command Bank B
- Precharge Command Bank A
- Activate Command Bank A
- Write Command Bank A
- Precharge Command Bank B

## 19.2 Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3

## 20.1 Full Page Read Cycle (1 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 2



The burst counter wraps from the highest order page address back to zero during this time interval.

Full Page burst operation does not terminate when the burst length is satisfied; the burst counter increments and continues bursting beginning with the starting address.

## 20.2 Full Page Read Cycle (2 of 2)

Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3



Full Page burst operation does not terminate when the length is satisfied; the burst counter increments and continues bursting beginning with the starting address.

The burst counter wraps from the highest order page address back to zero during this time interval.

## 21.1 Full Page Write Cycle (1 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 2
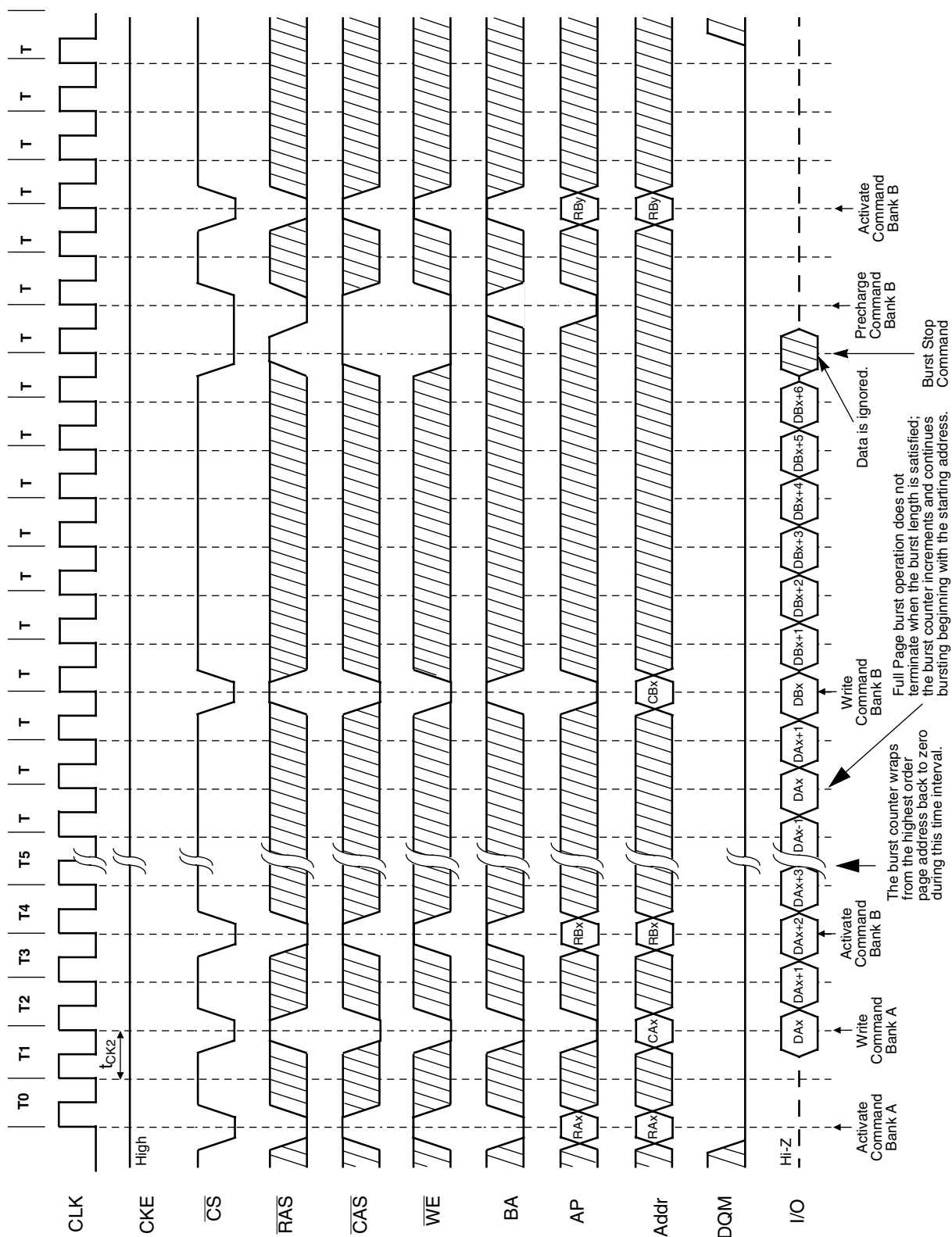
## 21.2 Full Page Write Cycle (2 of 2)

Burst Length = Full Page, $\overline{CAS}$ Latency = 3

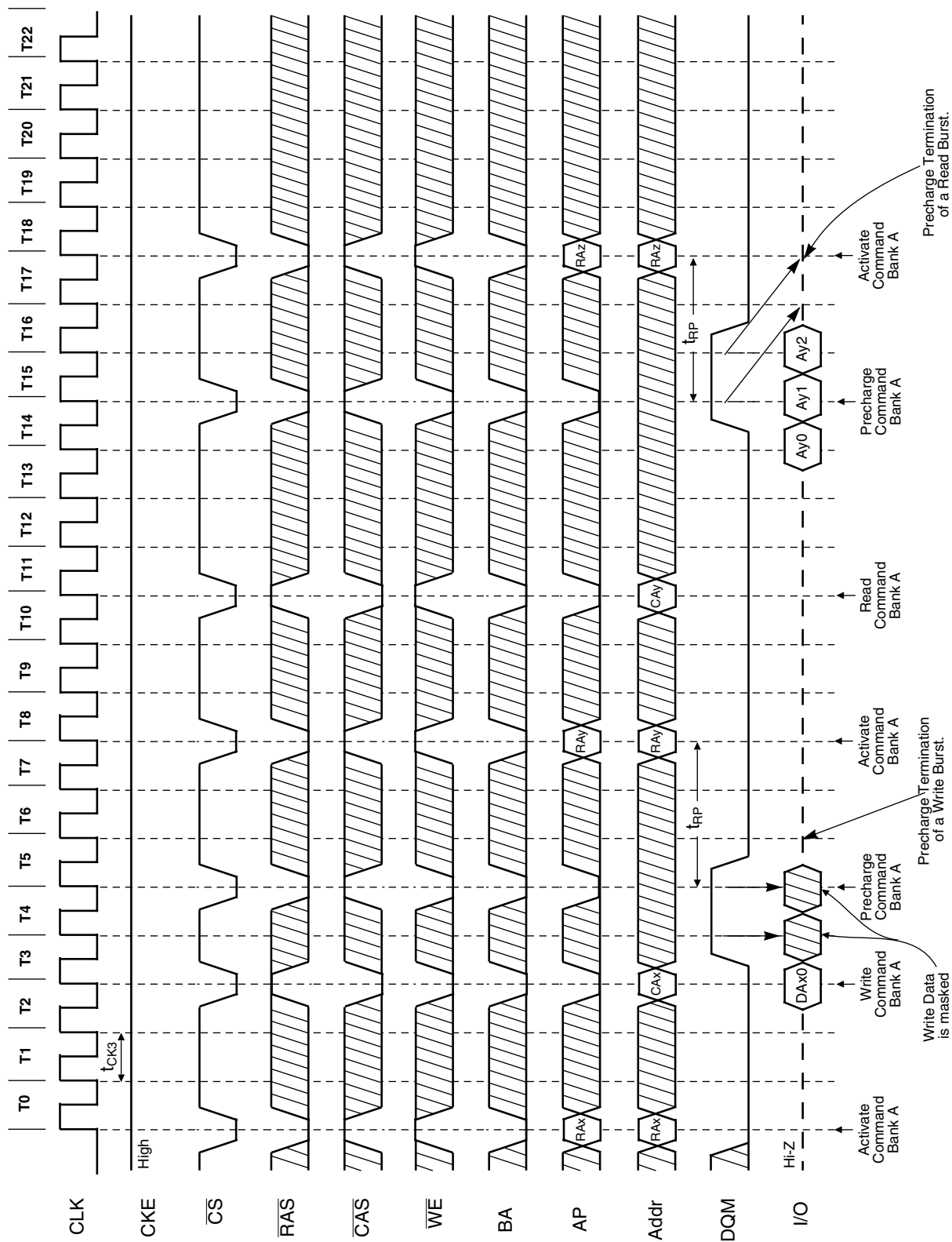## 22.1 Precharge Termination of a Burst (1 of 2)

Burst Length = 8 or Full Page, $\overline{CAS}$ Latency = 2
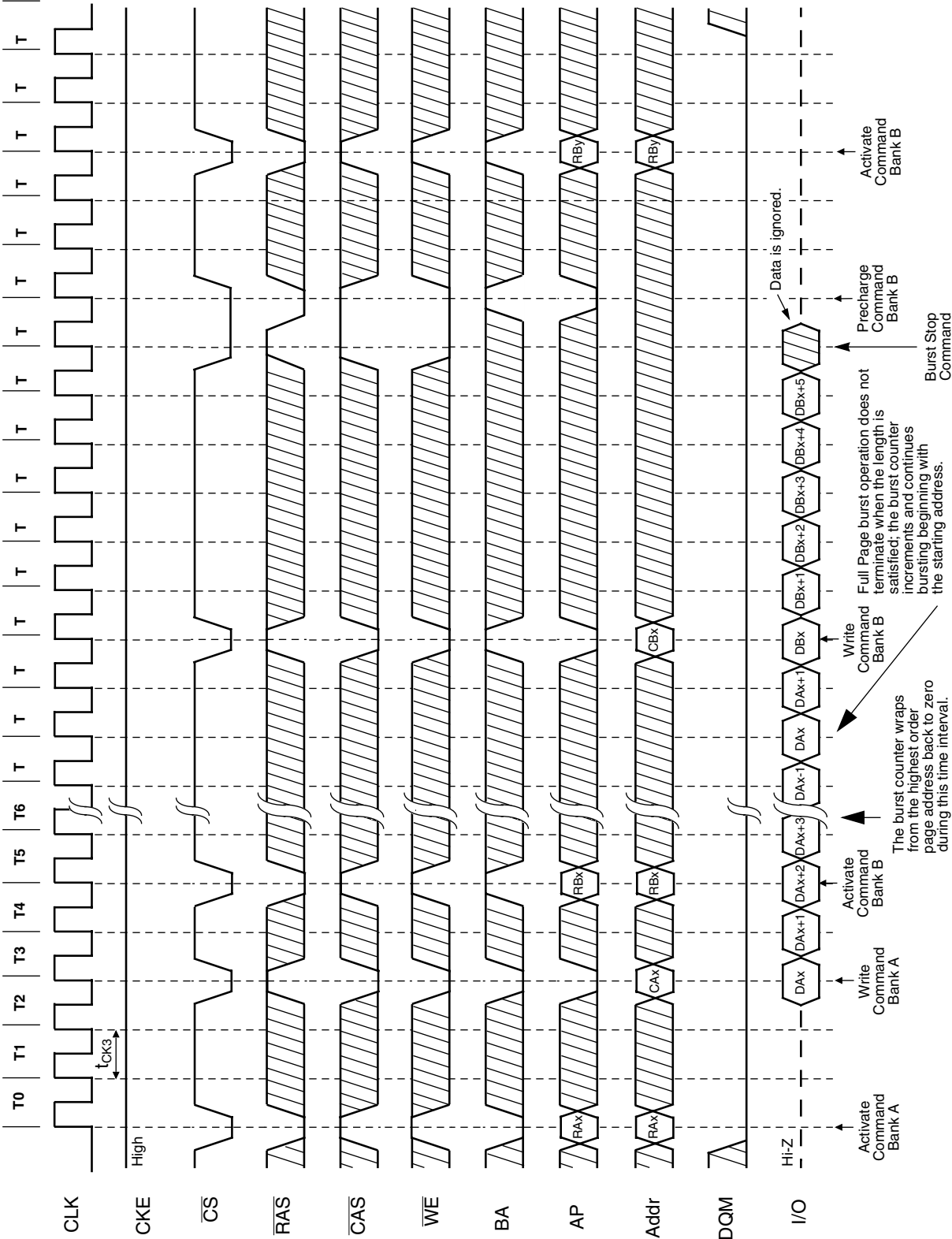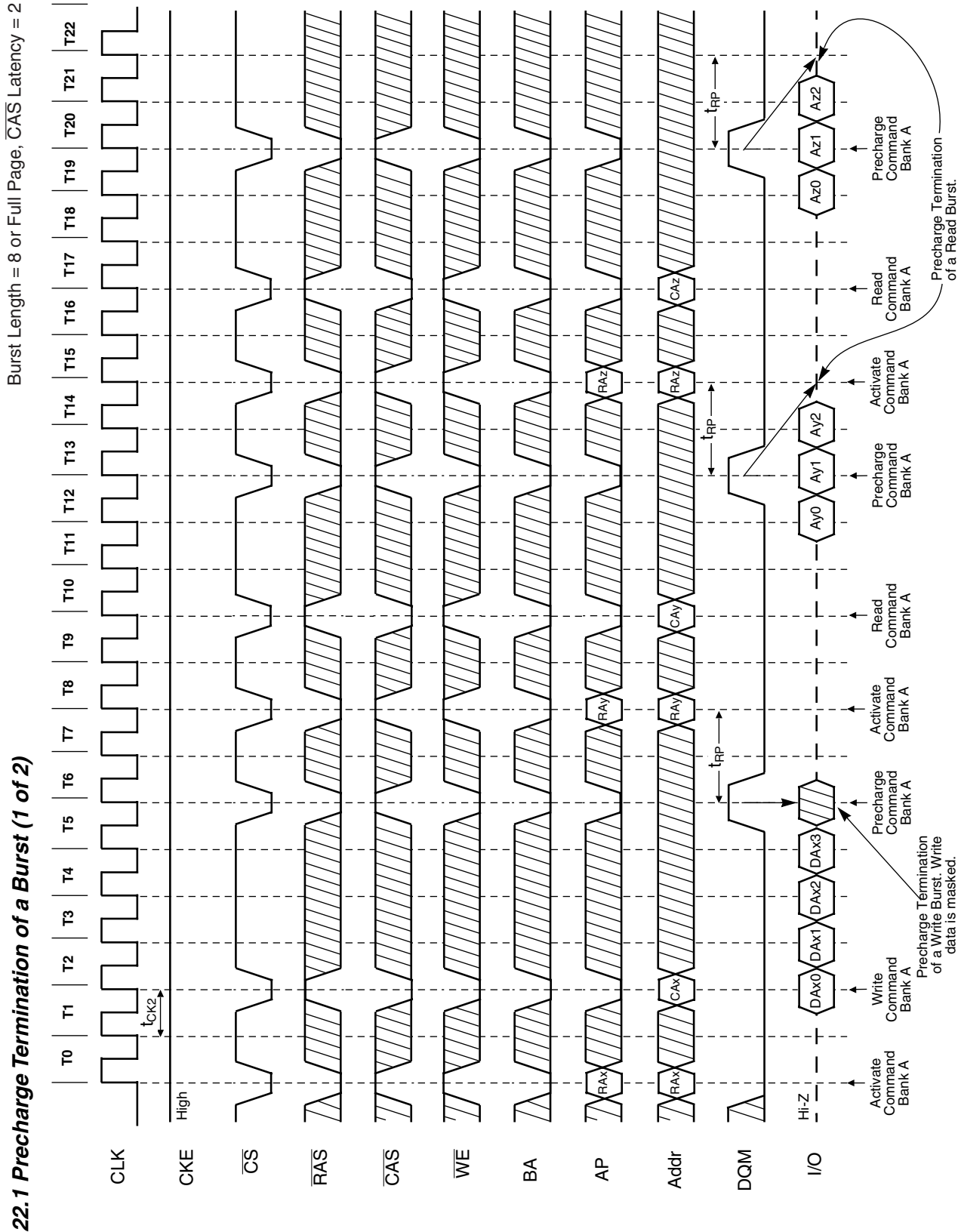
## 22.2 Precharge Termination of a Burst (2 of 2)

Burst Length = 4, 8 or Full Page, CAS Latency = 3

## Complete List of Operation Commands

### SDRAM Function Truth Table

| CURRENT STATE[1] | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $\overline{BS}$ | Addr | ACTION |
|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X | X | NOP or Power Down |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | RA | Row (&Bank) Active; Latch Row Address |
| | L | L | H | L | BS | AP | NOP[4] |
| | L | L | L | H | X | X | Auto-Refresh or Self-Refresh[5] |
| | L | L | L | L | Op- | Code | Mode reg. Access[5] |
| Row Active | H | X | X | X | X | X | NOP |
| | L | H | H | X | X | X | NOP |
| | L | H | L | H | BS | CA,AP | Begin Read; Latch CA; DetermineAP |
| | L | H | L | L | BS | CA,AP | Begin Write; Latch CA; DetermineAP |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Read | H | X | X | X | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | L | BS | X | Burst Stop Command > Row Active |
| | L | H | L | H | BS | CA,AP | Term Burst, New Read, DetermineAP[3] |
| | L | H | L | L | BS | CA,AP | Term Burst, Start Write, DetermineAP[3] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | Term Burst, Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Write | H | X | X | X | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;>Row Active) |
| | L | H | H | L | BS | X | Burst Stop Command > Row Active |
| | L | H | L | H | BS | CA,AP | Term Burst, Start Read, DetermineAP[3] |
| | L | H | L | L | BS | CA,AP | Term Burst, New Write, DetermineAP[3] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | Term Burst, Precharge[3] |
| | L | L | L | X | X | X | ILLEGAL |
| Read with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | H | BS | X | ILLEGAL[2] |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | ILLEGAL[2] |
| | L | L | L | X | X | X | ILLEGAL |

## SDRAM FUNCTION TRUTH TABLE(continued)

| CURRENT STATE[1] | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $\overline{BS}$ | Addr | ACTION |
|---|---|---|---|---|---|---|---|
| Write with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End;> Precharge) |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | H | BS | X | ILLEGAL[2] |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | ILLEGAL[2] |
| | L | L | L | X | X | X | ILLEGAL |
| Precharging | H | X | X | X | X | X | NOP;> Idle after tRP |
| | L | H | H | H | X | X | NOP;> Idle after tRP |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | NOP[4] |
| | L | L | L | X | X | X | ILLEGAL |
| Row Activating | H | X | X | X | X | X | NOP;> Row Active after tRCD |
| | L | H | H | H | X | X | NOP;> Row Active after tRCD |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | ILLEGAL[2] |
| | L | L | L | X | X | X | ILLEGAL |
| Write Recovering | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BS | X | ILLEGAL[2] |
| | L | H | L | X | BS | X | ILLEGAL[2] |
| | L | L | H | H | BS | X | ILLEGAL[2] |
| | L | L | H | L | BS | AP | ILLEGAL[2] |
| | L | L | L | X | X | X | ILLEGAL |
| Refreshing | H | X | X | X | X | X | NOP;> Idle after tRC |
| | L | H | H | H | X | X | NOP;> Idle after tRC |
| | L | H | H | L | X | X | ILLEGAL |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | H | X | X | X | ILLEGAL |
| | L | L | L | X | X | X | ILLEGAL |
| Mode Register Accessing | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | X | X | ILLEGAL |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | ILLEGAL |

## *Clock Enable (CKE) Truth Table:*

| STATE(n) | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Addr | ACTION |
|---|---|---|---|---|---|---|---|---|
| Self-Refresh[6] | H | X | X | X | X | X | X | INVALID |
|  | L | H | H | X | X | X | X | EXIT Self-Refresh, Idle after tRC |
|  | L | H | L | H | H | H | X | EXIT Self-Refresh, Idle after tRC |
|  | L | H | L | H | H | L | X | ILLEGAL |
|  | L | H | L | H | L | X | X | ILLEGAL |
|  | L | H | L | L | X | X | X | ILLEGAL |
|  | L | L | X | X | X | X | X | NOP (Maintain Self-Refresh) |
| Power-Down | H | X | X | X | X | X | X | INVALID |
|  | L | H | H | X | X | X | X | EXIT Power-Down, > Idle. |
|  | L | H | L | H | H | H | X | EXIT Power-Down, > Idle. |
|  | L | H | L | H | H | L | X | ILLEGAL |
|  | L | H | L | H | L | X | X | ILLEGAL |
|  | L | H | L | L | X | X | X | ILLEGAL |
|  | L | L | X | X | X | X | X | NOP (Maintain Low-Power Mode) |
| All. Banks Idle[7] | H | H | X | X | X | X | X | Refer to the function truth table |
|  | H | L | H | X | X | X | X | Enter Power- Down |
|  | H | L | L | H | H | H | X | Enter Power- Down |
|  | H | L | L | H | H | L | X | ILLEGAL |
|  | H | L | L | H | L | X | X | ILLEGAL |
|  | H | L | L | L | H | X | X | ILLEGAL |
|  | H | L | L | L | L | H | X | Enter Self-Refresh |
|  | H | L | L | L | L | L | X | ILLEGAL |
|  | L | L | X | X | X | X | X | NOP |
| Any State other than listed above | H | H | X | X | X | X | X | Refer to the function truth table |
|  | H | L | X | X | X | X | X | Begin Clock Suspend next cycle[8] |
|  | L | H | X | X | X | X | X | Exit Clock Suspend next cycle[8]. |
|  | L | L | X | X | X | X | X | Maintain Clock Suspend. |

Abbreviations:

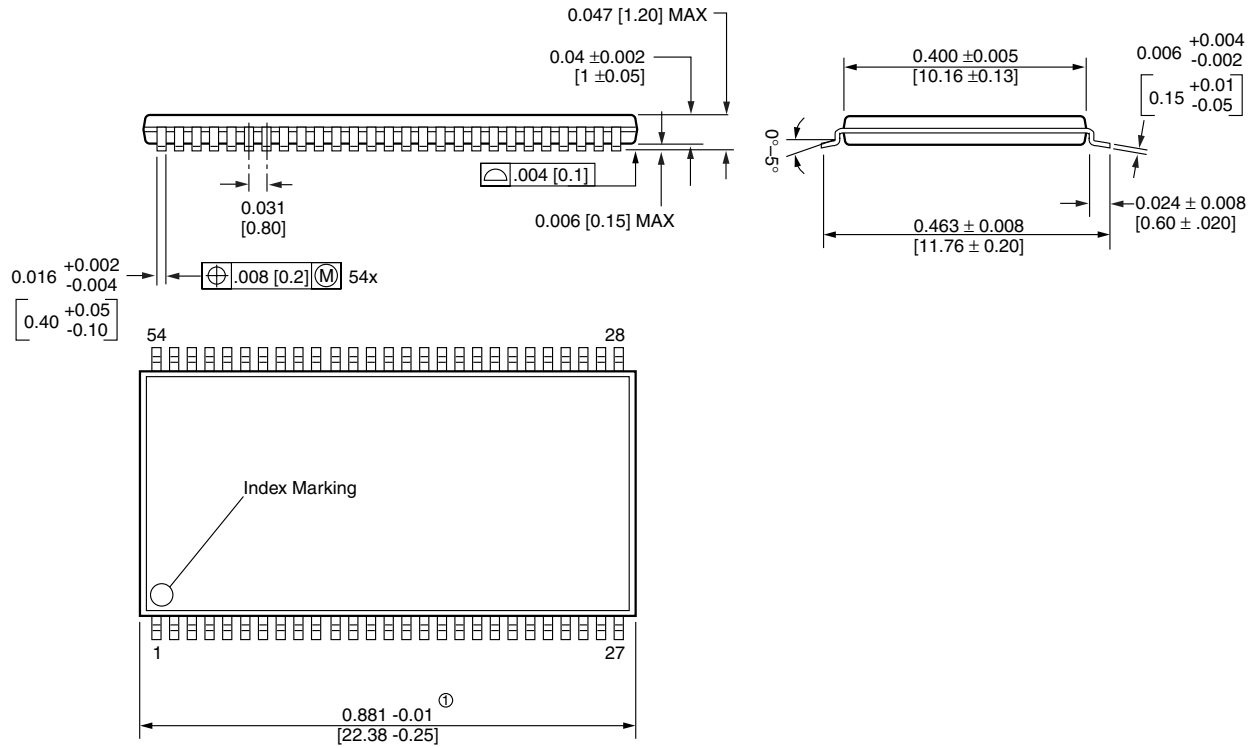RA = Row Address          BS = Bank Address

CA = Column Address       AP = Auto Precharge

**Notes for SDRAM function truth table:**

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (andAP).
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time  must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

## *Package Diagram*

### 54-Pin Plastic TSOP-II (400 mil)

0.047 [1.20] MAX

0.04 ±0.002
[1 ±0.05]

0.400 ±0.005
[10.16 ±0.13]

0.006 +0.004 -0.002

0.15 +0.01 -0.05

0°-5°

△ .004 [0.1]

0.031
[0.80]

0.006 [0.15] MAX

0.463 ± 0.008
[11.76 ± 0.20]

0.024 ± 0.008
[0.60 ± .020]

0.016 +0.002 -0.004

⊕ .008 [0.2] Ⓜ 54x

0.40 +0.05 -0.10

54                    28

Index Marking

1                     27

0.881 -0.01 ①
[22.38 -0.25]

① Does not include plastic or metal protrusion of 0.15 max. per side

Unit in inches [mm]

*Notes*

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