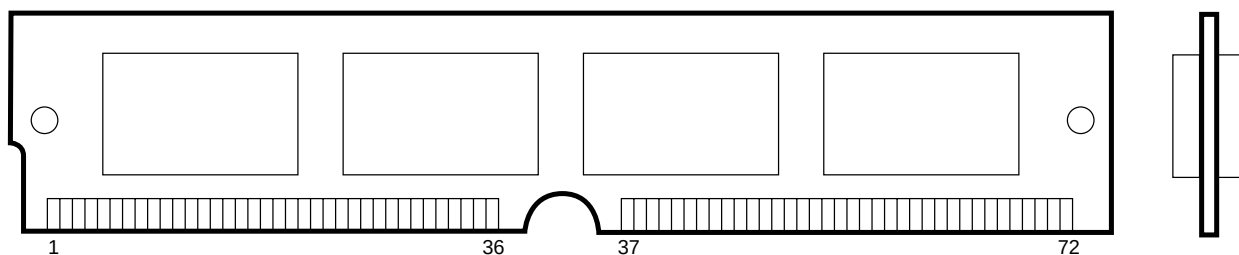


Features

- 2M x 32-bit organization
- V8DJX232BLT EDO
- V8DJ232BLT FPM
- Utilizes High Performance 1M x 8 CMOS DRAMs
- Fast access times: 45, 50, 60 ns
- Low power dissipation
- CAS before RAS refresh, $\overline{\text{RAS}}$ only refresh, and Hidden refresh capability
- Standard 72-lead single-in-line module
- Single 5 V $\pm 10\%$ Power Supply
- TTL Interface

Description

The V8DJX232BLT/V8DJ232BLT memory Module is organized as 2,097,152 x 32 bits in a 72-lead single-in-line module. The 2M x 32 memory module uses 8 Mosel-Vitellic 1M x 8 DRAMs. The x32 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

V8DJX232BLT/V8DJ232BLT Pin Configuration

1	VSS	19	NC	37	NC	55	I/O12
2	I/O1	20	I/O5	38	NC	56	I/O28
3	I/O17	21	I/O21	39	VSS	57	I/O13
4	I/O2	22	I/O6	40	$\overline{\text{CAS0}}$	58	I/O29
5	I/O18	23	I/O22	41	$\overline{\text{CAS2}}$	59	VCC
6	I/O3	24	I/O7	42	$\overline{\text{CAS3}}$	60	I/O30
7	I/O19	25	I/O23	43	$\overline{\text{CAS1}}$	61	I/O14
8	I/O4	26	I/O8	44	$\overline{\text{RAS0}}$	62	I/O31
9	I/O20	27	I/O24	45	$\overline{\text{RAS1}}$	63	I/O15
10	VCC	28	A7	46	NC	64	I/O32
11	NC	29	NC	47	$\overline{\text{WE}}$	65	I/O16
12	A0	30	VCC	48	NC	66	NC
13	A1	31	A8	49	I/O9	67	PD1*
14	A2	32	A9	50	I/O25	68	PD2*
15	A3	33	$\overline{\text{RAS3}}$	51	I/O10	69	PD3*
16	A4	34	$\overline{\text{RAS2}}$	52	I/O26	70	PD4*
17	A5	35	NC	53	I/O11	71	NC
18	A6	36	NC	54	I/O27	72	VSS

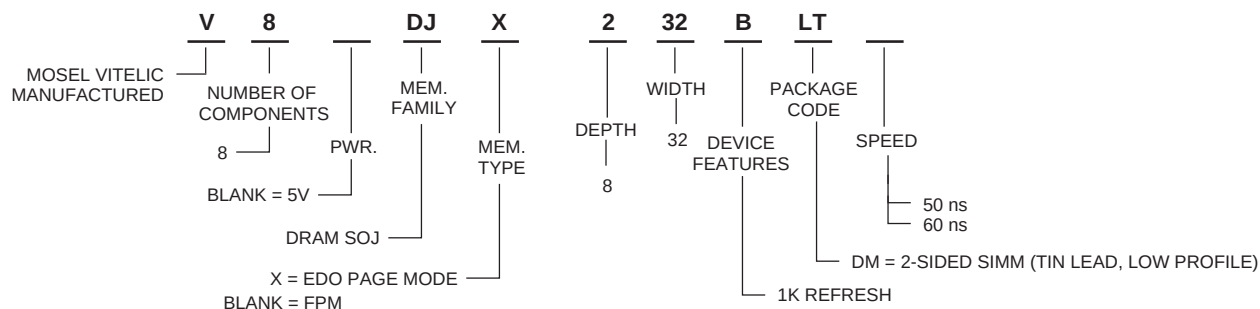
* Default Presence Detect is NC, Optional configurations are available.

Pin Names

Name	Description
A0–A9	Addresses
I/O1–I/O32	Data Inputs/Outputs
$\overline{\text{RAS0}}\text{--}\overline{\text{RAS3}}$	Row Address Strobes
$\overline{\text{CAS0}}\text{--}\overline{\text{CAS3}}$	Column Address Strobes
$\overline{\text{WE}}$	Write Enable
PD1–PD4	Presence Detect
V _{CC}	Power Supply (5V)
V _{SS}	Ground
NC	No Connection

Device Usage Chart

Operating Temperature Range	Organization	Module Type	Access Time (ns)		Power
	2M x 32	SIMM	50	60	Std
0°C to 70°C	•	•	•	•	•

Part Number Information

Edge Connector
Pin Names

1	VSS	2	I/O1
3	I/O17	4	I/O2
5	I/O18	6	I/O3
7	I/O19	8	I/O4
9	I/O20	10	VCC
11	NC	12	A0
13	A1	14	A2
15	A3	16	A4
17	A5	18	A6
19	NC	20	I/O5
21	I/O21	22	I/O6
23	I/O22	24	I/O7
25	I/O23	26	I/O8
27	I/O24	28	A7
29	NC	30	VCC
31	A8	32	A9
33	RAS3	34	RAS2
35	NC	36	NC

37	NC	38	NC
39	VSS	40	CAS0
41	CAS2	42	CAS3
43	CAS1	44	RAS0
45	RAS1	46	NC
47	WE	48	NC
49	I/O9	50	I/O25
51	I/O10	52	I/O26
53	I/O11	54	I/O27
55	I/O12	56	I/O28
57	I/O13	58	I/O29
59	VCC	60	I/O30
61	I/O14	62	I/O31
63	I/O15	64	I/O32
65	I/O16	66	NC
67	PD1	68	PD2
69	PD3	70	PD4
71	NC	72	VSS

Absolute Maximum Ratings*
Ambient Temperature

Under Bias -10°C to +80°C

Storage Temperature (plastic) -55°C to +125°C

Voltage on any Pin Except V_{CC}

Relative to V_{SS} -1.0 V to +7.0 V

Voltage on V_{CC} Relative to V_{SS} -1.0 V to +7.0 V

Data Out Current 50 mA

Power Dissipation

V8DJX232BLT 3.5 W

V8DJ232BLT 4.5 W

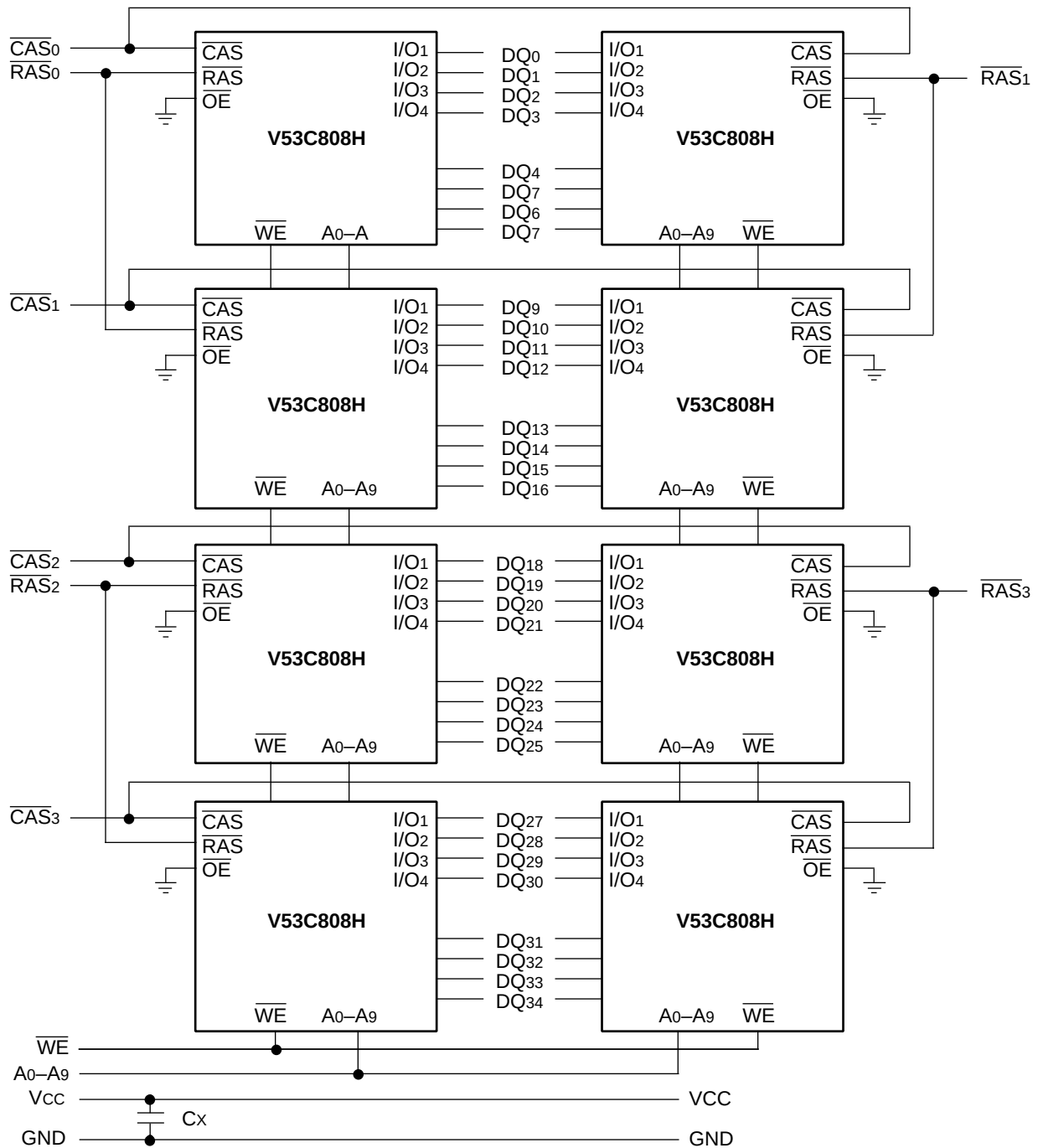
***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C _{IN}	Input Capacitance, Address Inputs		111	pF
C _{IN}	Input Capacitance, $\bar{W}$		127	pF
C _{I(O)}	Input/Output Capacitance, I/O1-I/O32		17	pF
C _{IN(RAS)}	Input Capacitance, RAS0, RAS2		32	pF
C _{IN(CAS)}	Input Capacitance, CAS0-CAS3		32	pF

***Note:** Capacitance is samples and not 100% tested.

V8DJX232BLT/V8DJ232BLT Functional Diagram


DC and Operating Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V8DJX232BLT			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-40		40	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-40		40	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	50			580	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		60			540			
I_{CC2}	V_{CC} Supply Current, TTL Standby				8	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, $\overline{\text{RAS}}$ -Only Refresh	50			580	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		60			540			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	50			340	mA	Minimum cycle	1, 2
		60			320			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				8	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ other inputs $\geq V_{SS}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				8	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$, All other inputs $\geq V_{SS}$	
I_{CC7}	Self Refresh Current				1.6	mA	CBR Cycle with $t_{RAS} \geq t_{RASS}$ (Min.) and $\overline{\text{CAS}} = V_{IL}$; $\text{WE} = V_{CC} - 0.2\text{ V}$; A0–A8 and $D_{IN} = V_{CC} - 0.2\text{ V}$	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		$V_{CC} + 1$	V		3
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 2\text{ mA}$	
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -2\text{ mA}$	

DC and Operating Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V8DJ232BLT			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-40		40	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-40		40	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	50			840	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		60			800			
I_{CC2}	V_{CC} Supply Current, TTL Standby				16	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, RAS-Only Refresh	50			840	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		60			800			
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	50			400	mA	Minimum cycle	1, 2
		60			360			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				8	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ other inputs $\geq V_{SS}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				8	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V},$ $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V},$ All other inputs $\geq V_{SS}$	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		$V_{CC} + 1$	V		3
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 4.2\text{ mA}$	
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -5\text{ mA}$	

AC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

#	Symbol	Parameter	V8DJ232BLT				Unit	Notes
			50		60			
			Min.	Max.	Min.	Max.		
1	t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	75K	60	75K	ns	
2	t _{RC}	Read or Write Cycle Time	90		110		ns	
3	t _{RP}	$\overline{\text{RAS}}$ Precharge Time	30		40		ns	
4	t _{CSH}	$\overline{\text{CAS}}$ Hold Time	50		60		ns	
5	t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	14		15		ns	
6	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	19	36	20	43	ns	
7	t _{RCS}	Read Command Setup Time	0		0		ns	4
8	t _{ASR}	Row Address Setup Time	0		0		ns	
9	t _{RAH}	Row Address Hold Time	9		10		ns	
10	t _{ASC}	Column Address Setup Time	0		0		ns	
11	t _{CAH}	Column Address Hold Time	7		10		ns	
12	t _{RSH (R)}	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	14		15		ns	
13	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5		5		ns	
14	t _{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0		0		ns	5
15	t _{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0		0		ns	5
16	t _{ROH}	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	10		10		ns	
17	t _{OAC}	Access Time from $\overline{\text{OE}}$		14		17	ns	
18	t _{CAC}	Access Time from $\overline{\text{CAS}}$		14		17	ns	6, 7
19	t _{RAC}	Access Time from $\overline{\text{RAS}}$		50		60	ns	6, 8, 9
20	t _{CAA}	Access Time from Column Address		24		30	ns	6, 7, 10
21	t _{LZ}	$\overline{\text{CAS}}$ to Low-Z Output	0		0		ns	16
22	t _{HZ}	Output buffer turn-off delay time	0	8	0	10	ns	16
23	t _{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	40		45		ns	
24	t _{RAD}	$\overline{\text{RAS}}$ to Column Address	14	26	15	30	ns	11
		Delay Time						
25	t _{RSH (W)}	$\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ Hold Time in Write Cycle	14		15		ns	
26	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	14		15		ns	
27	t _{WCS}	Write Command Setup Time	0		0		ns	12, 13
28	t _{WCH}	Write Command Hold Time	7		10		ns	
29	t _{WP}	Write Pulse Width	7		10		ns	

AC Characteristics (cont.)

#	Symbol	Parameter	V8DJ232BLT				Unit	Notes
			50		60			
			Min.	Max.	Min.	Max.		
30	t _{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	40		45		ns	
31	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	14		15		ns	
32	t _{DS}	Data in Setup Time	0		0		ns	14
33	t _{DH}	Data in Hold Time	7		10		ns	14
34	t _{WOH}	Write to $\overline{\text{OE}}$ Hold Time	8		10		ns	14
35	t _{OED}	$\overline{\text{OE}}$ to Data Delay Time	8		10		ns	14
36	t _{RWC}	Read-Modify-Write Cycle Time	130		170		ns	
37	t _{RRW}	Read-Modify-Write Cycle $\overline{\text{RAS}}$ Pulse Width	87		105		ns	
38	t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	34		40		ns	12
39	t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay in Read-Modify-Write Cycle	68		85		ns	12
40	t _{CRW}	$\overline{\text{CAS}}$ Pulse Width (RMW)	52		65		ns	
41	t _{AWD}	Col. Address to $\overline{\text{WE}}$ Delay	42		58		ns	12
42	t _{PC}	Fast Page Mode Read or Write Cycle Time	28		40		ns	
43	t _{CP}	$\overline{\text{CAS}}$ Precharge Time	7		8		ns	
44	t _{CAR}	Column Address to $\overline{\text{RAS}}$ Setup Time	24		30		ns	
45	t _{CAP}	Access Time from Column Precharge		27		34	ns	7
46	t _{DHR}	Data in Hold Time Referenced to $\overline{\text{RAS}}$	40		50		ns	
47	t _{CSR}	$\overline{\text{CAS}}$ Setup Time $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh	10		10		ns	
48	t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0		0		ns	
49	t _{CHR}	$\overline{\text{CAS}}$ Hold Time $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh	12		15		ns	
50	t _{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	70		85		ns	
51	t _T	Transition Time (Rise and Fall)	3	50	3	50	ns	15
52	t _{REF}	Refresh Interval (1024 Cycles)		16		16	ms	

AC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

#	Symbol	Parameter	V8DJX232BLT				Unit	Notes
			50		60			
			Min.	Max.	Min.	Max.		
1	t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	75K	60	75K	ns	
2	t _{RC}	Read or Write Cycle Time	90		110		ns	
3	t _{RP}	$\overline{\text{RAS}}$ Precharge Time	30		40		ns	
4	t _{CSH}	$\overline{\text{CAS}}$ Hold Time	50		60		ns	
5	t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	9		15		ns	
6	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	19	36	20	45	ns	
7	t _{RCS}	Read Command Setup Time	0		0		ns	4
8	t _{ASR}	Row Address Setup Time	0		0		ns	
9	t _{RAH}	Row Address Hold Time	9		10		ns	
10	t _{ASC}	Column Address Setup Time	0		0		ns	
11	t _{CAH}	Column Address Hold Time	7		10		ns	
12	t _{RSH (R)}	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	15		15		ns	
13	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5		5		ns	
14	t _{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0		0		ns	5
15	t _{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0		0		ns	5
16	t _{CAC}	Access Time from $\overline{\text{CAS}}$ (EDO)		14		15	ns	6, 7, 14
17	t _{RAC}	Access Time from $\overline{\text{RAS}}$		50		60	ns	6, 8, 9
18	t _{CAA}	Access Time from Column Address		24		30	ns	6, 7, 10
19	t _{LZ}	$\overline{\text{CAS}}$ to Low-Z Output	0		0		ns	16
20	t _{HZ}	$\overline{\text{CAS}}$ to High-Z Output	0	8	0	10	ns	16
21	t _{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	40		50		ns	
22	t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	14	26	15	30	ns	11
23	t _{RSH (W)}	$\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ Hold Time in Write Cycle	14		15		ns	
24	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	14		15		ns	
25	t _{WCS}	Write Command Setup Time	0		0		ns	12, 13
26	t _{WCH}	Write Command Hold Time	7		10		ns	
27	t _{WP}	Write Pulse Width	7		10		ns	
28	t _{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	40		50		ns	
29	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	14		15		ns	
30	t _{DS}	Data in Setup Time	0		0		ns	14
31	t _{DH}	Data in Hold Time	7		10		ns	14

#	Symbol	Parameter	V8DJX232BLT				Unit	Notes
			50		60			
			Min.	Max.	Min.	Max.		
32	t _{RWC} (RMW)	Read-Modify-Write Cycle Time	130		170		ns	
33	t _{RRW} (RMW)	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	87		105		ns	
34	t _{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	34		40		ns	12
35	t _{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	68		85		ns	12
36	t _{CRW}	$\overline{CAS}$ Pulse Width (RMW)	52		65		ns	
37	t _{AWD}	Col. Address to $\overline{WE}$ Delay	42		58		ns	12
38	t _{PC}	EDO Page Mode Read or Write Cycle Time	19		27		ns	
39	t _{CP}	CAS Precharge Time	7		10		ns	
40	t _{CAR}	Column Address to $\overline{RAS}$ Setup Time	24		30		ns	
41	t _{CAP}	Access Time from Column Precharge		27		34	ns	7
42	t _{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	40		50		ns	
43	t _{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		10		ns	
44	t _{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
45	t _{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	12		15		ns	
46	t _{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	70		85		ns	
47	t _{COH}	Output Hold After $\overline{CAS}$ Low	5		5		ns	
48	t _T	Transition Time (Rise and Fall)	3	50	3	50	ns	15
49	t _{REF}	Refresh Interval (1024 Cycles)		16		16	ms	17

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions. Specified I_{CC} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{CC}$.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC} .
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CAP} .
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RCD} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC} .
12. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume $t_T = 3$ ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 μ s pause and 8 $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

The technical drawing illustrates a mechanical component with two main views: a top view and a side view.

Top View Dimensions:

- Overall width: 4.25 [107.95]
- Overall height: 0.86 [21.76]
- Distance from left edge to first hole center: .13 [3.38]
- Distance between hole centers: 3.98 [101.19]
- Hole diameter: D = .12 [3.175]
- Radius at bottom corners: R = .06 [1.57]
- Bottom edge features include a series of vertical slots with a total width of .08 [2.03] and individual slot widths of .25 [6.35].
- Internal rectangular features are spaced at 1.75 [44.45] intervals.
- A circular feature labeled "A" is located near the bottom center.

Side View Dimensions:

- Thickness: 0.050
- Height from base to top surface: 0.33

Detail A:

Detail A provides a magnified view of the bottom edge features, showing five vertical slots with a total width of .10 [0.25], individual slot widths of .05 [1.27], and a gap between slots of .04 [1]. The height of the slots is .1 [2.54].

Unit in inches [mm]

Tolerances: ± 0.005 [0.13]

U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

HONG KONG

19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 852-2665-4883
FAX: 852-2664-7535

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

1 CREATION ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-578-3344
FAX: 886-3-579-2838

SINGAPORE

10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-3231801
FAX: 65-3237013

JAPAN

WBG MARINE WEST 25F
6, NAKASE 2-CHOME
MIHAMA-KU, CHIBA-SHI
CHIBA 261-71
PHONE: 81-43-299-6000
FAX: 81-43-299-6555

IRELAND & UK

BLOCK A UNIT 2
BROOMFIELD BUSINESS PARK
MALAHIDE
CO. DUBLIN, IRELAND
PHONE: +353 1 8038020
FAX: +353 1 8038049

**GERMANY
(CONTINENTAL
EUROPE & ISRAEL)**

71083 HERRENBERG
BENZSTR. 32
GERMANY
PHONE: +49 7032 2796-0
FAX: +49 7032 2796 22

U.S. SALES OFFICES**NORTHWESTERN**

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

NORTHEASTERN

SUITE 436
20 TRAFALGAR SQUARE
NASHUA, NH 03063
PHONE: 603-889-4393
FAX: 603-889-9347

SOUTHWESTERN

SUITE 200
5150 E. PACIFIC COAST HWY.
LONG BEACH, CA 90804
PHONE: 562-498-3314
FAX: 562-597-2174

**CENTRAL &
SOUTHEASTERN**

604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 972-690-1402
FAX: 972-690-0341

NORTHEASTERN

SUITE 436
20 TRAFALGAR SQUARE
NASHUA, NH 03063
PHONE: 603-889-4393
FAX: 603-889-9347

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.