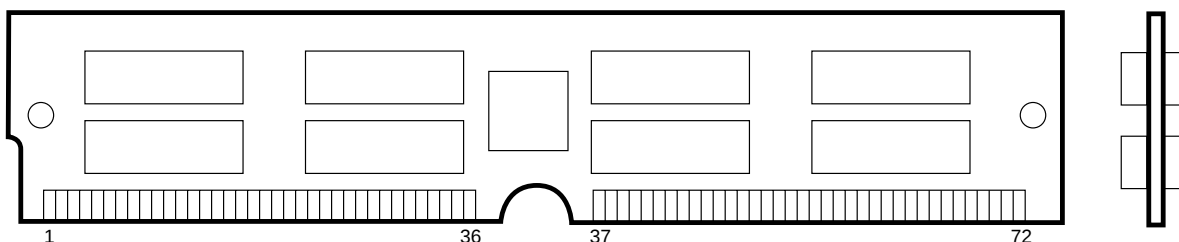


Features

- V16DJX432BLT EDO
- V16DJ432BLT FPM
- Utilizes High Performance 1M x 8 CMOS DRAMs
- Fast access times: 50 ns
- Low power dissipation
- CAS before RAS refresh, RAS only refresh, and Hidden refresh capability
- Standard 72-lead single-in-line module
- Single 5 V $\pm 10\%$ Power Supply
- TTL Interface

Description

The V16DJX432BLT/V16DJ432BLT memory Module is organized as 4,194,304 x 32 bits in a 72-lead single-in-line module. The 4M x 32 memory module uses 16 Mosel-Vitellic 1M x 8 DRAMs. The x32 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

V16DJX432BLT/V16DJ432BLT Pin Configuration


1	VSS	19	A10	37	NC	55	I/O12
2	I/O1	20	I/O5	38	NC	56	I/O28
3	I/O17	21	I/O21	39	VSS	57	I/O13
4	I/O2	22	I/O6	40	CAS0	58	I/O29
5	I/O18	23	I/O22	41	CAS2	59	VCC
6	I/O3	24	I/O7	42	CAS3	60	I/O30
7	I/O19	25	I/O23	43	CAS1	61	I/O14
8	I/O4	26	I/O8	44	RAS0	62	I/O31
9	I/O20	27	I/O24	45	RAS1	63	I/O15
10	VCC	28	A7	46	NC	64	I/O32
11	NC	29	NC	47	WE	65	I/O16
12	A0	30	VCC	48	NC	66	NC
13	A1	31	A8	49	I/O9	67	PD1*
14	A2	32	A9	50	I/O25	68	PD2*
15	A3	33	RAS3	51	I/O10	69	PD3*
16	A4	34	RAS2	52	I/O26	70	PD4*
17	A5	35	NC	53	I/O11	71	NC
18	A6	36	NC	54	I/O27	72	VSS

* Default Presence Detect is NC, Optional configurations are available.

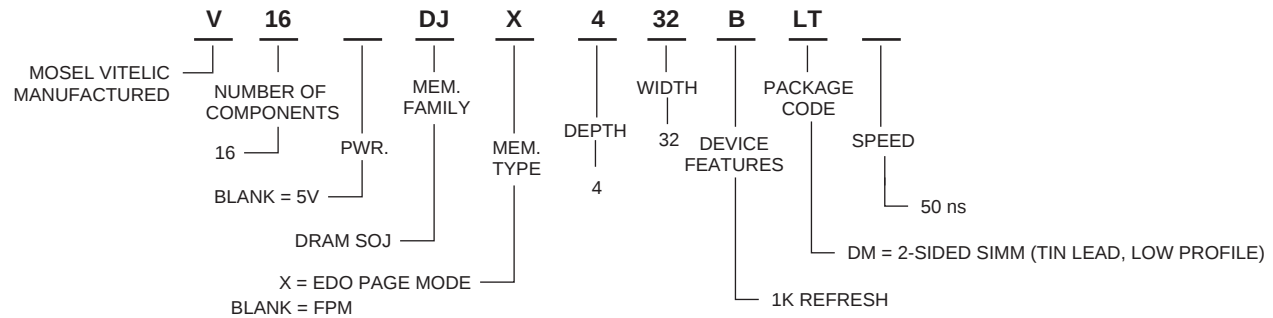
Pin Names

Name	Description
A0–A10	Addresses
I/O1–I/O32	Data Inputs/Outputs
RAS0–RAS3	Row Address Strobes
CAS0–CAS3	Column Address Strobes
WE	Write Enable
PD1–PD4	Presence Detect
V _{CC}	Power Supply (5V)
V _{SS}	Ground
NC	No Connection

Device Usage Chart

Operating Temperature Range	Organization	Module Type	Access Time (ns)	Power
	4M x 32	SIMM	50	Std
0°C to 70°C	•	•	•	•

Part Number Information



Edge Connector

Pin Names

1	VSS	2	I/O1
3	I/O17	4	I/O2
5	I/O18	6	I/O3
7	I/O19	8	I/O4
9	I/O20	10	VCC
11	NC	12	A0
13	A1	14	A2
15	A3	16	A4
17	A5	18	A6
19	A10	20	I/O5
21	I/O21	22	I/O6
23	I/O22	24	I/O7
25	I/O23	26	I/O8
27	I/O24	28	A7
29	NC	30	VCC
31	A8	32	A9
33	RAS3	34	RAS2
35	NC	36	NC

37	NC	38	NC
39	VSS	40	CAS0
41	CAS2	42	CAS3
43	CAS1	44	RAS0
45	RAS1	46	NC
47	WE	48	NC
49	I/O9	50	I/O25
51	I/O10	52	I/O26
53	I/O11	54	I/O27
55	I/O12	56	I/O28
57	I/O13	58	I/O29
59	VCC	60	I/O30
61	I/O14	62	I/O31
63	I/O15	64	I/O32
65	I/O16	66	NC
67	PD1	68	PD2
69	PD3	70	PD4
71	NC	72	VSS

Absolute Maximum Ratings*

Ambient Temperature

Under Bias -10°C to +80°C

Storage Temperature (plastic) -55°C to +125°C

Voltage on any Pin Except V_{CC}Relative to V_{SS} -1.0 V to +7.0 VVoltage on V_{CC} Relative to V_{SS} -1.0 V to +7.0 V

Data Out Current 50 mA

Power Dissipation

V16DJX232BLT 3.5 W

V16DJ232BLT 4.5 W

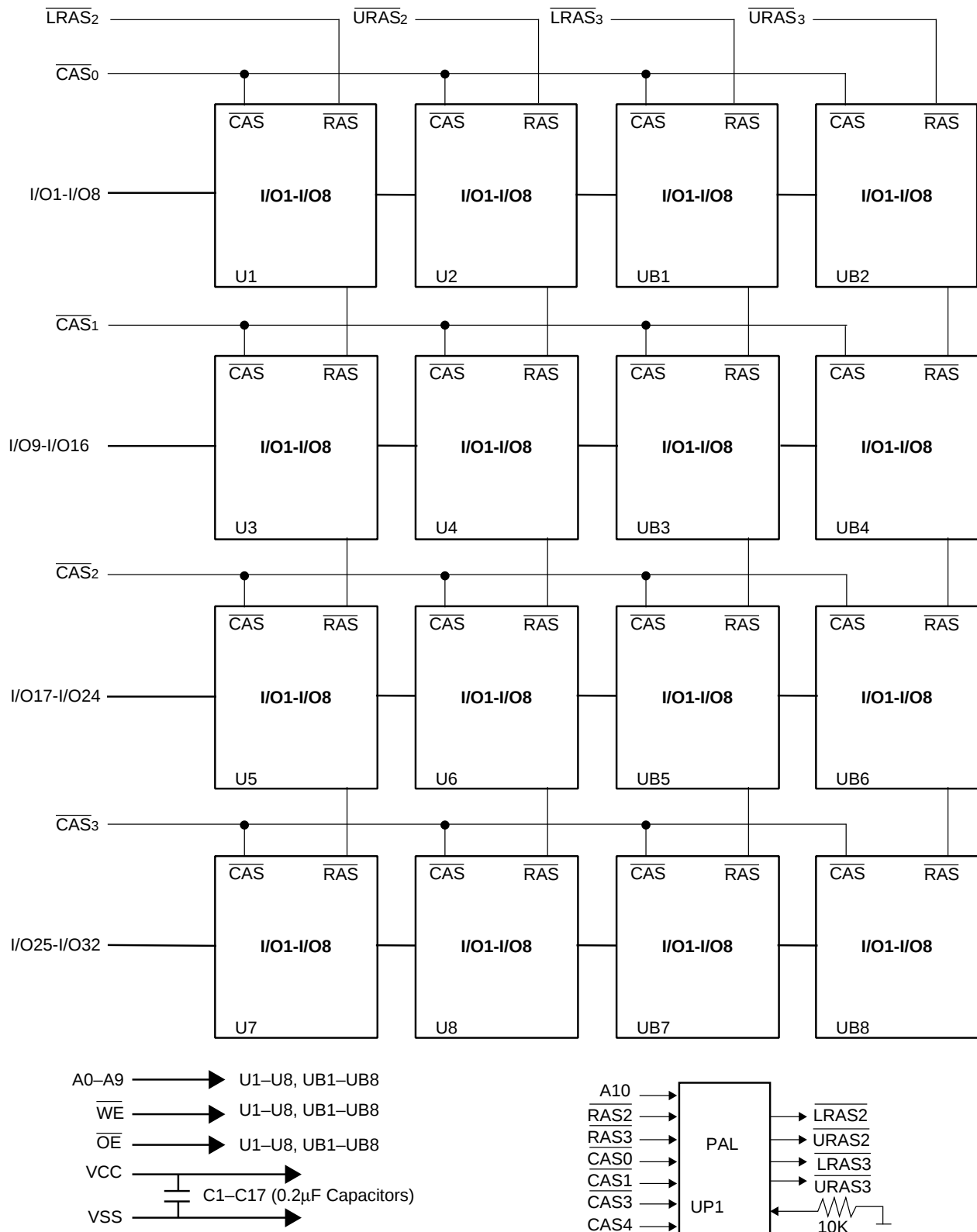
***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C _{IN}	Input Capacitance, Address Inputs		111	pF
C _{IN}	Input Capacitance, $\bar{W}$		127	pF
C _{I(O)}	Input/Output Capacitance, I/O1–I/O32		17	pF
C _{IN(RAS)}	Input Capacitance, RAS0, RAS2		32	pF
C _{IN(CAS)}	Input Capacitance, CAS0–CAS3		32	pF

***Note:** Capacitance is samples and not 100% tested.

Functional Diagram


DC and Operating Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V16DJX432BLT			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-40		40	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-40		40	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	50			640	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
I_{CC2}	V_{CC} Supply Current, TTL Standby				70	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, $\overline{\text{RAS}}$ -Only Refresh	50			640	mA	$t_{RC} = t_{RC}(\text{min.})$	2
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	50			400	mA	Minimum cycle	1, 2
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				70	mA	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$ other inputs $\geq V_{SS}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				70	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$, All other inputs $\geq V_{SS}$	
I_{CC7}	Self Refresh Current				6.4	mA	CBR Cycle with $t_{RAS} \geq t_{RASS}$ (Min.) and $\overline{\text{CAS}} = V_{IL}$; $WE = V_{CC} - 0.2\text{ V}$; A0-A8 and $D_{IN} = V_{CC} - 0.2\text{ V}$	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		$V_{CC} + 1$	V		3
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 2\text{ mA}$	
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -2\text{ mA}$	

DC and Operating Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V16DJ432BLT			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-40		40	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-40		40	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ RAS, CAS at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	50			840	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
I_{CC2}	V_{CC} Supply Current, TTL Standby				16	mA	RAS, CAS at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, RAS-Only Refresh	50			840	mA	$t_{RC} = t_{RC}(\text{min.})$	2
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	50			400	mA	Minimum cycle	1, 2
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				8	mA	RAS = V_{IH} , CAS = V_{IL} other inputs $\geq V_{SS}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				8	mA	RAS $\geq V_{CC} - 0.2\text{ V}$, CAS $\geq V_{CC} - 0.2\text{ V}$, All other inputs $\geq V_{SS}$	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		$V_{CC} + 1$	V		3
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 4.2\text{ mA}$	
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -5\text{ mA}$	

AC Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

#	Symbol	Parameter	V16DJ232BLT		Unit	Notes
			Min.	Max.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	50	75K	ns	
2	t_{RC}	Read or Write Cycle Time	90		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	30		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	50		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	14		ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	19	36	ns	
7	t_{RCS}	Read Command Setup Time	0		ns	4
8	t_{ASR}	Row Address Setup Time	0		ns	
9	t_{RAH}	Row Address Hold Time	9		ns	
10	t_{ASC}	Column Address Setup Time	0		ns	
11	t_{CAH}	Column Address Hold Time	7		ns	
12	$t_{RSH (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		ns	
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		ns	5
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		ns	5
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		14	ns	
18	t_{CAC}	Access Time from $\overline{CAS}$		14	ns	6, 7
19	t_{RAC}	Access Time from $\overline{RAS}$		50	ns	6, 8, 9
20	t_{CAA}	Access Time from Column Address		24	ns	6, 7, 10
21	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		ns	16
22	t_{HZ}	Output buffer turn-off delay time	0	8	ns	16
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	40		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	14	26	ns	11
25	$t_{RSH (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	14		ns	
26	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	14		ns	
27	t_{WCS}	Write Command Setup Time	0		ns	12, 13
28	t_{WCH}	Write Command Hold Time	7		ns	
29	t_{WP}	Write Pulse Width	7		ns	
30	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	40		ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	14		ns	
32	t_{DS}	Data in Setup Time	0		ns	14

AC Characteristics (cont.)

#	Symbol	Parameter	V16DJ232BLT		Unit	Notes
			Min.	Max.		
33	t_{DH}	Data in Hold Time	7		ns	14
34	t_{WOH}	Write to $\overline{OE}$ Hold Time	8		ns	14
35	t_{OED}	$\overline{OE}$ to Data Delay Time	8		ns	14
36	t_{RWC}	Read-Modify-Write Cycle Time	130		ns	
37	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	87		ns	
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	34		ns	12
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	68		ns	12
40	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	52		ns	
41	t_{AWD}	Col. Address to $\overline{WE}$ Delay	42		ns	12
42	t_{PC}	Fast Page Mode Read or Write Cycle Time	28		ns	
43	t_{CP}	$\overline{CAS}$ Precharge Time	7		ns	
44	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	24		ns	
45	t_{CAP}	Access Time from Column Precharge		27	ns	7
46	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	40		ns	
47	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		ns	
48	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		ns	
49	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	12		ns	
50	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	70		ns	
51	t_T	Transition Time (Rise and Fall)	3	50	ns	15
52	t_{REF}	Refresh Interval (1024 Cycles)		16	ms	

AC Characteristics
 $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

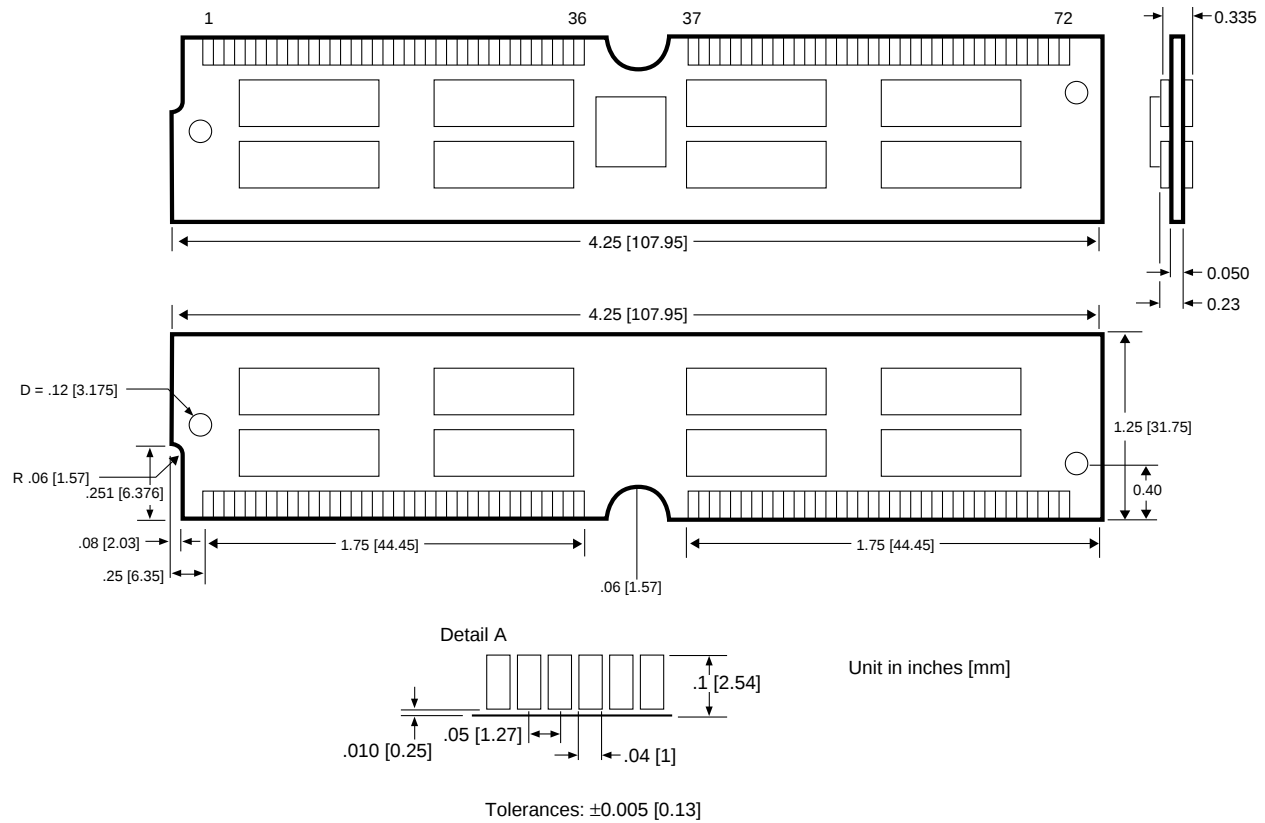
#	Symbol	Parameter	V16DJX232BLT		Unit	Notes
			Min.	Max.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	50	75K	ns	
2	t_{RC}	Read or Write Cycle Time	90		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	30		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	50		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	9		ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	19	36	ns	
7	t_{RCS}	Read Command Setup Time	0		ns	4
8	t_{ASR}	Row Address Setup Time	0		ns	
9	t_{RAH}	Row Address Hold Time	9		ns	
10	t_{ASC}	Column Address Setup Time	0		ns	
11	t_{CAH}	Column Address Hold Time	7		ns	
12	$t_{RSH}(R)$	$\overline{RAS}$ Hold Time (Read Cycle)	15		ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		ns	
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		ns	5
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		ns	5
16	t_{CAC}	Access Time from $\overline{CAS}$ (EDO)		14	ns	6, 7, 14
17	t_{RAC}	Access Time from $\overline{RAS}$		50	ns	6, 8, 9
18	t_{CAA}	Access Time from Column Address		24	ns	6, 7, 10
19	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		ns	16
20	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	8	ns	16
21	t_{AR}	Column Address Hold Time from $\overline{RAS}$	40		ns	
22	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	14	26	ns	11
23	$t_{RSH}(W)$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	14		ns	
24	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	14		ns	
25	t_{WCS}	Write Command Setup Time	0		ns	12, 13
26	t_{WCH}	Write Command Hold Time	7		ns	
27	t_{WP}	Write Pulse Width	7		ns	
28	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	40		ns	
29	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	14		ns	
30	t_{DS}	Data in Setup Time	0		ns	14
31	t_{DH}	Data in Hold Time	7		ns	14
32	$t_{RWC}(RMW)$	Read-Modify-Write Cycle Time	130		ns	

#	Symbol	Parameter	V16DJX232BLT		Unit	Notes
			Min.	Max.		
33	t_{RRW} (RMW)	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	87		ns	
34	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	34		ns	12
35	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	68		ns	12
36	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	52		ns	
37	t_{AWD}	Col. Address to $\overline{WE}$ Delay	42		ns	12
38	t_{PC}	EDO Page Mode Read or Write Cycle Time	19		ns	
39	t_{CP}	CAS Precharge Time	7		ns	
40	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	24		ns	
41	t_{CAP}	Access Time from Column Precharge		27	ns	7
42	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	40		ns	
43	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		ns	
44	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	12		ns	
46	t_{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	70		ns	
47	t_{COH}	Output Hold After $\overline{CAS}$ Low	5		ns	
48	t_T	Transition Time (Rise and Fall)	3	50	ns	15
49	t_{REF}	Refresh Interval (1024 Cycles)		16	ms	17

AC Characteristics (cont.)**Notes:**

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions. Specified I_{CC} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{CC}$.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC} .
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CAP} .
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RCD} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC} .
12. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume $t_T = 3$ ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 μ s pause and 8 $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Package Dimensions



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