VLSI Technology

VNS67200 ATM Quad UNI

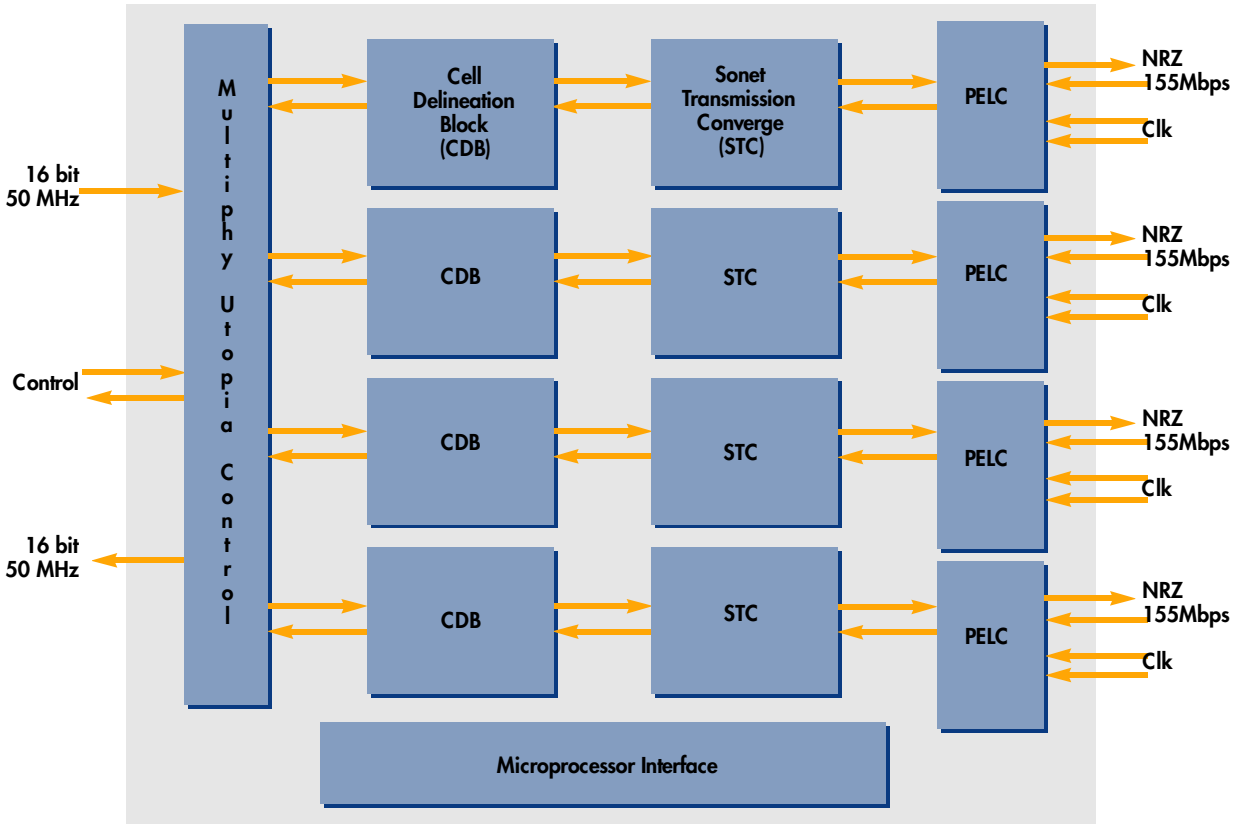
Four channel single-chip ATM physical layer I/O device

OVERVIEW

The VNS67200 ATM Quad User Network Interface (Quad UNI) from VLSI is a four channel single-chip ATM physical layer I/O device designed for use in ATM Local Area Network (LAN) or ATM Wide Area Network (WAN) access applications. Each of the four available high speed network ports is an independent, ECL compatible (PECL), full duplex, SONET/SDH formatted serial data interface that operates at either 155.52 Mbps (STS-3c/STM-1) or 51.84 Mbps (STS-1) as specified in version 3.1 of the ATM Forum UNI. A 50 MHz Level 2 Utopia bus implementing the ATM Forum's Multiple Physical Interface (Multi-PHY) capability provides independent 16-bit wide parallel transmit and receive data paths for the transfer of ATM cells between the ATM switching system and the VLSI Quad UNI. The Quad UNI's internal control and status registers are accessible through a generic 8-bit microprocessor bus interface. The Quad UNI design employs VLSI's proprietary low power, high density cell-based design methodology and modular Functional System Block (FSB™) architecture. The SONET Transmission Convergence (STC) block in each channel handles the processing required to create and receive SONET/SDH synchronous payload envelopes including transport (line and section) and path overhead processing, scrambling/ descrambling, performance monitoring and alarming. It supports fixed transmit framing and fixed/floating receive framing per ATM Forum specification.

The Cell Delineation Block (CDB) in each channel processes the received ATM cells recovered from within the SONET SPE by the STC block and prepares the ATM stream for transmission to the STC block. Its functions include cell rate decoupling, cell delineation (locating the start of the cell), Header Error Correction (HEC) generation/verification, and idle cell generation.

VNS67200 Block Diagram



FEATURES

- Four port ATM UNI implemented according to ATM Forum UNI 3.1 and ITU I.432
- Each port operates independently at 155.52 Mhz or 51.84 MHz to provide SONET/SDH STS-3c/STM1 or STS-1 formatted full duplex serial data
- 50 MHz Level 2 Utopia bus with Multi-PHY capability operates in direct (sec 4.3) or polled status (sec. 4.2) modes as specified in the 1995 ATM Forum standard provides independent 16-bit wide transmit and receive data paths
- Four cell deep transmit and receive FIFO buffers for each channel
- Maps ATM cells into SONET or SDH frames
- Generates and detects SONET/SDH path, line and section overhead including OAM signals
- Monitors network performance and reports alarm conditions
- Automatic SONET/SDH alarm generation capability
- Programmable SONET/SDH error insertion (A1/A2, B1, B2, B3) for network testing
- SONET/SDH scrambling may optionally be disabled
- Automatic ATM cell HEC generation
- Automatic HEC detection and verification with optional single-bit HEC error correction
- Optional tagging of valid/errored cells
- Programmable automatic filtering of received idle/unassigned ATM cells with option to have them passed through transparently
- Automatic generation of idle/unassigned cells upon transmit FIFO underrun
- User programmable idle/unassigned cell bit pattern
- Optional scrambling/descrambling of the ATM cell payload
- Compatible with various physical media such as single or multi-mode fiber, shielded twisted pair copper or coaxial cable
- Loop timing capability on each port allows the received data clock to be used as the transmit clock
- CMOS Positive Shifted ECL interface supports 155 MHz serial data rate
- Low power, +5V, CMOS technology
- 208 pin thermally enhanced plastic quad flat pack (TE-MQFP) package

APPLICATIONS

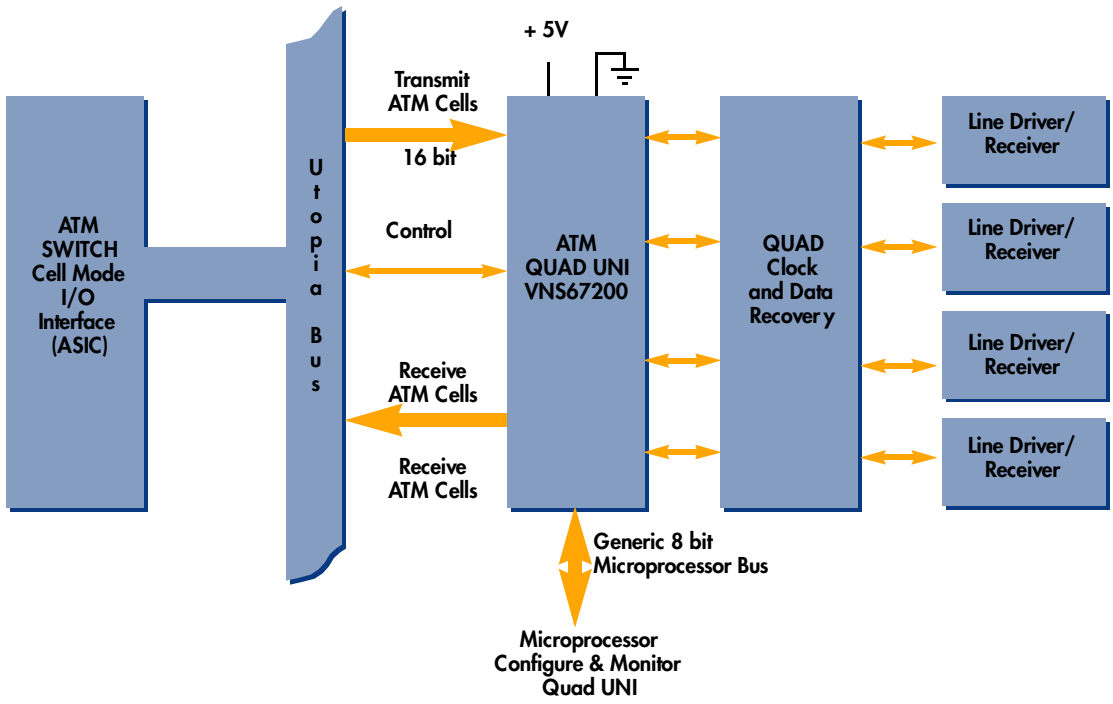
- ATM Switches and LAN Hubs
- Internetworking Devices (Bridges and Routers)
- Enterprise Multiplexers
- Access Multiplexers
- Video Servers & File Servers

FUNCTIONAL DESCRIPTION

ECL Interface

The CMOS Positive Shifted ECL (PECL) differential transmit/receive interface is used for the short interconnection between the Quad UNI and Physical Media Dependent (PMD) devices such as a clock and data recovery circuit. The PECL FSB™ macrocell operates at 155/52 MHz with a 50-Ohm termination to provide ECL-CMOS compatibility in SONET/SDH ATM applications.

System Block Diagram



SONET Transmission Convergence Block

The STC block provides the SONET transport and path overhead processing for the STS-1/STS-3c/STM1 formatted signals per ATM Forum UNI 3.1 and Bell Communications Research TR-NTW-000253 specifications.

In the receive direction, the frame detector locks to the SONET framing pattern (A1,A2). The STC block optionally descrambles the received data, interprets the receive payload pointer (H1,H2), extracts the path overhead and recovers the frame payload which contains the ATM cell data.

All alarm and error conditions are reported in status registers and counters. Counters record section, line and path (B1, B2, B3) errors, line Far End Block Errors (FEBE) and path FEBE. Registers indicate Loss of Signal (LOS), Loss of Frame (LOF), Out of Frame (OOF), Loss of Pointer (LOP), line Alarm Indication Signal (AIS), line Far End Receive Failure (K2-FERF), line Far end Block Error (Z2-FEBE), path AIS, path FEBE and path Remote Defect Indication (RDI).

In the transmit direction, the STC block generates the SONET/SDH frame including all required overhead and it places the ATM cell data in the payload and optionally scrambles the frame.

The STC block automatically inserts fixed transmit payload pointers (H1,H2), framing (A1,A2), identity (C1), section, line and path (B1,B2,B3) BIP performance monitor bytes, and (optionally) automatically inserts alarm and performance indications such as Path Alarm Indication Signal (PAIS), Path Far End Block Error (PFEB), path Remote Defect Indication (RDI), line Alarm Indication Signal (AIS), line Far End Block Error (FEBE) and line Far End Receive Failure (FERF). Intentional (A1,A2), B1, B2 and B3 errors can (optionally) be automatically generated for test purposes.

Cell Delineation Block

CDB receive functions include (optional) descrambling of the ATM cell payload, delineation/location of the ATM cells based on detection of the HEC in the header, recovery of valid cells with (optional) correction of single bit HEC errors and (optional) discard of idle/errored cells. Counters record the number of valid cells and errored cells received. The selected cells are then transferred to a four cell deep per channel FIFO and made available to the ATM switching system through the Utopia bus interface. Loss of cell delineation alarm is indicated in a status register and on per channel output pins.

CDB transmit functions include automatic generation of idle/unassigned cells containing a user programmable header and payload bit pattern when the channel's 4 cell deep transmit FIFO contains less than one valid cell, extraction of the ATM cells from the FIFO, HEC calculation (with coset polynomial option) and HEC insertion prior to transmission of the cell to the STC block. A counter records the number of valid cells transmitted.

BENEFITS

- Reduced silicon costs and board space for the end systems due to the highly integrated architecture of the Quad UNI
- Low power dissipation and reduced pin count compared to four discrete devices
- Interoperability with other devices is assured as Quad UNI is based on the widely followed ATM Forum standards
- System design time is reduced because of the easy to use diagnostic tests and microprocessor interface to monitor status information

STANDARDS COMPLIANCE

- ATM Forum UNI 3.1 and ITU recommendation I.432
- ATM Forum Utopia L2 1995
- STS-3c/STS-1 framing per TR-NWT-000253
- H1, H2, and H3 SONET pointers processed according to TR-NWT-000253

For update information, please visit our Web site at http://www.vlsi.com or call the Worldwide Headquarters at +1-408-434-3100 or the European Headquarters at +49/89/627 06-0

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