NEC

MOS INTEGRATED CIRCUIT

# μPD75P3116

## 4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD75P3116 replaces the μPD753108's internal mask ROM with a one-time PROM, and features expanded ROM capacity.

Because the μPD75P3116 supports programming by users, it is suitable for use in evaluation of systems in the development stage using the μPD753104, 753106, or 753108, and for use in small-scale production.

**Detailed information about functions is provided in the following User's Manual. Be sure to read it before designing:**

**μPD753108 User's Manual: U10890E**

## FEATURES

- ○ Compatible with μPD753108
- ○ Memory capacity:
  - PROM: 16384 × 8 bits
  - RAM: 512 × 4 bits
- ○ Can be operated in same power supply voltage range as the mask version μPD753108
  - $V_{DD}$ = 1.8 to 5.5 V
- ○ On-chip LCD controller/driver
- ○ QTOP™ microcontroller

**Remark** QTOP microcontrollers are microcontrollers with on-chip one-time PROM that are totally supported by NEC. This support includes writing application programs, marking, screening, and verification.

## ORDERING INFORMATION

| | Part Number | Package |
|---|---|---|
| | μPD75P3116GC-AB8 | 64-pin plastic QFP (14 × 14) |
| | μPD75P3116GK-8A8 | 64-pin plastic LQFP (12 × 12) |
| ★ | μPD75P3116GC-8BS | 64-pin plastic LQFP (14 × 14) |

**Caution This device does not provide an internal pull-up resistor connection function by means of mask option.**



Document No. U11369EJ3V0DS00 (3rd edition)
Date Published March 2002 N CP(K)
Printed in Japan

**The mark ★ shows major revised points.**

## FUNCTION OUTLINE

| Item | | Function | |
|---|---|---|---|
| Instruction execution time | | • 0.95, 1.91, 3.81, or 15.3 μs (main system clock: @ 4.19 MHz)<br>• 0.67, 1.33, 2.67, or 10.7 μs (main system clock: @ 6.0 MHz)<br>• 122 μs (subsystem clock: @ 32.768 kHz) | |
| Internal memory | PROM | 16384 × 8 bits | |
| | RAM | 512 × 4 bits | |
| General-purpose registers | | • 4-bit manipulation: 8 × 4 banks<br>• 8-bit manipulation: 4 × 4 banks | |
| I/O ports | CMOS input | 8 | Internal pull-up resistor connection can be specified by software setting: 7 |
| | CMOS I/O | 20 | Internal pull-up resistor connection can be specified by software setting: 12<br>Shared with segment pins: 8 |
| | N-ch open-drain I/O | 4 | 13 V withstanding voltage |
| | Total | 32 | |
| LCD controller/driver | | • Segment number selection: 16/20/24 segments (switchable to CMOS I/O ports in a batch of 4 pins, max. 8 pins)<br>• Display mode selection: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) | |
| Timers | | 5 channels: • 8-bit timer/event counter: 3 channels (Can be used as 16-bit timer/event counter, carrier generator, and timer with gate)<br>• Basic interval timer/watchdog timer: 1 channel<br>• Watch timer: 1 channel | |
| Serial interface | | • 3-wire serial I/O mode ··· MSB/LSB first switchable<br>• 2-wire serial I/O mode<br>• SBI mode | |
| Bit sequential buffer (BSB) | | 16 bits | |
| Clock output (PCL) | | Φ, 524, 262, and 65.5 kHz (main system clock: @ 4.19 MHz)<br>Φ, 750, 375, and 93.8 kHz (main system clock: @ 6.0 MHz) | |
| Buzzer output (BUZ) | | • 2, 4, and 32 kHz (main system clock: @ 4.19 MHz or subsystem clock: @ 32.768 kHz)<br>• 2.93, 5.86, 46.9 kHz (main system clock: @ 6.0 MHz) | |
| Vectored interrupts | | • External: 3<br>• Internal: 5 | |
| Test inputs | | • External: 1<br>• Internal: 1 | |
| System clock oscillator | | • Ceramic/crystal oscillator for main system clock<br>• Crystal oscillator for subsystem clock | |
| Standby function | | STOP/HALT mode | |
| Power supply voltage | | $V_{DD}$ = 1.8 to 5.5 V | |
| Package | | • 64-pin plastic QFP (14 × 14)<br>• 64-pin plastic LQFP (12 × 12)<br>★ • 64-pin plastic LQFP (14 × 14) | |

## CONTENTS

1. PIN CONFIGURATION (TOP VIEW) ... 4

2. BLOCK DIAGRAM ... 6

3. PIN FUNCTIONS ... 7
- 3.1 Port Pins ... 7
- 3.2 Non-Port Pins ... 9
- 3.3 Pin I/O Circuits ... 11
- 3.4 Recommended Connection of Unused Pins ... 13

4. Mk I AND Mk II MODE SELECTION FUNCTION ... 14
- 4.1 Differences Between Mk I Mode and Mk II Mode ... 14
- 4.2 Setting of Stack Bank Selection (SBS) Register ... 15

5. DIFFERENCES BETWEEN μPD75P3116 AND μPD753104, 753106, 753108 ... 16

6. MEMORY CONFIGURATION ... 17

7. INSTRUCTION SET ... 19

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY ... 28
- 8.1 Operation Modes for Program Memory Write/Verify ... 28
- 8.2 Program Memory Write Procedure ... 29
- 8.3 Program Memory Read Procedure ... 30
- 8.4 One-Time PROM Screening ... 31

9. ELECTRICAL SPECIFICATIONS ... 32

10. CHARACTERISTIC CURVES (REFERENCE VALUES) ... 47

11. PACKAGE DRAWINGS ... 49

12. RECOMMENDED SOLDERING CONDITIONS ... 52

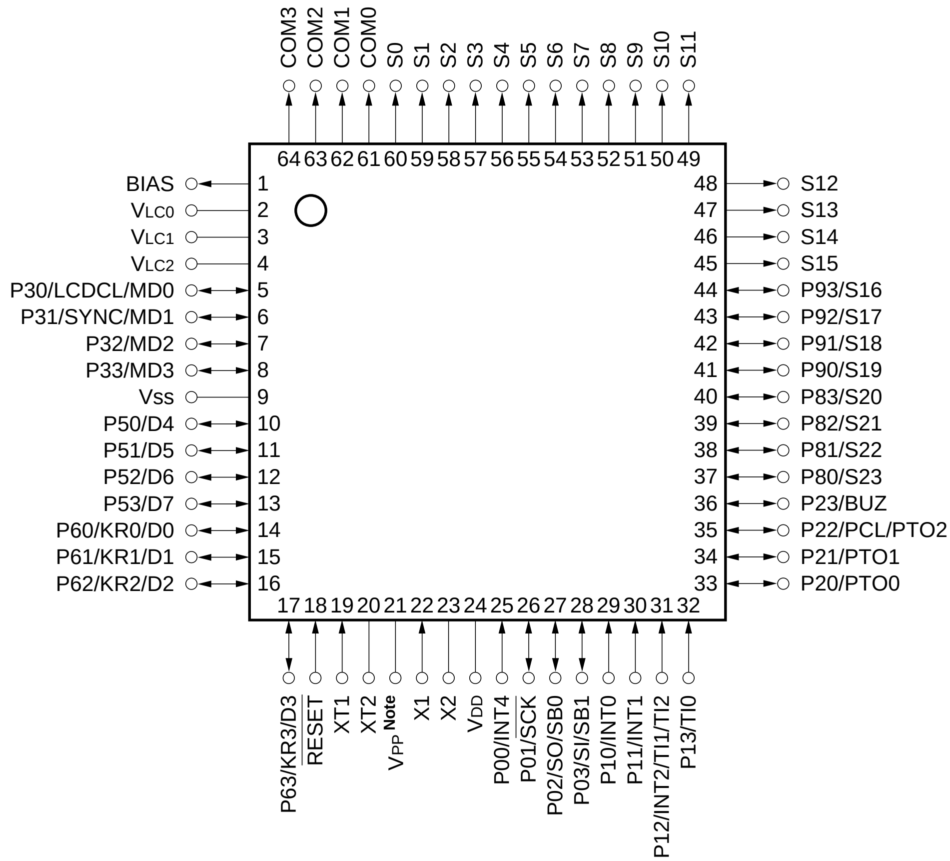
APPENDIX A. LIST OF μPD75308B, 753108, AND 75P3116 FUNCTIONS ... 54

APPENDIX B. DEVELOPMENT TOOLS ... 56

APPENDIX C. RELATED DOCUMENTS ... 65

## 1. PIN CONFIGURATION (TOP VIEW)

- 64-pin plastic QFP (14 × 14): μPD75P3116GC-AB8
- 64-pin plastic LQFP (12 × 12): μPD75P3116GK-8A8
- ★ 64-pin plastic LQFP (14 × 14): μPD75P3116GC-8BS

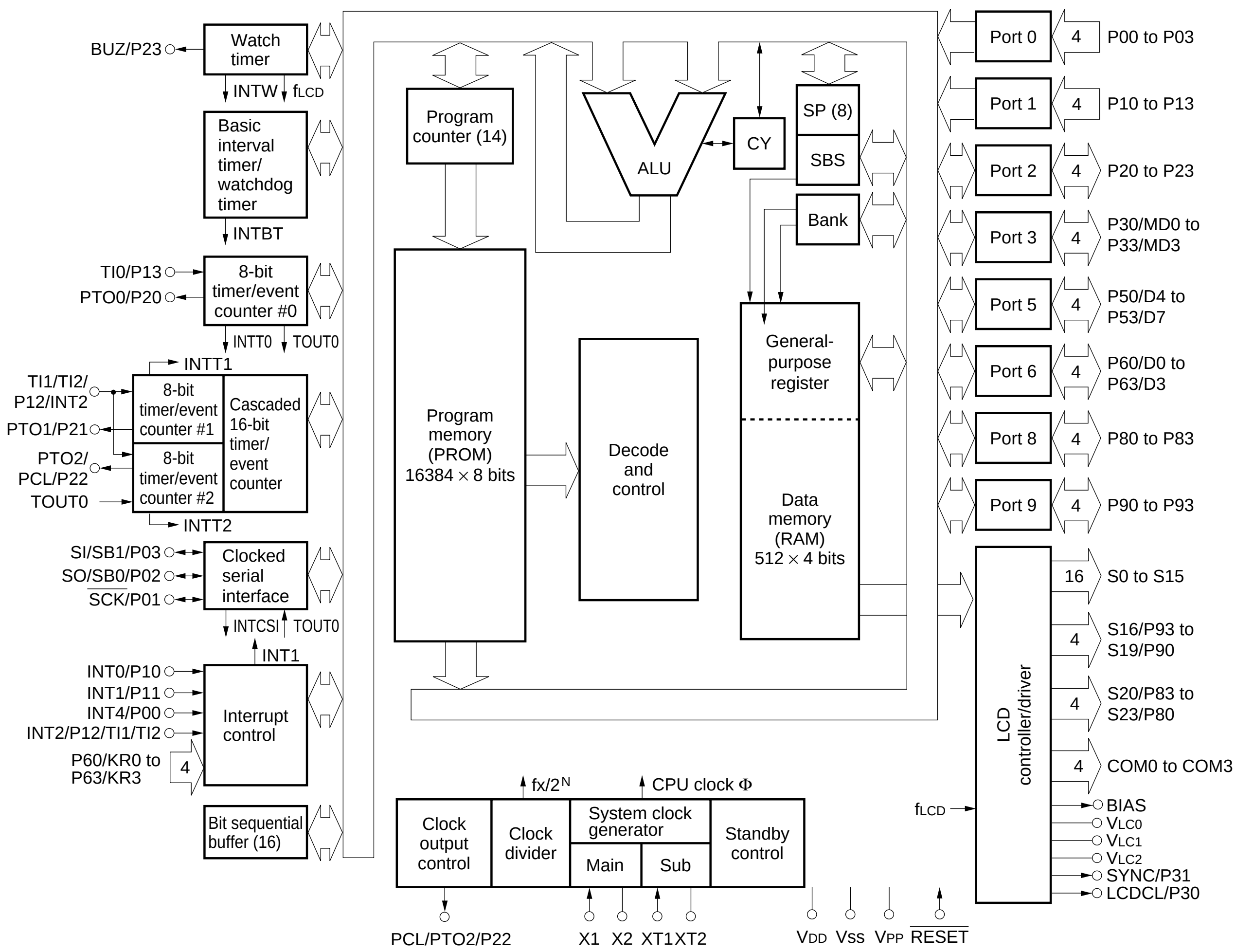



**Note** Always connect the $V_{PP}$ pin directly to $V_{DD}$ during normal operation.

## PIN IDENTIFICATIONS

| | | | |
|---|---|---|---|
| P00 to P03: | Port 0 | COM0 to COM3: | Common output 0 to 3 |
| P10 to P13: | Port 1 | $V_{LC0}$ to $V_{LC2}$: | LCD power supply 0 to 2 |
| P20 to P23: | Port 2 | BIAS: | LCD power supply bias control |
| P30 to P33: | Port 3 | LCDCL: | LCD clock |
| P50 to P53: | Port 5 | SYNC: | LCD synchronization |
| P60 to P63: | Port 6 | TI0 to TI2: | Timer input 0 to 2 |
| P80 to P83: | Port 8 | PTO0 to PTO2: | Programmable timer output 0 to 2 |
| P90 to P93: | Port 9 | BUZ: | Buzzer clock |
| KR0 to KR3: | Key return 0 to 3 | PCL: | Programmable clock |
| $\overline{SCK}$: | Serial clock | INT0, 1, 4: | External vectored interrupt 0, 1, 4 |
| SI: | Serial input | INT2: | External test input 2 |
| SO: | Serial output | X1, X2: | Main system clock oscillation 1, 2 |
| SB0, SB1: | Serial data bus 0, 1 | XT1, XT2: | Subsystem clock oscillation 1, 2 |
| $\overline{RESET}$: | Reset | $V_{PP}$: | Programming power supply |
| MD0 to MD3: | Mode selection 0 to 3 | $V_{DD}$: | Positive power supply |
| D0 to D7: | Data bus 0 to 7 | Vss: | Ground |
| S0 to S23: | Segment output 0 to 23 | | |

## 2. BLOCK DIAGRAM



## 3. PIN FUNCTIONS

### 3.1 Port Pins (1/2)

| Pin Name | I/O | Alternate Function | Function | 8-Bit I/O | Status After Reset | I/O Circuit Type Note 1 |
|---|---|---|---|---|---|---|
| P00 | Input | INT4 | 4-bit input port (Port 0) Connection of an internal pull-up resistor can be specified by a software setting in 3-bit units. | — | Input | <B> |
| ★ P01 | | $\overline{SCK}$ | | | | <F>-A |
| ★ P02 | | SO/SB0 | | | | <F>-B |
| ★ P03 | | SI/SB1 | | | | <M>-C |
| P10 | Input | INT0 | 4-bit input port (Port 1) Connection of an internal pull-up resistor can be specified by a software setting in 4-bit units. P10/INT0 can be used to select a noise eliminator. | — | Input | <B>-C |
| P11 | | INT1 | | | | |
| P12 | | TI1/TI2/INT2 | | | | |
| P13 | | TI0 | | | | |
| P20 | I/O | PTO0 | 4-bit I/O port (Port 2) Connection of an internal pull-up resistor can be specified by a software setting in 4-bit units. | — | Input | E-B |
| P21 | | PTO1 | | | | |
| P22 | | PCL/PTO2 | | | | |
| P23 | | BUZ | | | | |
| P30 | I/O | LCDCL/MD0 | Programmable 4-bit I/O port (Port 3) Input and output can be specified in 1-bit units. Connection of an internal pull-up resistor can be specified by a software setting in 4-bit units. | — | Input | E-B |
| P31 | | SYNC/MD1 | | | | |
| P32 | | MD2 | | | | |
| P33 | | MD3 | | | | |
| P50 Note 2 | I/O | D4 | N-ch open-drain 4-bit I/O port (Port 5) When set to open-drain, the withstanding voltage is 13 V. | — | High impedance | M-E |
| P51 Note 2 | | D5 | | | | |
| P52 Note 2 | | D6 | | | | |
| P53 Note 2 | | D7 | | | | |

**Notes 1.** Circuit types enclosed in angle brackets indicate Schmitt-triggered input.

**2.** The low-level input leakage current increases when input instructions or bit manipulation instructions are executed.

### 3.1 Port Pins (2/2)

| Pin Name | I/O | Alternate Function | Function | 8-Bit I/O | Status After Reset | I/O Circuit Type[Note 1] |
|---|---|---|---|---|---|---|
| P60 | I/O | KR0/D0 | Programmable 4-bit I/O port (Port 6)<br>Input and output can be specified in 1-bit units.<br>Connection of an internal pull-up resistor can be specified by a software setting in 4-bit units. | — | Input | <F>-A |
| P61 | | KR1/D1 | | | | |
| P62 | | KR2/D2 | | | | |
| P63 | | KR3/D3 | | | | |
| P80 | I/O | S23 | 4-bit I/O port (Port 8)<br>Connection of an internal pull-up resistor can be specified by a software setting in 4-bit units[Note 2]. | √ | Input | H |
| P81 | | S22 | | | | |
| P82 | | S21 | | | | |
| P83 | | S20 | | | | |
| P90 | I/O | S19 | Programmable 4-bit I/O port (Port 9)<br>Connection of an internal pull-up resistor can be specified by a software setting in 4-bit units[Note 2]. | | Input | H |
| P91 | | S18 | | | | |
| P92 | | S17 | | | | |
| P93 | | S16 | | | | |

**Notes 1.** Circuit types enclosed in angle brackets indicate Schmitt-triggered input.

**2.** Do not connect an internal pull-up resistor by software when these pins are used as segment signal outputs.

### 3.2 Non-Port Pins (1/2)

| Pin Name | I/O | Alternate Function | Function | | Status After Reset | I/O Circuit Type[Note 1] |
|---|---|---|---|---|---|---|
| TI0 | Input | P13 | External event pulse input to timer/event counter | | Input | <B>-C |
| TI1 | | P12/INT2/TI2 | | | | |
| TI2 | | P12/INT2/TI1 | | | | |
| PTO0 | Output | P20 | Timer/event counter output | | Input | E-B |
| PTO1 | | P21 | | | | |
| PTO2 | | P22/PCL | | | | |
| PCL | | P22/PTO2 | Clock output | | | |
| BUZ | | P23 | Frequency output (for buzzer or system clock trimming) | | | |
| $\overline{SCK}$ | I/O | P01 | Serial clock I/O | | Input | <F>-A |
| SO/SB0 | | P02 | Serial data output<br>Serial data bus I/O | | | <F>-B |
| SI/SB1 | | P03 | Serial data input<br>Serial data bus I/O | | | <M>-C |
| INT4 | Input | P00 | Edge detection vectored interrupt input<br>(valid for detecting both rising and falling edges) | | | <B> |
| INT0 | Input | P10 | Edge detection vectored interrupt input (detection edge is selectable) INT0/P10 can be used to select a noise eliminator. | With noise eliminator/ asynchronous is selectable | Input | <B>-C |
| INT1 | | P11 | | Asynchronous | | |
| INT2 | Input | P12/TI1/TI2 | Rising edge detection testable input | Asynchronous | | |
| KR0 to KR3 | I/O | P60 to P63 | Parallel falling edge detection testable input | | Input | <F>-A |
| X1 | Input | — | Ceramic/crystal resonator connection for main system clock oscillation. If using an external clock, input the signal to X1 and input the inverted signal to X2. | | — | — |
| X2 | — | | | | | |
| XT1 | Input | — | Crystal resonator connection for subsystem clock oscillation. If using an external clock, input the signal to XT1 and input the inverted signal to XT2. XT1 can be used as a 1-bit (test) input. | | — | — |
| XT2 | — | | | | | |
| $\overline{RESET}$ | Input | — | System reset input (low-level active) | | — | <B> |
| MD0 to MD3 | Input | P30 to P33 | Mode selection for program memory (PROM) write/verify | | Input | E-B |
| D0 to D3 | I/O | P60/KR0 to P63/KR3 | Data bus for program memory (PROM) write/verify | | Input | <F>-A |
| D4 to D7 | | P50 to P53 | | | | M-E |
| $V_{PP}$[Note 2] | — | — | Programmable power supply voltage applied for program memory (PROM) write/verify.<br>During normal operation, connect directly to $V_{DD}$.<br>Apply +12.5 V for PROM write/verify. | | — | — |
| $V_{DD}$ | — | — | Positive power supply | | — | — |
| Vss | — | — | Ground potential | | — | — |

**Notes 1.** Circuit types enclosed in angle brackets indicate Schmitt-triggered input.

**2.** The $V_{PP}$ pin does not operate correctly when it is not connected to the $V_{DD}$ pin during normal operation.

### 3.2 Non-Port Pins (2/2)

| Pin Name | I/O | Alternate Function | Function | Status After Reset | I/O Circuit Type |
|---|---|---|---|---|---|
| S0 to S15 | Output | — | Segment signal output | **Note 1** | G-A |
| S16 to S19 | Output | P93 to P90 | Segment signal output | Input | H |
| S20 to S23 | Output | P83 to P80 | Segment signal output | Input | H |
| COM0 to COM3 | Output | — | Common signal output | **Note 1** | G-B |
| $V_{LC0}$ to $V_{LC2}$ | — | — | Power supply for driving LCD | — | — |
| BIAS | Output | — | Output for external split resistor cut | **Note 2** | — |
| LCDCL[Note 3] | Output | P30/MD0 | Clock output for driving external expansion driver | Input | E-B |
| SYNC[Note 3] | Output | P31/MD1 | Clock output for synchronization of external expansion driver | Input | E-B |

**Notes 1.** $V_{LCX}$ (X = 0, 1, 2) is selected as the input source for the display outputs as shown below.
S0 to S23: $V_{LC1}$, COM0 to COM2: $V_{LC2}$, COM3: $V_{LC0}$

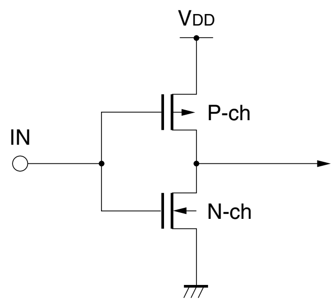
**2.** When the split resistor is incorporated: Low level
When the split resistor is not incorporated: High impedance

**3.** These pins are provided for future system expansion. Currently, only P30 and P31 are used.

### 3.3 Pin I/O Circuits

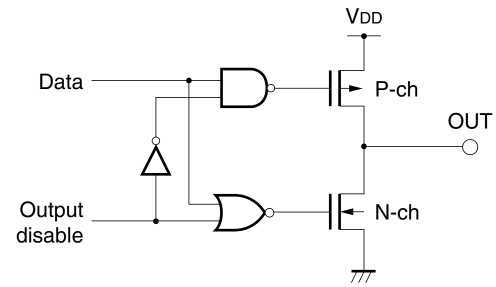
The I/O circuits for the μPD75P3116's pins are shown in abbreviated form below.

**Type A**



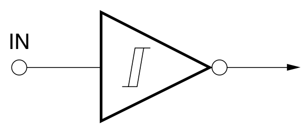

CMOS standard input buffer

**Type D**



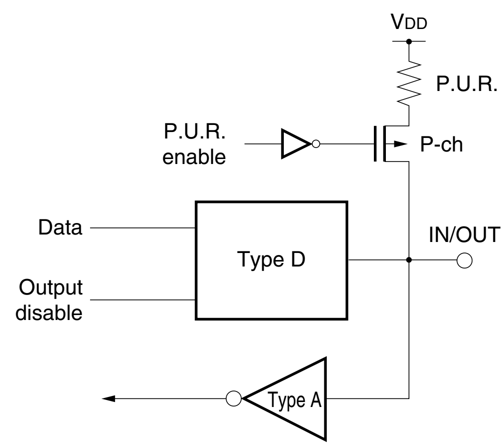

Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

**Type B**



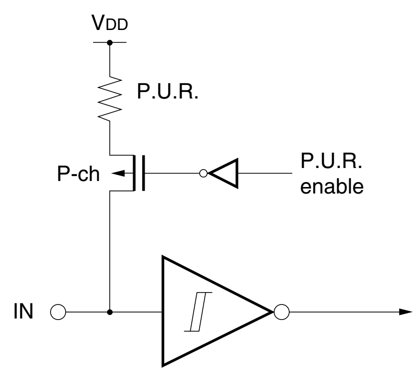

Schmitt-triggered input with hysteresis characteristics.

**Type E-B**



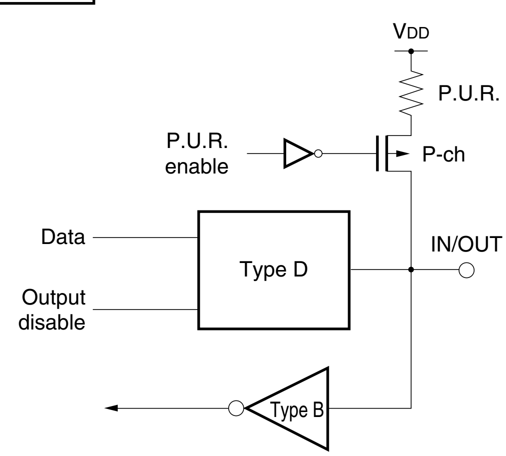

P.U.R. : Pull-Up Resistor

**Type B-C**




P.U.R. : Pull-Up Resistor

**Type F-A**

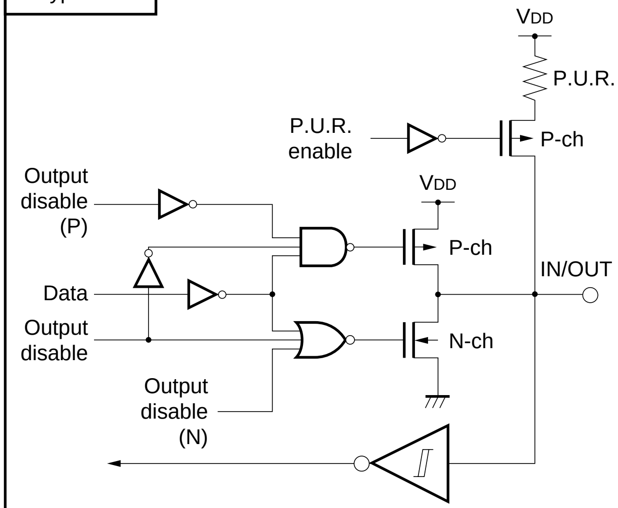



P.U.R. : Pull-Up Resistor

(Continued)

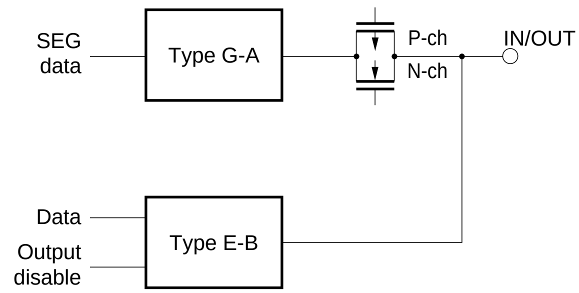
(Continued)

Type F-B

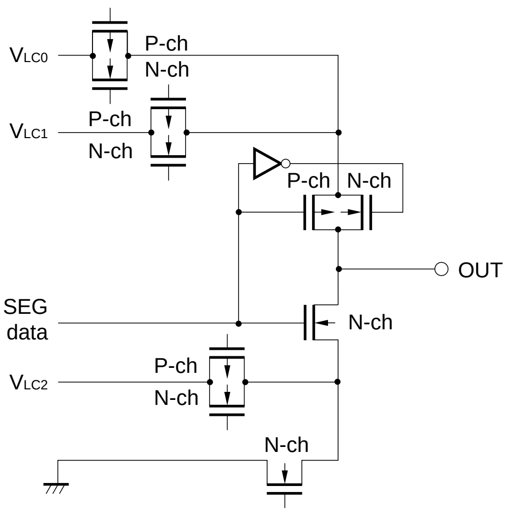



P.U.R. : Pull-Up Resistor

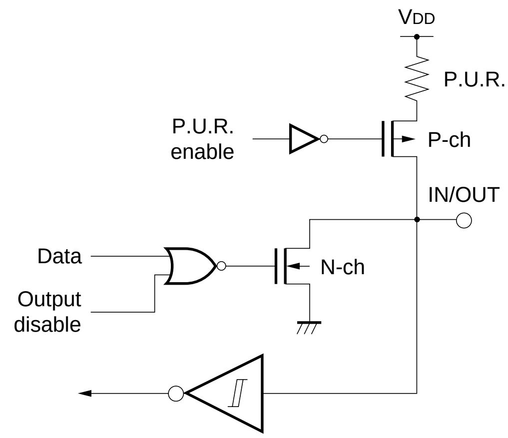
Type H




Type G-A

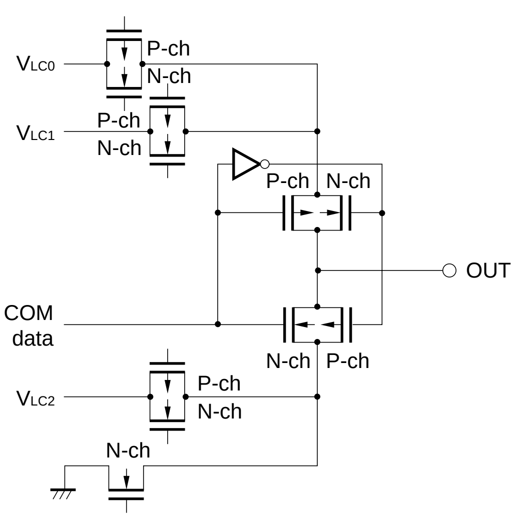



Type M-C

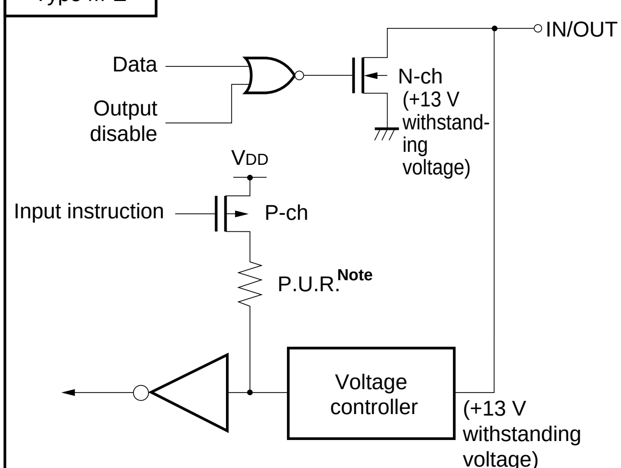



P.U.R. : Pull-Up Resistor

Type G-B




Type M-E




**Note** Pull-up resistor that operates only when an input instruction is executed. (The current flows from $V_{DD}$ to a pin when the pin is at low level.)

### 3.4 Recommended Connection of Unused Pins

★ **Table 3-1. List of Unused Pin Connections**

| Pin | Recommended Connection |
|---|---|
| P00/INT4 | Connect to $V_{SS}$ or $V_{DD}$. |
| P01/$\overline{SCK}$ | Input: Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor. |
| P02/SO/SB0 | Output: Leave open. |
| P03/SI/SB1 | Connect to $V_{SS}$. |
| P10/INT0 and P11/INT1 | Connect to $V_{SS}$ or $V_{DD}$. |
| P12/TI1/TI2/INT2 | |
| P13/TI0 | |
| P20/PTO0 | Input: Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor. |
| P21/PTO1 | Output: Leave open. |
| P22/PTO2/PCL | |
| P23/BUZ | |
| P30/LCDCL/MD0 | |
| P31/SYNC/MD1 | |
| P32/MD2 | |
| P33/MD3 | |
| P50/D4 to P53/D7 | Input: Connect to $V_{SS}$.<br>Output: Connect to $V_{SS}$. |
| P60/KR0/D0 to P63/KR3/D3 | Input: Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor.<br>Output: Leave open. |
| S0 to S15 | Leave open. |
| COM0 to COM3 | |
| S16/P93 to S19/P90 | Input: Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor. |
| S20/P83 to S23/P80 | Output: Leave open. |
| $V_{LC0}$ to $V_{LC2}$ | Connect to $V_{SS}$. |
| BIAS | Connect to $V_{SS}$ only when none of $V_{LC0}$, $V_{LC1}$ or $V_{LC2}$ is used.<br>In other cases, leave open. |
| XT1 Note | Connect to $V_{SS}$. |
| XT2 Note | Leave open. |
| $V_{PP}$ | Always connect to $V_{DD}$ directly. |

**Note** When the subsystem clock is not used, select SOS.0 = 1 (on-chip feedback resistor not used).

## 4. Mk I AND Mk II MODE SELECTION FUNCTION

Setting the stack bank selection (SBS) register for the μPD75P3116 enables the program memory to be switched between the Mk I mode and Mk II mode. This function is applicable when using the μPD75P3116 to evaluate the μPD753104, 753106, or 753108.

When bit 3 of SBS is set to 1: Sets the Mk I mode (supports the Mk I mode for the μPD753104, 753106, and 753108)
When bit 3 of SBS is set to 0: Sets the Mk II mode (supports the Mk II mode for the μPD753104, 753106, and 753108)

### 4.1 Differences Between Mk I Mode and Mk II Mode

Table 4-1 lists the differences between the Mk I mode and the Mk II mode for the μPD75P3116.

**Table 4-1. Differences Between Mk I Mode and Mk II Mode**

| Item | | Mk I Mode | Mk II Mode |
|---|---|---|---|
| Program counter | | $PC_{13-0}$ | |
| Program memory (bytes) | | 16384 | |
| Data memory (bits) | | 512 × 4 | |
| Stack | Stack bank | Selectable via memory banks 0 and 1 | |
| | No. of stack bytes | 2 bytes | 3 bytes |
| Instruction | BRA !addr1 instruction<br>CALLA !addr1 instruction | Not available | Available |
| Instruction execution time | CALL !addr instruction | 3 machine cycles | 4 machine cycles |
| | CALLF !faddr instruction | 2 machine cycles | 3 machine cycles |
| Supported mask ROM products | | When set to Mk I mode:<br>μPD753104, 753106, and 753108 | When set to Mk II mode:<br>μPD753104, 753106, and 753108 |

**Caution The Mk II mode supports a program area exceeding 16 KB for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 KB.**
**With regard to the number of stack bytes during execution of subroutine call instructions, the usable area increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected.**
**However, when the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.**

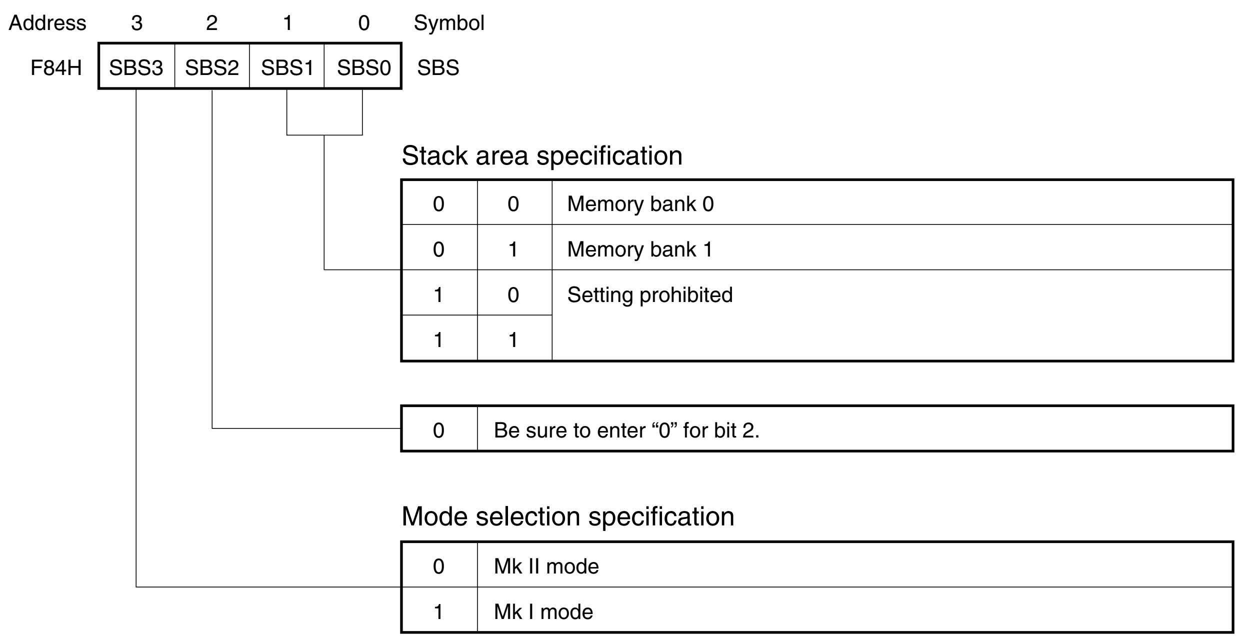
### 4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between the Mk I mode and Mk II mode. Figure 4-1 shows the format of the stack bank selection register.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 100×B[Note] at the beginning of the program. When using the Mk II mode, be sure to initialize it to 000×B[Note].

**Note** Set the desired value for ×.

**Figure 4-1. Format of Stack Bank Selection Register**




**Caution SBS3 is set to 1 after $\overline{\text{RESET}}$ input, and consequently the CPU operates in the Mk I mode. When using instructions for the Mk II mode, set SBS3 to 0 and set the Mk II mode before using the instructions.**

## 5. DIFFERENCES BETWEEN μPD75P3116 AND μPD753104, 753106, 753108

The μPD75P3116 replaces the internal mask ROM in the μPD753104, 753106, and 753108 with a one-time PROM and features expanded ROM capacity. The μPD75P3116's Mk I mode supports the Mk I mode in the μPD753104, 753106, and 753108 and the μPD75P3116's Mk II mode supports the Mk II mode in the μPD753104, 753106, and 753108.

Table 5-1 lists differences between the μPD75P3116 and the μPD753104, 753106, and 753108. Be sure to check the differences between these products before using them with PROMs for debugging or prototype testing of application systems or, later, when using them with a mask ROM for full-scale production.

For details of the CPU functions and internal hardware, refer to the **User's Manual**.

**Table 5-1. Differences Between μPD75P3116 and μPD753104, 753106, and 753108**

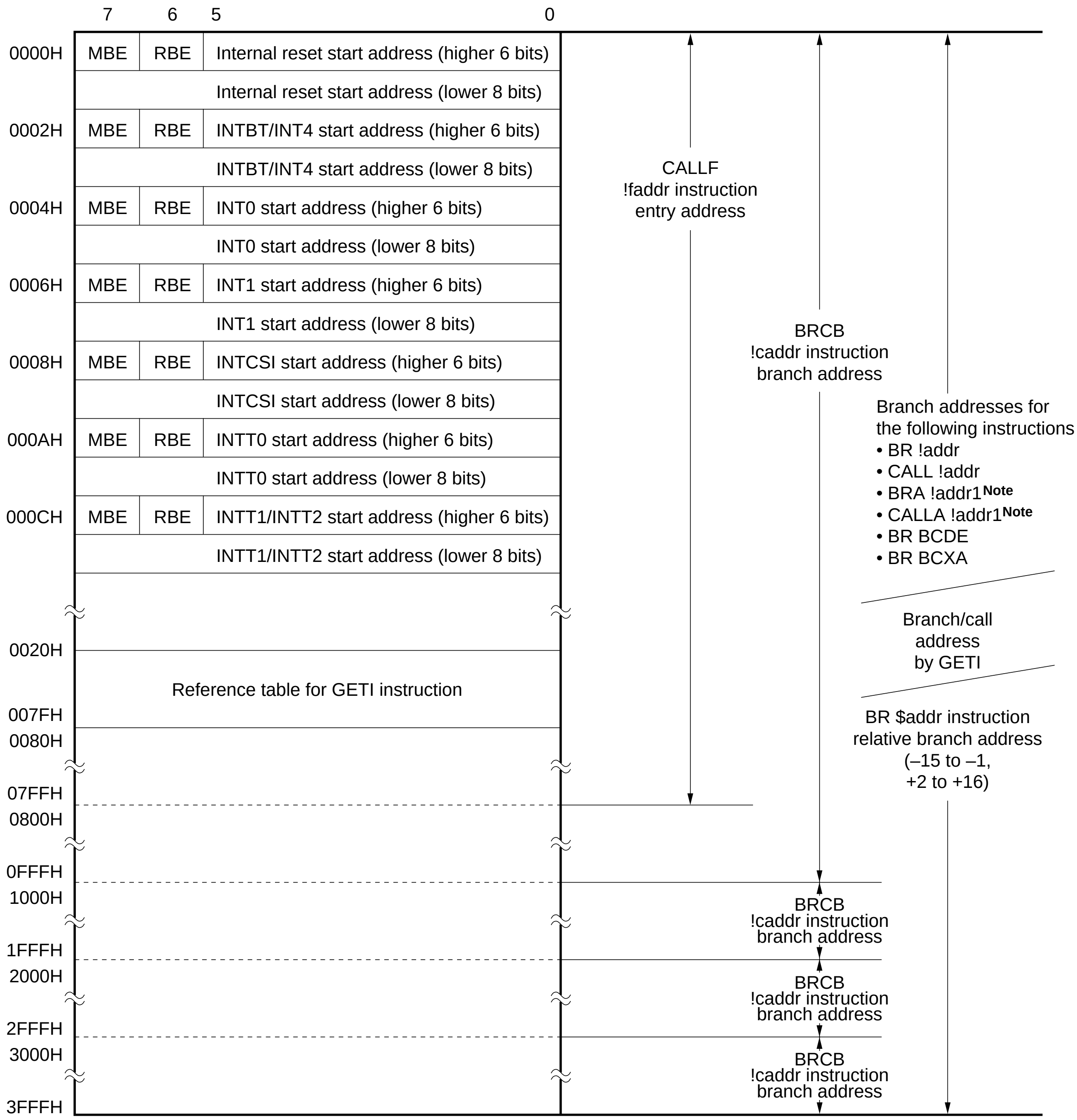
| Item | | μPD753104 | μPD753106 | μPD753108 | μPD75P3116 |
|---|---|---|---|---|---|
| Program counter | | 12 bits | 13 bits | | 14 bits |
| Program memory (bytes) | | Mask ROM 4096 | Mask ROM 6144 | Mask ROM 8192 | One-time PROM 16384 |
| Data memory (× 4 bits) | | 512 | | | |
| Mask options | Pull-up resistor for Port 5 | Available (On chip/not on chip can be specified.) | | | Not available (Not on chip) |
| | Split resistor for LCD driving power supply | | | | |
| | Wait time after $\overline{\text{RESET}}$ | Available (Selectable between $2^{17}$/fx and $2^{15}$/fx)Note | | | Not available (Fixed to $2^{15}$/fx)Note |
| | Feedback resistor of subsystem clock | Available (Use/not use can be selected.) | | | Not available (Enable) |
| Pin configuration | Pins 5 to 8 | P30 to P33 | | | P30/MD0 to P33/MD3 |
| | Pins 10 to 13 | P50 to P53 | | | P50/D4 to P53/D7 |
| | Pins 14 to 17 | P60/KR0 to P63/KR3 | | | P60/KR0/D0 to P63/KR3/D3 |
| | Pin 21 | IC | | | $V_{PP}$ |
| Other | | Noise resistance and noise radiation may differ due to the different circuit sizes and mask layouts. | | | |

**Note** $2^{17}$/fx: 21.8 ms at 6.0 MHz operation, 31.3 ms at 4.19 MHz operation
$2^{15}$/fx: 5.46 ms at 6.0 MHz operation, 7.81 ms at 4.19 MHz operation

**Caution There are differences in the amount of noise tolerance and noise radiation between flash memory versions and mask ROM versions. When considering changing from a flash memory version to a mask ROM version during the process from experimental manufacturing to mass production, make sure to sufficiently evaluate commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.**

## 6. MEMORY CONFIGURATION

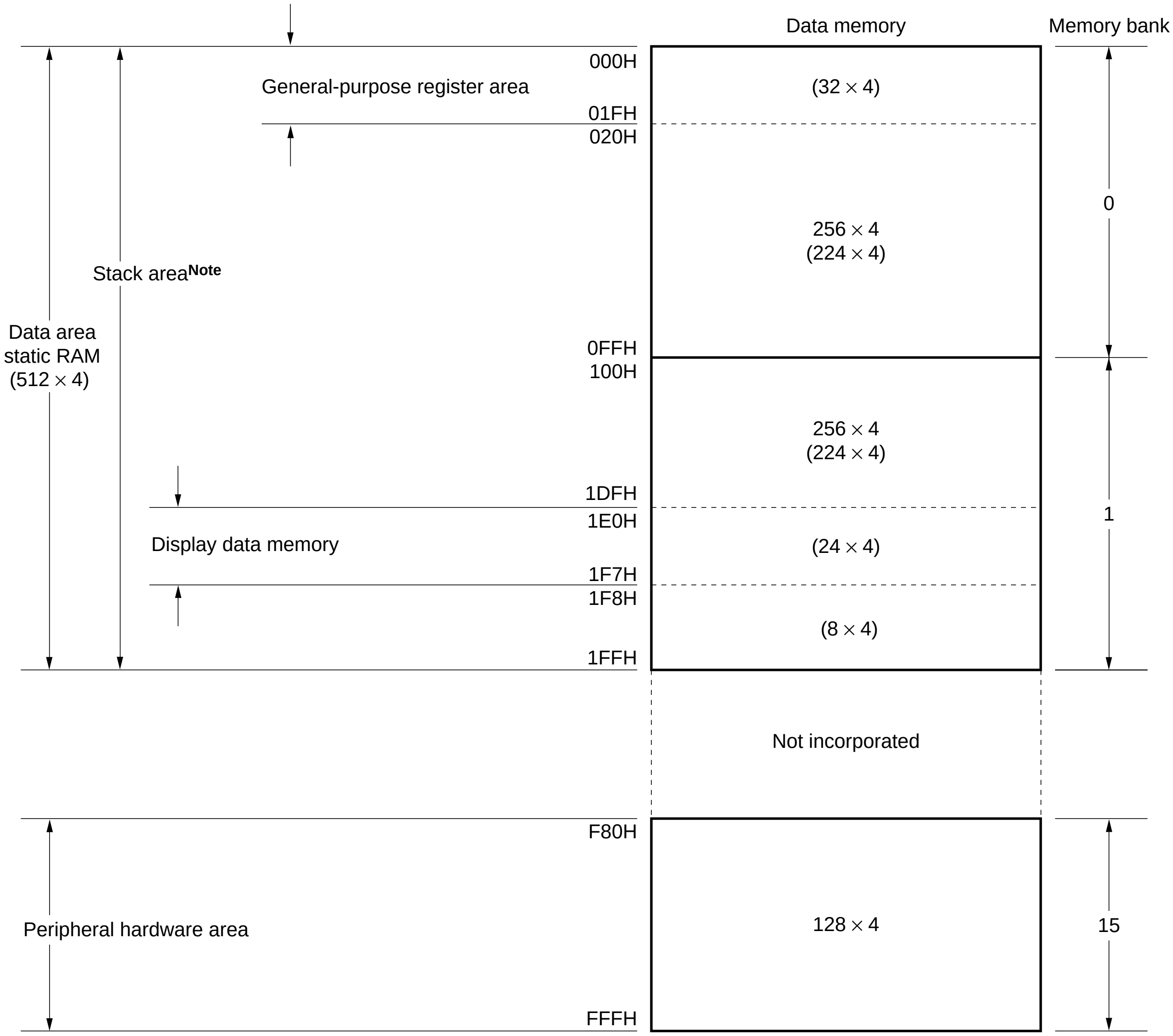
**Figure 6-1. Program Memory Map**




**Note** Can only be used in the Mk II mode.

**Remark** For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's lower 8 bits only.

**Figure 6-2. Data Memory Map**




**Note** Memory bank 0 or 1 can be selected as the stack area.

## 7. INSTRUCTION SET

### (1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further details, refer to the **RA75X Assembler Package Language User's Manual (U12385E)**). When there are several codes, select and use just one. Codes that consist of uppercase letters and + or – symbols are keywords that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Enter register flag symbols as label descriptors instead of mem, fmem, pmem, bit, etc. (for further details, refer to the **User's Manual**). The number of labels that can be entered for fmem and pmem are restricted.

| Representation | Coding Format |
|---|---|
| reg | X, A, B, C, D, E, H, L |
| reg1 | X, B, C, D, E, H, L |
| rp | XA, BC, DE, HL |
| rp1 | BC, DE, HL |
| rp2 | BC, DE |
| rp' | XA, BC, DE, HL, XA', BC', DE', HL' |
| rp'1 | BC, DE, HL, XA', BC', DE', HL' |
| rpa | HL, HL+, HL–, DE, DL |
| rpa1 | DE, DL |
| n4 | 4-bit immediate data or label |
| n8 | 8-bit immediate data or label |
| mem | 8-bit immediate data or label[Note] |
| bit | 2-bit immediate data or label |
| fmem | FB0H to FBFH, FF0H to FFFH immediate data or label |
| pmem | FC0H to FFFH immediate data or label |
| addr | 0000H to 3FFFH immediate data or label |
| addr1 | 0000H to 3FFFH immediate data or label (Mk II mode only) |
| caddr | 12-bit immediate data or label |
| faddr | 11-bit immediate data or label |
| taddr | 20H to 7FH immediate data (however, bit 0 = 0) or label |
| PORTn | Port 0 to Port 3, Port 5, Port 6, Port 8, Port 9 |
| IE××× | IEBT, IECSI, IET0 to IET2, IE0 to IE2, IE4, IEW |
| RBn | RB0 to RB3 |
| MBn | MB0, MB1, MB15 |

**Note** When processing 8-bit data, only even-numbered addresses can be specified.

**(2) Operation conventions**

| | |
|---|---|
| A: | A register; 4-bit accumulator |
| B: | B register |
| C: | C register |
| D: | D register |
| E: | E register |
| H: | H register |
| L: | L register |
| X: | X register |
| XA: | Register pair (XA); 8-bit accumulator |
| BC: | Register pair (BC) |
| DE: | Register pair (DE) |
| HL: | Register pair (HL) |
| XA’: | Expansion register pair (XA’) |
| BC’: | Expansion register pair (BC’) |
| DE’: | Expansion register pair (DE’) |
| HL’: | Expansion register pair (HL’) |
| PC: | Program counter |
| SP: | Stack pointer |
| CY: | Carry flag; bit accumulator |
| PSW: | Program status word |
| MBE: | Memory bank enable flag |
| RBE: | Register bank enable flag |
| PORTn: | Port n (n = 0 to 3, 5, 6, 8, 9) |
| IME: | Interrupt master enable flag |
| IPS: | Interrupt priority selection register |
| IE×××: | Interrupt enable flag |
| RBS: | Register bank selection register |
| MBS: | Memory bank selection register |
| PCC: | Processor clock control register |
| .: | Delimiter for address and bit |
| (××): | Data addressed with ×× |
| ××H: | Hexadecimal data |

### (3) Description of symbols used in addressing area

| | | |
|---|---|---|
| *1 | MB = MBE • MBS<br>MBS = 0, 1, 15 | Data memory addressing |
| *2 | MB = 0 | |
| *3 | MBE = 0: MB = 0 (000H to 07FH)<br>MB = 15 (F80H to FFFH)<br>MBE = 1: MB = MBS<br>MBS = 0, 1, 15 | |
| *4 | MB = 15, fmem = FB0H to FBFH, FF0H to FFFH | |
| *5 | MB = 15, pmem = FC0H to FFFH | |
| *6 | addr = 0000H to 3FFFH | Program memory addressing |
| *7 | addr, addr1 = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 | |
| *8 | caddr = 0000H to 0FFFH ($PC_{13, 12}$ = 00B) or<br>1000H to 1FFFH ($PC_{13, 12}$ = 01B) or<br>2000H to 2FFFH ($PC_{13, 12}$ = 10B) or<br>3000H to 3FFFH ($PC_{13, 12}$ = 11B) | |
| *9 | faddr = 0000H to 07FFH | |
| *10 | taddr = 0020H to 007FH | |
| *11 | addr1 = 0000H to 3FFFH (Mk II mode only) | |

**Remarks 1.** MB indicates access-enabled memory banks.
**2.** In area *2, MB = 0 for both MBE and MBS.
**3.** In areas *4 and *5, MB = 15 for both MBE and MBS.
**4.** Areas *6 to *11 indicate corresponding address-enabled areas.

### (4) Description of machine cycles

S indicates the number of machine cycles required for skipping skip-specified instructions. The value of S varies as shown below.

- No skip ..................................................................... S = 0
- Skipped instruction is 1-byte or 2-byte instruction .... S = 1
- Skipped instruction is 3-byte instruction[Note] ............. S = 2

**Note** 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, and CALLA !addr1

**Caution The GETI instruction is skipped for one machine cycle.**

One machine cycle equals one cycle (= $t_{CY}$) of the CPU clock Φ. Use the PCC setting to select from among four cycle times.

| Instruction Group | Mnemonic | Operand | No. of Bytes | Machine Cycle | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Transfer | MOV | A, #n4 | 1 | 1 | A ← n4 | | String-effect A |
| | | reg1, #n4 | 2 | 2 | reg1 ← n4 | | |
| | | XA, #n8 | 2 | 2 | XA ← n8 | | String-effect A |
| | | HL, #n8 | 2 | 2 | HL ← n8 | | String-effect B |
| | | rp2, #n8 | 2 | 2 | rp2 ← n8 | | |
| | | A, @HL | 1 | 1 | A ← (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A ← (HL), then L ← L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A ← (HL), then L ← L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ← (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ← (HL) | *1 | |
| | | @HL, A | 1 | 1 | (HL) ← A | *1 | |
| | | @HL, XA | 2 | 2 | (HL) ← XA | *1 | |
| | | A, mem | 2 | 2 | A ← (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ← (mem) | *3 | |
| | | mem, A | 2 | 2 | (mem) ← A | *3 | |
| | | mem, XA | 2 | 2 | (mem) ← XA | *3 | |
| | | A, reg | 2 | 2 | A ← reg | | |
| | | XA, rp' | 2 | 2 | XA ← rp' | | |
| | | reg1, A | 2 | 2 | reg1 ← A | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← XA | | |
| | XCH | A, @HL | 1 | 1 | A ←→ (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A ←→ (HL), then L ← L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A ←→ (HL), then L ← L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ←→ (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ←→ (HL) | *1 | |
| | | A, mem | 2 | 2 | A ←→ (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ←→ (mem) | *3 | |
| | | A, reg1 | 1 | 1 | A ←→ reg1 | | |
| | | XA, rp' | 2 | 2 | XA ←→ rp' | | |
| Table reference | MOVT | XA, @PCDE | 1 | 3 | XA ← $(PC_{13\text{-}8}+DE)_{ROM}$ | | |
| | | XA, @PCXA | 1 | 3 | XA ← $(PC_{13\text{-}8}+XA)_{ROM}$ | | |
| | | XA, @BCDE Note | 1 | 3 | XA ← $(BCDE)_{ROM}$ | *6 | |
| | | XA, @BCXA Note | 1 | 3 | XA ← $(BCXA)_{ROM}$ | *6 | |

**Note** Only the lower 3 bits in the B register are valid.

| Instruction Group | Mnemonic | Operand | No. of Bytes | Machine Cycle | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Bit transfer | MOV1 | CY, fmem.bit | 2 | 2 | CY ← (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← ($pmem_{7-2}$+$L_{3-2}$.bit($L_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← (H+$mem_{3-0}$.bit) | *1 | |
| | | fmem.bit, CY | 2 | 2 | (fmem.bit) ← CY | *4 | |
| | | pmem.@L, CY | 2 | 2 | ($pmem_{7-2}$+$L_{3-2}$.bit($L_{1-0}$)) ← CY | *5 | |
| | | @H+mem.bit, CY | 2 | 2 | (H+$mem_{3-0}$.bit) ← CY | *1 | |
| Arithmetic | ADDS | A, #n4 | 1 | 1+S | A ← A+n4 | | carry |
| | | XA, #n8 | 2 | 2+S | XA ← XA+n8 | | carry |
| | | A, @HL | 1 | 1+S | A ← A+(HL) | *1 | carry |
| | | XA, rp' | 2 | 2+S | XA ← XA+rp' | | carry |
| | | rp'1, XA | 2 | 2+S | rp'1 ← rp'1+XA | | carry |
| | ADDC | A, @HL | 1 | 1 | A, CY ← A+(HL)+CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA+rp'+CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1+XA+CY | | |
| | SUBS | A, @HL | 1 | 1+S | A ← A–(HL) | *1 | borrow |
| | | XA, rp' | 2 | 2+S | XA ← XA–rp' | | borrow |
| | | rp'1, XA | 2 | 2+S | rp'1 ← rp'1–XA | | borrow |
| | SUBC | A, @HL | 1 | 1 | A, CY ← A–(HL)–CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA–rp'–CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1–XA–CY | | |
| | AND | A, #n4 | 2 | 2 | A ← A ∧ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∧ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∧ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∧ XA | | |
| | OR | A, #n4 | 2 | 2 | A ← A ∨ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∨ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∨ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∨ XA | | |
| | XOR | A, #n4 | 2 | 2 | A ← A ⩛ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ⩛ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ⩛ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ⩛ XA | | |
| Accumulator manipulation | RORC | A | 1 | 1 | CY ← $A_0$, $A_3$ ← CY, $A_{n-1}$ ← $A_n$ | | |
| | NOT | A | 2 | 2 | A ← $\overline{A}$ | | |
| Increment/ decrement | INCS | reg | 1 | 1+S | reg ← reg+1 | | reg = 0 |
| | | rp1 | 1 | 1+S | rp1 ← rp1+1 | | rp1 = 00H |
| | | @HL | 2 | 2+S | (HL) ← (HL)+1 | *1 | (HL) = 0 |
| | | mem | 2 | 2+S | (mem) ← (mem)+1 | *3 | (mem) = 0 |
| | DECS | reg | 1 | 1+S | reg ← reg–1 | | reg = FH |
| | | rp' | 2 | 2+S | rp' ← rp'–1 | | rp' = FFH |

| Instruction Group | Mnemonic | Operand | No. of Bytes | Machine Cycle | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Comparison | SKE | reg, #n4 | 2 | 2+S | Skip if reg=n4 | | reg = n4 |
| | | @HL, #n4 | 2 | 2+S | Skip if (HL)=n4 | *1 | (HL) = n4 |
| | | A, @HL | 1 | 1+S | Skip if A=(HL) | *1 | A = (HL) |
| | | XA, @HL | 2 | 2+S | Skip if XA=(HL) | *1 | XA = (HL) |
| | | A, reg | 2 | 2+S | Skip if A=reg | | A = reg |
| | | XA, rp' | 2 | 2+S | Skip if XA=rp' | | XA = rp' |
| Carry flag manipulation | SET1 | CY | 1 | 1 | CY ← 1 | | |
| | CLR1 | CY | 1 | 1 | CY ← 0 | | |
| | SKT | CY | 1 | 1+S | Skip if CY=1 | | CY = 1 |
| | NOT1 | CY | 1 | 1 | CY ← $\overline{CY}$ | | |
| Memory bit manipulation | SET1 | mem.bit | 2 | 2 | (mem.bit) ← 1 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 1 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 1 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) ← 1 | *1 | |
| | CLR1 | mem.bit | 2 | 2 | (mem.bit) ← 0 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 0 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 0 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) ← 0 | *1 | |
| | SKT | mem.bit | 2 | 2+S | Skip if(mem.bit)=1 | *3 | (mem.bit) = 1 |
| | | fmem.bit | 2 | 2+S | Skip if(fmem.bit)=1 | *4 | (fmem.bit) = 1 |
| | | pmem.@L | 2 | 2+S | Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 | *5 | (pmem.@L) = 1 |
| | | @H+mem.bit | 2 | 2+S | Skip if(H+mem$_{3-0}$.bit)=1 | *1 | (@H+mem.bit) = 1 |
| | SKF | mem.bit | 2 | 2+S | Skip if(mem.bit)=0 | *3 | (mem.bit) = 0 |
| | | fmem.bit | 2 | 2+S | Skip if(fmem.bit)=0 | *4 | (fmem.bit) = 0 |
| | | pmem.@L | 2 | 2+S | Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0 | *5 | (pmem.@L) = 0 |
| | | @H+mem.bit | 2 | 2+S | Skip if(H+mem$_{3-0}$.bit)=0 | *1 | (@H+mem.bit) = 0 |
| | SKTCLR | fmem.bit | 2 | 2+S | Skip if(fmem.bit)=1 and clear | *4 | (fmem.bit) = 1 |
| | | pmem.@L | 2 | 2+S | Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 and clear | *5 | (pmem.@L) = 1 |
| | | @H+mem.bit | 2 | 2+S | Skip if(H+mem$_{3-0}$.bit)=1 and clear | *1 | (@H+mem.bit) = 1 |
| | AND1 | CY, fmem.bit | 2 | 2 | CY ← CY ∧ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∧ (H+mem$_{3-0}$.bit) | *1 | |
| | OR1 | CY, fmem.bit | 2 | 2 | CY ← CY v (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY v (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY v (H+mem$_{3-0}$.bit) | *1 | |
| | XOR1 | CY, fmem.bit | 2 | 2 | CY ← CY ∀ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∀ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∀ (H+mem$_{3-0}$.bit) | *1 | |

| Instruction Group | Mnemonic | Operand | No. of Bytes | Machine Cycle | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Branch | BR[Note 1] | addr | — | — | $PC_{13-0}$ ← addr<br>(Use the assembler to select the most appropriate instruction among the following.<br>• BR !addr<br>• BRCB !caddr<br>• BR $addr) | *6 | |
| | | addr1 | — | — | $PC_{13-0}$ ← addr1<br>(Use the assembler to select the most appropriate instruction among the following.<br>• BRA !addr1<br>• BR !addr<br>• BRCB !caddr<br>• BR $addr1) | *11 | |
| | | !addr | 3 | 3 | $PC_{13-0}$ ← addr | *6 | |
| | | $addr | 1 | 2 | $PC_{13-0}$ ← addr | *7 | |
| | | $addr1 | 1 | 2 | $PC_{13-0}$ ← addr1 | | |
| | | PCDE | 2 | 3 | $PC_{13-0}$ ← $PC_{13-8}$+DE | | |
| | | PCXA | 2 | 3 | $PC_{13-0}$ ← $PC_{13-8}$+XA | | |
| | | BCDE | 2 | 3 | $PC_{13-0}$ ← BCDE[Note 2] | *6 | |
| | | BCXA | 2 | 3 | $PC_{13-0}$ ← BCXA[Note 2] | *6 | |
| | BRA[Note 1] | !addr1 | 3 | 3 | $PC_{13-0}$ ← addr1 | *11 | |
| | BRCB | !caddr | 2 | 2 | $PC_{13-0}$ ← $PC_{13, 12}$+$caddr_{11-0}$ | *8 | |

**Notes 1.** The sections in double boxes are only supported in the Mk II mode. The other sections are only supported in the MK I mode.

**2.** Only the lower two bits in the B register are valid.

| Instruction Group | Mnemonic | Operand | No. of Bytes | Machine Cycle | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | CALLA[Note] | !addr1 | 3 | 3 | (SP–6)(SP–3)(SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, $PC_{13, 12}$<br>(SP–2) ← X, X, MBE, RBE<br>$PC_{13-0}$ ← addr1, SP ← SP–6 | *11 | |
| | CALL[Note] | !addr | 3 | 3 | (SP–4)(SP–1)(SP–2) ← $PC_{11-0}$<br>(SP–3) ← MBE, RBE, $PC_{13, 12}$<br>$PC_{13-0}$ ← addr, SP ← SP–4 | *6 | |
| | | | | 4 | (SP–6)(SP–3)(SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, $PC_{13, 12}$<br>(SP–2) ← X, X, MBE, RBE<br>$PC_{13-0}$ ← addr, SP ← SP–6 | | |
| | CALLF[Note] | !faddr | 2 | 2 | (SP–4)(SP–1)(SP–2) ← $PC_{11-0}$<br>(SP–3) ← MBE, RBE, $PC_{13, 12}$<br>$PC_{13-0}$ ← 000+faddr, SP ← SP–4 | *9 | |
| | | | | 3 | (SP–6)(SP–3)(SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, $PC_{13, 12}$<br>(SP–2) ← X, X, MBE, RBE<br>$PC_{13-0}$ ← 000+faddr, SP ← SP–6 | | |
| | RET[Note] | | 1 | 3 | MBE, RBE, $PC_{13, 12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>SP ← SP+4 | | |
| | | | | | X, X, MBE, RBE ← (SP+4)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>0, 0, $PC_{13, 12}$ ← (SP+1)<br>SP ← SP+6 | | |
| | RETS[Note] | | 1 | 3+S | MBE, RBE, $PC_{13, 12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>SP ← SP+4<br>then skip unconditionally | | Unconditional |
| | | | | | X, X, MBE, RBE ← (SP+4)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>0, 0, $PC_{13, 12}$ ← (SP+1)<br>SP ← SP+6<br>then skip unconditionally | | |
| | RETI[Note] | | 1 | 3 | MBE, RBE, $PC_{13, 12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>PSW ← (SP+4)(SP+5)<br>SP ← SP+6 | | |
| | | | | | 0, 0, $PC_{13, 12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>PSW ← (SP+4)(SP+5), SP ← SP+6 | | |

**Note** The sections in double boxes are only supported in the Mk II mode. The other sections are only supported in the Mk I mode.

| Instruction Group | Mnemonic | Operand | No. of Bytes | Machine Cycle | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | PUSH | rp | 1 | 1 | (SP–1)(SP–2) ← rp, SP ← SP–2 | | |
| | | BS | 2 | 2 | (SP–1) ← MBS, (SP–2) ← RBS,<br>SP ← SP–2 | | |
| | POP | rp | 1 | 1 | rp ← (SP+1)(SP), SP ← SP+2 | | |
| | | BS | 2 | 2 | MBS ← (SP+1), RBS ← (SP), SP ← SP+2 | | |
| Interrupt control | EI | | 2 | 2 | IME(IPS.3) ← 1 | | |
| | | IE××× | 2 | 2 | IE××× ← 1 | | |
| | DI | | 2 | 2 | IME(IPS.3) ← 0 | | |
| | | IE××× | 2 | 2 | IE××× ← 0 | | |
| I/O | IN[Note 1] | A, PORTn | 2 | 2 | A ← PORTn (n=0 to 3, 5, 6, 8, 9) | | |
| | | XA, PORTn | 2 | 2 | XA ← PORTn+1, PORTn (n=8) | | |
| | OUT[Note 1] | PORTn, A | 2 | 2 | PORTn ← A (n=2 to 3, 5, 6, 8, 9) | | |
| | | PORTn, XA | 2 | 2 | PORTn+1, PORTn ← XA (n=8) | | |
| CPU control | HALT | | 2 | 2 | Set HALT Mode(PCC.2 ← 1) | | |
| | STOP | | 2 | 2 | Set STOP Mode(PCC.3 ← 1) | | |
| | NOP | | 1 | 1 | No Operation | | |
| Special | SEL | RBn | 2 | 2 | RBS ← n (n=0 to 3) | | |
| | | MBn | 2 | 2 | MBS ← n (n=0, 1, 15) | | |
| | GETI[Notes 2, 3] | taddr | 1 | 3 | • When using TBR instruction<br>$PC_{13-0}$ ← $(taddr)_{5-0}$+(taddr+1) | *10 | |
| | | | | | • When using TCALL instruction<br>(SP–4)(SP–1)(SP–2) ← $PC_{11-0}$<br>(SP–3) ← MBE, RBE, $PC_{13, 12}$<br>$PC_{13-0}$ ← $(taddr)_{5-0}$+(taddr+1)<br>SP ← SP–4 | | |
| | | | | | • When using instruction other than TBR or TCALL<br>Execute (taddr)(taddr+1) instructions | | Determined by referenced instruction |
| | | | 1 | 3 | • When using TBR instruction<br>$PC_{13-0}$ ← $(taddr)_{5-0}$+(taddr+1) | *10 | |
| | | | | 4 | • When using TCALL instruction<br>(SP–6)(SP–3)(SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, $PC_{13, 12}$<br>(SP–2) ← X, X, MBE, RBE<br>$PC_{13-0}$ ← $(taddr)_{5-0}$+(taddr+1)<br>SP ← SP–6 | | |
| | | | | 3 | • When using instruction other than TBR or TCALL<br>Execute (taddr)(taddr+1) instructions | | Determined by referenced instruction |

**Notes 1.** Setting MBE = 0 or MBE = 1, MBS = 15 is required during the execution of the IN or OUT instruction.

**2.** The TBR and TCALL instructions are assembler quasi-directives for the GETI instruction table definitions.

**3.** The sections in double boxes are only supported in the Mk II mode. The other sections are only supported in the Mk I mode.

## 8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory contained in the μPD75P3116 is a 16384 × 8-bit one-time PROM that can be electrically written one time only. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

| Pin | Function |
|---|---|
| $V_{PP}$ | Pin where program voltage is applied during program memory write/verify (usually $V_{DD}$ potential) |
| X1, X2 | Clock input pins for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin. |
| MD0 to MD3 | Operation mode selection pin for program memory write/verify |
| D0/P60 to D3/P63 (lower 4 bits)<br>D4/P50 to D7/P53 (higher 4 bits) | 8-bit data I/O pins for program memory write/verify |
| $V_{DD}$ | Pin where power supply voltage is applied. Apply 1.8 to 5.5 V in normal operation mode and +6 V for program memory write/verify. |

**Caution  Pins not used for program memory write/verify should be connected to Vss.**

### 8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the $V_{DD}$ pin and +12.5 V to the $V_{PP}$ pin, the μPD75P3116 enters the program memory write/verify mode. The following operation modes can be specified by setting pins MD0 to MD3 as shown below.

| Operation Mode Specification | | | | | | Operation Mode |
|---|---|---|---|---|---|---|
| $V_{PP}$ | $V_{DD}$ | MD0 | MD1 | MD2 | MD3 | |
| +12.5 V | +6 V | H | L | H | L | Zero-clear program memory address |
| | | L | H | H | H | Write mode |
| | | L | L | H | H | Verify mode |
| | | H | × | H | H | Program inhibit mode |

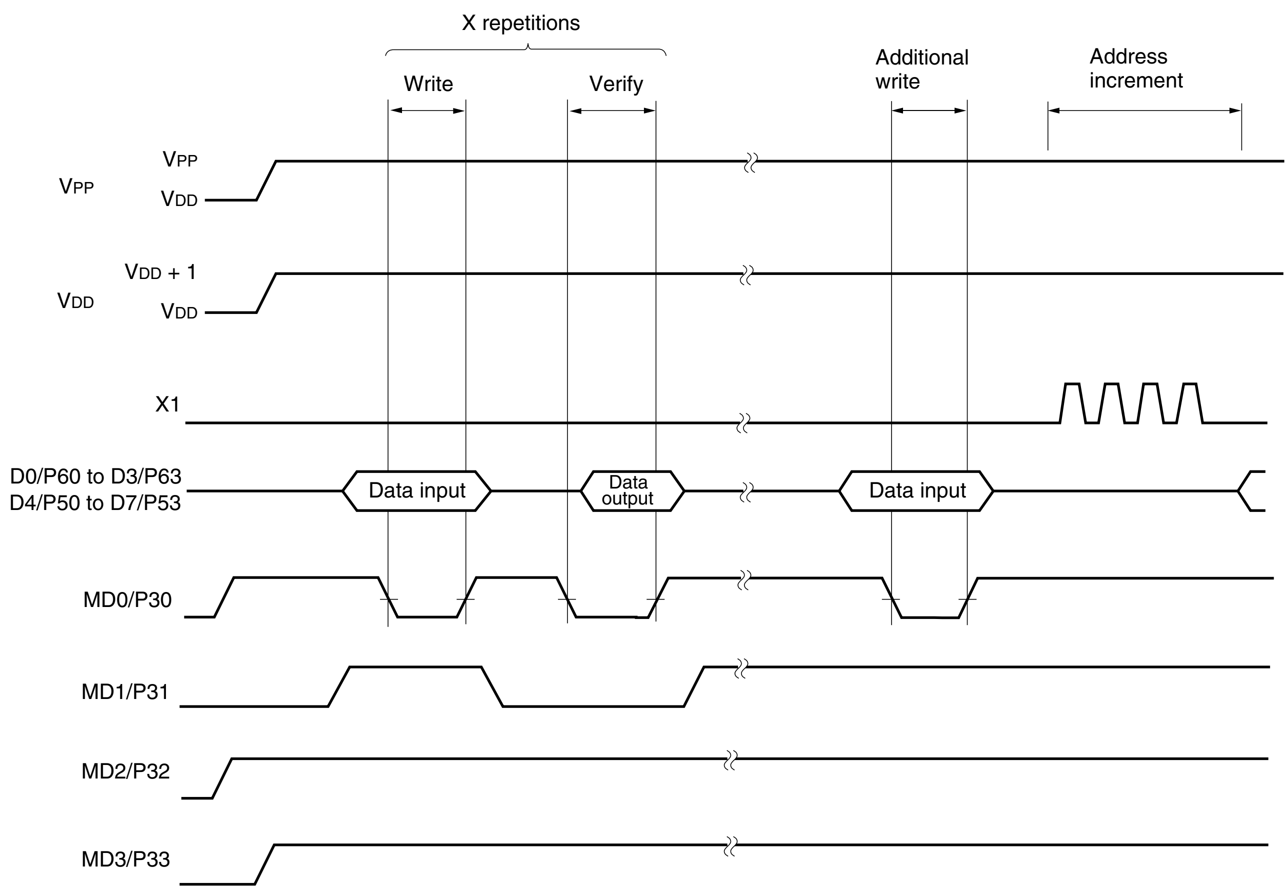
×: L or H

### 8.2 Program Memory Write Procedure

Program memory can be written at high speed using the following procedure.

(1) Pull down unused pins to Vss via resistors. Set the X1 pin to low.
(2) Supply 5 V to the $V_{DD}$ and $V_{PP}$ pins.
(3) Wait 10 μs.
(4) Select the program memory address zero-clear mode.
(5) Supply 6 V to $V_{DD}$ and 12.5 V to $V_{PP}$.
(6) Write data in the 1 ms write mode.
(7) Select the verify mode. If the data is written, go to (8) and if not, repeat (6) and (7).
(8) Additional write. (X: Number of write operations from (6) and (7)) × 1 ms
(9) Apply four pulses to the X1 pin to increment the program memory address by one.
(10) Repeat (6) to (9) until the end address is reached.
(11) Select the program memory address zero-clear mode.
(12) Return the $V_{DD}$- and $V_{PP}$-pin voltages to 5 V.
(13) Turn off the power.

The following figure shows steps (2) to (9).



### 8.3 Program Memory Read Procedure

The μPD75P3116 can read program memory contents using the following procedure.

(1) Pull down unused pins to $V_{SS}$ via resistors. Set the X1 pin to low.

(2) Supply 5 V to the $V_{DD}$ and $V_{PP}$ pins.

(3) Wait 10 μs.

(4) Select the program memory address zero-clear mode.

(5) Supply 6 V to $V_{DD}$ and 12.5 V to $V_{PP}$.

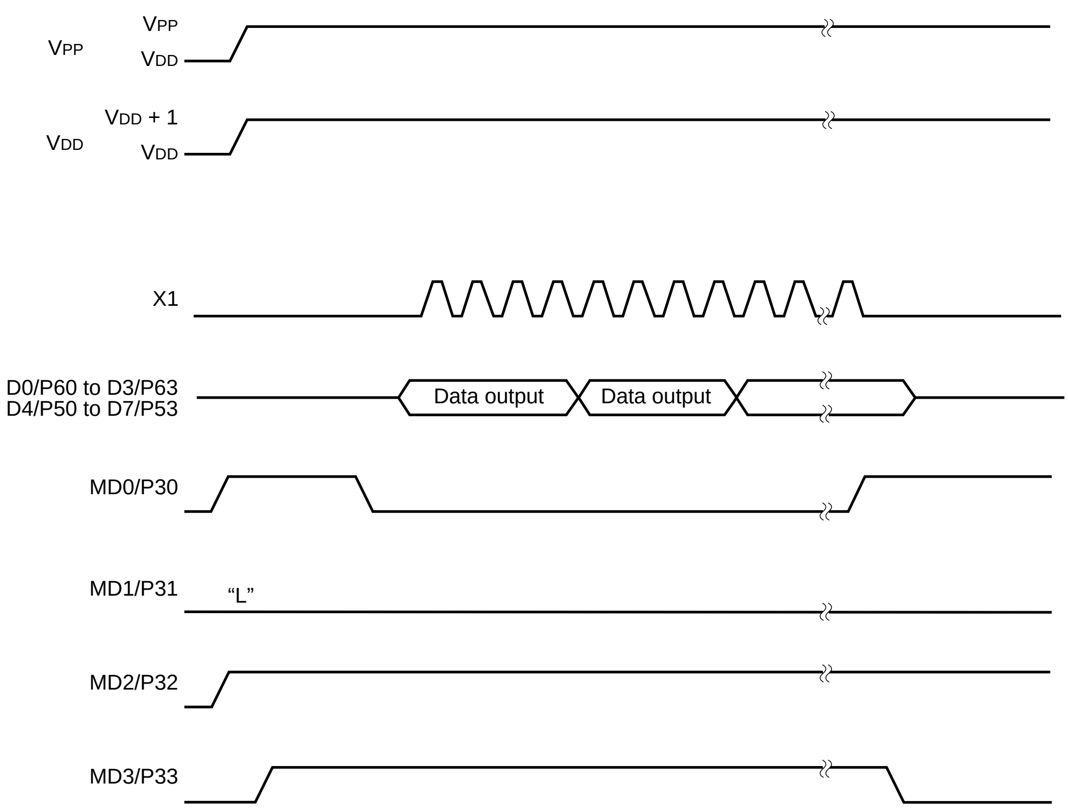
(6) Select the verify mode. Apply four pulses to the X1 pin. The data stored in one address will be output every four clock pulses.

(7) Select the program memory address zero-clear mode.

(8) Return the $V_{DD}$- and $V_{PP}$-pin voltages to 5 V.

(9) Turn off the power.

The following figure shows steps (2) to (7).



### 8.4 One-Time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends that after the required data is written and the PROM is stored under the temperature and time conditions shown below, the PROM should be verified via screening.

| Storage Temperature | Storage Time |
|---|---|
| 125˚C | 24 hours |

NEC offers QTOP microcontrollers for which one-time PROM writing, marking, screening, and verification are provided at additional cost. For further details, contact an NEC sales representative.

## 9. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings ($T_A$ = 25°C)

| Parameter | Symbol | Test Conditions | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | –0.3 to +7.0 | V |
| PROM power supply voltage | $V_{PP}$ | | –0.3 to +13.5 | V |
| Input voltage | $V_{I1}$ | Except port 5 | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{I2}$ | Port 5 (N-ch open drain) | –0.3 to +14 | V |
| Output voltage | $V_O$ | | –0.3 to $V_{DD}$ + 0.3 | V |
| Output current, high | $I_{OH}$ | Per pin | –10 | mA |
| | | Total of all pins | –30 | mA |
| Output current, low | $I_{OL}$ | Per pin | 30 | mA |
| | | Total of all pins | 220 | mA |
| Operating ambient temperature | $T_A$ | | –40 to +85 Note | °C |
| Storage temperature | $T_{stg}$ | | –65 to +150 | °C |

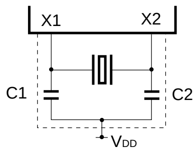
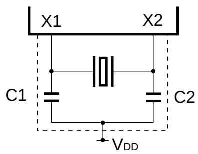
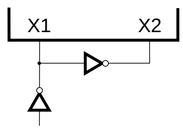
**Note** When LCD is driven in normal mode: $T_A$ = –10 to +85°C

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

### Capacitance ($T_A$ = 25°C, $V_{DD}$ = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | f = 1 MHz | | | 15 | pF |
| Output capacitance | $C_{OUT}$ | Unmeasured pins returned to 0 V. | | | 15 | pF |
| I/O capacitance | $C_{IO}$ | | | | 15 | pF |

**Main System Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Constant | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |  | Oscillation frequency (fx)[Note 1] | | 1.0 | | 6.0[Note 2] | MHz |
| | | Oscillation stabilization time[Note 3] | After $V_{DD}$ reaches oscillation voltage range MIN. | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency (fx)[Note 1] | | 1.0 | | 6.0[Note 2] | MHz |
| | | Oscillation stabilization time[Note 3] | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | $V_{DD}$ = 1.8 to 5.5 V | | | 30 | |
| External clock |  | X1 input frequency (fx)[Note 1] | | 1.0 | | 6.0[Note 2] | MHz |
| | | X1 input high-/low-level width ($t_{XH}$, $t_{XL}$) | | 83.3 | | 500 | ns |

**Notes 1.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

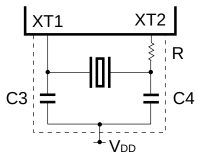
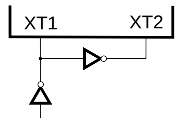
**2.** When the power supply voltage is 1.8 V ≤ $V_{DD}$ < 2.7 V and the oscillation frequency is 4.19 MHz < fx ≤ 6.0 MHz, setting the processor clock control register (PCC) to 0011 makes 1 machine cycle less than the required 0.95 μs. Therefore, set PCC to a value other than 0011.

**3.** The oscillation stabilization time is necessary for oscillation to stabilize after applying $V_{DD}$ or releasing the STOP mode.

**Caution When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as $V_{DD}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

**Subsystem Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Constant | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator |  | Oscillation frequency ($f_{XT}$)Note 1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization timeNote 2 | $V_{DD}$ = 4.5 to 5.5 V | | 1.0 | 2 | s |
| | | | $V_{DD}$ = 1.8 to 5.5 V | | | 10 | |
| External clock |  | XT1 input frequency ($f_{XT}$)Note 1 | | 32 | | 100 | kHz |
| | | XT1 input high-/low-level width ($t_{XTH}$, $t_{XTL}$) | | 5 | | 15 | μs |

**Notes 1.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**2.** The oscillation stabilization time is necessary for oscillation to stabilize after applying $V_{DD}$.

**Caution When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as $V_{DD}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

**The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, and is more liable to misoperation by noise than the main system clock oscillator. Special care should therefore be taken regarding the wiring method when the subsystem clock is used.**

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low | $I_{OL}$ | Per pin | | | | 15 | mA |
| | | Total of all pins | | | | 150 | mA |
| Input voltage, high | $V_{IH1}$ | Ports 2, 3, 8, and 9 | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | $0.7V_{DD}$ | | $V_{DD}$ | V |
| | | | 1.8 ≤ $V_{DD}$ < 2.7 V | $0.9V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | Ports 0, 1, 6, $\overline{\text{RESET}}$ | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | $0.8V_{DD}$ | | $V_{DD}$ | V |
| | | | 1.8 ≤ $V_{DD}$ < 2.7 V | $0.9V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | Port 5 (N-ch open-drain) | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | $0.7V_{DD}$ | | 13 | V |
| | | | 1.8 ≤ $V_{DD}$ < 2.7 V | $0.9V_{DD}$ | | 13 | V |
| | $V_{IH4}$ | X1, XT1 | | $V_{DD}$ – 0.1 | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Ports 2, 3, 5, 8, and 9 | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0 | | $0.3V_{DD}$ | V |
| | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0 | | $0.1V_{DD}$ | V |
| | $V_{IL2}$ | Ports 0, 1, 6, $\overline{\text{RESET}}$ | 2.7 ≤ $V_{DD}$ ≤ 5.5 V | 0 | | $0.2V_{DD}$ | V |
| | | | 1.8 ≤ $V_{DD}$ < 2.7 V | 0 | | $0.1V_{DD}$ | V |
| | $V_{IL3}$ | X1, XT1 | | 0 | | 0.1 | V |
| Output voltage, high | $V_{OH}$ | $\overline{\text{SCK}}$, SO, Ports 2, 3, 6, 8, and 9 | $I_{OH}$ = –1.0 mA | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | $\overline{\text{SCK}}$, SO, Ports 2, 3, 5, 6, 8, and 9 | $I_{OL}$ = 15 mA, $V_{DD}$ = 4.5 to 5.5 V | | 0.2 | 2.0 | V |
| | | | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | SB0, SB1 | When N-ch open-drain pull-up resistor ≥ 1 kΩ | | | $0.2V_{DD}$ | V |
| Input leakage current, high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | Pins other than X1, XT1 | | | 3 | μA |
| | $I_{LIH2}$ | | X1, XT1 | | | 20 | μA |
| | $I_{LIH3}$ | $V_{IN}$ = 13 V | Port 5 (N-ch open-drain) | | | 20 | μA |
| Input leakage current, low | $I_{LIL1}$ | $V_{IN}$ = 0 V | Pins other than X1, XT1, and Port 5 | | | –3 | μA |
| | $I_{LIL2}$ | | X1, XT1 | | | –20 | μA |
| | $I_{LIL3}$ | | Port 5 (N-ch open-drain) When another instruction than input instruction is executed | | | –3 | μA |
| | | | Port 5 (N-ch open-drain) When input instruction is executed, $V_{DD}$ = 1.8 to 5.5 V | | | –30 | μA |
| | | | $V_{DD}$ = 5.0 V | | –10 | –27 | μA |
| | | | $V_{DD}$ = 3.0 V | | –3 | –8 | μA |
| Output leakage current, high | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | $\overline{\text{SCK}}$, SO/SB0, SB1, Ports 2, 3, 6, 8, and 9 | | | 3 | μA |
| | $I_{LOH2}$ | $V_{OUT}$ = 13 V | Port 5 (N-ch open-drain) | | | 20 | μA |
| Output leakage current, low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | –3 | μA |
| On-chip pull-up resistor | $R_L$ | $V_{IN}$ = 0 V | Ports 0, 1, 2, 3, 6, 8, and 9 (Excluding P00 pin) | 50 | 100 | 200 | kΩ |

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| LCD drive voltage | $V_{LCD}$ | VAC0 = 0 | $T_A$ = –40 to +85°C | | | 2.7 | | $V_{DD}$ | V |
| | | | $T_A$ = –10 to +85°C | | | 2.2 | | $V_{DD}$ | V |
| | | VAC0 = 1 | | | | 1.8 | | $V_{DD}$ | V |
| VAC current[Note 1] | $I_{VAC}$ | VAC0 = 1, $V_{DD}$ = 2.0 V ±10% | | | | | 1 | 4 | μA |
| LCD output voltage deviation[Note 2] (common) | $V_{ODC}$ | Io = ±1.0 μA | $V_{LCD0}$ = $V_{LCD}$<br>$V_{LCD1}$ = $V_{LCD}$ × 2/3<br>$V_{LCD2}$ = $V_{LCD}$ × 1/3<br>1.8 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | | | 0 | | ±0.2 | V |
| LCD output voltage deviation[Note 2] (segment) | $V_{ODS}$ | Io = ±0.5 μA | | | | 0 | | ±0.2 | V |
| Supply current[Note 3] | $I_{DD1}$ | 6.00 MHz[Note 4] Crystal oscillation C1 = C2 = 22 pF | $V_{DD}$ = 5.0 V ±10%[Note 5] | | | | 3.2 | 9.5 | mA |
| | | | $V_{DD}$ = 3.0 V ±10%[Note 6] | | | | 0.55 | 1.6 | mA |
| | $I_{DD2}$ | | HALT mode | $V_{DD}$ = 5.0 V ±10% | | | 0.7 | 2.0 | mA |
| | | | | $V_{DD}$ = 3.0 V ±10% | | | 0.25 | 0.8 | mA |
| | $I_{DD1}$ | 4.19 MHz[Note 4] Crystal oscillation C1 = C2 = 22 pF | $V_{DD}$ = 5.0 V ±10%[Note 5] | | | | 2.5 | 7.5 | mA |
| | | | $V_{DD}$ = 3.0 V ±10%[Note 6] | | | | 0.45 | 1.35 | mA |
| | $I_{DD2}$ | | HALT mode | $V_{DD}$ = 5.0 V ±10% | | | 0.65 | 1.8 | mA |
| | | | | $V_{DD}$ = 3.0 V ±10% | | | 0.22 | 0.7 | mA |
| | $I_{DD3}$ | 32.768 kHz[Note 7] Crystal oscillation | Low-voltage mode[Note 8] | $V_{DD}$ = 3.0 V ±10% | | | 45 | 130 | μA |
| | | | | $V_{DD}$ = 2.0 V ±10% | | | 20 | 55 | μA |
| | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | | | 45 | 90 | μA |
| | | | Low current consumption mode[Note 9] | $V_{DD}$ = 3.0 V ±10% | | | 42 | 120 | μA |
| | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | | | 42 | 85 | μA |
| | $I_{DD4}$ | | HALT mode | Low-voltage mode[Note 8] | $V_{DD}$ = 3.0 V ±10% | | 5.5 | 18 | μA |
| | | | | | $V_{DD}$ = 2.0 V ±10% | | 2.2 | 7 | μA |
| | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | | 5.5 | 12 | μA |
| | | | | Low current consumption mode[Note 9] | $V_{DD}$ = 3.0 V ±10% | | 4.0 | 12 | μA |
| | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | | 4.0 | 8 | μA |
| | $I_{DD5}$ | XT1 = 0 V[Note 10] STOP mode | $V_{DD}$ = 5.0 V ±10% | | | | 0.05 | 10 | μA |
| | | | $V_{DD}$ = 3.0 V ±10% | $T_A$ = –40 to +85°C | | | 0.02 | 5 | μA |
| | | | | $T_A$ = 25°C | | | 0.02 | 3 | μA |

**Notes 1.** Set to VAC0 = 0 when the low current consumption mode and the stop mode are used. If VAC0 = 1 is set, the current increases for approx. 1 μA.

**2.** The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs ($V_{LCDn}$; n = 0, 1, 2).

**3.** Not including currents flowing through on-chip pull-up resistors.

**4.** Including oscillation of the subsystem clock.

**5.** When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

**6.** When PCC is set to 0000 and the device is operated in the low-speed mode.

**7.** When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

**8.** When the sub-oscillator control register (SOS) is set to 0000.

**9.** When SOS is set to 0010.

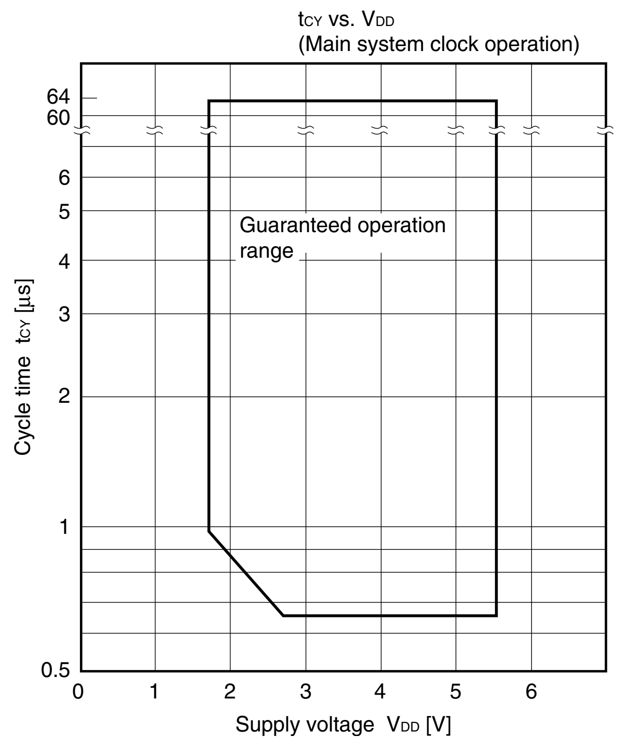
**10.** When SOS is set to 00×1 and the feedback resistor of the sub-oscillator is not used (×: Don't care).

**AC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU clock cycle time[Note 1] (Min. instruction execution time = 1 machine cycle) | $t_{CY}$ | Operating on main system clock | $V_{DD}$ = 2.7 to 5.5 V | 0.67 | | 64 | μs |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0.95 | | 64 | μs |
| | | Operating on subsystem clock | | 114 | 122 | 125 | μs |
| TI0, TI1, TI2 input frequency | $f_{TI}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0 | | 1.0 | MHz |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 0 | | 275 | kHz |
| TI0, TI1, TI2 input high-/low-level width | $t_{TIH}$, $t_{TIL}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0.48 | | | μs |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 1.8 | | | μs |
| Interrupt input high-/low-level width | $t_{INTH}$, $t_{INTL}$ | INT0 | IM02 = 0 | **Note 2** | | | μs |
| | | | IM02 = 1 | 10 | | | μs |
| | | INT1, 2, 4 | | 10 | | | μs |
| | | KR0 to KR7 | | 10 | | | μs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | μs |

**Notes 1.** The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC) and the processor clock control register (PCC). The figure on the right indicates the cycle time $t_{CY}$ versus supply voltage $V_{DD}$ characteristics with the main system clock operating.

**2.** 2$t_{CY}$ or 128/fx is set by setting the interrupt mode register (IM0).



### Serial Transfer Operation

**2-wire and 3-wire serial I/O mode ($\overline{SCK}$...Internal clock output): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 3800 | | | ns |
| $\overline{SCK}$ high-/low-level width | $t_{KL1}$, $t_{KH1}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY1}$/2–50 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | $t_{KCY1}$/2–150 | | | ns |
| SI[Note 1] setup time (to $\overline{SCK}$↑) | $t_{SIK1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 500 | | | ns |
| SI[Note 1] hold time (from $\overline{SCK}$↑) | $t_{KSI1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 600 | | | ns |
| SO[Note 1] output delay time from $\overline{SCK}$↓ | $t_{KSO1}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF[Note 2] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 1000 | ns |

**Notes 1.** In 2-wire serial I/O mode, read this parameter as SB0 or SB1 instead.

**2.** $R_L$ and $C_L$ are the load resistance and load capacitance of the SO output lines, respectively.

**2-wire and 3-wire serial I/O mode ($\overline{SCK}$...External clock input): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 3200 | | | ns |
| $\overline{SCK}$ high-/low-level width | $t_{KL2}$, $t_{KH2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 1600 | | | ns |
| SI[Note 1] setup time (to $\overline{SCK}$↑) | $t_{SIK2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 150 | | | ns |
| SI[Note 1] hold time (from $\overline{SCK}$↑) | $t_{KSI2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 600 | | | ns |
| SO[Note 1] output delay time from $\overline{SCK}$↓ | $t_{KSO2}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF[Note 2] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 1000 | ns |

**Notes 1.** In 2-wire serial I/O mode, read this parameter as SB0 or SB1 instead.

**2.** $R_L$ and $C_L$ are the load resistance and load capacitance of the SO output lines, respectively.

**SBI mode ($\overline{SCK}$...Internal clock output (master)): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 3800 | | | ns |
| $\overline{SCK}$ high-/low-level width | $t_{KL3}$, $t_{KH3}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY3}$/2–50 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | $t_{KCY3}$/2–150 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}$↑) | $t_{SIK3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 500 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}$↑) | $t_{KSI3}$ | | | $t_{KCY3}$/2 | | | ns |
| SB0, 1 output delay time from $\overline{SCK}$↓ | $t_{KSO3}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF[Note] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 1000 | ns |
| SB0, 1↓ from $\overline{SCK}$↑ | $t_{KSB}$ | | | $t_{KCY3}$ | | | ns |
| $\overline{SCK}$↓ from SB0, 1↓ | $t_{SBK}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY3}$ | | | ns |

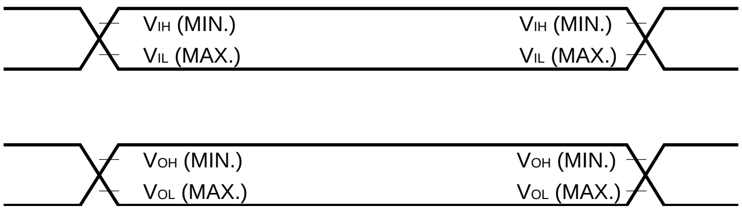
**Note** $R_L$ and $C_L$ are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

**SBI mode ($\overline{SCK}$...External clock input (slave)): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

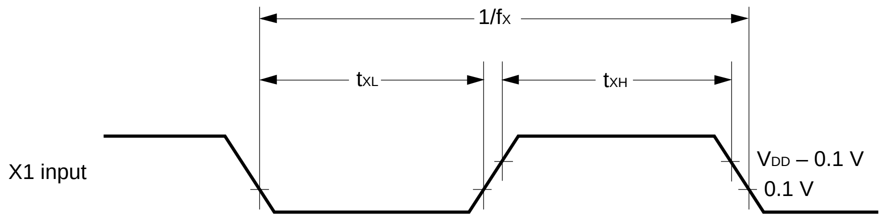
| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 3200 | | | ns |
| $\overline{SCK}$ high-/low-level width | $t_{KL4}$, $t_{KH4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 1600 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}$↑) | $t_{SIK4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 150 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}$↑) | $t_{KSI4}$ | | | $t_{KCY4}$/2 | | | ns |
| SB0, 1 output delay time from $\overline{SCK}$↓ | $t_{KSO4}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF[Note] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 1000 | ns |
| SB0, 1↓ from $\overline{SCK}$↑ | $t_{KSB}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK}$↓ from SB0, 1↓ | $t_{SBK}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY4}$ | | | ns |

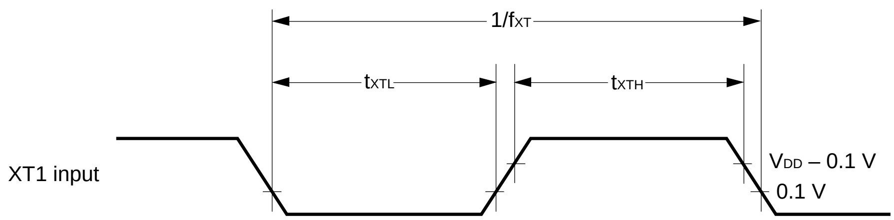
**Note** $R_L$ and $C_L$ are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

**AC Timing Test Points (Excluding X1, XT1 Input)**

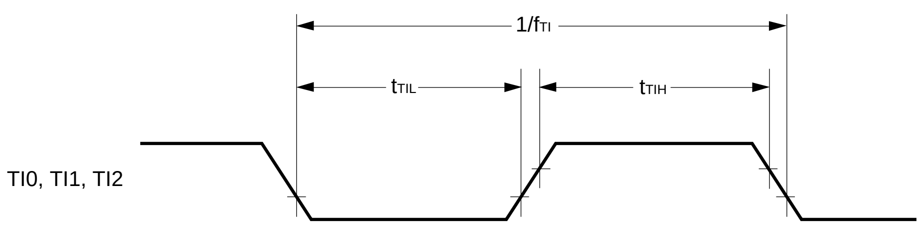



**Clock Timing**



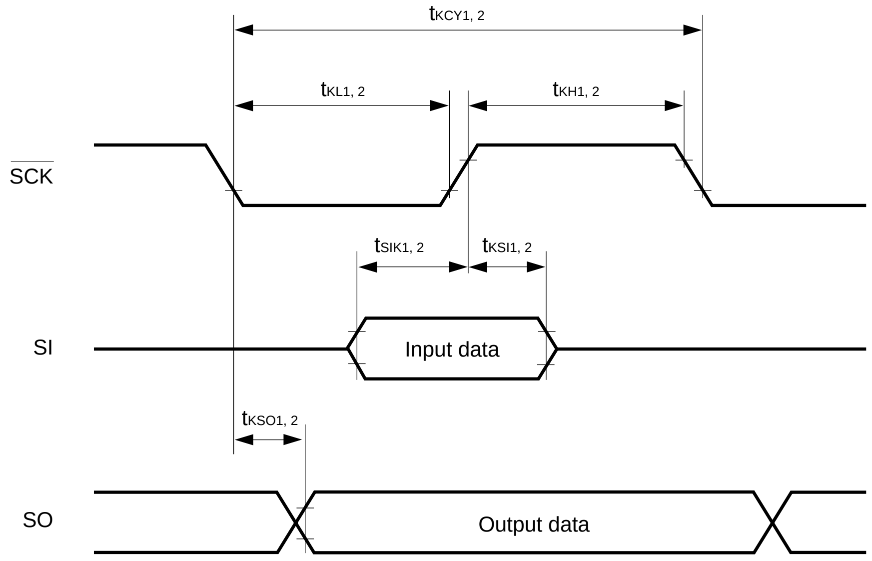




**TI0, TI1, TI2 Timing**

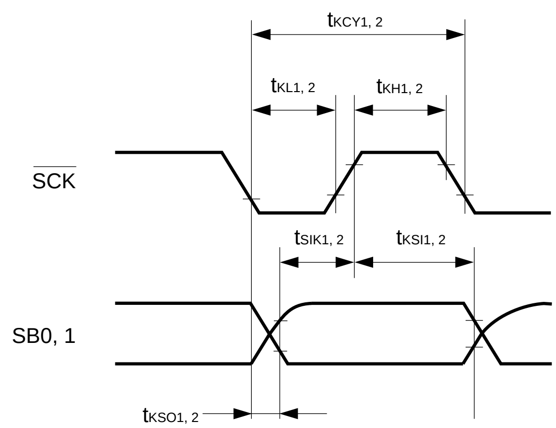


**Serial Transfer Timing**

**3-wire serial I/O mode**

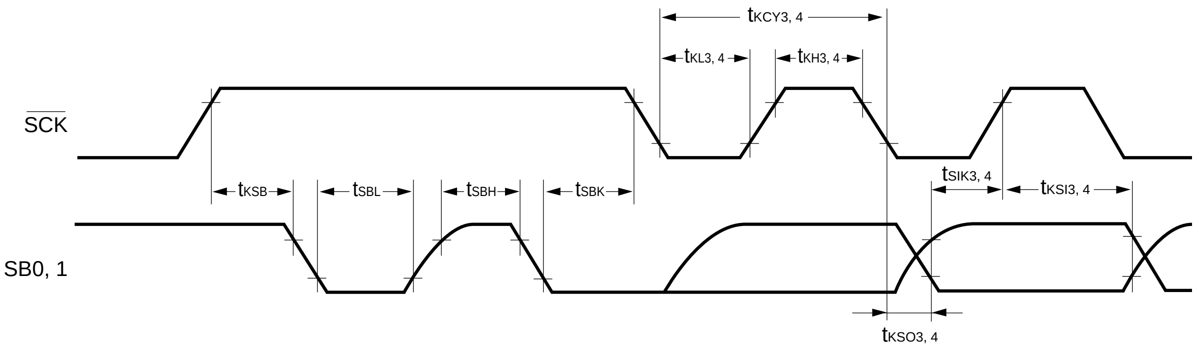



**2-wire serial I/O mode**

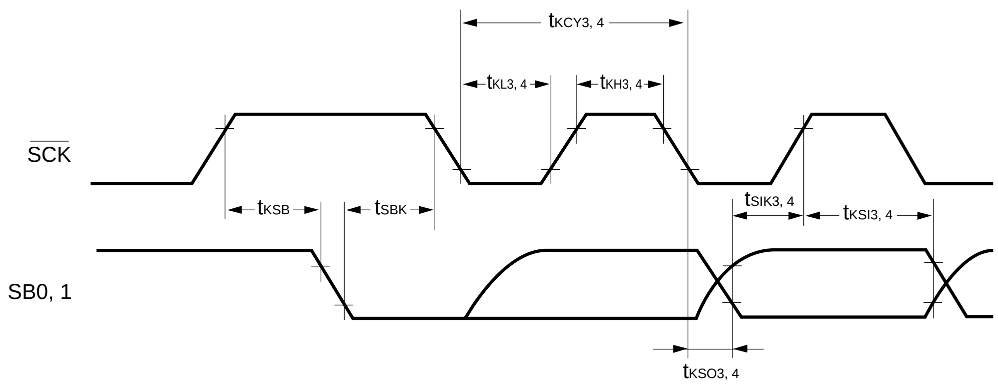


**Serial Transfer Timing**

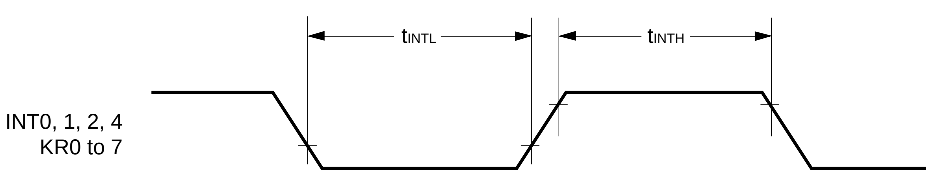
**Bus release signal transfer**



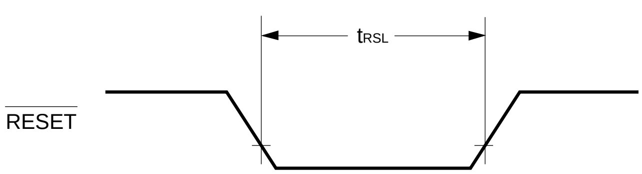

**Command signal transfer**




**Interrupt input timing**




**RESET input timing**



**Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics ($T_A$ = –40 to +85°C)**

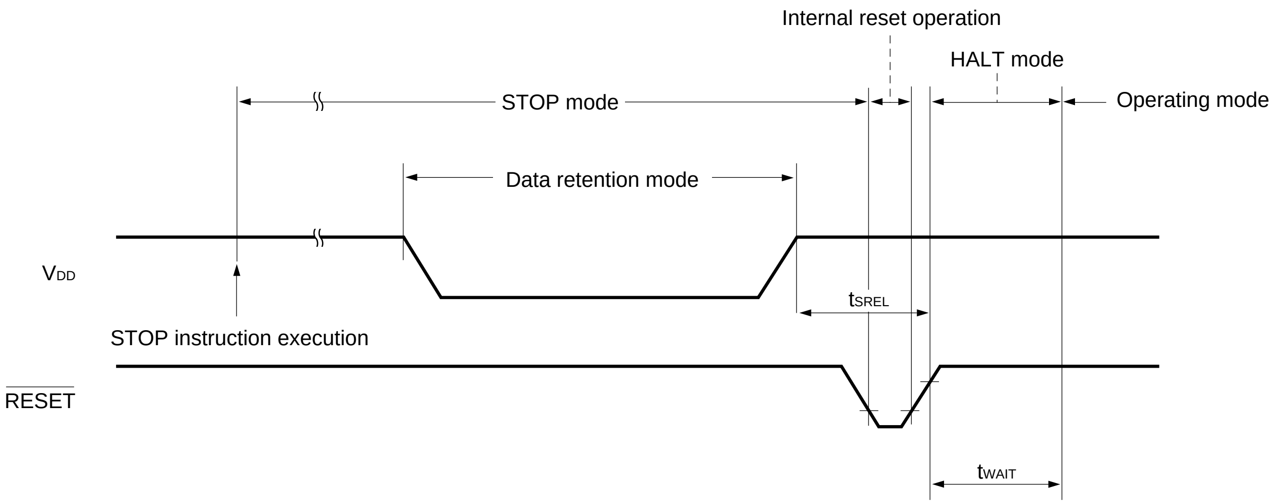
| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Release signal set time | $t_{SREL}$ | | 0 | | | μs |
| Oscillation stabilization wait time^Note 1 | $t_{WAIT}$ | Release by $\overline{RESET}$ | | $2^{15}/f_X$ | | ms |
| | | Release by interrupt request | | **Note 2** | | ms |

**Notes 1.** The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the start of oscillation.

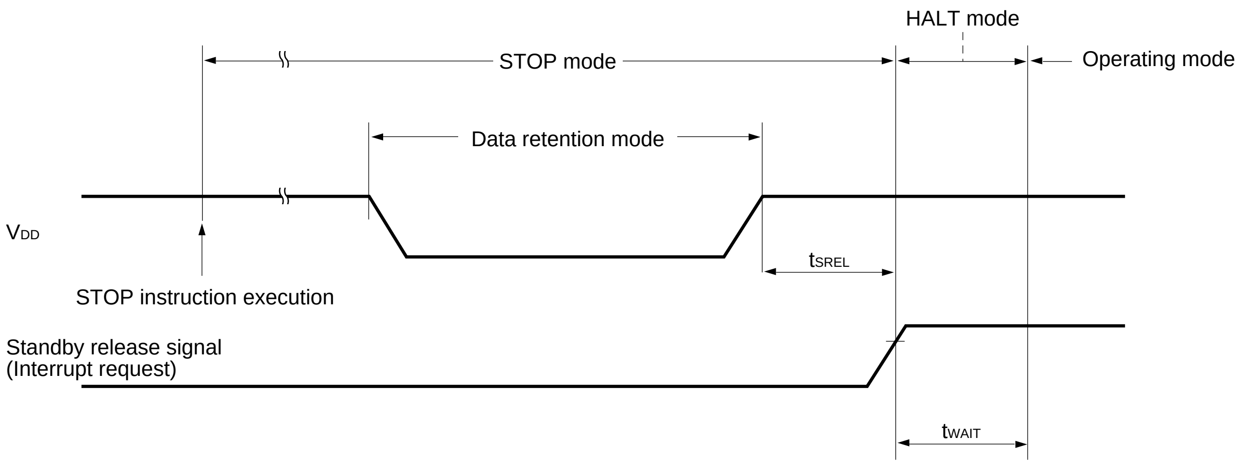
**2.** Depends on the basic interval timer mode register (BTM) settings (see the table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait Time | |
|---|---|---|---|---|---|
| | | | | fx = 4.19 MHz | fx = 6.0 MHz |
| — | 0 | 0 | 0 | $2^{20}$/fx (approx. 250 ms) | $2^{20}$/fx (approx. 175 ms) |
| — | 0 | 1 | 1 | $2^{17}$/fx (approx. 31.3 ms) | $2^{17}$/fx (approx. 21.8 ms) |
| — | 1 | 0 | 1 | $2^{15}$/fx (approx. 7.81 ms) | $2^{15}$/fx (approx. 5.46 ms) |
| — | 1 | 1 | 1 | $2^{13}$/fx (approx. 1.95 ms) | $2^{13}$/fx (approx. 1.37 ms) |

**Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)**




**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**



### DC Programming Characteristics ($T_A$ = 25 ±5°C, $V_{DD}$ = 6.0 ±0.25 V, $V_{PP}$ = 12.5 ±0.3 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | Except X1 and X2 pins | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | X1, X2 | $V_{DD}$ – 0.5 | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Except X1 and X2 pins | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL2}$ | X1, X2 | 0 | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | | | 10 | μA |
| Output voltage, high | $V_{OH}$ | $I_{OH}$ = –1 mA | $V_{DD}$ – 1.0 | | | V |
| Output voltage, low | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $V_{DD}$ power supply current | $I_{DD}$ | | | | 30 | mA |
| $V_{PP}$ power supply current | $I_{PP}$ | MD0 = $V_{IL}$, MD1 = $V_{IH}$ | | | 30 | mA |

**Cautions 1. Do not exceed +13.5 V for $V_{PP}$, including the overshoot.**

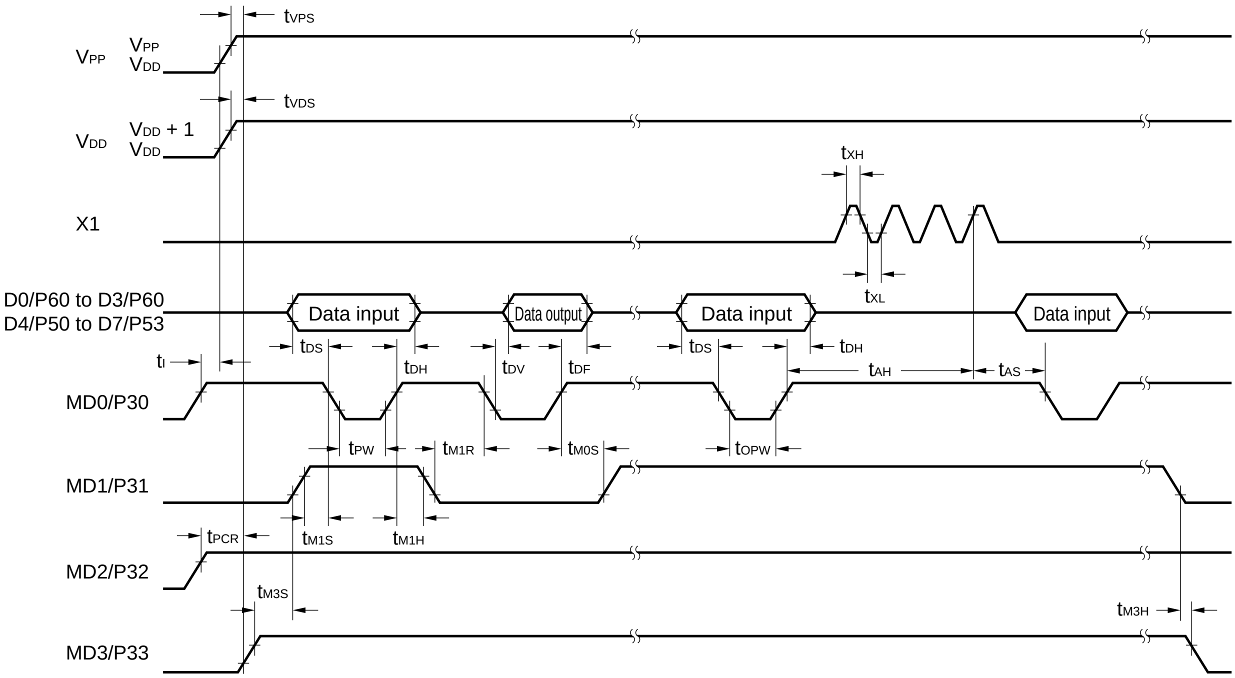
**2. $V_{DD}$ must be applied before $V_{PP}$, and cut after $V_{PP}$.**

★ ### AC Programming Characteristics ($T_A$ = 25 ±5°C, $V_{DD}$ = 6.0 ±0.25 V, $V_{PP}$ = 12.5 ±0.3 V, $V_{SS}$ = 0 V)

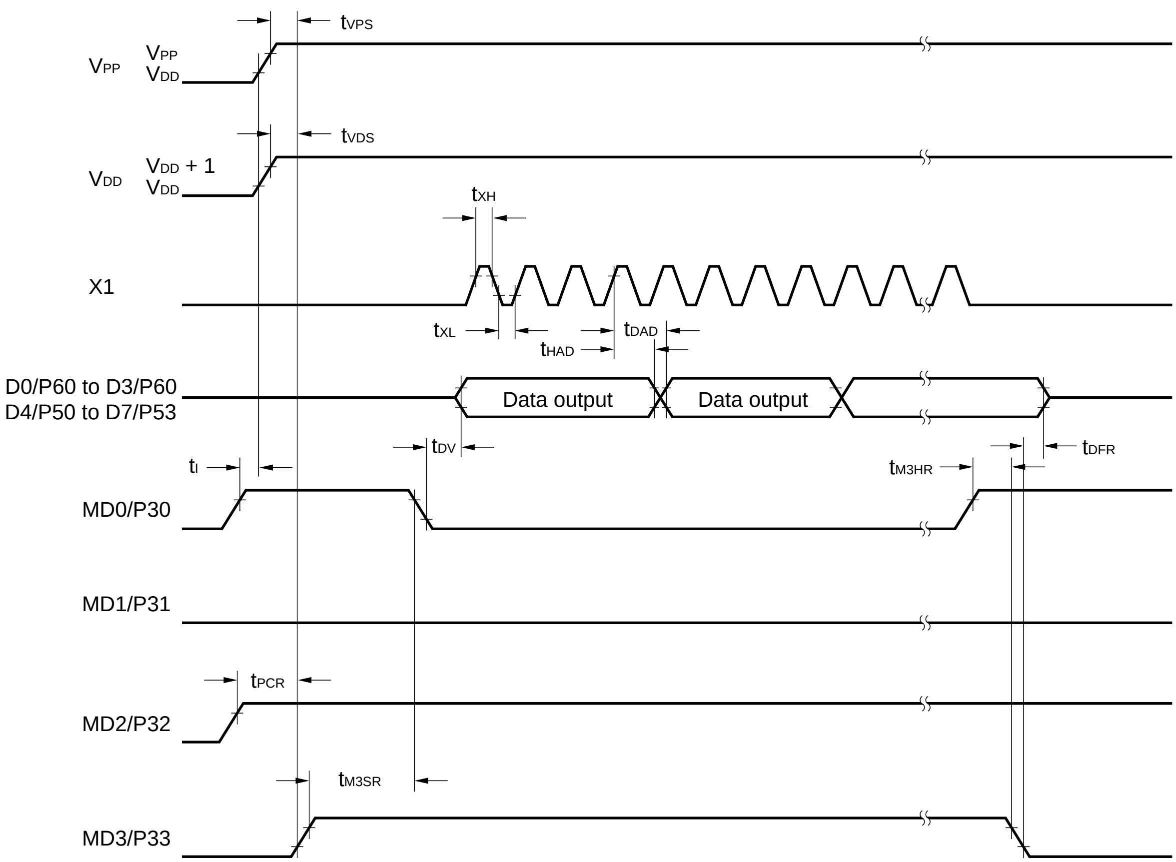
| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Address setup time[Note] (to MD0↓) | $t_{AS}$ | | 2 | | | μs |
| MD1 setup time (to MD0↓) | $t_{M1S}$ | | 2 | | | μs |
| Data setup time (to MD0↓) | $t_{DS}$ | | 2 | | | μs |
| Address hold time[Note] (from MD0↑) | $t_{AH}$ | | 2 | | | μs |
| Data hold time (from MD0↑) | $t_{DH}$ | | 2 | | | μs |
| Data output float delay time from MD0↑ | $t_{DF}$ | | 0 | | 130 | ns |
| $V_{PP}$ setup time (to MD3↑) | $t_{VPS}$ | | 2 | | | μs |
| $V_{DD}$ setup time (to MD3↑) | $t_{VDS}$ | | 2 | | | μs |
| Initial program pulse width | $t_{PW}$ | | 0.95 | 1.0 | 1.05 | ms |
| Additional program pulse width | $t_{OPW}$ | | 0.95 | | 21.0 | ms |
| MD0 setup time (to MD1↑) | $t_{M0S}$ | | 2 | | | μs |
| Data output delay time from MD0↓ | $t_{DV}$ | MD0 = MD1 = $V_{IL}$ | | | 1 | μs |
| MD1 hold time (from MD0↑) | $t_{M1H}$ | $t_{M1H}$ + $t_{M1R}$ ≥ 50 μs | 2 | | | μs |
| MD1 recovery time (from MD0↓) | $t_{M1R}$ | | 2 | | | μs |
| Program counter reset time | $t_{PCR}$ | | 10 | | | μs |
| X1 input high-/low-level width | $t_{XH}$, $t_{XL}$ | | 0.125 | | | μs |
| X1 input frequency | $f_X$ | | | | 4.19 | MHz |
| Initial mode set time | $t_I$ | | 2 | | | μs |
| MD3 setup time (to MD1↑) | $t_{M3S}$ | | 2 | | | μs |
| MD3 hold time (from MD1↓) | $t_{M3H}$ | | 2 | | | μs |
| MD3 setup time (to MD0↓) | $t_{M3SR}$ | During program memory read | 2 | | | μs |
| Data output delay time from Address[Note] | $t_{DAD}$ | During program memory read | | | 2 | μs |
| Data output hold time from Address[Note] | $t_{HAD}$ | During program memory read | 0 | | 130 | ns |
| MD3 hold time (from MD0↑) | $t_{M3HR}$ | During program memory read | 2 | | | μs |
| Data output float delay time from MD3↓ | $t_{DFR}$ | During program memory read | | | 2 | μs |

**Note** The internal address signal is incremented by 1 at the rising edge of the fourth X1 input and is not connected to a pin.

**Program Memory Write Timing**

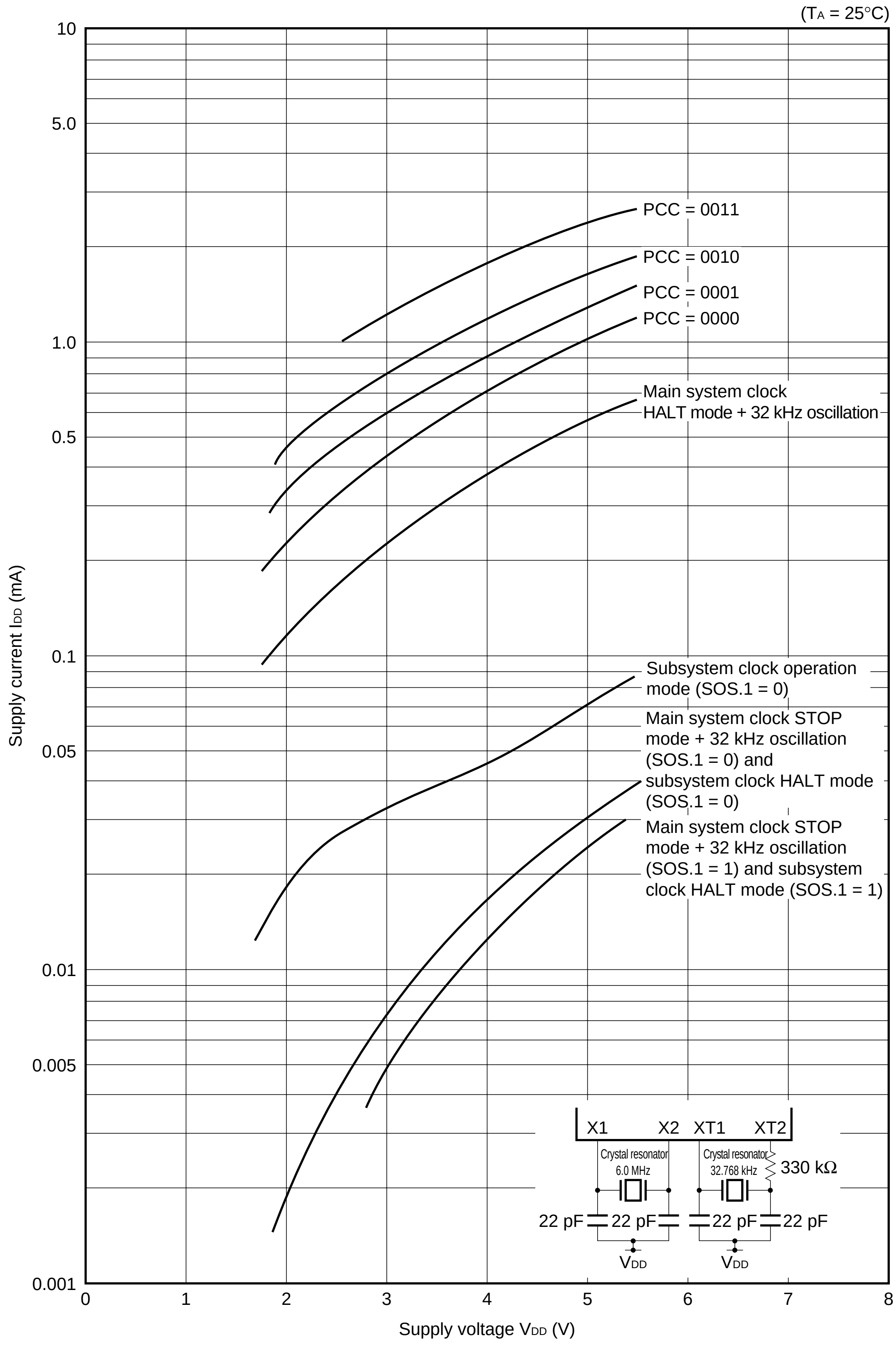



**Program Memory Read Timing**

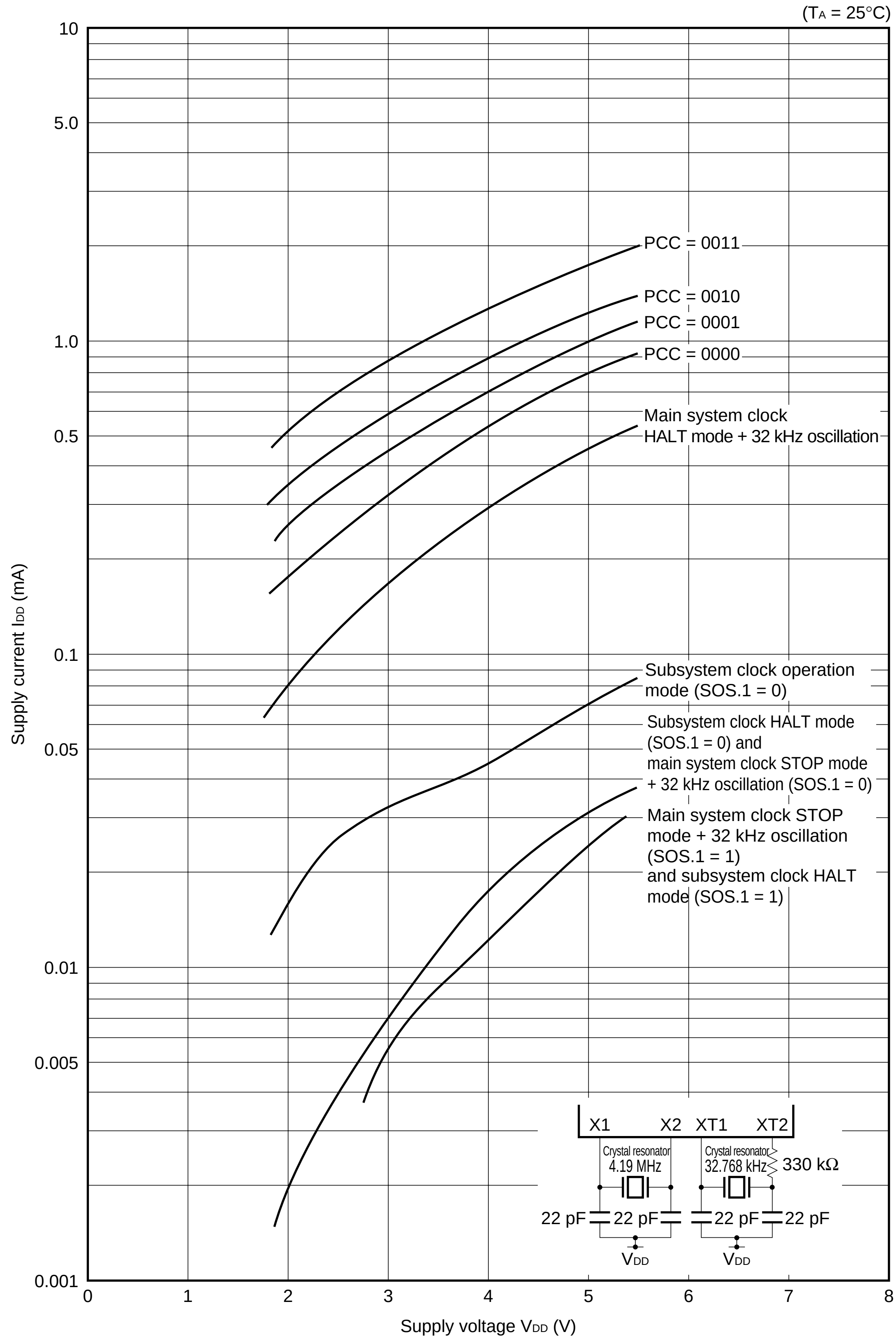


## 10. CHARACTERISTIC CURVES (REFERENCE VALUES)

**$I_{DD}$ vs $V_{DD}$ (Main System Clock: 6.0 MHz Crystal Resonator)**

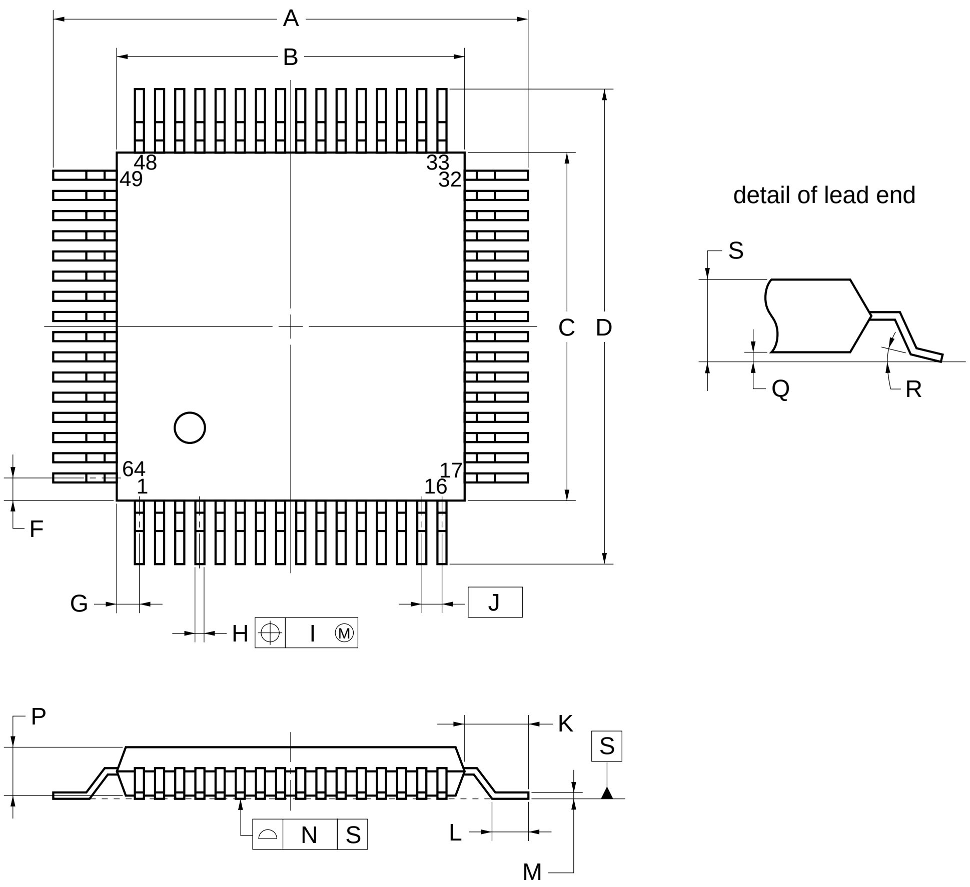


**$I_{DD}$ vs $V_{DD}$ (Main System Clock: 4.19 MHz Crystal Resonator)**



## 11. PACKAGE DRAWINGS

## ★ 64-PIN PLASTIC QFP (14x14)



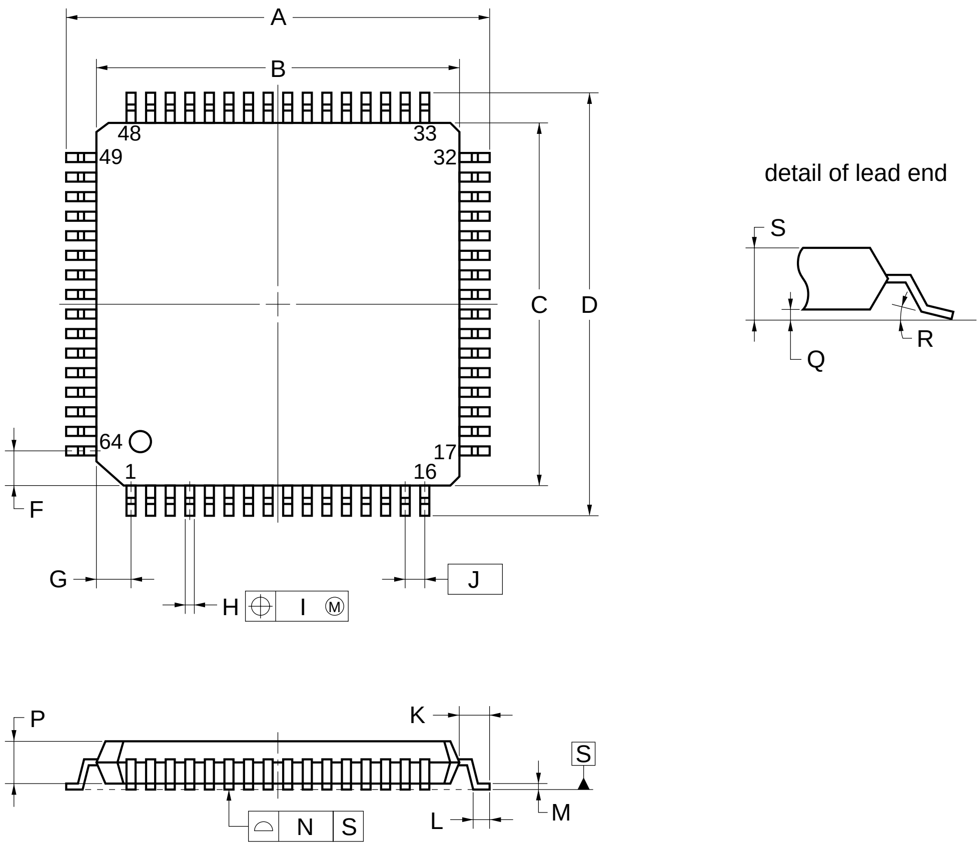

**NOTE**

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 17.6±0.4 |
| B | 14.0±0.2 |
| C | 14.0±0.2 |
| D | 17.6±0.4 |
| F | 1.0 |
| G | 1.0 |
| H | $0.37^{+0.08}_{-0.07}$ |
| I | 0.15 |
| J | 0.8 (T.P.) |
| K | 1.8±0.2 |
| L | 0.8±0.2 |
| M | $0.17^{+0.08}_{-0.07}$ |
| N | 0.10 |
| P | 2.55±0.1 |
| Q | 0.1±0.1 |
| R | 5°±5° |
| S | 2.85 MAX. |

**P64GC-80-AB8-5**

## ★ 64-PIN PLASTIC LQFP (12x12)



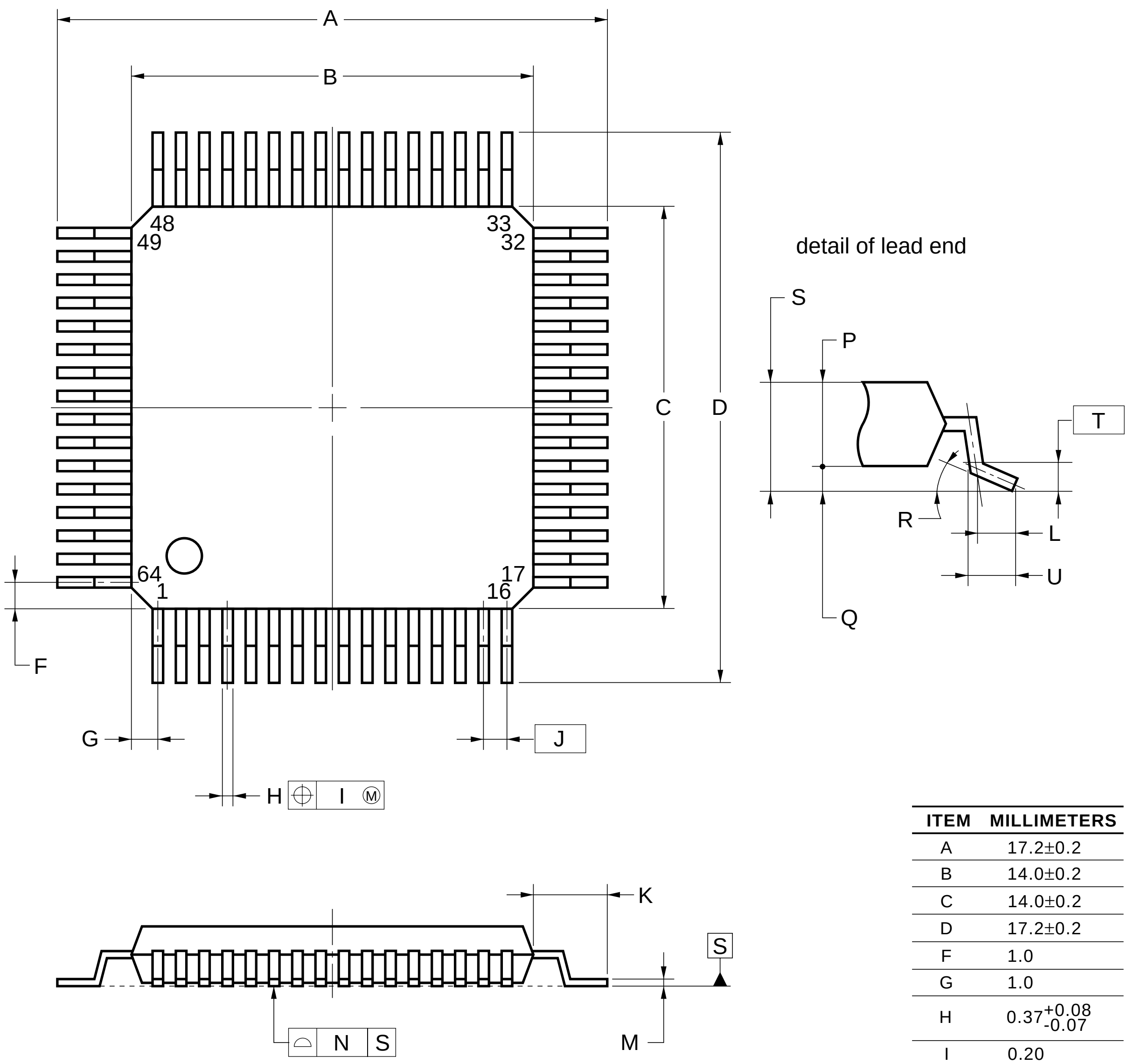

**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 14.8±0.4 |
| B | 12.0±0.2 |
| C | 12.0±0.2 |
| D | 14.8±0.4 |
| F | 1.125 |
| G | 1.125 |
| H | 0.32±0.08 |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.4±0.2 |
| L | 0.6±0.2 |
| M | $0.17^{+0.08}_{-0.07}$ |
| N | 0.10 |
| P | 1.4±0.1 |
| Q | 0.125±0.075 |
| R | 5°±5° |
| S | 1.7 MAX. |

**P64GK-65-8A8-3**

## ★ 64-PIN PLASTIC LQFP (14x14)




| ITEM | MILLIMETERS |
|---|---|
| A | 17.2±0.2 |
| B | 14.0±0.2 |
| C | 14.0±0.2 |
| D | 17.2±0.2 |
| F | 1.0 |
| G | 1.0 |
| H | $0.37^{+0.08}_{-0.07}$ |
| I | 0.20 |
| J | 0.8 (T.P.) |
| K | 1.6±0.2 |
| L | 0.8 |
| M | $0.17^{+0.03}_{-0.06}$ |
| N | 0.10 |
| P | 1.4±0.1 |
| Q | 0.127±0.075 |
| R | $3°^{+4°}_{-3°}$ |
| S | 1.7 MAX. |
| T | 0.25 |
| U | 0.886±0.15 |

P64GC-80-8BS

**NOTE**

Each lead centerline is located within 0.20 mm of its true position (T.P.) at maximum material condition.

## 12. RECOMMENDED SOLDERING CONDITIONS

The μPD75P3116 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC Sales representative.

**Table 12-1. Surface Mounting Type Soldering Conditions (1/2)**

(1) μPD75P3116GC-AB8: 64-pin plastic QFP (14 × 14)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less | IR35-00-3 |
| VPS | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less | VP15-00-3 |
| Wave soldering | Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | — |

**Caution Do not use different soldering methods together (except for partial heating).**

(2) μPD75P3116GK-8A8: 64-pin plastic LQFP (12 × 12)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | IR35-107-2 |
| VPS | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | VP15-107-2 |
| Wave soldering | Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | WS 60-107-1 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | — |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution Do not use different soldering methods together (except for partial heating).**

### Table 12-1. Surface Mounting Type Soldering Conditions (2/2)

★ (3) μPD75P3116GC-8BS: 64-pin plastic LQFP (14 × 14)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less | IR35-00-2 |
| VPS | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less | VP15-00-2 |
| Wave soldering | Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | — |

**Caution Do not use different soldering methods together (except for partial heating).**

## APPENDIX A. LIST OF μPD75308B, 753108, AND 75P3116 FUNCTIONS

| Parameter | | μPD75308B | μPD753108 | μPD75P3116 |
|---|---|---|---|---|
| Program memory | | Mask ROM<br>0000H to 1F7FH<br>(8064 × 8 bits) | Mask ROM<br>0000H to 1FFFH<br>(8192 × 8 bits) | One-time PROM<br>0000H to 3FFFH<br>(16384 × 8 bits) |
| Data memory | | | 000H to 1FFH<br>(512 × 4 bits) | |
| CPU | | 75X Standard | 75XL CPU | |
| Instruction execution time | When main system clock is selected | 0.95, 1.91, 15.3 μs<br>(during 4.19 MHz operation) | • 0.95, 1.91, 3.81, 15.3 μs (during 4.19 MHz operation)<br>• 0.67, 1.33, 2.67, 10.7 μs (during 6.0 MHz operation) | |
| | When subsystem clock is selected | 122 μs (during 32.768 kHz operation) | | |
| Stack | SBS register | None | SBS.3 = 1: Mk I mode selection<br>SBS.3 = 0: Mk II mode selection | |
| | Stack area | 000H to 0FFH | 000H to 1FFH | |
| | Subroutine call instruction stack operation | 2-byte stack | When Mk I mode: 2-byte stack<br>When Mk II mode: 3-byte stack | |
| Instruction | BRA !addr1<br>CALLA !addr1 | Unavailable | When Mk I mode: Unavailable<br>When Mk II mode: Available | |
| | MOVT XA, @BCDE<br>MOVT XA, @BCXA<br>BR BCDE<br>BR BCXA | | Available | |
| | CALL !addr | 3 machine cycles | Mk I mode: 3 machine cycles<br>Mk II mode: 4 machine cycles | |
| | CALLF !faddr | 2 machine cycles | Mk I mode: 2 machine cycles<br>Mk II mode: 3 machine cycles | |
| I/O ports | CMOS input | 8 | 8 | |
| | CMOS I/O | 16 | 20 | |
| | Bit port output | 8 | 0 | |
| | N-ch open-drain I/O | 8 | 4 | |
| | Total | 40 | 32 | |
| LCD controller/driver | | Segment selection: 24/28/32 (can be changed to CMOS I/O port in 4-bit units; max. 8) | Segment selection: 16/20/24 segments (can be changed to CMOS I/O port in 4-bit units; max. 8) | |
| | | Display mode selection: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) | | |
| | | On-chip split resistor for LCD driver can be specified by using mask option. | | No on-chip split resistor for LCD driver |
| Timer | | 3 channels<br>• Basic interval timer: 1 channel<br>• 8-bit timer/event counter: 1 channel<br>• Watch timer: 1 channel | 5 channels<br>• Basic interval timer/watchdog timer: 1 channel<br>• 8-bit timer/event counter: 3 channels (can be used as 16-bit timer/event counter)<br>• Watch timer: 1 channel | |

| Parameter | | μPD75308B | μPD753108 | μPD75P3116 |
|---|---|---|---|---|
| Clock output (PCL) | | Φ, 524, 262, 65.5 kHz<br>(Main system clock:<br>during 4.19 MHz operation) | • Φ, 524, 262, 65.5 kHz<br>(Main system clock: during 4.19 MHz operation)<br>• Φ, 750, 375, 93.8 kHz<br>(Main system clock: during 6.0 MHz operation) | |
| BUZ output (BUZ) | | 2 kHz<br>(Main system clock:<br>during 4.19 MHz operation) | • 2, 4, 32 kHz<br>(Main system clock: during 4.19 MHz operation or subsystem clock: during 32.768 kHz operation)<br>• 2.93, 5.86, 46.9 kHz<br>(Main system clock: during 6.0 MHz operation) | |
| Serial interface | | 3 modes are available<br>• 3-wire serial I/O mode ··· MSB/LSB can be selected for transfer first bit<br>• 2-wire serial I/O mode<br>• SBI mode | | |
| SOS register | Feedback resistor cut flag (SOS.0) | None | Contained | |
| | Sub-oscillator current cut flag (SOS.1) | None | Contained | |
| Register bank selection register (RBS) | | None | Yes | |
| Standby release by INT0 | | No | Yes | |
| Vectored interrupts | | External: 3, Internal: 3 | External: 3, Internal: 5 | |
| Supply voltage | | $V_{DD}$ = 2.0 to 6.0 V | $V_{DD}$ = 1.8 to 5.5 V | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C | | |
| ★ Package | | • 80-pin plastic QFP (14 × 20)<br>• 80-pin plastic QFP (14 × 14)<br>• 80-pin plastic TQFP (Fine pitch) (12 × 12) | • 64-pin plastic QFP (14 × 14)<br>• 64-pin plastic LQFP (12 × 12)<br>• 64-pin plastic TQFP (12 × 12)<br>• 64-pin plastic LQFP (14 × 14) | • 64-pin plastic QFP (14 × 14)<br>• 64-pin plastic LQFP (12 × 12)<br>• 64-pin plastic LQFP (14 × 14) |

## APPENDIX B. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD75P3116.
In the 75XL Series, a common relocatable assembler is used in combination with a device file dedicated to each model.

| ★ RA75X relocatable assembler | Host Machine | | | Part Number (Product Name) |
|---|---|---|---|---|
| | | OS | Supply Medium | |
| | PC-9800 Series | MS-DOS™ (Ver.3.30 to Ver.6.2Note) | 3.5" 2HD | μS5A13RA75X |
| | IBM PC/AT™ or compatibles | Refer to **OS for IBM PCs** | 3.5" 2HC | μS7B13RA75X |

| ★ Device file | Host Machine | | | Part Number (Product Name) |
|---|---|---|---|---|
| | | OS | Supply Medium | |
| | PC-9800 Series | MS-DOS (Ver.3.30 to Ver.6.2Note) | 3.5" 2HD | μS5A13DF753108 |
| | IBM PC/AT or compatibles | Refer to **OS for IBM PCs** | 3.5" 2HC | μS7B13DF753108 |

**Note** Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

**Remark** Operation of the assembler and device file is guaranteed only when using the host machine and OS described above.

### PROM Write Tools

<table>
<tr><td rowspan="4">Hardware</td><td>PG-1500</td><td colspan="4">This is a PROM writer that can program a single-chip microcontroller with PROM in stand-alone mode or under the control of a host machine when connected with the supplied accessory board and optional programmer adapter.<br>It can also program typical PROMs in capacities ranging from 256 Kb to 4 Mb.</td></tr>
<tr><td>★ PA-75P3116GC</td><td colspan="4">This is a PROM programmer adapter for the μPD75P3116GC-AB8.<br>It can be used when connected to the PG-1500.</td></tr>
<tr><td>★ PA-75P3116GK</td><td colspan="4">This is a PROM programmer adapter for the μPD75P3116GK-8A8.<br>It can be used when connected to the PG-1500.</td></tr>
<tr><td>★ PA-75P3116GC-8BS</td><td colspan="4">This is a PROM programmer adapter for the μPD75P3116GC-8BS.<br>It can be used when connected to the PG-1500.</td></tr>
<tr><td rowspan="5">Software</td><td rowspan="5">PG-1500 controller</td><td colspan="4">Connects the PG-1500 to the host machine via serial and parallel interfaces and controls the PG-1500 on the host machine.</td></tr>
<tr><td colspan="3">Host machine</td><td rowspan="2">Part number (Product name)</td></tr>
<tr><td></td><td>OS</td><td>Supply medium</td></tr>
<tr><td>PC-9800 Series</td><td>MS-DOS (Ver.3.30 to Ver.6.2Note)</td><td>3.5" 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>IBM PC/AT or compatible</td><td>Refer to OS for IBM PCs</td><td>3.5" 2HD</td><td>μS7B13PG1500</td></tr>
</table>

**Note** Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

**Remark** Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

### Debugging Tools

An in-circuit emulator (IE-75001-R) is provided as a program debugging tool for the μPD75P3116.

The system configuration using this in-circuit emulator is shown below.

| | | |
|---|---|---|
| ★ Hardware | IE-75001-R | The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products.<br>The IE-75001-R is used in combination with an emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R) (both sold separately).<br>Highly efficient debugging can be performed when connected to the host machine and PROM programmer. |
| | IE-75300-R-EM | This is an emulation board for evaluating application systems using the μPD75P3116.<br>It is used in combination with the IE-75001-R. |
| | EP-753108GC-R<br>EV-9200GC-64 | This is an emulation probe for the μPD75P3116GC.<br>When being used, it is connected with the IE-75001-R and the IE-75300-R-EM.<br>It includes a 64-pin conversion socket (EV-9200GC-64) to facilitate connection with the target system. |
| | EP-753108GK-R<br>TGK-064SBW Note 1 | This is an emulation probe for the μPD75P3116GK.<br>When being used, it is connected with the IE-75001-R and the IE-75300-R-EM.<br>It includes a 64-pin conversion adapter (TGK-064SBW) to facilitate connection with the target system. |
| Software | IE control program | This program can control the IE-75001-R on a host machine when connected to the IE-75001-R via an RS-232C or Centronics interface. |

| Host machine | OS | Supply medium | Part number (Product name) |
|---|---|---|---|
| PC-9800 Series | MS-DOS (Ver.3.30 to Ver.6.2 Note 2) | 3.5" 2HD | μS5A13IE75X |
| IBM PC/AT or compatible | Refer to **OS for IBM PCs** | 3.5" 2HC | μS7B13IE75X |

★ **Notes 1.** This is a product of TOKYO ELETECH CORPORATION.

Contact: Daimaru Kogyo, Ltd. Tokyo Electronic Department (TEL: +81-3-3820-7112)

Osaka Electronic Department (TEL: +81-6-6244-6672)

**2.** Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

**Remarks 1.** Operation of the IE control program is guaranteed only when using the host machine and OS described above.

**2.** The μPD753104, 753106, 753108, and 75P3116 are generically called the μPD753108 Subseries.

### OS for IBM PCs

The following operating systems for IBM PCs are supported.

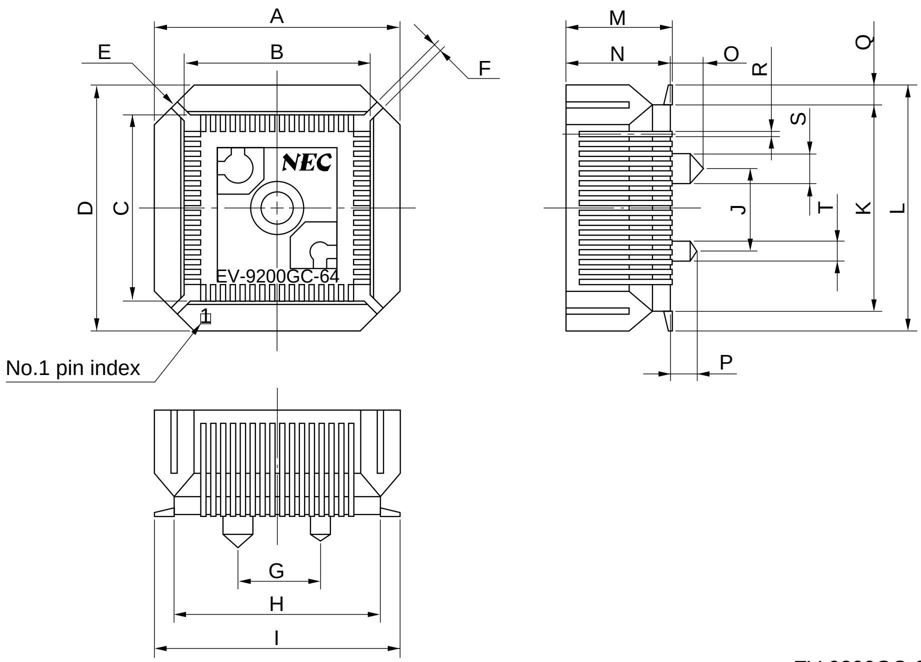
| OS | Version |
|---|---|
| PC DOS™ | Ver.3.1 to 6.3<br>J6.1/V[Note] to J6.3/V[Note] |
| MS-DOS | Ver.5.0 to 6.2<br>5.0/V[Note] to 6.2/V[Note] |
| IBM DOS™ | J5.02/V[Note] |

**Note** Only English mode is supported.

**Caution Ver. 5.0 and later include a task swapping function, but this function cannot be used in this software.**

## ★ Package Drawing and Recommended Footprint of Conversion Socket (EV-9200GC-64)

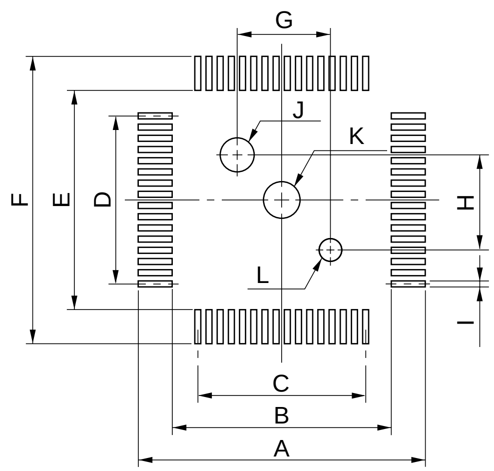
**Figure B-1. EV-9200GC-64 Package Drawing (For Reference Only)**




EV-9200GC-64-G0E

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 18.8 | 0.74 |
| B | 14.1 | 0.555 |
| C | 14.1 | 0.555 |
| D | 18.8 | 0.74 |
| E | 4-C 3.0 | 4-C 0.118 |
| F | 0.8 | 0.031 |
| G | 6.0 | 0.236 |
| H | 15.8 | 0.622 |
| I | 18.5 | 0.728 |
| J | 6.0 | 0.236 |
| K | 15.8 | 0.622 |
| L | 18.5 | 0.728 |
| M | 8.0 | 0.315 |
| N | 7.8 | 0.307 |
| O | 2.5 | 0.098 |
| P | 2.0 | 0.079 |
| Q | 1.35 | 0.053 |
| R | $0.35\pm0.1$ | $0.014^{+0.004}_{-0.005}$ |
| S | $\phi$2.3 | $\phi$0.091 |
| T | $\phi$1.5 | $\phi$0.059 |

**Figure B-2. EV-9200GC-64 Recommended Footprint (For Reference Only)**



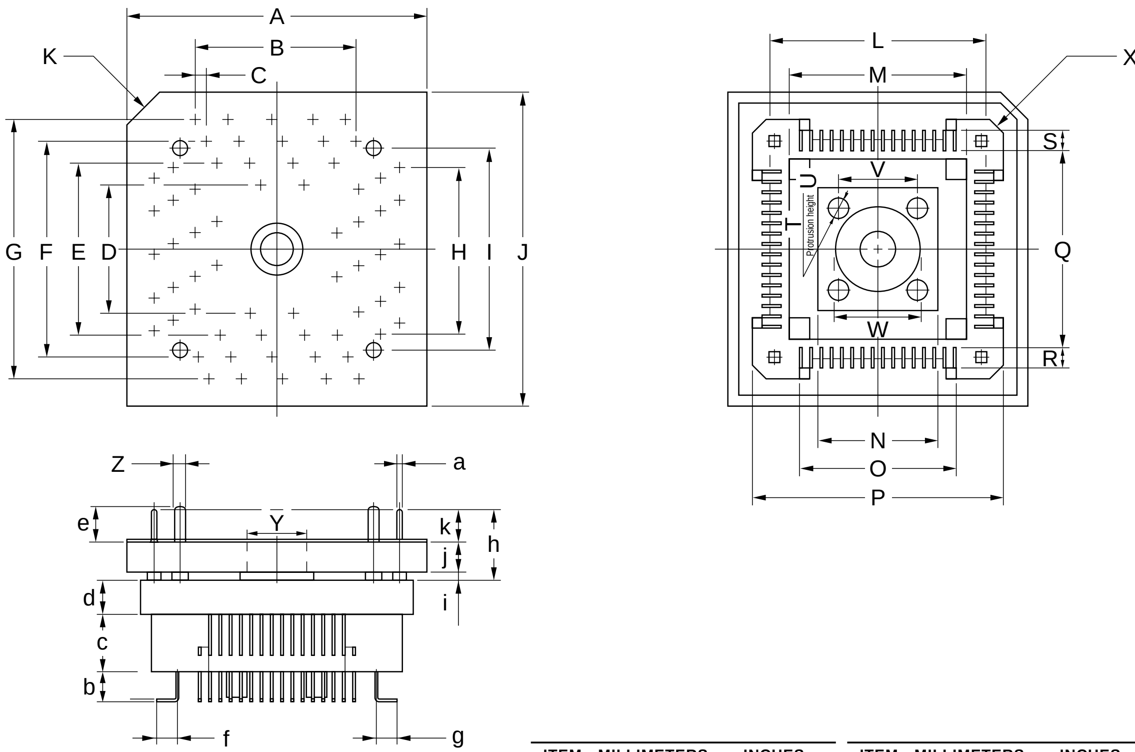

EV-9200GC-64-P1E

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 19.5 | 0.768 |
| B | 14.8 | 0.583 |
| C | 0.8±0.02 × 15=12.0±0.05 | $0.031^{+0.002}_{-0.001}$ × 0.591=$0.472^{+0.003}_{-0.002}$ |
| D | 0.8±0.02 × 15=12.0±0.05 | $0.031^{+0.002}_{-0.001}$ × 0.591=$0.472^{+0.003}_{-0.002}$ |
| E | 14.8 | 0.583 |
| F | 19.5 | 0.768 |
| G | 6.00±0.08 | $0.236^{+0.004}_{-0.003}$ |
| H | 6.00±0.08 | $0.236^{+0.004}_{-0.003}$ |
| I | 0.5±0.02 | $0.197^{+0.001}_{-0.002}$ |
| J | $\phi$2.36±0.03 | $\phi 0.093^{+0.001}_{-0.002}$ |
| K | $\phi$2.2±0.1 | $\phi 0.087^{+0.004}_{-0.005}$ |
| L | $\phi$1.57±0.03 | $\phi 0.062^{+0.001}_{-0.002}$ |

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

## ★ Package Drawing of Conversion Adapter (TGK-064SBW)

### Figure B-3. TGK-064SBW Package Drawing (For Reference Only)




| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 18.4 | 0.724 |
| B | 0.65x15=9.75 | 0.026x0.591=0.384 |
| C | 0.65 | 0.026 |
| D | 7.75 | 0.305 |
| E | 10.15 | 0.400 |
| F | 12.55 | 0.494 |
| G | 14.95 | 0.589 |
| H | 0.65x15=9.75 | 0.026x0.591=0.384 |
| I | 11.85 | 0.467 |
| J | 18.4 | 0.724 |
| K | C 2.0 | C 0.079 |
| L | 12.45 | 0.490 |
| M | 10.25 | 0.404 |
| N | 7.7 | 0.303 |
| O | 10.02 | 0.394 |
| P | 14.92 | 0.587 |
| Q | 11.1 | 0.437 |
| R | 1.45 | 0.057 |
| S | 1.45 | 0.057 |
| T | 4-$\phi$1.3 | 4-$\phi$0.051 |
| U | 1.8 | 0.071 |
| V | 5.0 | 0.197 |
| W | $\phi$5.3 | $\phi$0.209 |
| X | 4-C 1.0 | 4-C 0.039 |
| Y | $\phi$3.55 | $\phi$0.140 |
| Z | $\phi$0.9 | $\phi$0.035 |

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| a | $\phi$0.3 | $\phi$0.012 |
| b | 1.85 | 0.073 |
| c | 3.5 | 0.138 |
| d | 2.0 | 0.079 |
| e | 3.9 | 0.154 |
| f | 1.325 | 0.052 |
| g | 1.325 | 0.052 |
| h | 5.9 | 0.232 |
| i | 0.8 | 0.031 |
| j | 2.4 | 0.094 |
| k | 2.7 | 0.106 |

**TGK-064SBW-G1E**

## ★ Notes on Target System Design

The following shows a diagram of the connection conditions between the emulation probe, conversion connector and conversion socket or conversion adapter.

Design your system making allowances for conditions such as the form of parts mounted on the target system, as shown below.

**Table B-1. Distance Between In-Circuit Emulator and Conversion Socket**

| Emulation Probe | Conversion Socket/ Conversion Adapter | Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter |
|---|---|---|
| EP-753108GC-R | EV-9200GC-64 | 700 mm |
| EP-753108GK-R | TGK-064SBW | 700 mm |

**Figure B-4. Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter (1)**

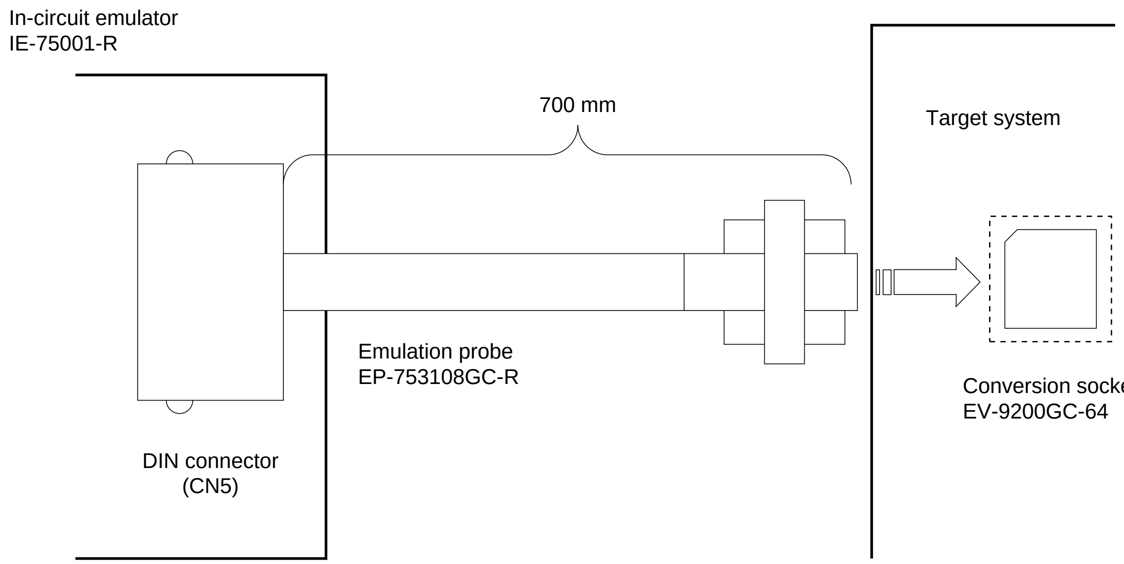



**Figure B-5. Distance Between In-Circuit Emulator and Conversion Socket or Conversion Adapter (2)**

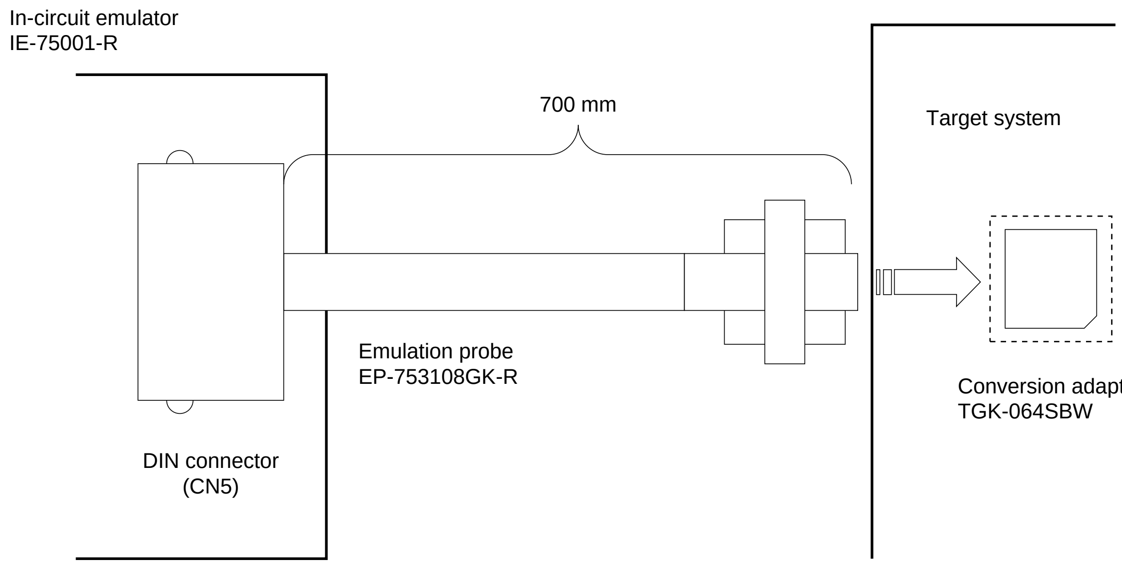


**Figure B-6. Connection Conditions of Target System (1)**

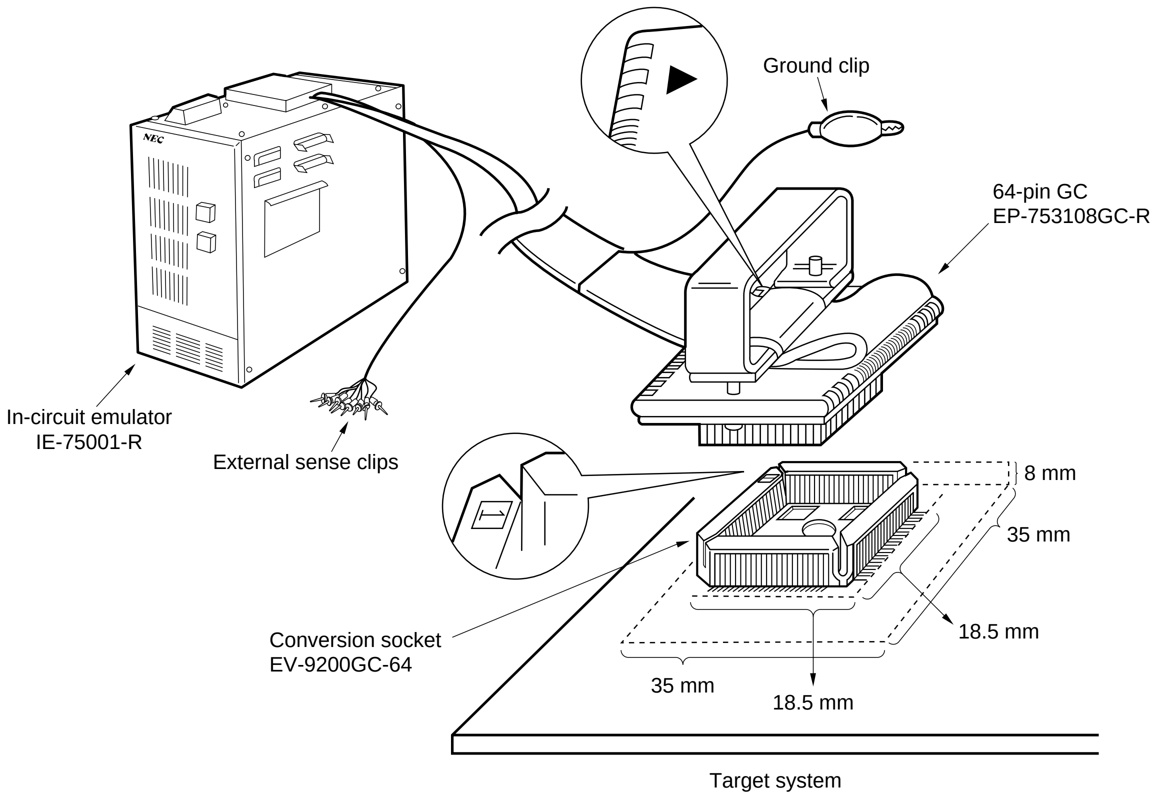
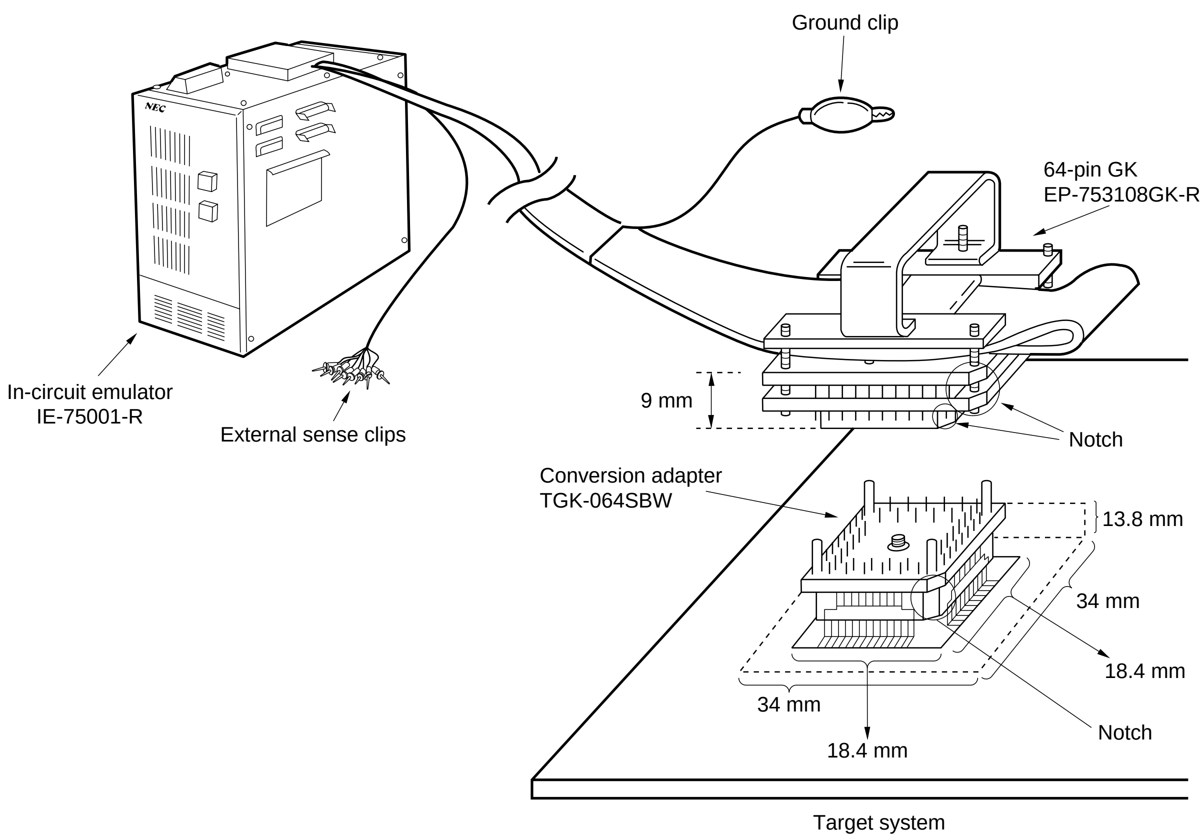



**Figure B-7. Connection Conditions of Target System (2)**



## ★ APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### Documents Related to Devices

| Document Name | Document No. |
|---|---|
| μPD753104, 753106, 753108 Data Sheet | U10086E |
| μPD75P3116 Data Sheet | This document |
| μPD753108 User's Manual | U10890E |
| 75XL Series Selection Guide | U10453E |

### Documents Related to Development Tools (Software) (User's Manuals)

| Document Name | | Document No. |
|---|---|---|
| RA75X Assembler Package | Operation | U12622E |
| | Language | U12385E |
| | Structured Assembler Preprocessor | U12598E |

### Documents Related to Development Tools (Hardware) (User's Manuals)

| Document Name | Document No. |
|---|---|
| IE-75000-R, IE-75001-R In-Circuit Emulator | EEU-1455 |
| IE-75300-R-EM Emulation Board | U11354E |
| EP-753108GC-R, EP-753108GK-R Emulation Probe | EEU-1495 |

### Documents Related to PROM Writing (User's Manuals)

| Document Name | | Document No. |
|---|---|---|
| PG-1500 PROM Programmer | | U11940E |
| PG-1500 Controller | PC-9800 Series (MS-DOS) Based | EEU-1291 |
| | IBM PC Series (PC DOS) Based | U10540E |

**Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.**

### Other Related Documents

| Document Name | Document No. |
|---|---|
| SEMICONDUCTOR SELECTION GUIDE – Products & Packages – | X13769E |
| Semiconductor Device Mounting Technology Manual | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892E |

**Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.**

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

**NEC Electronics Inc. (U.S.)**
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

**NEC do Brasil S.A.**
Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

**NEC Electronics (Europe) GmbH**
Duesseldorf, Germany
Tel: 0211-65 03 01
Fax: 0211-65 03 327

- Branch The Netherlands
Eindhoven, The Netherlands
Tel: 040-244 58 45
Fax: 040-244 45 80

- Branch Sweden
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

**NEC Electronics (France) S.A.**
Vélizy-Villacoublay, France
Tel: 01-3067-58-00
Fax: 01-3067-58-99

**NEC Electronics (France) S.A.**
**Representación en España**
Madrid, Spain
Tel: 091-504-27-87
Fax: 091-504-28-60

**NEC Electronics Italiana S.R.L.**
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

**NEC Electronics (UK) Ltd.**
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

**NEC Electronics Hong Kong Ltd.**
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

**NEC Electronics Hong Kong Ltd.**
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

**NEC Electronics Shanghai, Ltd.**
Shanghai, P.R. China
Tel: 021-6841-1138
Fax: 021-6841-1137

**NEC Electronics Taiwan Ltd.**
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

**NEC Electronics Singapore Pte. Ltd.**
Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

J02.3