

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA1742TP is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

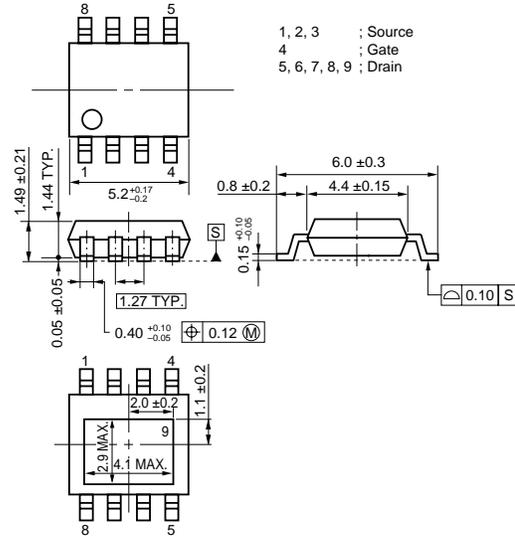
FEATURES

- High voltage: $V_{BSS} = 250$ V
- Gate voltage rating: ± 30 V
- Low on-state resistance
 $R_{DS(on)} = 0.55 \Omega$ MAX. ($V_{GS} = 10$ V, $I_D = 3.5$ A)
- Low input capacitance
 $C_{iss} = 460$ pF TYP. ($V_{DS} = 10$ V, $V_{GS} = 0$ V)
- Built-in gate protection diode
- Small and surface mount package (Power HSOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1742TP	Power HSOP8

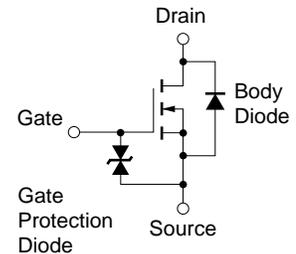
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted. All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0$ V)	V_{DSS}	250	V
Gate to Source Voltage ($V_{DS} = 0$ V)	V_{GSS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 7.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 21	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	24	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	7.0	A
Single Avalanche Energy ^{Note3}	E_{AS}	4.9	mJ
Repetitive Avalanche Current ^{Note4}	I_{AR}	7.0	A
Repetitive Pulse Avalanche Energy ^{Note4}	E_{AR}	4.9	mJ

EQUIVALENT CIRCUIT



- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$
 2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm
 3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 125$ V, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = 20 \rightarrow 0$ V
 4. $T_{ch(peak)} \leq 150^\circ\text{C}$, $L = 100 \mu\text{H}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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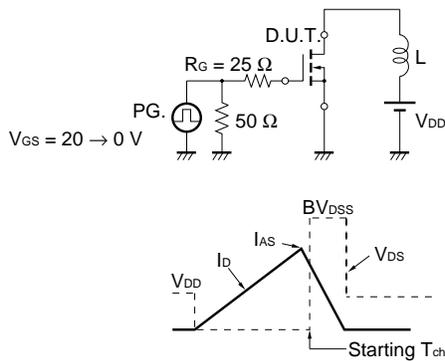
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted. All terminals are connected.)

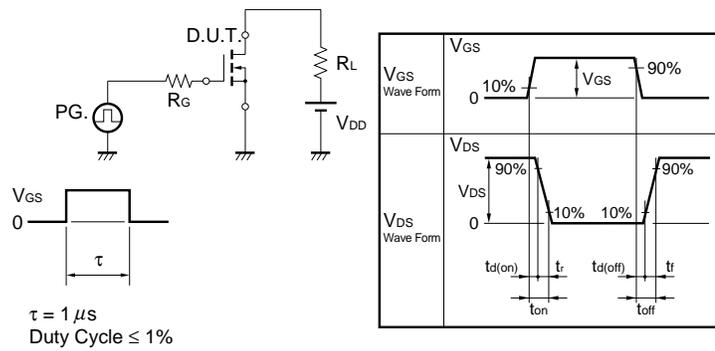
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 250 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5	3.5	4.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	2.5	5		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 3.5 A		0.41	0.55	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		460		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		100		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		45		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 125 V, I _D = 3.5 A		11		ns
Rise Time	t _r	V _{GS} = 10 V		9		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		24		ns
Fall Time	t _f			8		ns
Total Gate Charge	Q _G	V _{DD} = 200 V		14		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		3		nC
Gate to Drain Charge	Q _{GD}	I _D = 7.0 A		7		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 7.0 A, V _{GS} = 0 V		0.9	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 7.0 A, V _{GS} = 0 V		140		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		560		nC

Note Pulsed: PW ≤ 800 μs, Duty Cycle ≤ 2%

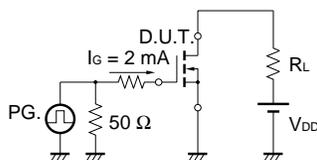
TEST CIRCUIT 1 AVALANCHE CAPABILITY



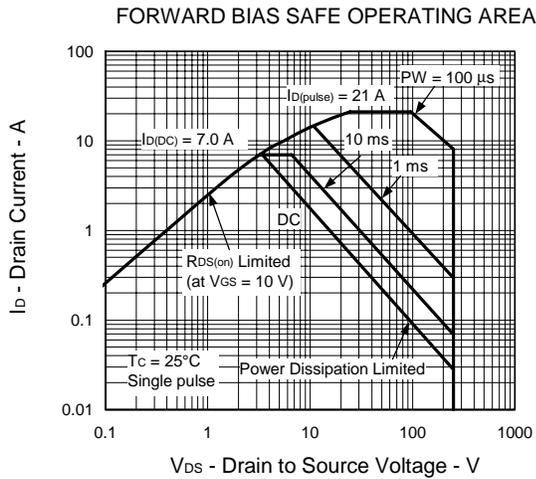
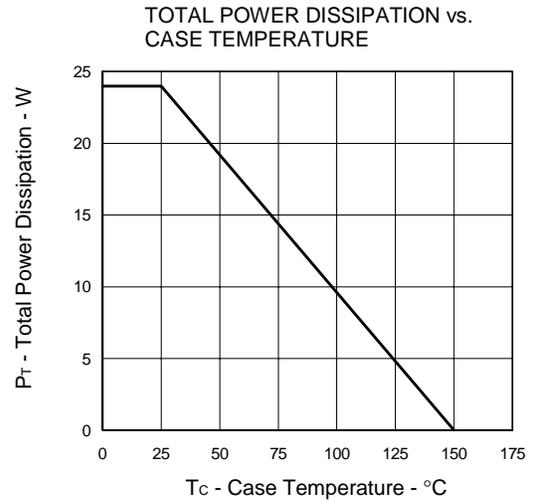
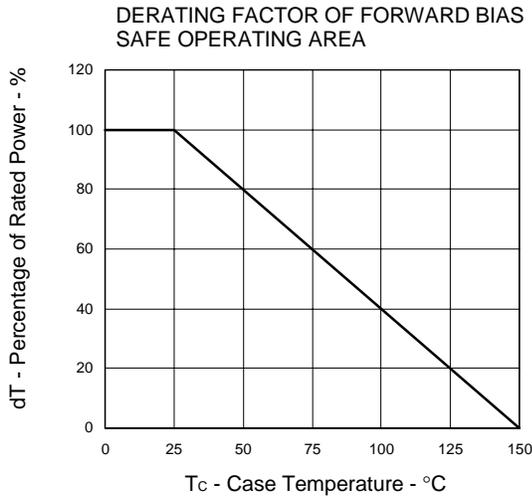
TEST CIRCUIT 2 SWITCHING TIME



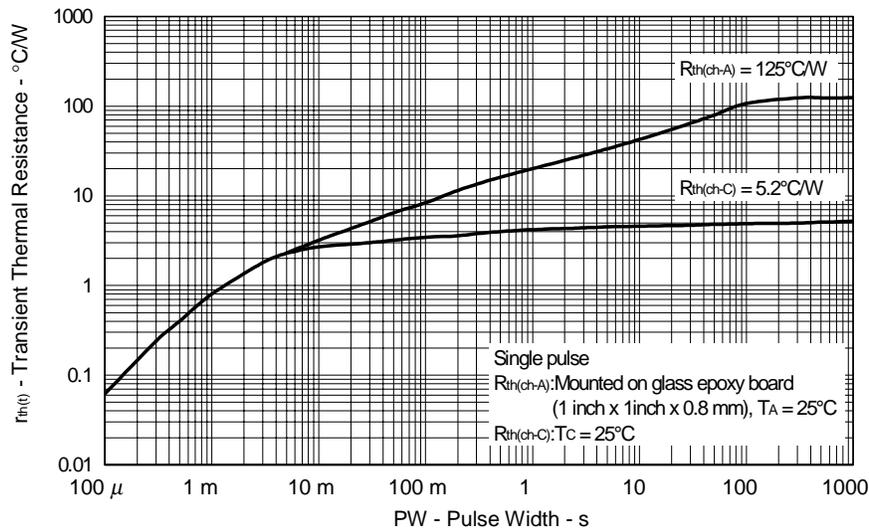
TEST CIRCUIT 3 GATE CHARGE



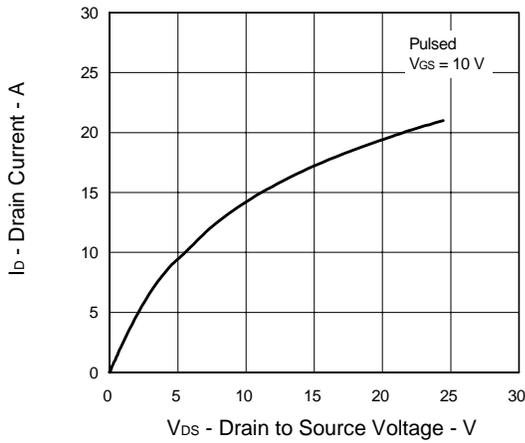
TYPICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted. All terminals are connected.)



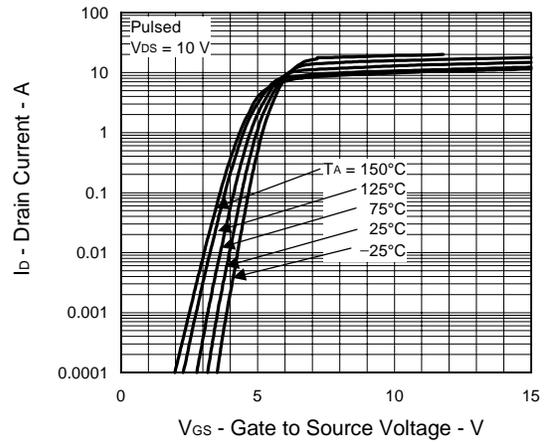
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



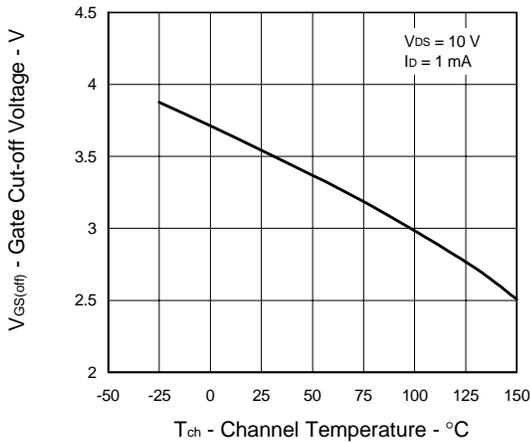
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



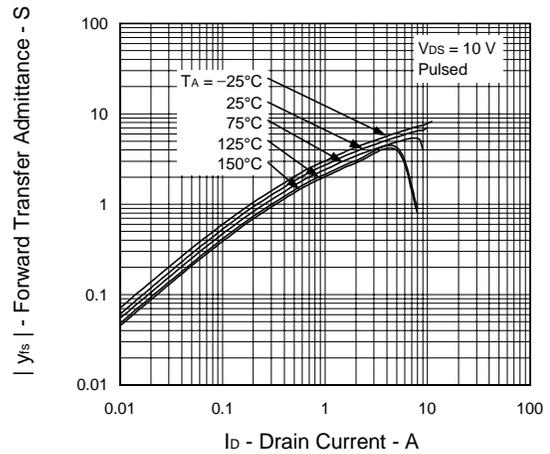
FORWARD TRANSFER CHARACTERISTICS



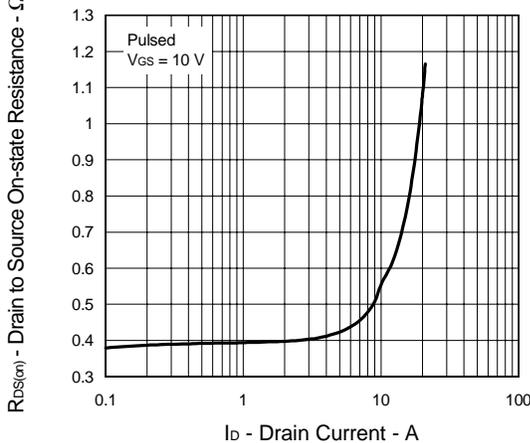
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



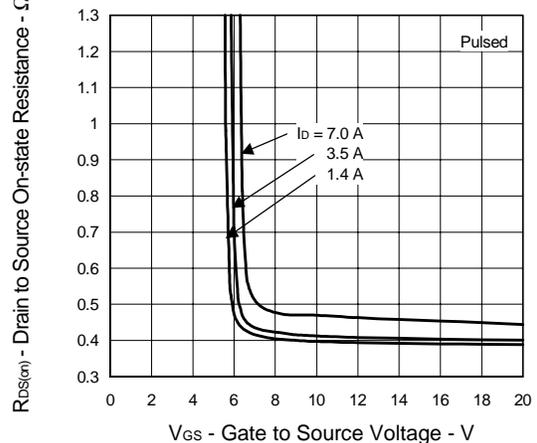
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



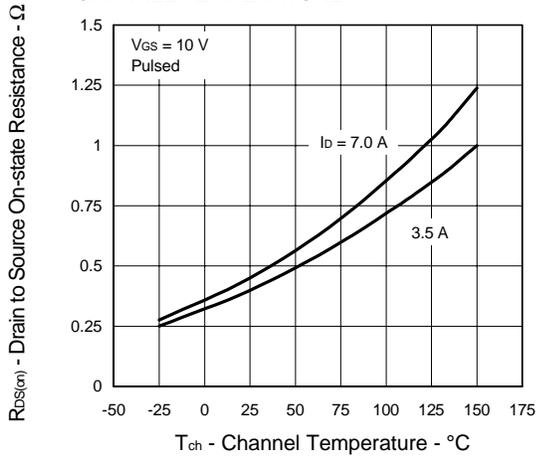
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



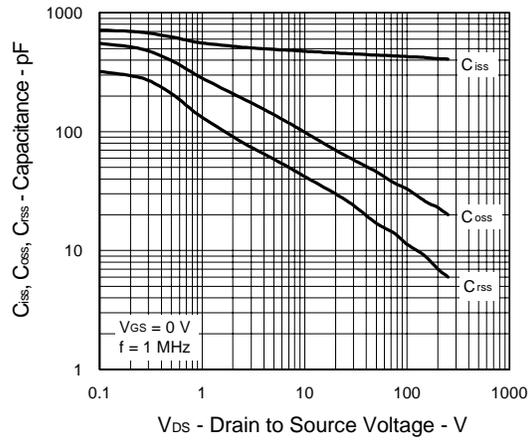
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



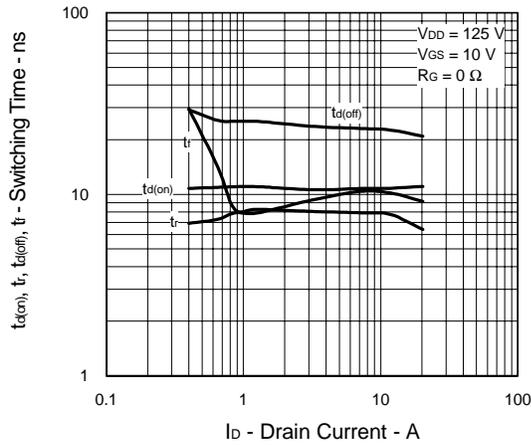
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



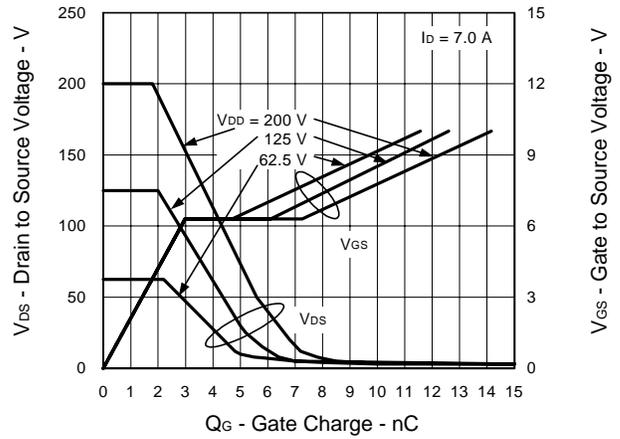
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



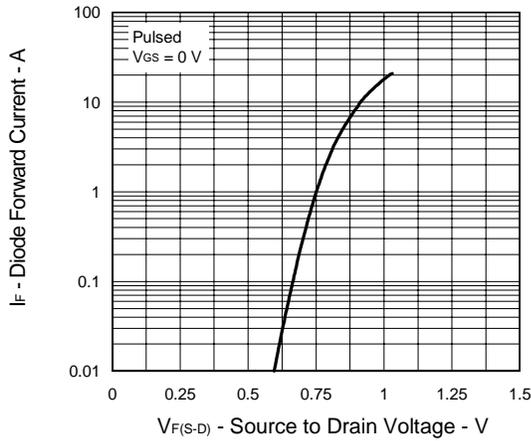
SWITCHING CHARACTERISTICS



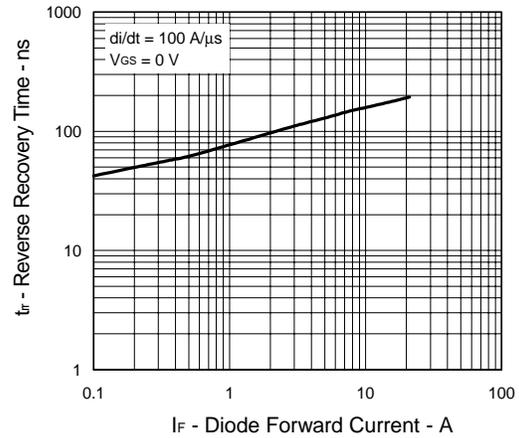
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

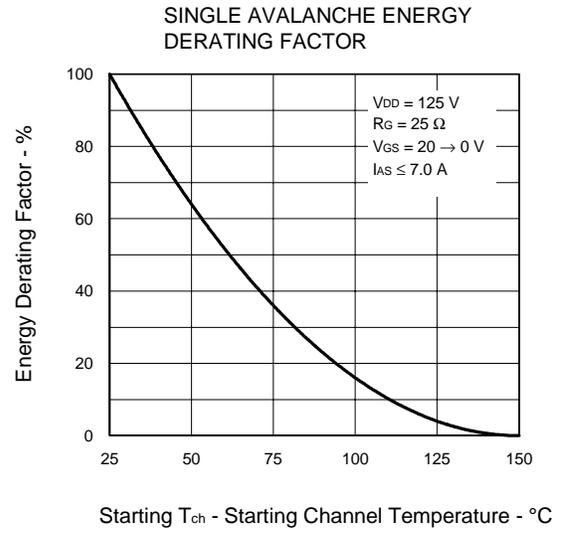
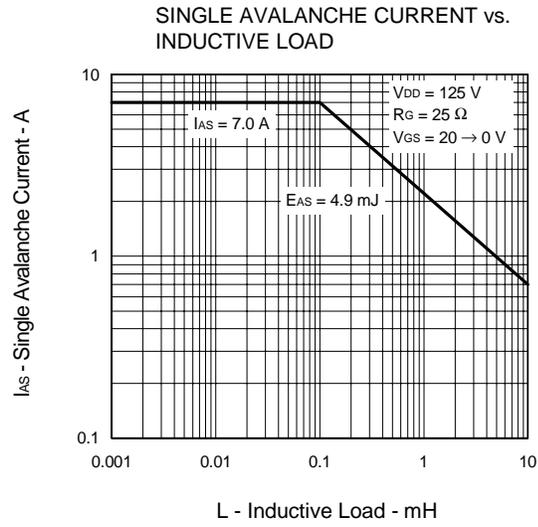


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT





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