NEC

User's Manual

μPD789104A, 789114A, 789124A, 789134A Subseries

8-Bit Single-Chip Microcontrollers

μPD789101A
μPD789102A
μPD789104A
μPD789111A
μPD789112A
μPD789114A
μPD78F9116A
μPD78F9116B
μPD789101A(A)
μPD789102A(A)
μPD789104A(A)
μPD789111A(A)
μPD789112A(A)
μPD789114A(A)
μPD78F9116B(A)
μPD789101A(A1)
μPD789102A(A1)
μPD789104A(A1)
μPD789111A(A1)
μPD789112A(A1)
μPD789114A(A1)
μPD78F9116B(A1)
μPD789101A(A2)
μPD789102A(A2)
μPD789104A(A2)
μPD789111A(A2)
μPD789112A(A2)
μPD789114A(A2)
μPD789121A
μPD789122A
μPD789124A
μPD789131A
μPD789132A
μPD789134A
μPD78F9136A
μPD78F9136B
μPD789121A(A)
μPD789122A(A)
μPD789124A(A)
μPD789131A(A)
μPD789132A(A)
μPD789134A(A)
μPD78F9136B(A)
μPD789121A(A1)
μPD789122A(A1)
μPD789124A(A1)
μPD789131A(A1)
μPD789132A(A1)
μPD789134A(A1)
μPD78F9136B(A1)
μPD789121A(A2)
μPD789122A(A2)
μPD789124A(A2)
μPD789131A(A2)
μPD789132A(A2)
μPD789134A(A2)

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Major Revisions in This Edition

Pages	Description
Throughout	• Addition of μPD789101A(A1), 789102A(A1), 789104A(A1), 789111A(A1), 789112A(A1), 789114A(A1), 789121A(A1), 789122A(A1), 789124A(A1), 789131A(A1), 789132A(A1), 789134A(A1), 789101A(A2), 789102A(A2), 789104A(A2), 789111A(A2), 789112A(A2), 789114A(A2), 789121A(A2), 789122A(A2), 789124A(A2), 789131A(A2), 789132A(A2), 789134A(A2), 78F9116B, 78F9136B, 78F9116B(A), 78F9136B(A), 78F9116B(A1), 78F9136B(A1) • Addition of description related to expanded-specification products
pp.24, 36	**CHAPTER 1 GENERAL (μPD789104A, 789114A SUBSERIES)** • Addition of **1.1 Expanded-Specification Products and Conventional-Specification Products** • Addition of **1.10 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**
p.48	**CHAPTER 2 GENERAL (μPD789124A, 789134A SUBSERIES)** • Addition of **2.9 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**
pp.116 to 118, 121	**CHAPTER 8 16-BIT TIMER 20** • Modification of description in **8.4.1 Operation as timer interrupt** • Modification of **Figure 8-5 Timing of Timer Interrupt Operation** • Modification of description in **8.4.2 Operation as timer output** • Modification of description in **Figure 8-7 Timer Output Timing** • Addition of **8.5 Notes on Using 16-Bit Timer 20**
p.134	**CHAPTER 9 8-BIT TIMER/EVENT COUNTER 80** • Addition of description to **9.5 Notes on Using 8-Bit Timer/Event Counter 80**
p.152	**CHAPTER 11 8-BIT A/D CONVERTER (μPD789104A, 789124A SUBSERIES)** • Addition of **11.5 (8) Input impedance of ANI0 to ANI3 pins**
pp.155, 164	**CHAPTER 12 10-BIT A/D CONVERTER (μPD789114A, 789134A SUBSERIES)** • Modification of description in **12.2 (2) A/D conversion result register 0 (ADCR0)** • Addition of **12.5 (8) Input impedance of ANI0 to ANI3 pins**
pp.167, 177, 190	**CHAPTER 13 SERIAL INTERFACE 20** • Modification of **Figure 13-1 Block Diagram of Serial Interface 20** • Addition of **13.3 (4) (c) Generation of serial clock from system clock in 3-wire serial I/O mode** • Addition of **13.4.2 (2) (f) Reading receive data**
p.210	**CHAPTER 15 INTERRUPT FUNCTIONS** • Addition of **Caution 3** in **Figure 15-2 Format of Interrupt Request Flag Register**
p.233	Revision of **CHAPTER 18 μPD78F9116A, 78F9116B, 78F9136A, 78F9136B**
p.258	Addition of **CHAPTER 21** to **CHAPTER 31 ELECTRICAL SPECIFICATIONS**
p.387	Addition of **CHAPTER 32** and **CHAPTER 33 CHARACTERISTICS CURVES (REFERENCE VALUES)**
p.393	Addition of **CHAPTER 34** and **CHAPTER 35 EXAMPLE OF RC OSCILLATOR FREQUENCY CHARACTERISTICS (REFERENCE VALUES)**
p.397	Addition of **CHAPTER 36 PACKAGE DRAWING**
p.398	Addition of **CHAPTER 37 RECOMMENDED SOLDERING CONDITIONS**
p.400	Revision of **APPENDIX A DEVELOPMENT TOOLS**
p.406	Addition of **APPENDIX B NOTES ON TARGET SYSTEM DESIGN**
p.412	Addition of **APPENDIX D REVISION HISTORY**
p.257 in 1st edition	Deletion of **APPENDIX B EMBEDDED SOFTWARE**

The mark ★ shows major revised points.

Target Readers

This manual is intended for users who wish to understand the functions of the μPD789104A, 789114A, 789124A, 789134A Subseries and to design and develop application systems and programs using these microcontrollers.

The target devices are shown as follows:

- μPD789104A Subseries: μPD789101A, 789102A, 789104A, 789101A(A), 789102A(A), 789104A(A), 789101A(A1), 789102A(A1), 789104A(A1), 789101A(A2), 789102A(A2), 789104A(A2)
- μPD789114A Subseries: μPD789111A, 789112A, 789114A, 78F9116A, 78F9116B, 789111A(A), 789112A(A), 789114A(A), 78F9116B(A), 789111A(A1), 789112A(A1), 789114A(A1), 78F9116B(A1), 789111A(A2), 789112A(A2), 789114A(A2)
- μPD789124A Subseries: μPD789121A, 789122A, 789124A, 789121A(A), 789122A(A), 789124A(A), 789121A(A1), 789122A(A1), 789124A(A1), 789121A(A2), 789122A(A2), 789124A(A2)
- μPD789134A Subseries: μPD789131A, 789132A, 789134A, 78F9136A, 78F9136B, 789131A(A), 789132A(A), 789134A(A), 78F9136B(A), 789131A(A1), 789132A(A1), 789134A(A1), 78F9136B(A1), 789131A(A2), 789132A(A2), 789134A(A2)

The μPD789104A/114A/124A/134A Subseries is a generic term for all the target devices in this manual.

Generic names in this document indicate the following products.

[Standard quality grade products] μPD789101A, 789102A, 789104A, 789111A, 789112A, 789114A, 78F9116A, 78F9116B, 789121A, 789122A, 789124A, 789131A, 789132A, 789134A, 78F9136A, 78F9136B

[(A) products] μPD789101A(A), 789102A(A), 789104A(A), 789111A(A), 789112A(A), 789114A(A), 78F9116B(A), 789121A(A), 789122A(A), 789124A(A), 789131A(A), 789132A(A), 789134A(A), 78F9136B(A)

[(A1) products] μPD789101A(A1), 789102A(A1), 789104A(A1), 789111A(A1), 789112A(A1), 789114A(A1), 78F9116B(A1), 789121A(A1), 789122A(A1), 789124A(A1), 789131A(A1), 789132A(A1), 789134A(A1), 78F9136B(A1)

[(A2) products] μPD789101A(A2), 789102A(A2), 789104A(A2), 789111A(A2), 789112A(A2), 789114A(A2), 789121A(A2), 789122A(A2), 789124A(A2), 789131A(A2), 789132A(A2), 789134A(A2)

[Mask ROM products] μPD789101A, 789102A, 789104A, 789111A, 789112A, 789114A, 789121A, 789122A, 789124A, 789131A, 789132A, 789134A, 789101A(A), 789102A(A), 789104A(A), 789111A(A), 789112A(A), 789114A(A), 789121A(A), 789122A(A), 789124A(A), 789131A(A), 789132A(A), 789134A(A), 789101A(A1), 789102A(A1), 789104A(A1), 789111A(A1), 789112A(A1), 789114A(A1), 789121A(A1), 789122A(A1), 789124A(A1), 789131A(A1), 789132A(A1), 789134A(A1), 789101A(A2), 789102A(A2), 789104A(A2), 789111A(A2), 789112A(A2), 789114A(A2), 789121A(A2), 789122A(A2), 789124A(A2), 789131A(A2), 789132A(A2), 789134A(A2)

[Flash memory products] μPD78F9116A, 78F9116B, 78F9116B(A), 78F9116B(A1), 78F9136A, 78F9136B, 78F9136B(A), 78F9136B(A1)

The oscillation frequency of the system clock is regarded as f_X for ceramic/crystal oscillation (μPD789104A and 789114A Subseries), and regarded as f_{CC} for an RC oscillation (μPD789124A and 789134A Subseries).

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual is divided into two parts: this manual and instructions (common to the 78K/0S Series).

μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual (This manual)	78K/0S Series Instructions User's Manual
• Pin functions • Internal block functions • Interrupts • Other internal peripheral functions • Electrical specifications	• CPU function • Instruction set • Instruction description

How to Read This Manual It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

☐ When using this manual as a manual for the μPD789101A(A), 789102A(A), 789104A(A), 789111A(A), 789112A(A), 789114A(A), 78F9116B(A), 789121A(A), 789122A(A), 789124A(A), 789131A(A), 789132A(A), 789134A(A), 78F9136B(A), 789101A(A1), 789102A(A1), 789104A(A1), 789111A(A1), 789112A(A1), 789114A(A1), 78F9116B(A1), 789121A(A1), 789122A(A1), 789124A(A1), 789131A(A1), 789132A(A1), 789134A(A1), 78F9136B(A1), 789101A(A2), 789102A(A2), 789104A(A2), 789111A(A2), 789112A(A2), 789114A(A2), 789121A(A2), 789122A(A2), 789124A(A2), 789131A(A2), 789132A(A2), and 789134A(A2)

→ Only the quality grade, supply voltage, operating ambient temperature, minimum instruction execution time, and electrical specifications differ from the μPD789101A, 789102A, 789104A, 789111A, 789112A, 789114A, 78F9116B, 789121A, 789122A, 789124A, 789131A, 789132A, 789134A, and 78F9136B (refer to **1.10 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**, **2.9 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**). For the (A), (A1), and (A2) products, read the part numbers in CHAPTER 3 to CHAPTER 20 as follows.

μPD789101A → μPD789101A(A), 789101A(A1), 789101A(A2)
μPD789102A → μPD789102A(A), 789102A(A1), 789102A(A2)
μPD789104A → μPD789104A(A), 789104A(A1), 789104A(A2)
μPD789111A → μPD789111A(A), 789111A(A1), 789111A(A2)
μPD789112A → μPD789112A(A), 789112A(A1), 789112A(A2)
μPD789114A → μPD789114A(A), 789114A(A1), 789114A(A2)
μPD78F9116B → μPD78F9116B(A), 78F9116B(A1)
μPD789121A → μPD789121A(A), 789121A(A1), 789121A(A2)
μPD789122A → μPD789122A(A), 789122A(A1), 789122A(A2)
μPD789124A → μPD789124A(A), 789124A(A1), 789124A(A2)
μPD789131A → μPD789131A(A), 789131A(A1), 789131A(A2)
μPD789132A → μPD789132A(A), 789132A(A1), 789132A(A2)
μPD789134A → μPD789134A(A), 789134A(A1), 789134A(A2)
μPD78F9136B → μPD78F9136B(A), 78F9136B(A1)

☐ To understand the overall functions in general
→ Read this manual in the order of the **CONTENTS**.

☐ How to interpret register formats
→ The name of a bit whose number is in angle brackets (<>) is reserved in the assembler and is defined in the C compiler by the header file **sfrbit.h**.

☐ To learn the detailed functions of a register whose register name is known
→ Refer to **APPENDIX C REGISTER INDEX**.

☐ To learn the details of the instruction functions of the 78K/0S Series
→ Refer to **78K/0S Series Instructions User's Manual (U11047E)**.

☐ To know the electrical specifications of the μPD789104A/114A/124A/134A Subseries
→ Refer to **CHAPTER 21** to **CHAPTER 31 ELECTRICAL SPECIFICATIONS**.

Caution The application examples in this manual are created for "Standard" quality grade products for general electric equipment. When using the application examples in this manual for purposes which require "Special" quality grades, thoroughly examine the quality grade of each part and circuit actually used.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{\times\times\times}$ (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary ... ×××× or ××××B
	Decimal ... ××××
	Hexadecimal ... ××××H

★ **Related Documents** The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual	This manual
78K/0S Series Instructions User's Manual	U11047E

Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U14876E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U14871E
	Language	U14872E
SM78K Series System Simulator Ver. 2.30 or Later	Operation (Windows™ Based)	U15373E
	External Part User Open Interface Specification	U15802E
ID78K Series Integrated Debugger Ver. 2.30 or Later	Operation (Windows Based)	U15185E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789136-NS-EM1 Emulation Board	U14363E

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Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products and Packages -	X13769X
Semiconductor Device Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Note See the “Semiconductor Device Mount Manual” website (http://www.necel.com/pkg/en/mount/index.html).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

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CHAPTER 1 GENERAL (μPD789104A, 789114A SUBSERIES)

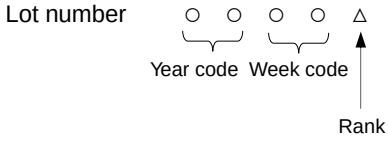
★ 1.1 Expanded-Specification Products and Conventional-Specification Products

The expanded-specification products and the conventional-specification products indicate the following products.

Expanded-specification products..... Products other than rank[Note 1] K
- Mask ROM products ordered on or later than December 1, 2001 (excluding (A1) and (A2) products[Note 2])
- Flash memory products shipped on or later than January 1, 2002 (excluding (A1), (A2) products[Note 2] and the μPD78F9116A)

Conventional-specification products .....Rank[Note 1] K products
- Products other than above

Notes 1. The rank is indicated by the letter at the 5th digit from the left in the lot number in the package marking.



2. For (A1) and (A2) products, refer to **1.10 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**.

The operating frequency specification differs between the expanded-specification products and the conventional-specification products as shown in Table 1-1.

Table 1-1. Differences Between Expanded-Specification Products and Conventional-Specification Products

Supply Voltage (V_{DD})	Guaranteed Operating Speed (Operating Frequency)	
	Conventional-Specification Products	Expanded-Specification Products
4.5 to 5.5 V	5 MHz (0.4 μs)	10 MHz (0.2 μs)
3.0 to 5.5 V	5 MHz (0.4 μs)	6 MHz (0.33 μs)
2.7 to 5.5 V	5 MHz (0.4 μs)	5 MHz (0.4 μs)
1.8 to 5.5 V	1.25 MHz (1.6 μs)	1.25 MHz (1.6 μs)

Remark The figures in parentheses indicate the minimum instruction execution time.

1.2 Features

★ • ROM and RAM capacities

Part Number \ Item	Program Memory		Data Memory (Internal High-Speed RAM)
μPD789101A, 789111A, 789101A(A), 789111A(A), 789101A(A1), 789111A(A1), 789101A(A2), 789111A(A2)	Mask ROM	2 KB	256 bytes
μPD789102A, 789112A, 789102A(A), 789112A(A), 789102A(A1), 789112A(A1), 789102A(A2), 789112A(A2)		4 KB	
μPD789104A, 789114A, 789104A(A), 789114A(A), 789104A(A1), 789114A(A1), 789104A(A2), 789114A(A2)		8 KB	
μPD78F9116A, 78F9116B, 78F9116B(A), 78F9116B(A1)	Flash memory	16 KB	

- System clock: Crystal/ceramic oscillation

★ • Minimum instruction execution times switchable between high speed (0.2 μs) and low speed (0.8 μs) (system clock: 10.0 MHz[Note])

- 20 I/O ports
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode selectable
- 8-bit resolution A/D converter: 4 channels (μPD789104A Subseries)
- 10-bit resolution A/D converter: 4 channels (μPD789114A Subseries)
- 3 timers
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watchdog timer: 1 channel
- Multiplier: 8 bits × 8 bits = 16 bits
- Vectored interrupt sources: 10

★ • Supply voltage
  - V_{DD} = 1.8 to 5.5 V (μPD78910xA, 78911xA, 78910xA(A), 78911xA(A), 78F9116A, 78F9116B, 78F9116B(A))
  - V_{DD} = 4.5 to 5.5 V (μPD78910xA(A1), 78911xA(A1), 78910xA(A2), 78911xA(A2), 78F9116B(A1))

★ • Operating ambient temperature
  - T_A = –40 to + 85°C (μPD78910xA, 78911xA, 78910xA(A), 78911xA(A), 78F9116A, 78F9116B, 78F9116B(A))
  - T_A = –40 to +105°C (μPD78F9116B(A1))
  - T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1))
  - T_A = –40 to +125°C (μPD78910xA(A2), 78911xA(A2))

Note When V_{DD} = 4.5 to 5.5 V and for expanded-specification products only

1.3 Applications

Vacuum cleaners, washing machines, refrigerators, battery chargers, etc.

★ 1.4 Ordering Information

Part Number	Package	Internal ROM
μPD789101AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789102AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789104AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789111AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789112AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789114AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD78F9116AMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD78F9116BMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD789101AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789102AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789104AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789111AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789112AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789114AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD78F9116BMC(A)-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD789101AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789102AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789104AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789111AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789112AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789114AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD78F9116BMC(A1)-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD789101AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789102AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789104AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789111AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789112AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789114AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM

Remark ××× indicates ROM code suffix.

★ 1.5 Quality Grade

Part Number	Package	Quality Grade
μPD789101AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789102AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789104AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789111AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789112AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789114AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD78F9116AMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD78F9116BMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789101AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789102AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789104AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789111AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789112AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789114AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD78F9116BMC(A)-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789101AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789102AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789104AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789111AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789112AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789114AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD78F9116BMC(A1)-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789101AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789102AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789104AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789111AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789112AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789114AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special

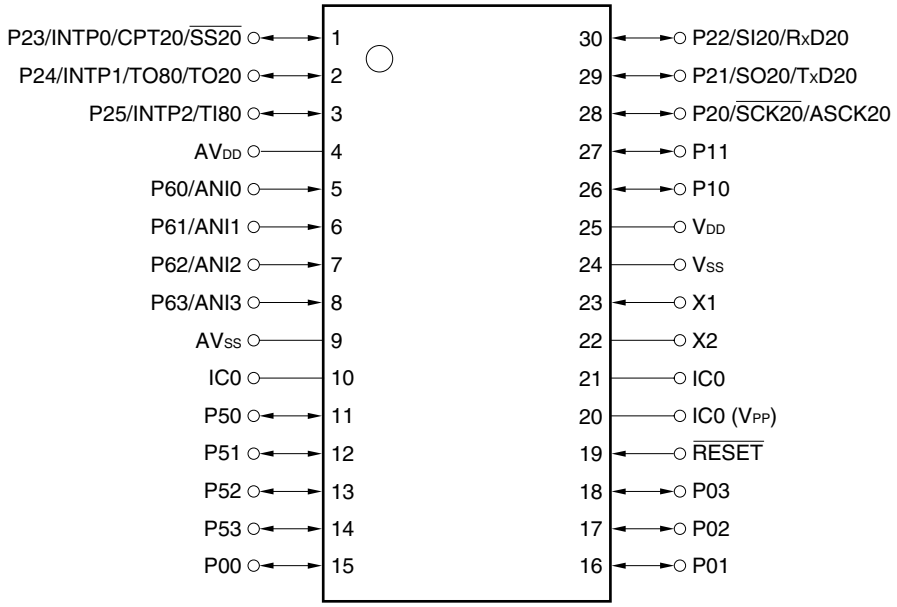
Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

★ 1.6 Pin Configuration (Top View)

- 30-pin plastic SSOP (7.62 mm (300))

μPD789101AMC-×××-5A4 μPD789102AMC-×××-5A4 μPD789104AMC-×××-5A4
μPD789111AMC-×××-5A4 μPD789112AMC-×××-5A4 μPD789114AMC-×××-5A4
μPD78F9116AMC-5A4 μPD78F9116BMC-5A4
μPD789101AMC(A)-×××-5A4 μPD789102AMC(A)-×××-5A4 μPD789104AMC(A)-×××-5A4
μPD789111AMC(A)-×××-5A4 μPD789112AMC(A)-×××-5A4 μPD789114AMC(A)-×××-5A4
μPD78F9116BMC(A)-5A4
μPD789101AMC(A1)-×××-5A4 μPD789102AMC(A1)-×××-5A4 μPD789104AMC(A1)-×××-5A4
μPD789111AMC(A1)-×××-5A4 μPD789112AMC(A1)-×××-5A4 μPD789114AMC(A1)-×××-5A4
μPD78F9116BMC(A1)-5A4
μPD789101AMC(A2)-×××-5A4 μPD789102AMC(A2)-×××-5A4 μPD789104AMC(A2)-×××-5A4
μPD789111AMC(A2)-×××-5A4 μPD789112AMC(A2)-×××-5A4 μPD789114AMC(A2)-×××-5A4



Cautions 1. Connect the IC0 (internally connected) pin directly to the VSS pin.

2. Connect the AVDD pin to the VDD pin.

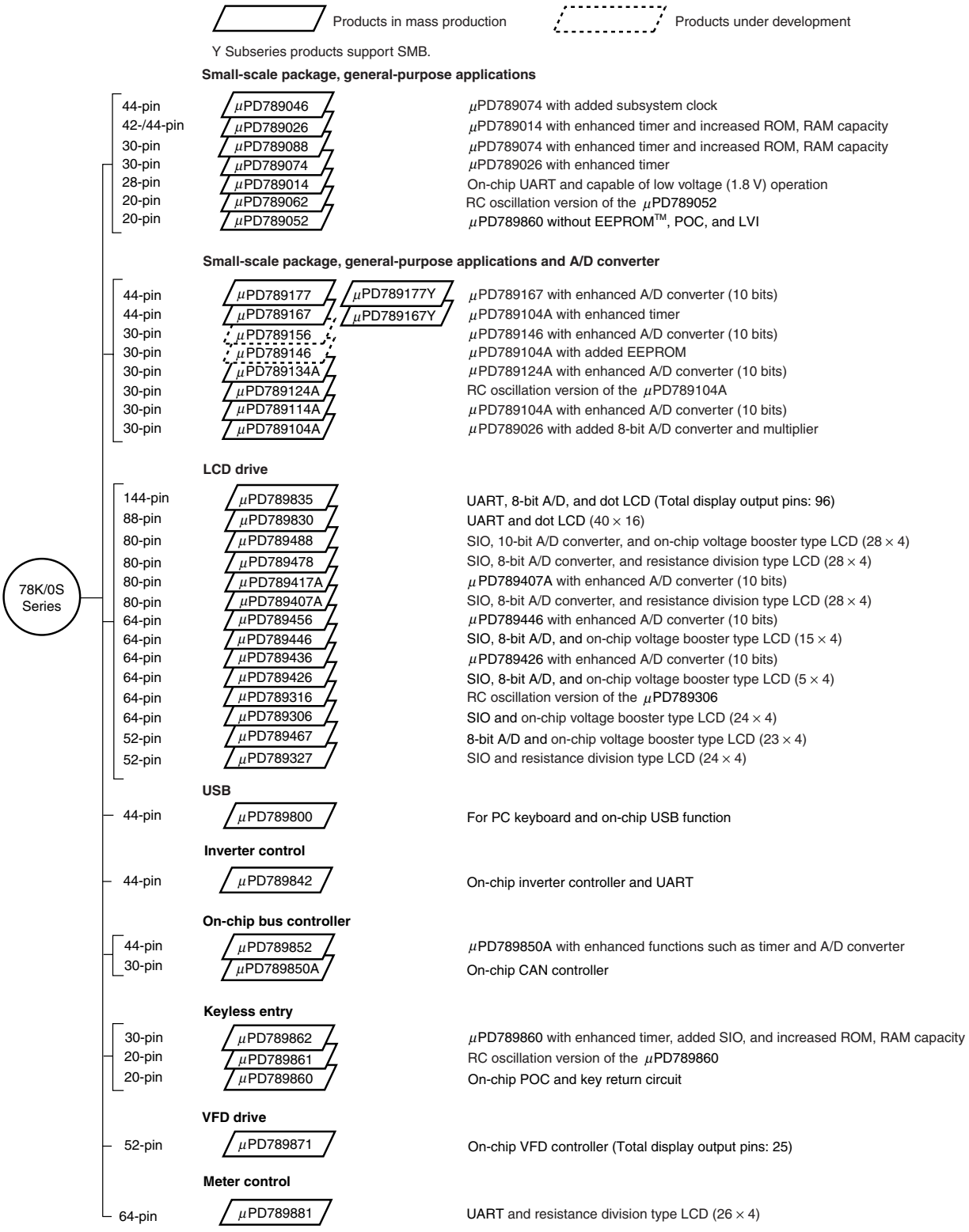
3. Connect the AVSS pin to the VSS pin.

Remark The pin connection in parentheses is intended for the μPD78F9116A, 78F9116B, 78F9116B(A), and 78F9116B(A1).

ANI0 to ANI3:	Analog input	RxD20:	Receive data
ASCK20:	Asynchronous serial input	$\overline{\text{SCK20}}$:	Serial clock
AV_{DD}:	Analog power supply	SI20:	Serial input
AV_{SS}:	Analog ground	SO20:	Serial output
CPT20:	Capture trigger input	$\overline{\text{SS20}}$:	Chip select input
IC0:	Internally connected	TI80:	Timer input
INTP0 to INTP2:	External interrupt input	TO20, TO80:	Timer output
P00 to P03:	Port 0	TxD20:	Transmit data
P10, P11:	Port 1	V_{DD}:	Power supply
P20 to P25:	Port 2	V_{PP}:	Programming power supply
P50 to P53:	Port 5	V_{SS}:	Ground
P60 to P63:	Port 6	X1, X2:	Crystal 1, 2
$\overline{\text{RESET}}$:	Reset		

★ 1.7 78K/0S Series Lineup

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences between the subseries are listed below.

Series for general-purpose applications and LCD drive

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 KB	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 KB to 16 KB			–							
	μPD789088	16 KB to 32 KB	3 ch							24		
	μPD789074	2 KB to 8 KB	1 ch									
	μPD789014	2 KB to 4 KB	2 ch	–						22		
	μPD789062	4 KB							–	14		RC oscillation version
	μPD789052											–
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 KB to 24 KB	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 KB to 16 KB	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 KB to 8 KB					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835	24 KB to 60 KB	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	37	1.8 V[Note]	Dot LCD supported
	μPD789830	24 KB	1 ch	1 ch			–			30	2.7 V	
	μPD789488	32 KB to 48 KB	3 ch					8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789478	24 KB to 48 KB					8 ch	–				
	μPD789417A	12 KB to 24 KB					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 KB to 16 KB	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 KB to 16 KB					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789467	4 KB to 24 KB		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note Flash memory version: 3.0 V

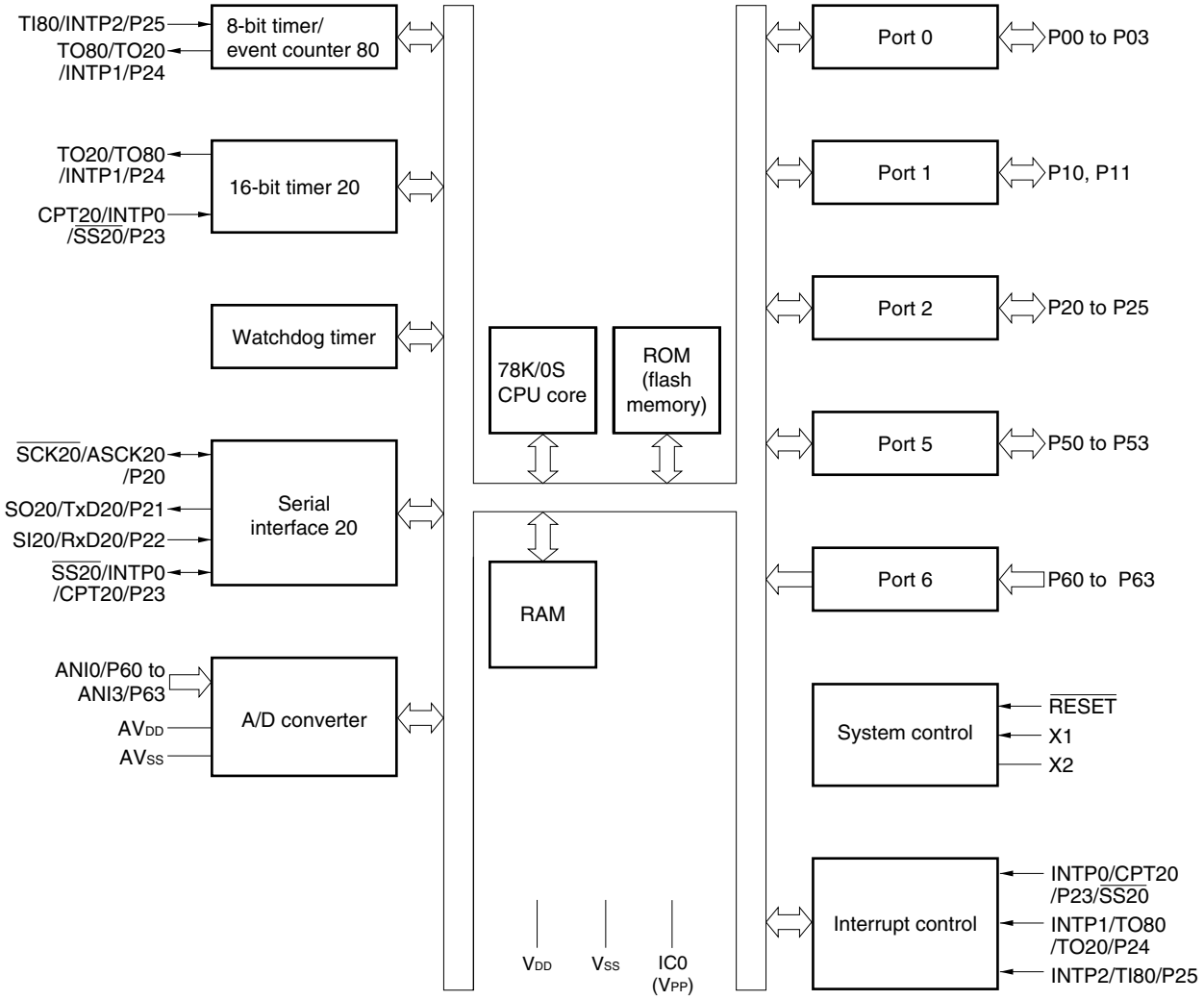
Series for ASSP

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789800	8 KB	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	31	4.0 V	–
Inverter control	μPD789842	8 KB to 16 KB	3 ch	**Note 1**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
On-chip bus controller	μPD789852	24 KB to 32 KB	3 ch	1 ch	–	1 ch	–	8 ch	3 ch (UART: 2 ch)	31	4.0 V	–
	μPD789850A	16 KB	1 ch				4 ch	–	2 ch (UART: 1 ch)	18		
Keyless entry	μPD789861	4 KB	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
	μPD789862	16 KB	1 ch	2 ch					1 ch (UART: 1 ch)	22		
VFD drive	μPD789871	4 KB to 8 KB	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 KB	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V[Note 2]	–

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

1.8 Block Diagram



Remarks 1. The size of the internal ROM varies depending on the product.

2. Items in parentheses apply to the μPD78F9116A, 78F9116B, 78F9116B(A), and 78F9116B(A1).

★ 1.9 Outline of Functions

Item		μPD789101A, 789111A, 789101A(A), 789111A(A), 789101A(A1), 789111A(A1), 789101A(A2), 789111A(A2)	μPD789102A, 789112A, 789102A(A), 789112A(A), 789102A(A1), 789112A(A1), 789102A(A2), 789112A(A2)	μPD789104A, 789114A, 789104A(A), 789114A(A), 789104A(A1), 789114A(A1), 789104A(A2), 789114A(A2)	μPD78F9116A, 78F9116B, 78F9116B(A), 78F9116B(A1)
Internal memory	ROM	Mask ROM			Flash memory
		2 KB	4 KB	8 KB	16 KB
	High-speed RAM	256 bytes			
System clock		Crystal/ceramic oscillation			
Minimum instruction execution time		Expanded-specification products of the μPD78910xA, 78910xA(A), 78911xA, 78911xA(A), 78F9116B, 78F9116B(A) • 0.2 μs/0.8 μs (@ system clock: 10.0 MHz operation, V_{DD} = 4.5 to 5.5 V) Other • 0.4 μs/1.6 μs (@ system clock: 5.0 MHz operation)			
General-purpose registers		8 bits × 8 registers			
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)			
Multiplier		8 bits × 8 bits = 16 bits			
I/O ports		Total: 20 • CMOS input: 4 • CMOS I/O: 12 • N-ch open-drain: 4			
A/D converter		8-bit resolution × 4 channels (μPD789104A Subseries) 10-bit resolution × 4 channels (μPD789114A Subseries)			
Serial interface		3-wire serial I/O mode/UART mode selectable: 1 channel			
Timer		16-bit timer: 1 channel 8-bit timer/event counter: 1 channel Watchdog timer: 1 channel			
Timer outputs		One output			
Vectored interrupts	Maskable	Internal: 6, External: 3			
	Non-maskable	Internal: 1			
Supply voltage		V_{DD} = 1.8 to 5.5 V (μPD78910xA, 78911xA, 78910xA(A), 78911xA(A), 78F9116A, 78F9116B, 78F9116B(A)) V_{DD} = 4.5 to 5.5 V (μPD78910xA(A1), 78911xA(A1), 78910xA(A2), 78911xA(A2), 78F9116B(A1))			
Operating ambient temperature		T_A = –40 to +85°C (μPD78910xA, 78911xA, 78910xA(A), 78911xA(A), 78F9116A, 78F9116B, 78F9116B(A)) T_A = –40 to +105°C (μPD78F9116B(A1)) T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)) T_A = –40 to +125°C (μPD78910xA(A2), 78911xA(A2))			
Package		30-pin plastic SSOP (7.62 mm (300))			

An outline of the timers is shown below.

		16-Bit Timer 20	8-Bit Timer/Event Counter 80	Watchdog Timer
Operating Mode	Interval timer	–	1 channel	1 channel[Note]
	External event timer	–	1 channel	–
Function	Timer output	1 output	1 output	–
	PWM output	–	1 output	–
	Square-wave output	–	1 output	–
	Capture	1 input	–	–
	Interrupt sources	1	1	1

Note The watchdog timer provides a watchdog timer function and an interval timer function, but only one of the two functions can be used at a time.

★ 1.10 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products

The standard quality grade products and the (A), (A1), and (A2) products refer to the following products.

[Standard quality grade products]... μPD789101A, 789102A, 789104A, 789111A, 789112A, 789114A, 78F9116A, 78F9116B

[(A) products].... μPD789101A(A), 789102A(A), 789104A(A), 789111A(A), 789112A(A), 789114A(A), 78F9116B(A)

[(A1) products].... μPD789101A(A1), 789102A(A1), 789104A(A1), 789111A(A1), 789112A(A1), 789114A(A1), 78F9116B(A1)

[(A2) products].... μPD789101A(A2), 789102A(A2), 789104A(A2), 789111A(A2), 789112A(A2), 789114A(A2)

The differences between the standard quality grade products and the (A), (A1), and (A2) products are shown in Table 1-2.

Table 1-2. Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products

Item \ Products	Standard Quality Grade Products	(A) Products	(A1) Products	(A2) Products
Quality grade	Standard	Special		
Supply voltage	V_{DD} = 1.8 to 5.5 V		V_{DD} = 4.5 to 5.5 V	
Operating ambient temperature	T_A = –40 to +85°C		• μPD78F9116B(A1) T_A = –40 to +105°C • Other than μPD78F9116B(A1) T_A = –40 to +110°C	T_A = –40 to +125°C
Minimum instruction execution time	Expanded-specification products[Note]: 0.2 μs (@ 10.0 MHz operation) Conventional-specification products[Note]: 0.4 μs (@ 5.0 MHz operation)		0.4 μs (@ 5.0 MHz operation)	
Electrical specifications	Refer to the relevant electrical specifications chapter.			

Note Refer to **1.1 Expanded-Specification Products and Conventional-Specification Products**.

CHAPTER 2 GENERAL (μPD789124A, 789134A SUBSERIES)

Caution All μPD789124A, 789134A Subseries products are conventional-specification products. No expanded-specification products are available in the μPD789124A, 789134A Subseries.

2.1 Features

★ • ROM and RAM capacities

Item / Part Number	Program Memory		Data Memory (Internal High-Speed RAM)
μPD789121A, 789131A, 789121A(A), 789131A(A), 789121A(A1), 789131A(A1), 789121A(A2), 789131A(A2)	Mask ROM	2 KB	256 bytes
μPD789122A, 789132A, 789122A(A), 789132A(A), 789122A(A1), 789132A(A1), 789122A(A2), 789132A(A2)		4 KB	
μPD789124A, 789134A, 789124A(A), 789134A(A), 789124A(A1), 789134A(A1), 789124A(A2), 789134A(A2)		8 KB	
μPD78F9136A, 78F9136B, 78F9136B(A), 78F9136B(A1)	Flash memory	16 KB	

- System clock: RC oscillation
- Minimum instruction execution times switchable between high speed (0.5 μs) and low speed (2.0 μs) (system clock: 4.0 MHz)
- 20 I/O ports
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode selectable
- 8-bit resolution A/D converter: 4 channels (μPD789124A Subseries)
- 10-bit resolution A/D converter: 4 channels (μPD789134A Subseries)
- 3 timers
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watchdog timer: 1 channel
- Multiplier: 8 bits × 8 bits = 16 bits
- Vectored interrupt sources: 10

★ • Supply voltage
  - V_{DD} = 1.8 to 5.5 V (μPD78912xA, 78913xA, 78912xA(A), 78913xA(A), 78F9136A, 78F9136B, 78F9136B(A))
  - V_{DD} = 4.5 to 5.5 V (μPD78912xA(A1), 78913xA(A1), 78912xA(A2), 78913xA(A2), 78F9136B(A1))

★ • Operating ambient temperature
  - T_A = –40 to + 85°C (μPD78912xA, 78913xA, 78912xA(A), 78913xA(A), 78F9136A, 78F9136B, 78F9136B(A))
  - T_A = –40 to +105°C (μPD78F9136B(A1))
  - T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1))
  - T_A = –40 to +125°C (μPD78912xA(A2), 78913xA(A2))

2.2 Applications

Vacuum cleaners, washing machines, refrigerators, battery chargers, etc.

★ 2.3 Ordering Information

Part Number	Package	Internal ROM
μPD789121AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789122AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789124AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789131AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789132AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789134AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD78F9136AMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD78F9136BMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD789121AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789122AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789124AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789131AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789132AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789134AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD78F9136BMC(A)-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD789121AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789122AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789124AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789131AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789132AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789134AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD78F9136BMC(A1)-5A4	30-pin plastic SSOP (7.62 mm (300))	Flash memory
μPD789121AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789122AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789124AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789131AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789132AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM
μPD789134AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Mask ROM

Remark ××× indicates ROM code suffix.

★ 2.4 Quality Grade

Part Number	Package	Quality Grade
μPD789121AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789122AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789124AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789131AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789132AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789134AMC-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD78F9136AMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD78F9136BMC-5A4	30-pin plastic SSOP (7.62 mm (300))	Standard
μPD789121AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789122AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789124AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789131AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789132AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789134AMC(A)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD78F9136BMC(A)-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789121AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789122AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789124AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789131AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789132AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789134AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD78F9136BMC(A1)-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789121AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789122AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789124AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789131AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789132AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789134AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special

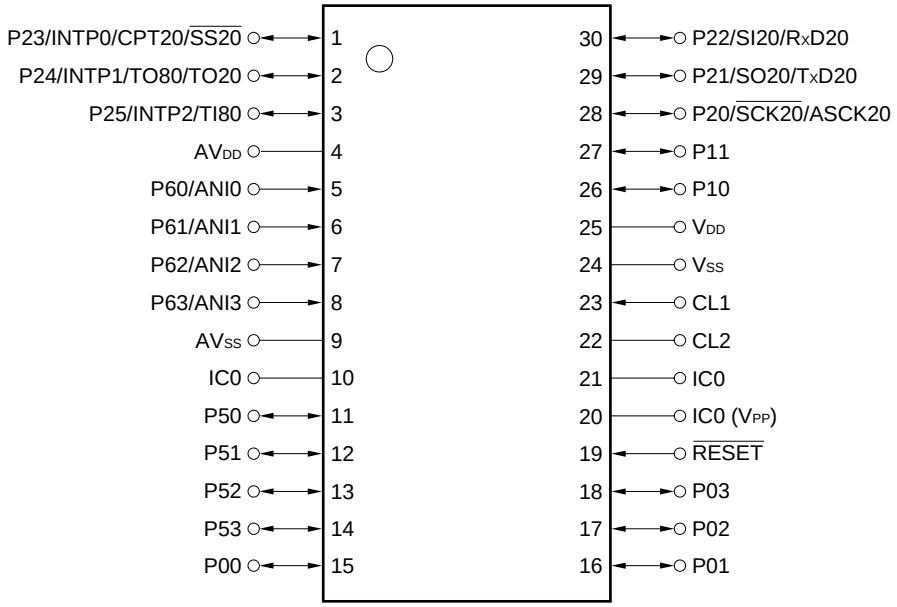
Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

★ 2.5 Pin Configuration (Top View)

- 30-pin plastic SSOP (7.62 mm (300))

μPD789121AMC-×××-5A4 μPD789122AMC-×××-5A4 μPD789124AMC-×××-5A4
μPD789131AMC-×××-5A4 μPD789132AMC-×××-5A4 μPD789134AMC-×××-5A4
μPD78F9136AMC-5A4 μPD78F9136BMC-5A4
μPD789121AMC(A)-×××-5A4 μPD789122AMC(A)-×××-5A4 μPD789124AMC(A)-×××-5A4
μPD789131AMC(A)-×××-5A4 μPD789132AMC(A)-×××-5A4 μPD789134AMC(A)-×××-5A4
μPD78F9136BMC(A)-5A4
μPD789121AMC(A1)-×××-5A4 μPD789122AMC(A1)-×××-5A4 μPD789124AMC(A1)-×××-5A4
μPD789131AMC(A1)-×××-5A4 μPD789132AMC(A1)-×××-5A4 μPD789134AMC(A1)-×××-5A4
μPD78F9136BMC(A1)-5A4
μPD789121AMC(A2)-×××-5A4 μPD789122AMC(A2)-×××-5A4 μPD789124AMC(A2)-×××-5A4
μPD789131AMC(A2)-×××-5A4 μPD789132AMC(A2)-×××-5A4 μPD789134AMC(A2)-×××-5A4



Cautions 1. Connect the IC0 (internally connected) pin directly to the V_{SS} pin.

2. Connect the AV_{DD} pin to the V_{DD} pin.

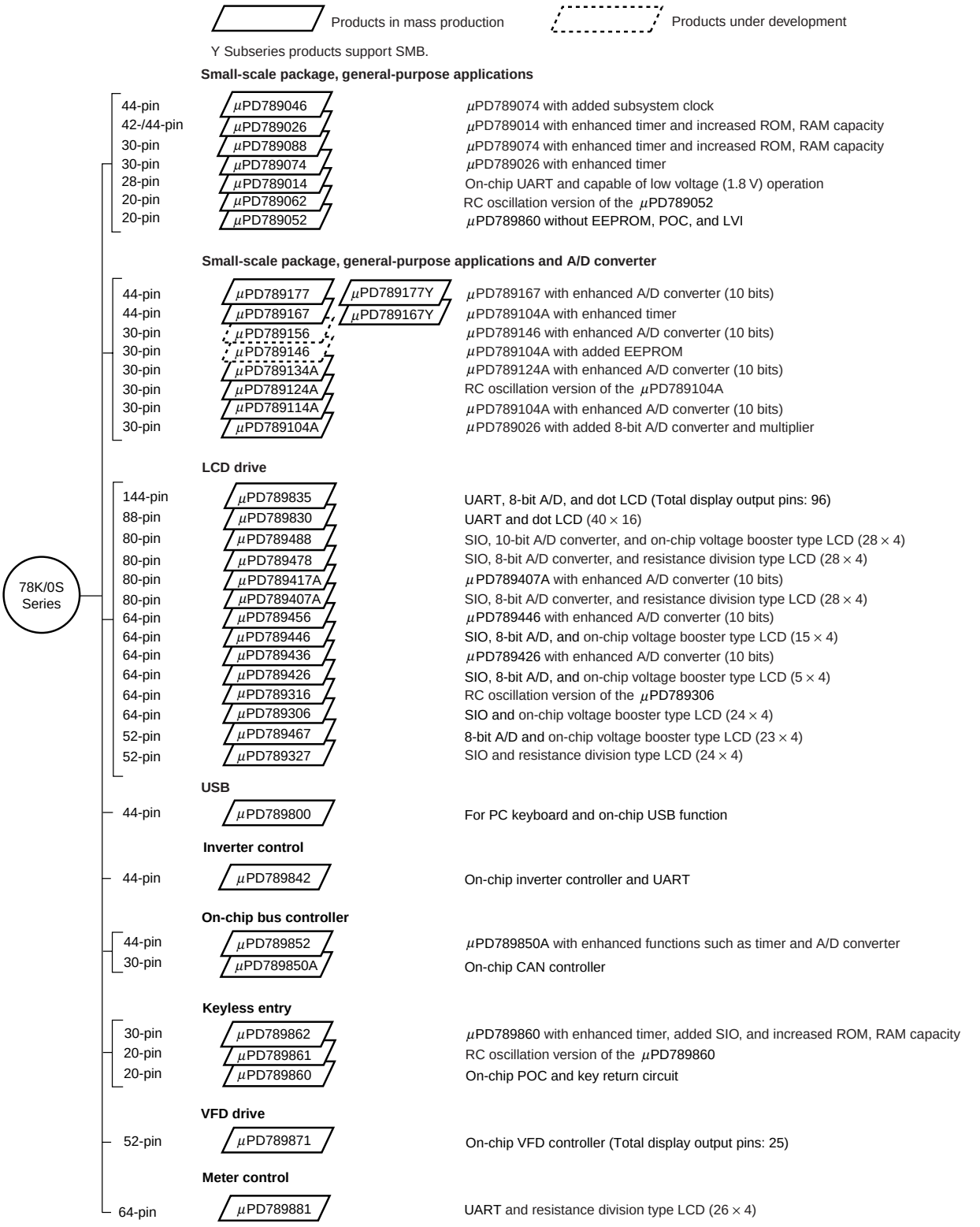
3. Connect the AV_{SS} pin to the V_{SS} pin.

Remark The pin connection in parentheses is intended for the μPD78F9136A, 78F9136B, 78F9136B(A), and 78F9136B(A1).

ANI0 to ANI3:	Analog input	$\overline{\text{RESET}}$:	Reset
ASCK20:	Asynchronous serial input	RxD20:	Receive data
AV_{DD}:	Analog power supply	$\overline{\text{SCK20}}$:	Serial clock
AV_{SS}:	Analog ground	SI20:	Serial input
CL1, CL2:	RC oscillator	SO20:	Serial output
CPT20:	Capture trigger input	$\overline{\text{SS20}}$:	Chip select input
IC0:	Internally connected	TI80:	Timer input
INTP0 to INTP2:	External interrupt input	TO20, TO80:	Timer output
P00 to P03:	Port 0	TxD20:	Transmit data
P10, P11:	Port 1	V_{DD}:	Power supply
P20 to P25:	Port 2	V_{PP}:	Programming power supply
P50 to P53:	Port 5	V_{SS}:	Ground
P60 to P63:	Port 6		

★ 2.6 78K/0S Series Lineup

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences between the subseries are listed below.

Series for general-purpose applications and LCD drive

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 KB	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 KB to 16 KB			–							
	μPD789088	16 KB to 32 KB	3 ch							24		
	μPD789074	2 KB to 8 KB	1 ch									
	μPD789014	2 KB to 4 KB	2 ch	–						22		
	μPD789062	4 KB							–	14		RC oscillation version
	μPD789052											–
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 KB to 24 KB	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 KB to 16 KB	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 KB to 8 KB					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835	24 KB to 60 KB	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	37	1.8 V[Note]	Dot LCD supported
	μPD789830	24 KB	1 ch	1 ch			–			30	2.7 V	
	μPD789488	32 KB to 48 KB	3 ch					8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789478	24 KB to 48 KB					8 ch	–				
	μPD789417A	12 KB to 24 KB					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 KB to 16 KB	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 KB to 16 KB					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789467	4 KB to 24 KB		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note Flash memory version: 3.0 V

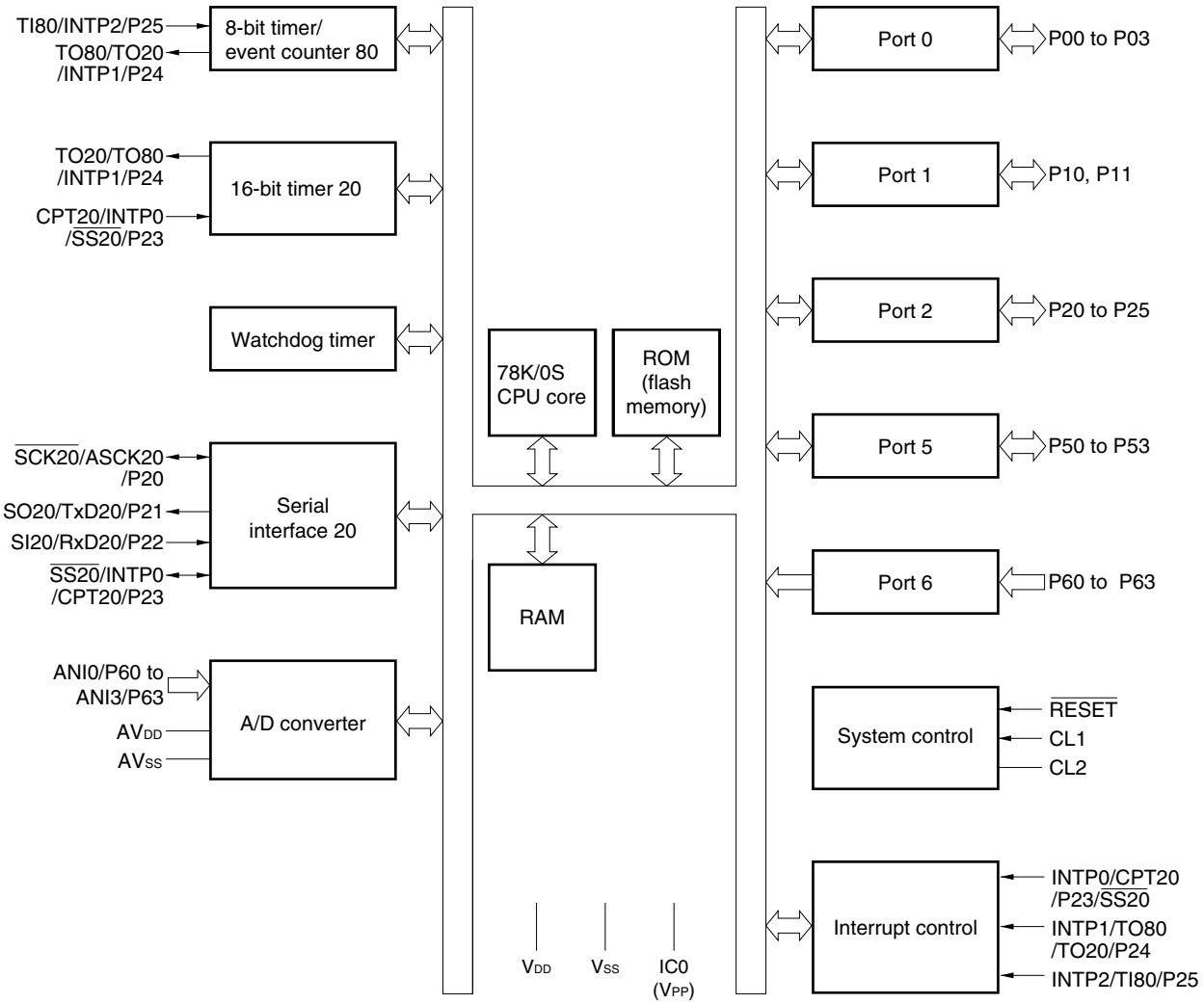
Series for ASSP

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789800	8 KB	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	31	4.0 V	–
Inverter control	μPD789842	8 KB to 16 KB	3 ch	**Note 1**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
On-chip bus controller	μPD789852	24 KB to 32 KB	3 ch	1 ch	–	1 ch	–	8 ch	3 ch (UART: 2 ch)	31	4.0 V	–
	μPD789850A	16 KB	1 ch				4 ch	–	2 ch (UART: 1 ch)	18		
Keyless entry	μPD789861	4 KB	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
	μPD789862	16 KB	1 ch	2 ch					1 ch (UART: 1 ch)	22		
VFD drive	μPD789871	4 KB to 8 KB	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 KB	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V[Note 2]	–

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

2.7 Block Diagram



Remarks 1. The size of the internal ROM varies depending on the product.

2. Items in parentheses apply to the μPD78F9136A, 78F9136B, 78F9136B(A), 78F9136B(A1).

★ 2.8 Outline of Functions

Item		μPD789121A, 789131A, 789121A(A), 789131A(A), 789121A(A1), 789131A(A1), 789121A(A2), 789131A(A2)	μPD789122A, 789132A, 789122A(A), 789132A(A), 789122A(A1), 789132A(A1), 789122A(A2), 789132A(A2)	μPD789124A, 789134A, 789124A(A), 789134A(A), 789124A(A1), 789134A(A1), 789124A(A2), 789134A(A2)	μPD78F9136A, 78F9136B, 78F9136B(A), 78F9136B(A1)
Internal memory	ROM	Mask ROM			Flash memory
		2 KB	4 KB	8 KB	16 KB
	High-speed RAM	256 bytes			
System clock		RC oscillation			
Minimum instruction execution time		0.5/2.0 μs (@ system clock: 4.0 MHz operation)			
General-purpose registers		8 bits × 8 registers			
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)			
Multiplier		8 bits × 8 bits = 16 bits			
I/O ports		Total: 20 • CMOS input: 4 • CMOS I/O: 12 • N-ch open-drain: 4			
A/D converter		8-bit resolution × 4 channels (μPD789124A Subseries) 10-bit resolution × 4 channels (μPD789134A Subseries)			
Serial interface		3-wire serial I/O mode/UART mode selectable: 1 channel			
Timer		16-bit timer: 1 channel 8-bit timer/event counter: 1 channel Watchdog timer: 1 channel			
Timer outputs		One output			
Vectored interrupts	Maskable	Internal: 6, External: 3			
	Non-maskable	Internal: 1			
Supply voltage		V_{DD} = 1.8 to 5.5 V (μPD78912xA, 78913xA, 78912xA(A), 78913xA(A), 78F9136A, 78F9136B, 78F9136B(A)) V_{DD} = 4.5 to 5.5 V (μPD78912xA(A1), 78913xA(A1), 78912xA(A2), 78913xA(A2), 78F9136B(A1))			
Operating ambient temperature		T_A = –40 to +85°C (μPD78912xA, 78913xA, 78912xA(A), 78913xA(A), 78F9136A, 78F9136B, 78F9136B(A)) T_A = –40 to +105°C (μPD78F9136B(A1)) T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)) T_A = –40 to +125°C (μPD78912xA(A2), 78913xA(A2))			
Package		30-pin plastic SSOP (7.62 mm (300))			

An outline of the timers is shown below.

		16-Bit Timer 20	8-Bit Timer/Event Counter 80	Watchdog Timer
Operating Mode	Interval timer	–	1 channel	1 channel[Note]
	External event timer	–	1 channel	–
Function	Timer output	1 output	1 output	–
	PWM output	–	1 output	–
	Square-wave output	–	1 output	–
	Capture	1 input	–	–
	Interrupt sources	1	1	1

Note The watchdog timer provides a watchdog timer function and an interval timer function, but only one of the two functions can be used at a time.

★ 2.9 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products

The standard quality grade products and the (A), (A1), and (A2) products refer to the following products.

[Standard quality grade products]... μPD789121A, 789122A, 789124A, 789131A, 789132A, 789134A, 78F9136A, 78F9136B

[(A) products]....μPD789121A(A), 789122A(A), 789124A(A), 789131A(A), 789132A(A), 789134A(A) , 78F9136B(A)

[(A1) products]....μPD789121A(A1), 789122A(A1), 789124A(A1), 789131A(A1), 789132A(A1), 789134A(A1), 78F9136B(A1)

[(A2) products]....μPD789121A(A2), 789122A(A2), 789124A(A2), 789131A(A2), 789132A(A2), 789134A(A2)

The differences between the standard quality grade products and the (A), (A1), and (A2) products are shown in Table 2-1.

Table 2-1. Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products

Item \ Products	Standard Quality Grade Products	(A) Products	(A1) Products	(A2) Products
Quality grade	Standard	Special		
Supply voltage	V_{DD} = 1.8 to 5.5 V		V_{DD} = 4.5 to 5.5 V	
Operating ambient temperature	T_A = –40 to +85°C		• μPD78F9136B(A1) T_A = –40 to +105°C • Other than μPD78F9136B(A1) T_A = –40 to +110°C	T_A = –40 to +125°C
Electrical specifications	Refer to the relevant electrical specifications chapter.			

CHAPTER 3 PIN FUNCTIONS

3.1 Pin Function List

(1) Port pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0 4-bit I/O port Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).	Input	–
P10, P11	I/O	Port 1 2-bit I/O port Input/output can be specified in 1-bit units. When used as an input port, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).	Input	–
P20	I/O	Port 2 6-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by pull-up resistor option register B2 (PUB2).	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				INTP0/CPT20/$\overline{\text{SS20}}$
P24				INTP1/TO80/TO20
P25				INTP2/TI80
P50 to P53	I/O	Port 5 4-bit N-channel open-drain I/O port Input/output can be specified in 1-bit units. For a mask ROM version, use of an on-chip pull-up resistor can be specified by a mask option.	Input	–
P60 to P63	Input	Port 6 4-bit input-only port	Input	ANI0 to ANI3

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P23/CPT20/$\overline{SS20}$
INTP1				P24/TO80/TO20
INTP2				P25/TI80
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
$\overline{SCK20}$	I/O	Serial clock I/O for serial interface	Input	P20/ASCK20
ASCK20	Input	Serial clock input to asynchronous serial interface	Input	P20/$\overline{SCK20}$
$\overline{SS20}$	Input	Chip select input to serial interface	Input	P23/CPT20/INTP0
RxD20	Input	Serial data input to asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output from asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer/event counter 80	Input	P25/INTP2
TO80	Output	8-bit timer/event counter 80 output	Input	P24/INTP1/TO20
TO20	Output	16-bit timer 20 output	Input	P24/INTP1/TO80
CPT20	Input	Capture edge input	Input	P23/INTP0/$\overline{SS20}$
ANI0 to ANI3	Input	A/D converter analog input	Input	P60 to P63
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
X1	Input	Connecting ceramic resonator/crystal resonator for system clock oscillation (μPD789104A, 789114A Subseries)	–	–
X2	–		–	–
CL1	Input	Connecting resistor (R) and capacitor (C) for system clock oscillation (μPD789124A and 789134A Subseries)	–	–
CL2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
IC0	–	Internally connected. Directly connect to the V_{SS} pin.	–	–
V_{PP}	–	Sets flash memory programming mode. Applies a high voltage when a program is written or verified.	–	–

3.2 Description of Pin Functions

3.2.1 P00 to P03 (Port 0)

These pins constitute a 4-bit I/O port and can be set in input or output port mode in 1-bit units by using port mode register 0 (PM0). When these pins are used as an input port, use of an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).

3.2.2 P10, P11 (Port 1)

These pins constitute a 2-bit I/O port and can be set in input or output port mode in 1-bit units by using port mode register 1 (PM1). When these pins are used as an input port, use of an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).

3.2.3 P20 to P25 (Port 2)

These pins constitute a 6-bit I/O port. In addition, they function as timer I/O, external interrupt inputs, and serial interface data and clock I/O.

Port 2 can be specified in the following operation modes in 1-bit units.

(1) Port mode

In this mode, P20 to P25 function as a 6-bit I/O port. Port 2 can be specified as input or output mode in 1-bit units by using port mode register 2 (PM2). Use of an on-chip pull-up resistor can be specified in 1-bit units by using pull-up resistor option register B2 (PUB2), regardless of the setting of port mode register 2 (PM2).

(2) Control mode

In this mode, P20 to P25 function as timer I/O, external interrupt input, clock I/O of the serial interface and the data I/O.

(a) TI80

This is the external clock input pin for 8-bit timer/event counter 80.

(b) TO20, TO80

TO20 is the output pin of 16-bit timer 20. TO80 is the output pin of 8-bit timer/event counter 80.

(c) CPT20

This is the input pin of the capture edge.

(d) INTP0 to INTP2

These are external interrupt input pins for which the valid edge (rising edge, falling edge, and both rising and falling edges) can be specified.

(e) SI20, SO20

These are the serial data I/O pins of the serial interface.

(f) $\overline{\text{SCK20}}$

These are the serial clock I/O pins of the serial interface.

(g) $\overline{\text{SS20}}$

This is the chip select input pin of the serial interface.

(h) RxD20, TxD20

These are the serial data I/O pins of the asynchronous serial interface.

(i) ASCK20

This is the serial clock input pin of the asynchronous serial interface.

Caution When using these pins as serial interface pins, the I/O mode and output latch must be set according to the function to be used. For details of the setting, refer to Table 13-2 Serial Interface 20 Operating Mode Settings.

3.2.4 P50 to P53 (Port 5)

These pins constitute a 4-bit N-ch open-drain I/O port and can be specified in input or output mode in 1-bit units by using port mode register 5 (TM5). For a mask ROM version, use of an on-chip pull-up resistor can be specified by a mask option.

3.2.5 P60 to P63 (Port 6)

These pins constitute a 4-bit input-only port. In addition to general-purpose input ports, these pins function as the A/D converter input pins.

(1) Port mode

In the port mode, these pins function as a 4-bit input-only port.

(2) Control mode

In the control mode, the pins of port 6 can be used as A/D converter analog inputs (ANI0 to ANI3).

3.2.6 $\overline{\text{RESET}}$

This pin inputs an active-low system reset signal.

3.2.7 X1, X2 (μPD789104A, 789114A Subseries)

These pins are used to connect a ceramic resonator/crystal resonator for system clock oscillation.

To supply an external clock, input the clock to X1 and input the inverted signal to X2.

3.2.8 CL1, CL2 (μPD789124A, 789134A Subseries)

These are resistor (R) and capacitor (C) connection pins for system clock oscillation.

3.2.9 AV_{DD}

This is the analog power supply pin of the A/D converter. Always use the same potential as that of the V_{DD} pin even when the A/D converter is not used.

3.2.10 AV_{SS}

This is the ground potential pin of the A/D converter. Always use the same potential as that of the V_{SS} pin even when the A/D converter is not used.

3.2.11 V_{DD}

This is the positive power supply pin.

3.2.12 V_{SS}

This is the ground pin.

3.2.13 V_{PP} (μPD78F9116A, 78F9116B, 78F9136A, 78F9136B only)

A high voltage should be applied to this pin when the flash memory programming mode is set and when the program is written or verified.

★ Connect this pin in either of the following ways.

- Independently connect to a 10 kΩ pull-down resistor.
- By using a jumper on the board, connect directly to the dedicated flash programmer in the programming mode or to V_{SS} in the normal operation mode.

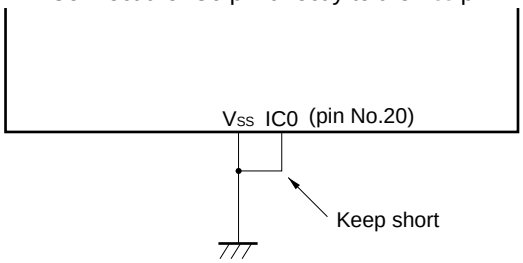
If the wiring between the V_{PP} and V_{SS} pins is long or external noise is superimposed on the V_{PP} pin, the user program may malfunction.

3.2.14 IC0 (pin No.20) (mask ROM versions only)

The IC0 (internally connected) pin (No. 20) (refer to **1.6 Pin Configuration (Top View)**, **2.5 Pin Configuration (Top View)**) is used to set the μPD789104A/114A/124A/134A Subseries in the test mode before shipment. In the normal operation mode, connect this pin directly to the V_{SS} pin with as short a wiring length as possible.

If a potential difference is generated between the IC0 pin and V_{SS} pin due to a long wiring length between the IC0 pin and V_{SS} pin or external noise superimposed on the IC0 pin, the user program may malfunction.

○ Connect the IC0 pin directly to the V_{SS} pin.



3.2.15 IC0 (pins No.10 and No.21)

The IC0 pins (No.10 and No.21) (refer to **1.6 Pin Configuration (Top View)**, **2.5 Pin Configuration (Top View)** are internally connected.

Connect the IC0 pins directly to V_{SS}.

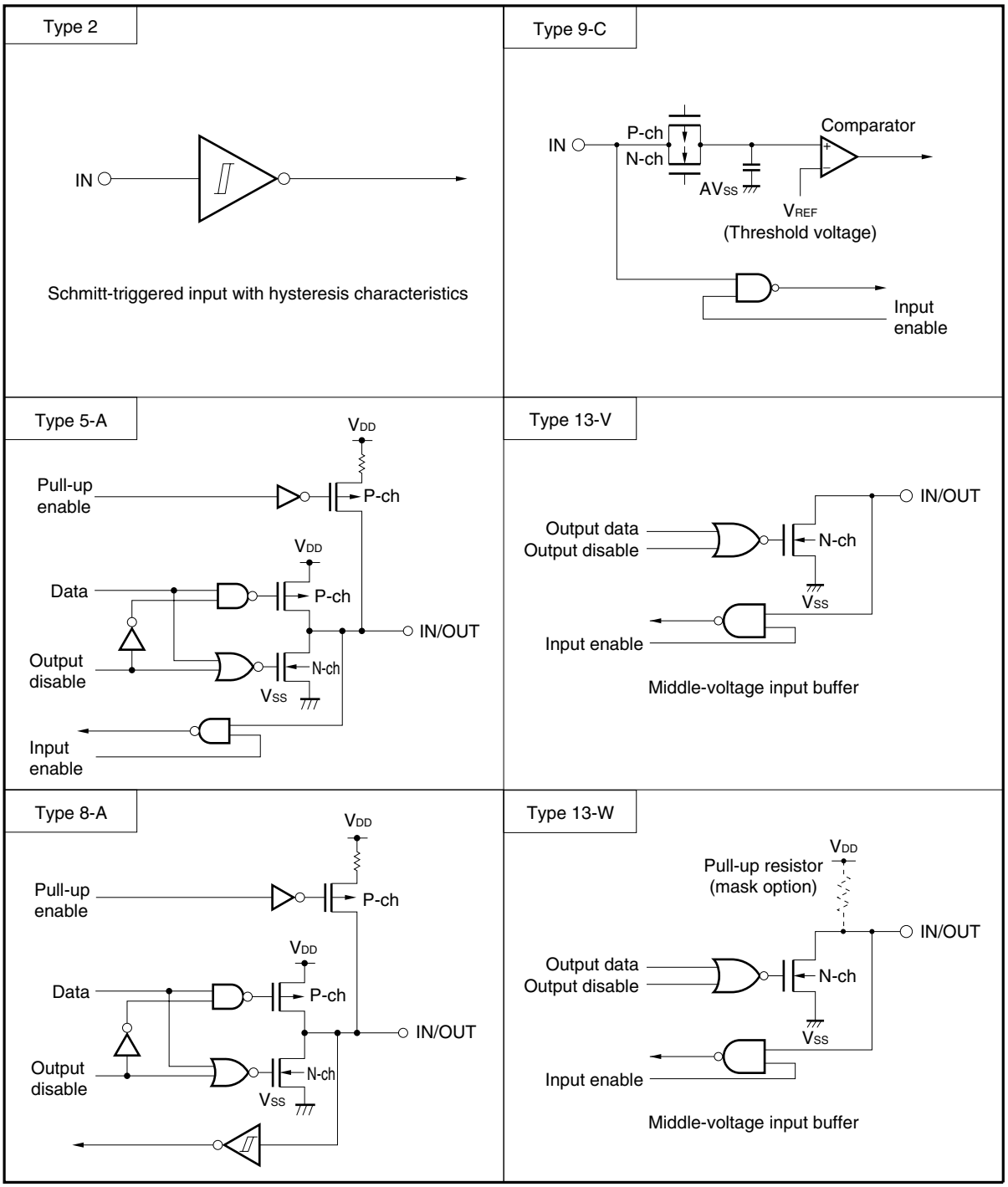
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type for each pin and the recommended connection of pins are shown in Table 3-1.
For the I/O circuit configuration of each type, refer to **Figure 3-1**.

★ **Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P03	5-A	I/O	Input: Independently connect these pins to V_{DD} or V_{SS} via a resistor. Output: Leave open
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-A		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/INTP0/CPT20/$\overline{SS20}$			Input: Independently connect these pins to V_{SS} via a resistor. Output: Leave open
P24/INTP1/TO80/TO20			
P25/INTP2/TI80			
P50 to P53 (Mask ROM version)	13-W		Input: Directly connect these pins to V_{SS}. Output: Leave these pins open at low-level output after setting the port output latch to 0.
P50 to P53 (μPD78F9116A, 78F9116B, 78F9136A, 78F9136B)	13-V		
P60/ANI0 to P63/ANI3	9-C	Input	Directly connect to V_{DD} or V_{SS}.
AV_{DD}	–	–	Directly connect to V_{DD}.
AV_{SS}			Directly connect to V_{SS}.
$\overline{RESET}$	2	Input	–
IC0	–	–	Directly connect to V_{SS}.
V_{PP}			Independently connect 10 kΩ pull-down resistor to this pin or connect this pin directly to V_{SS}.

Figure 3-1. Pin I/O Circuits



CHAPTER 4 CPU ARCHITECTURE

4.1 Memory Space

The μPD789104A/114A/124A/134A Subseries can access 64 KB of memory space. Figures 4-1 to 4-4 show the memory maps.

Figure 4-1. Memory Map (μPD789101A, 789111A, 789121A, 789131A)

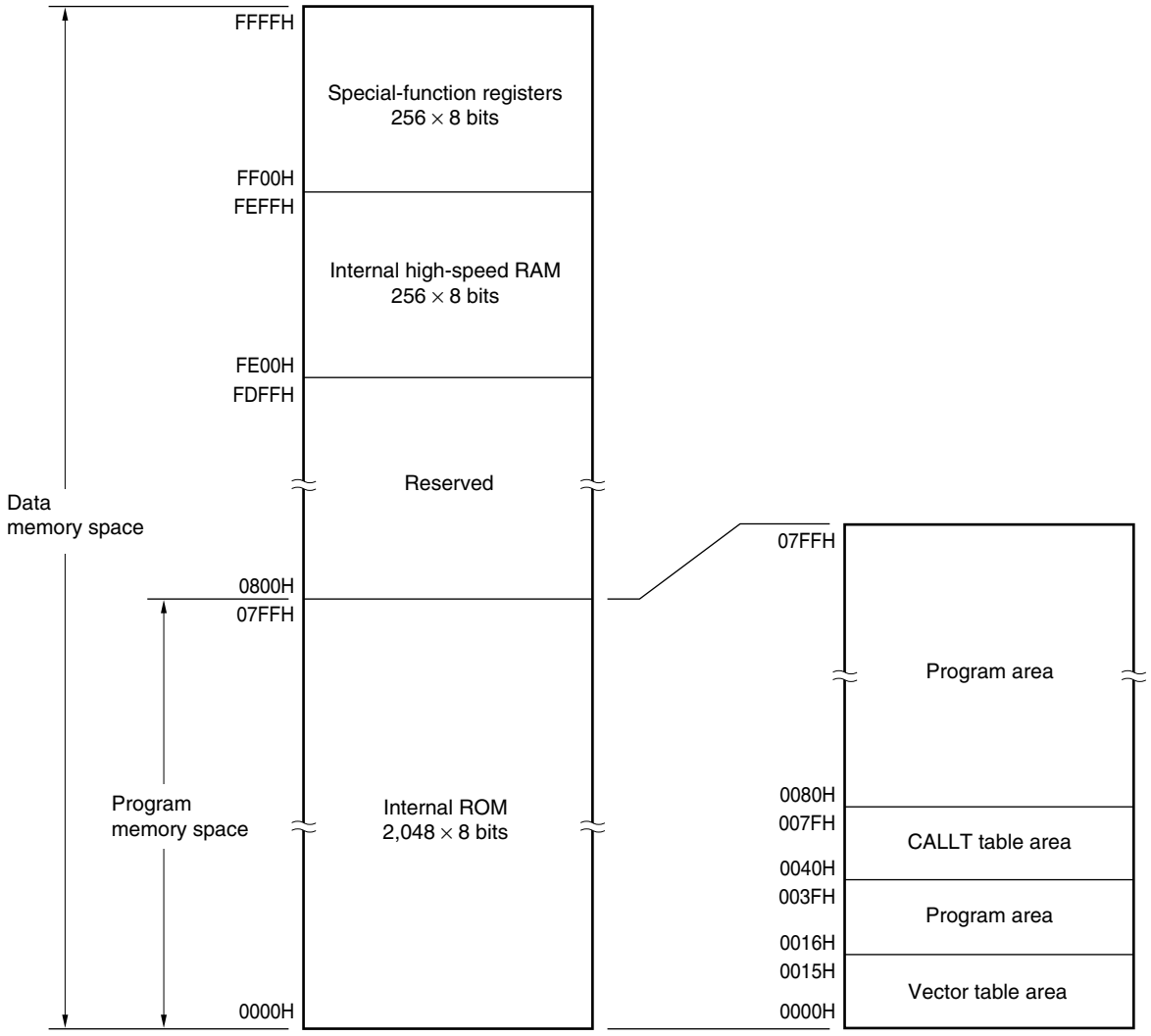


Figure 4-2. Memory Map (μPD789102A, 789112A, 789122A, 789132A)

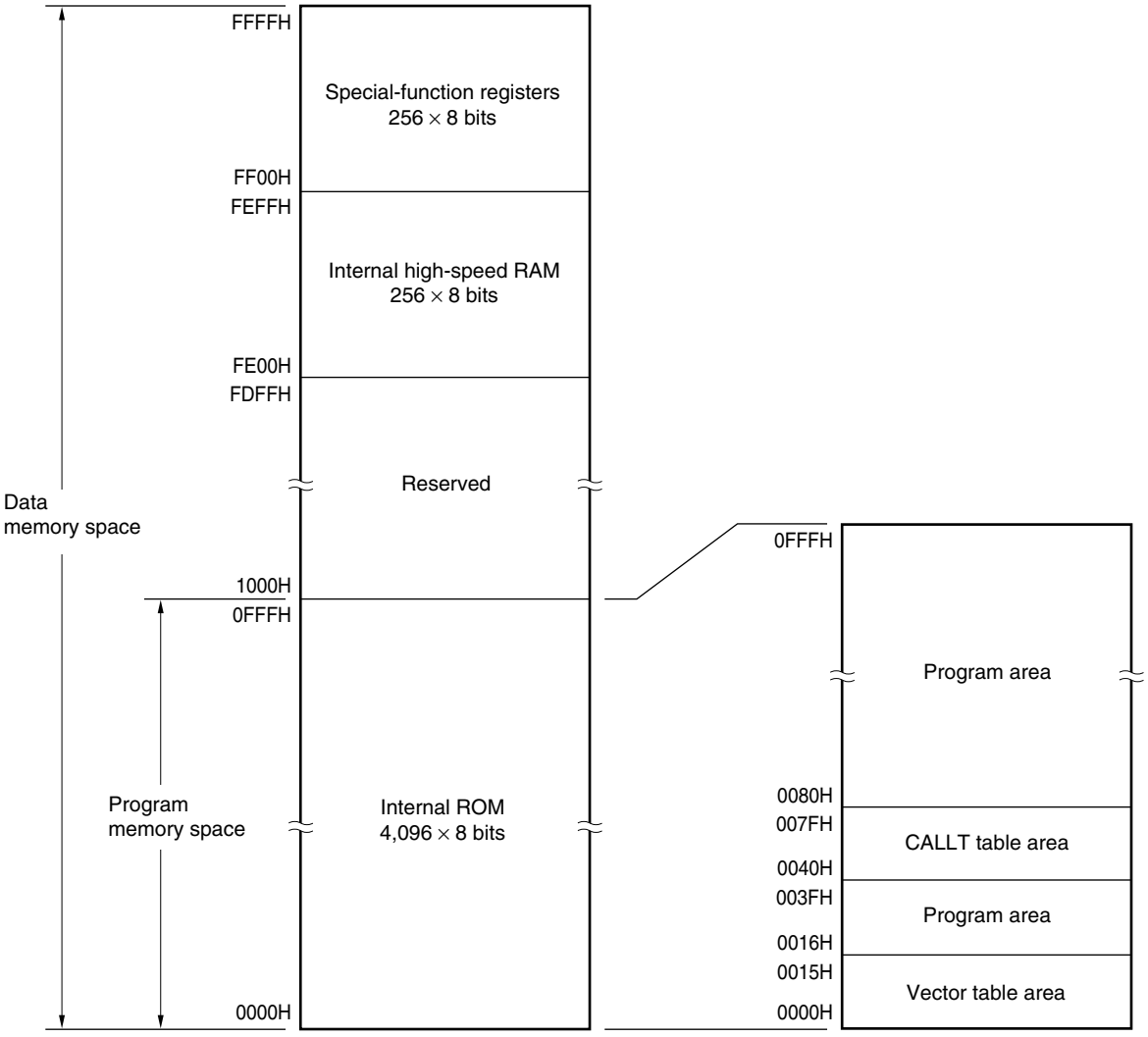


Figure 4-3. Memory Map (μPD789104A, 789114A, 789124A, 789134A)

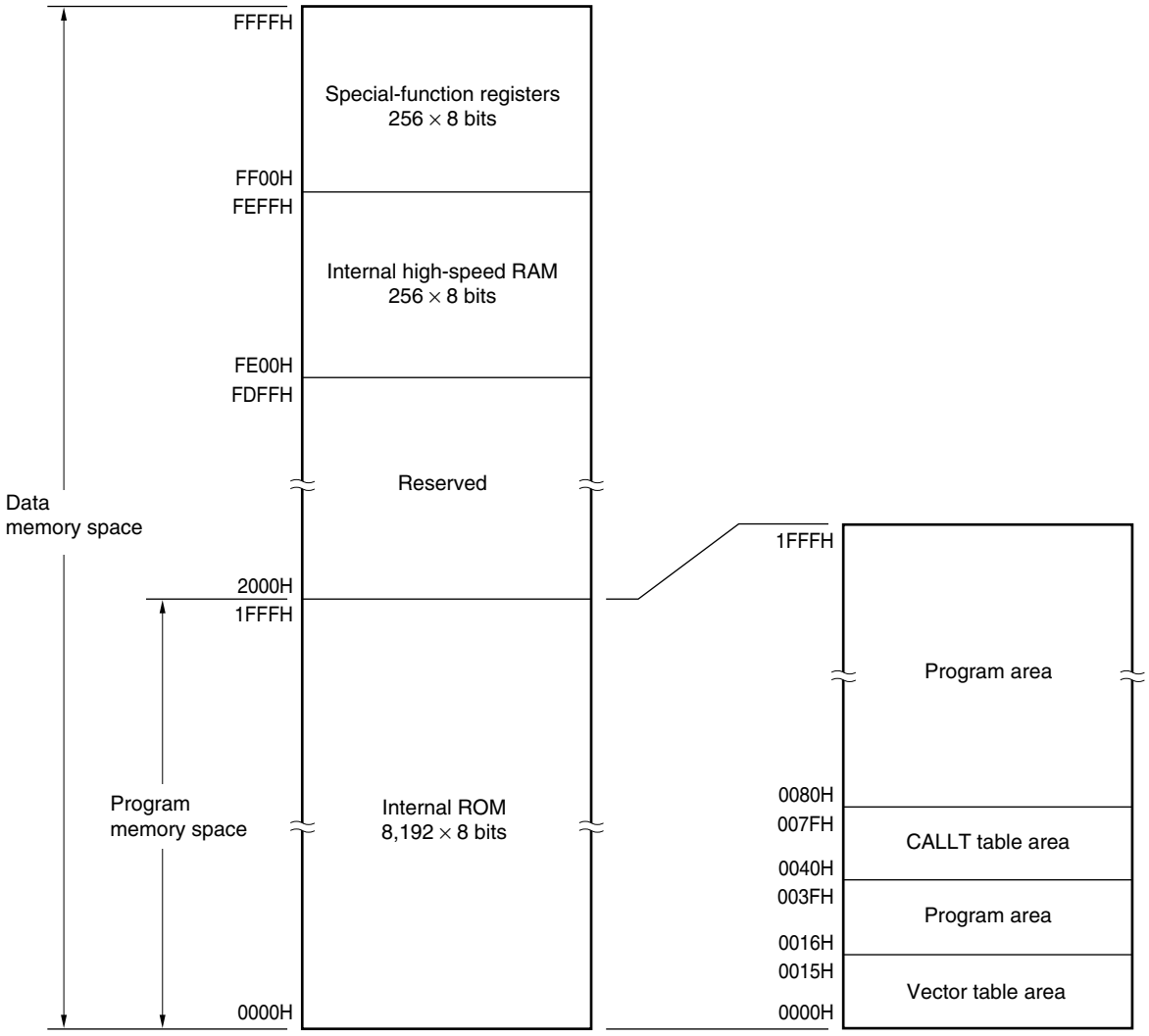
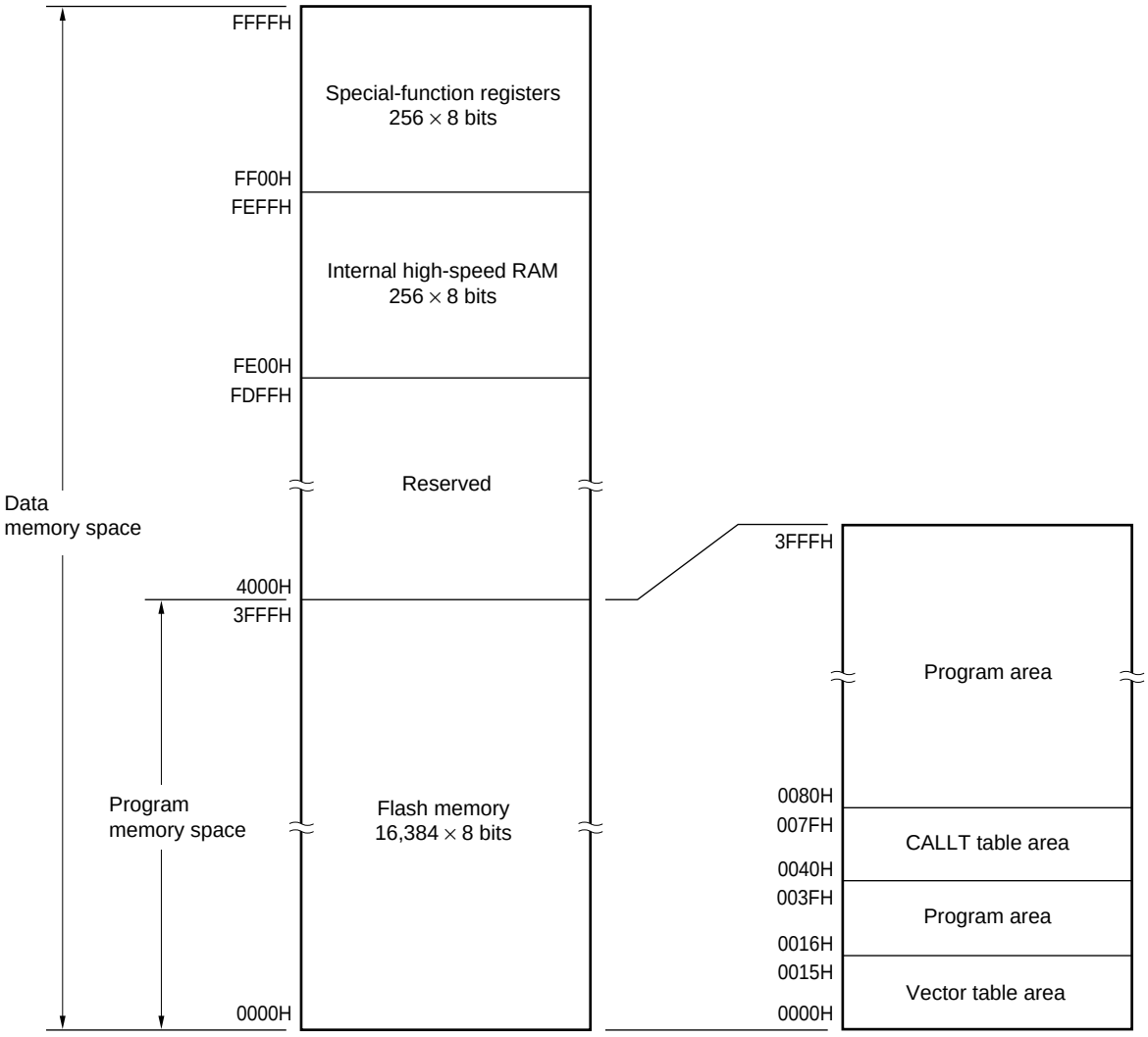


Figure 4-4. Memory Map (μPD78F9116A, 78F9116B, 78F9136A, 78F9136B)



4.1.1 Internal program memory space

The internal program memory space stores programs and table data. This space is usually addressed by the program counter (PC).

The μPD789104A/114A/124A/134A Subseries provides the following internal ROMs (or flash memory) containing the following capacities.

Table 4-1. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD789101A, 789111A, 789121A, 789131A	Mask ROM	2,048 × 8 bits
μPD789102A, 789112A, 789122A, 789132A		4,096 × 8 bits
μPD789104A, 789114A, 789124A, 789134A		8,192 × 8 bits
μPD78F9116A, 78F9116B, 78F9136A, 78F9136B	Flash memory	16,384 × 8 bits

The following areas are allocated to the internal program memory space.

(1) Vector table area

The 22-byte area of addresses 0000H to 0015H is reserved as a vector table area. This area stores program start addresses to be used when branching by $\overline{\text{RESET}}$ input or interrupt request generation. Of a 16-bit program address, the lower 8 bits are stored in an even address, and the higher 8 bits are stored in an odd address.

Table 4-2. Vector Table

Vector Table Address	Interrupt Request	Vector Table Address	Interrupt Request
0000H	$\overline{\text{RESET}}$ input	000CH	INTSR20/INTCSI20
0004H	INTWDT	000EH	INTST20
0006H	INTP0	0010H	INTTM80
0008H	INTP1	0012H	INTTM20
000AH	INTP2	0014H	INTAD0

(2) CALLT instruction table area

The subroutine entry address of a 1-byte call instruction (CALLT) can be stored in the 64-byte area of addresses 0040H to 007FH.

4.1.2 Internal data memory (internal high-speed RAM) space

The μPD789104A/114A/124A/134A Subseries provides a 256-byte internal high-speed RAM.

The internal high-speed RAM can also be used as a stack memory.

4.1.3 Special-function register (SFR) area

Special-function registers (SFRs) of on-chip peripheral hardware are allocated to the area of FF00H to FFFFH (refer to **Table 4-3**).

4.1.4 Data memory addressing

The μPD789104A/114A/124A/134A Subseries provides a variety of addressing modes which take account of memory manipulability, etc. Especially at addresses corresponding to data memory area (FE00H to FEFFH), particular addressing modes can be used to meet the functions of the special-function registers (SFRs) and general-purpose registers. Figures 4-5 to 4-8 show the data memory addressing modes.

Figure 4-5. Data Memory Addressing (μPD789101A, 789111A, 789121A, 789131A)

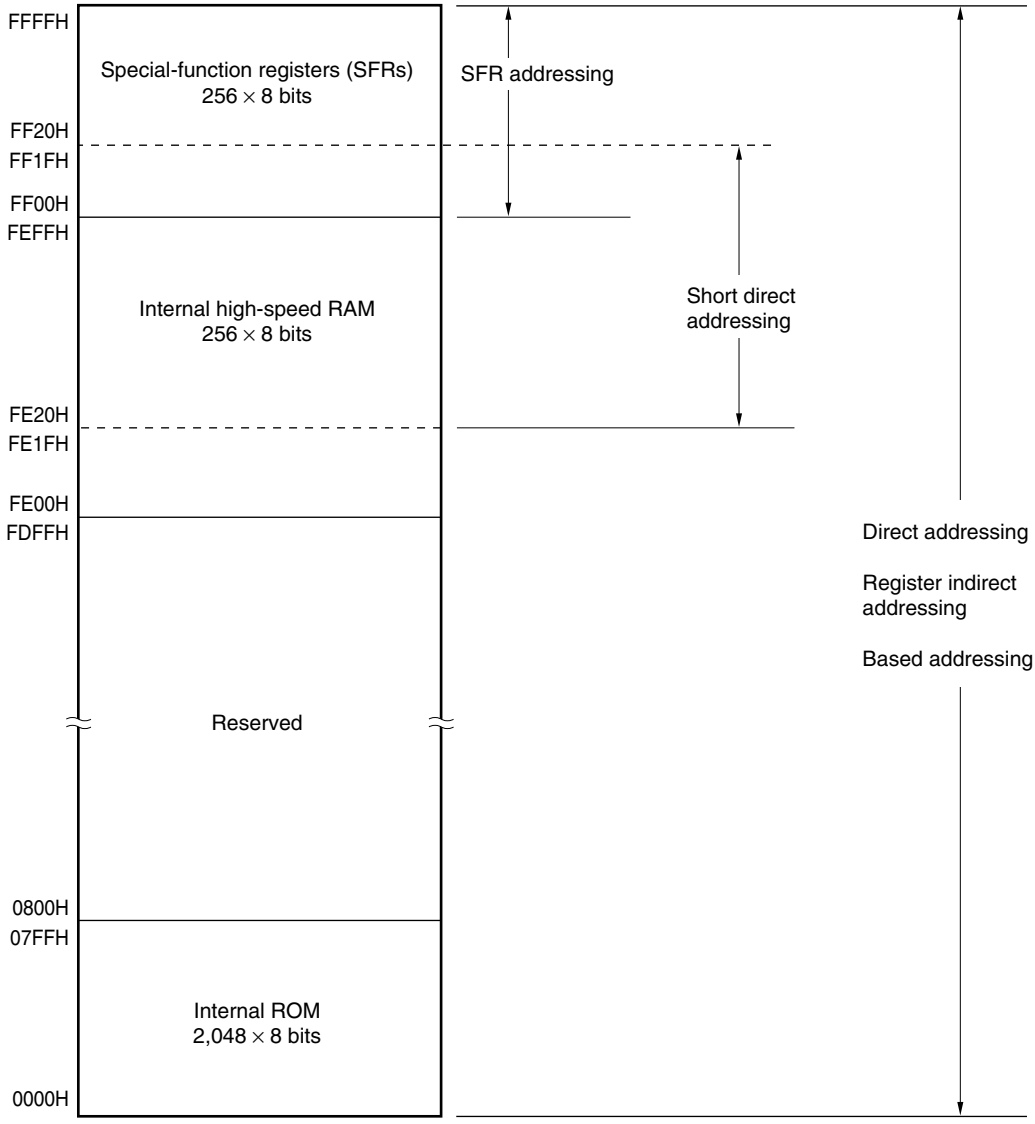


Figure 4-6. Data Memory Addressing (μPD789102A, 789112A, 789122A, 789132A)

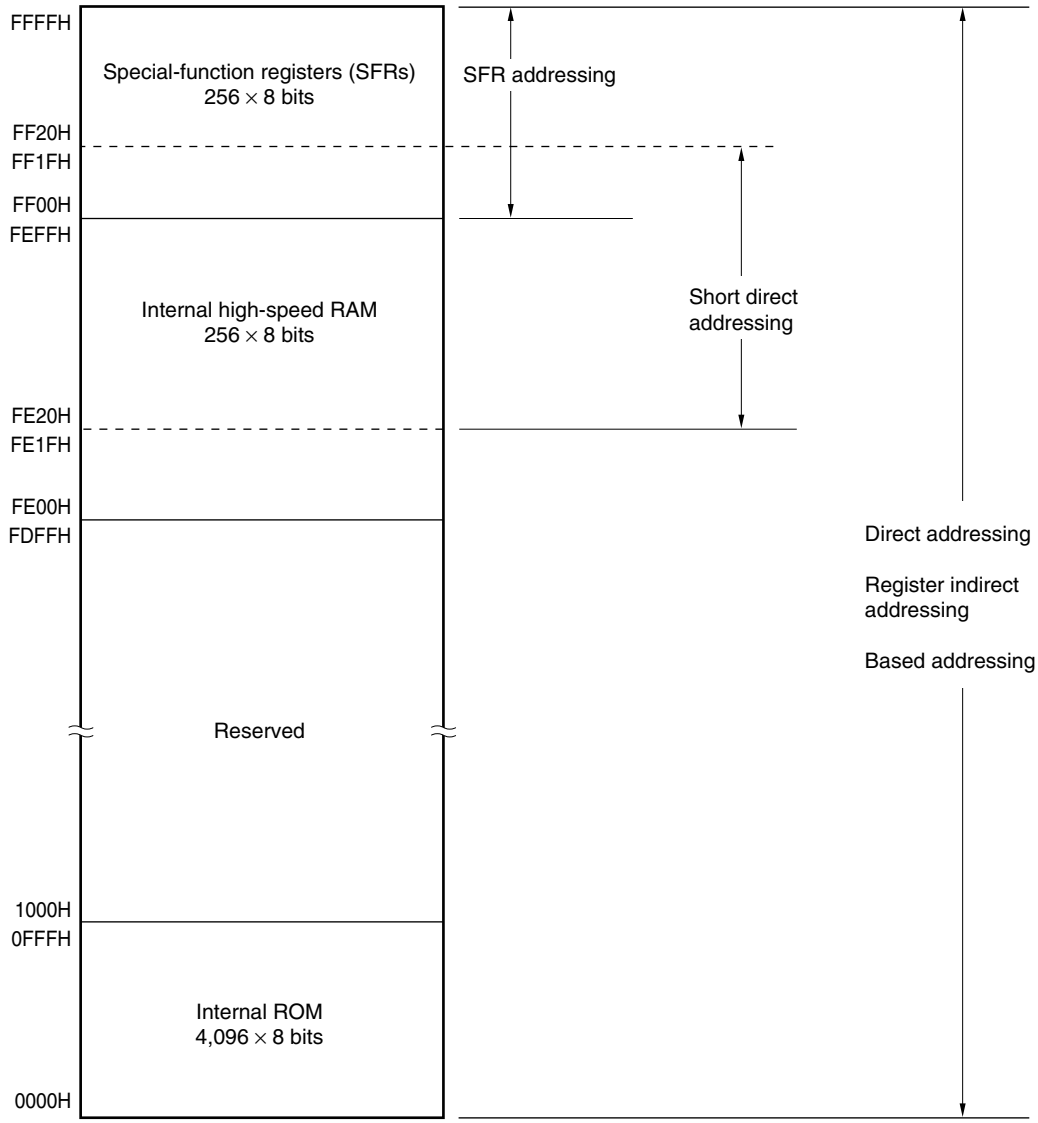


Figure 4-7. Data Memory Addressing (μPD789104A, 789114A, 789124A, 789134A)

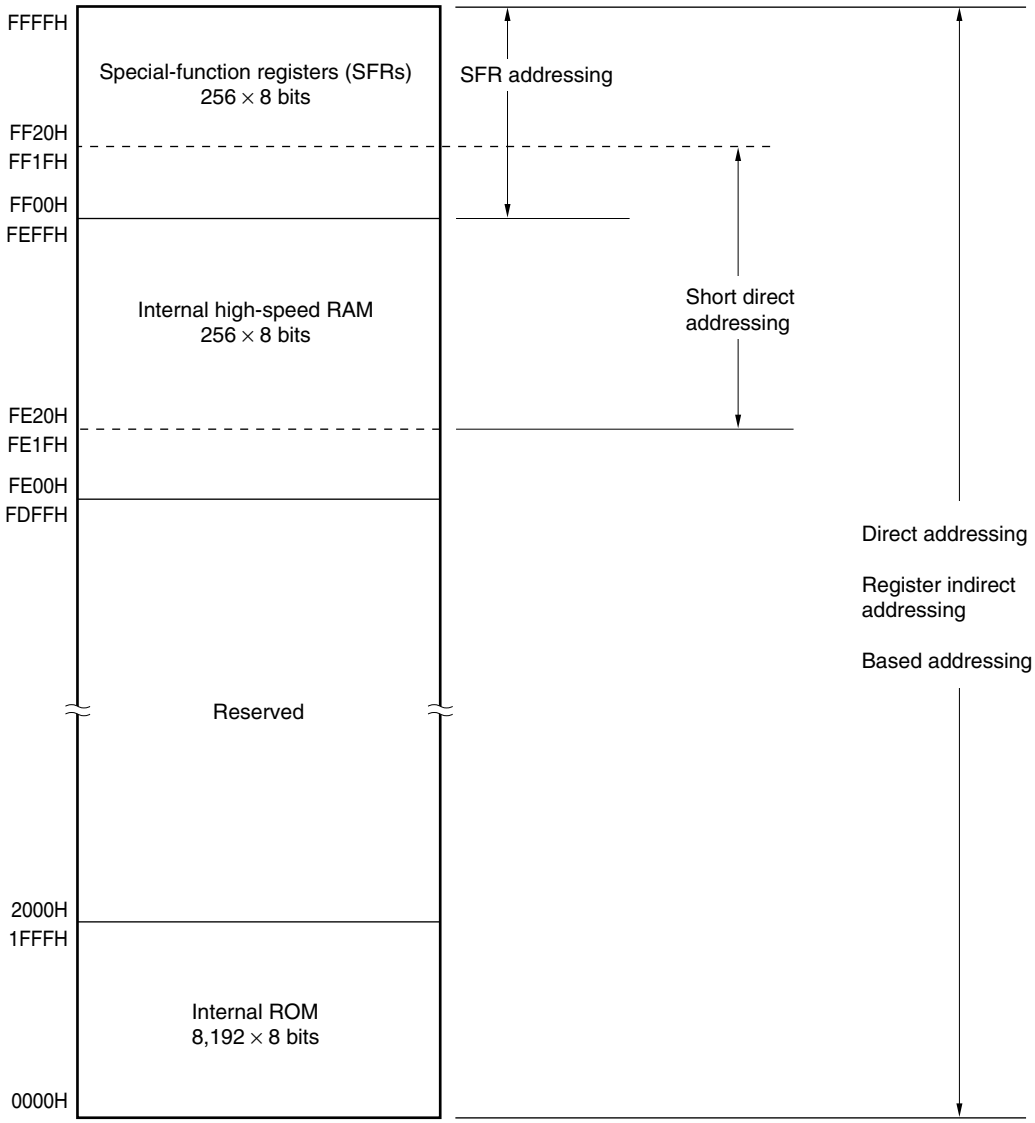
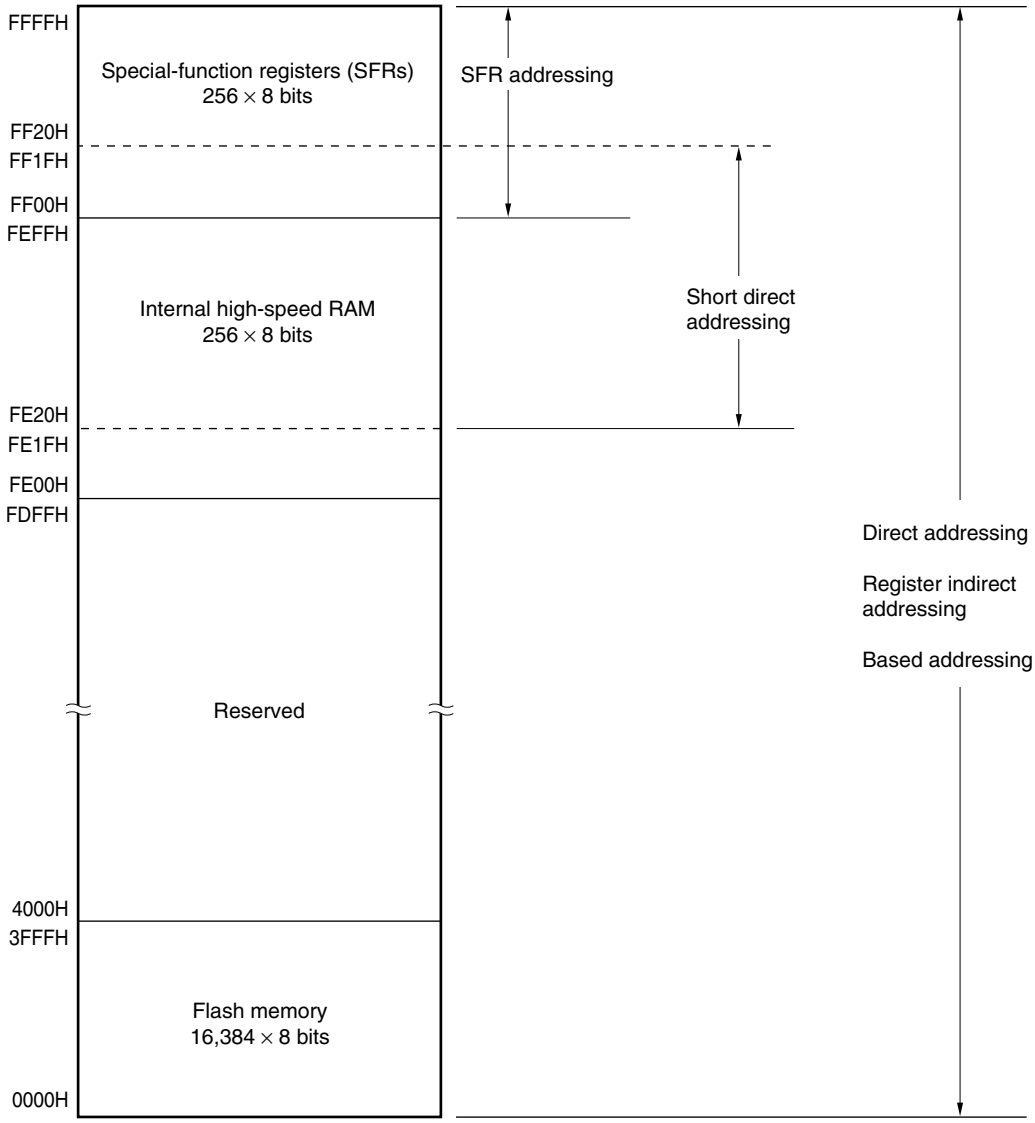


Figure 4-8. Data Memory Addressing (μPD78F9116A, 78F9116B, 78F9136A, 78F9136B)



4.2 Processor Registers

The μPD789104A/114A/124A/134A Subseries provides the following on-chip processor registers.

4.2.1 Control registers

The control registers contain special functions to control the program sequence statuses and stack memory. The program counter, program status word, and stack pointer are control registers.

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address information of the next program to be executed. In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data or register contents are set.

$\overline{\text{RESET}}$ input sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 4-9. Program Counter Configuration

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution. Program status word contents are automatically stacked upon interrupt request generation or PUSH PSW instruction execution and are automatically restored upon execution of the RETI and POP PSW instructions.

$\overline{\text{RESET}}$ input sets the PSW to 02H.

Figure 4-10. Program Status Word Configuration

	7							0
PSW	IE	Z	0	AC	0	0	1	CY

(a) Interrupt enable flag (IE)

This flag controls interrupt request acknowledgment operations of CPU.

When IE = 0, the IE flag is set to the interrupt disabled (DI) status. All interrupt requests except non-maskable interrupts are disabled.

When IE = 1, the IE flag is set to the interrupt enabled (EI) status and interrupt request acknowledgment is controlled by the interrupt mask flag for each interrupt source.

This flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(d) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit manipulation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register used to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 4-11. Stack Pointer Configuration

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of a write (save) to the stack memory and is incremented after a read (restore) from the stack memory.

Each stack operation saves/restores data as shown in Figures 4-12 and 4-13.

Caution Since $\overline{\text{RESET}}$ input makes the SP contents undefined, be sure to initialize the SP before instruction execution.

Figure 4-12. Data to Be Saved to Stack Memory

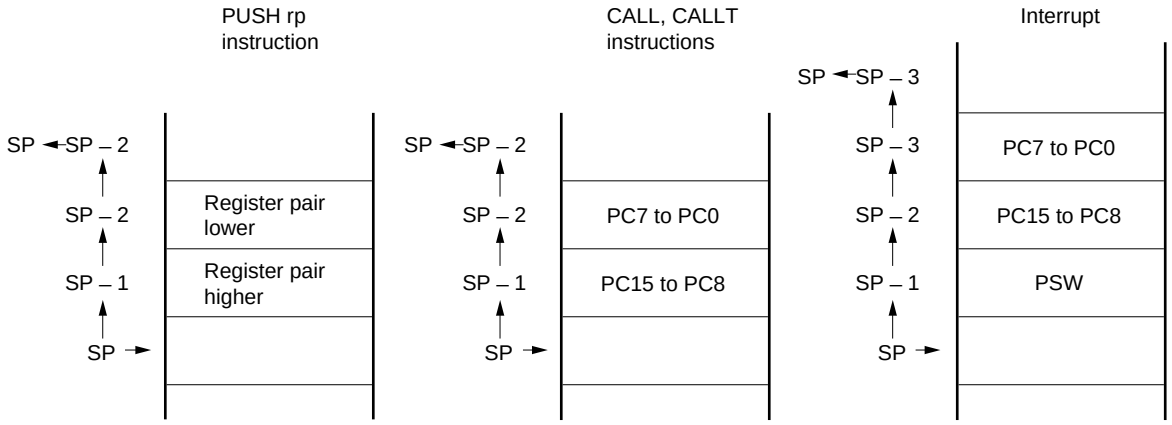
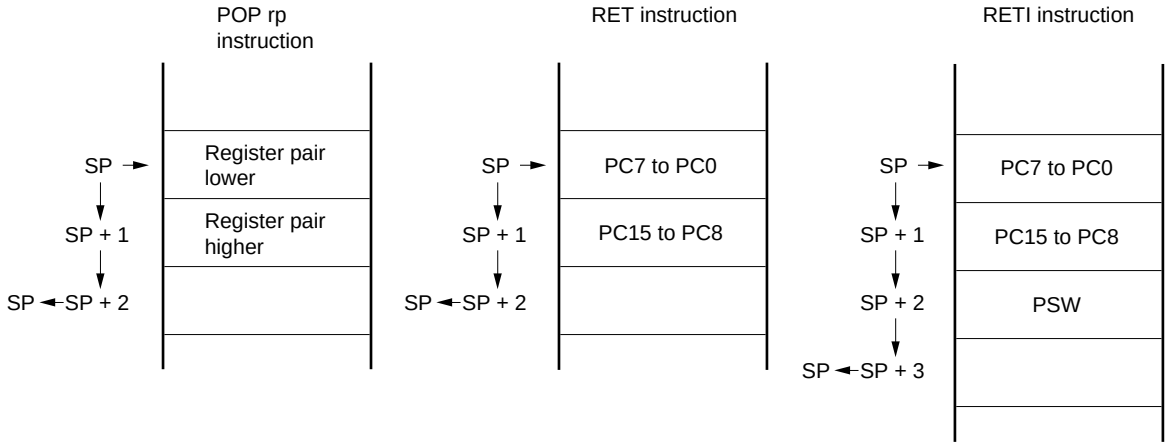


Figure 4-13. Data to Be Restored from Stack Memory



4.2.2 General-purpose registers

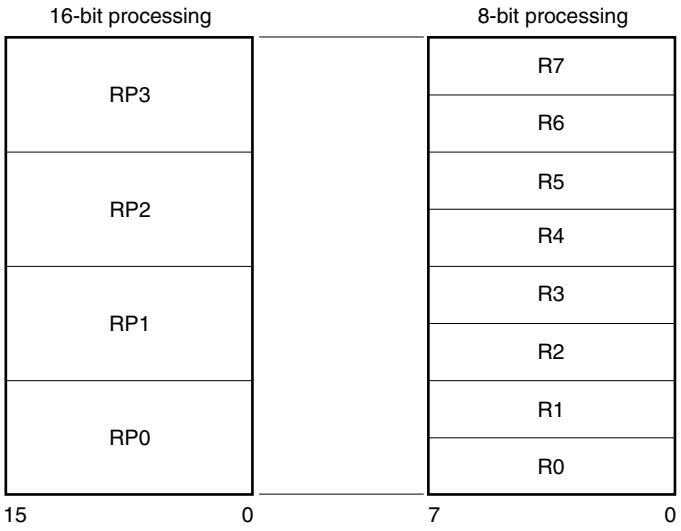
The general-purpose registers consist of eight 8-bit registers (X, A, C, B, E, D, L, and H).

Each register can be used as an 8-bit register, and in addition, two 8-bit registers in pairs can be used as a 16-bit register (AX, BC, DE, and HL).

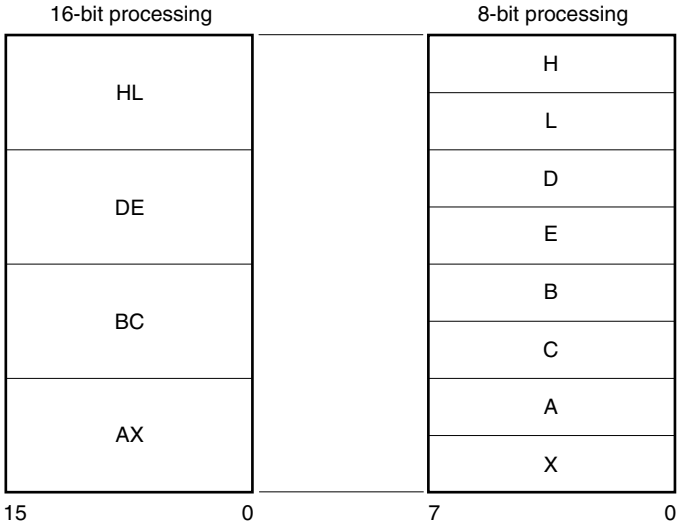
They can be described in terms of functional names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

Figure 4-14. General-Purpose Register Configuration

(a) Absolute names



(b) Functional names



4.2.3 Special-function registers (SFRs)

Unlike general-purpose registers, special-function registers have their own functions and are allocated to the 256-byte area FF00H to FFFFH.

Special-function registers can be manipulated, like general-purpose registers, with operation, transfer, and bit manipulation instructions. The bit units in which one register can be manipulated (1, 8, and 16) differ depending on the special-function register type.

Each bit unit for manipulation can be specified as follows.

- 1-bit manipulation
  A symbol reserved by the assembler is described as the operand (sfr.bit) of a 1-bit manipulation instruction. This manipulation can also be specified with an address.

- 8-bit manipulation
  A symbol reserved by the assembler is described as the operand (sfr) of an 8-bit manipulation instruction. This manipulation can also be specified with an address.

- 16-bit manipulation
  A symbol reserved by the assembler is described as the operand of a 16-bit manipulation instruction. When specifying an address, describe an even address.

Table 4-3 lists the special-function registers. The meanings of the symbols in this table are as follows.

- Symbol
  Indicates the addresses of the implemented special-function register. The symbols shown in this column are the reserved words of the assembler, and have already been defined in the header file “sfrbit.h” in the C compiler. Therefore, these symbols can be used as instruction operands if an assembler or integrated debugger is used.

- R/W
  Indicates whether the special-function register in question can be read or written.
  R/W: Read/write
  R: Read only
  W: Write only

- Bit units for manipulation
  Indicates the bit units (1, 8, and 16) in which the special-function register in question can be manipulated.

- After reset
  Indicates the status of the special-function register when the $\overline{\text{RESET}}$ signal is input.

Table 4-3. Special-Function Register List (1/2)

Address	Special-Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 Bit	8 Bits	16 Bits	
FF00H	Port 0	P0		R/W	√	√	–	00H
FF01H	Port 1	P1			√	√	–	
FF02H	Port 2	P2			√	√	–	
FF05H	Port 5	P5			√	√	–	
FF06H	Port 6	P6		R	√	√	–	
FF10H	16-bit multiplication result storage register 0	MUL0L	MUL0		–	√Note 1	√Note 2	Undefined
FF11H		MUL0H						
FF14H	A/D conversion result registerNote 3	ADCR0			–	√	√Note 2	
FF15H								
FF16H	16-bit compare register 20	CR20L	CR20	W	–	√Note 1	√Note 2	FFFFH
FF17H		CR20H						
FF18H	16-bit timer counter 20	TM20L	TM20	R	–	√Note 1	√Note 2	0000H
FF19H		TM20H						
FF1AH	16-bit capture register 20	TCP20L	TCP20		–	√Note 1	√Note 2	Undefined
FF1BH		TCP20H						
FF20H	Port mode register 0	PM0		R/W	√	√	–	FFH
FF21H	Port mode register 1	PM1			√	√	–	
FF22H	Port mode register 2	PM2			√	√	–	
FF25H	Port mode register 5	PM5			√	√	–	
FF32H	Pull-up resistor option register B2	PUB2			√	√	–	00H
FF42H	Time clock select register 2	TCL2			–	√	–	
FF48H	16-bit timer mode control register 20	TMC20			√	√	–	
FF50H	8-bit compare register 80	CR80		W	–	√	–	
FF51H	8-bit timer counter 80	TM80		R	–	√	–	Undefined
FF53H	8-bit timer mode control register 80	TMC80		R/W	√	√	–	00H

Notes 1. Although these registers are usually accessed in 16-bit units, they can also be accessed in 8-bit units. Access these registers in 8-bit units by means of direct addressing.

2. These registers can be accessed in 16-bit units only by means of short direct addressing.

3. When this register is used for an 8-bit A/D converter (μPD789104A and 789124A Subseries), it can be accessed only in 8-bit units. At this time, the register address is FF15H. When this register is used for a 10-bit A/D converter (μPD789114A and 789134A Subseries), it can be accessed only in 16-bit units. When using the μPD78F9116A and 78F9116B as the flash memory versions of the μPD789101A, 789102A, or 789104A, or when using the μPD78F9136A and 78F9136B as the flash memory versions of the μPD789121A, 789122A, or 789124A, this register can be accessed in 8-bit units. However, only the object file assembled with the μPD789101A, 789102A, or 789104A, or object file assembled with the μPD789121A, 789122A, or 789124A can be used.

Table 4-3. Special-Function Register List (2/2)

Address	Special-Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 Bit	8 Bits	16 Bits	
FF70H	Asynchronous serial interface mode register 20	ASIM20		R/W	√	√	–	00H
FF71H	Asynchronous serial interface status register 20	ASIS20		R	√	√	–	
FF72H	Serial operating mode register 20	CSIM20		R/W	√	√	–	
FF73H	Baud rate generator control register 20	BRGC20			–	√	–	
FF74H	Transmit shift register 20	TXS20	SIO20	W	–	√	–	FFH
	Receive buffer register 20	RXB20		R	–	√	–	Undefined
FF80H	A/D converter mode register 0	ADM0		R/W	√	√	–	00H
FF84H	Analog input channel specification register 0	ADS0			√	√	–	
FFD0H	Multiplication data register A0	MRA0		W	√	√	–	Undefined
FFD1H	Multiplication data register B0	MRB0			√	√	–	
FFD2H	Multiplier control register 0	MULC0		R/W	√	√	–	00H
FFE0H	Interrupt request flag register 0	IF0			√	√	–	
FFE1H	Interrupt request flag register 1	IF1			√	√	–	
FFE4H	Interrupt mask flag register 0	MK0			√	√	–	FFH
FFE5H	Interrupt mask flag register 1	MK1			√	√	–	
FFECH	External interrupt mode register 0	INTM0			–	√	–	00H
FFF7H	Pull-up resistor option register 0	PU0			√	√	–	
FFF9H	Watchdog timer mode register	WDTM			√	√	–	
FFFAH	Oscillation stabilization time select register[Note]	OSTS			–	√	–	04H
FFFBH	Processor clock control register	PCC			√	√	–	02H

Note μPD789104A, 789114A Subseries only

4.3 Instruction Address Addressing

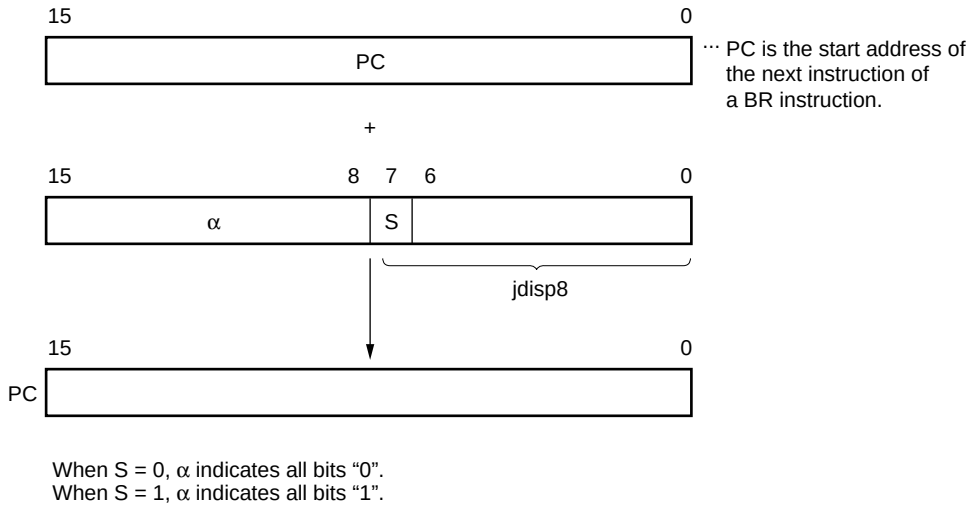
An instruction address is determined by the program counter (PC) contents. The PC contents are normally incremented (+1 for each byte) automatically according to the number of bytes of the instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to the PC and branched by the following addressing (for details of each instruction, refer to the **78K/0S Series Instructions User's Manual (U11047E)**).

4.3.1 Relative addressing

[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit. In other words, the range of branch in relative addressing is between −128 and +127 of the start address of the following instruction. This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, α indicates all bits "0".
When S = 1, α indicates all bits "1".

4.3.2 Immediate addressing

[Function]

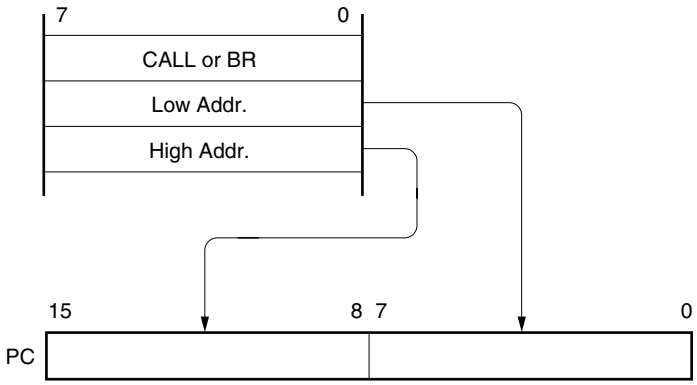
Immediate data in the instruction word is transferred to the program counter (PC) and branched.

This function is carried out when the CALL !addr16 and BR !addr16 instructions are executed.

The CALL !addr16 and BR !addr16 instructions can branch to all the memory spaces.

[Illustration]

In case of CALL !addr16, BR !addr16 instruction



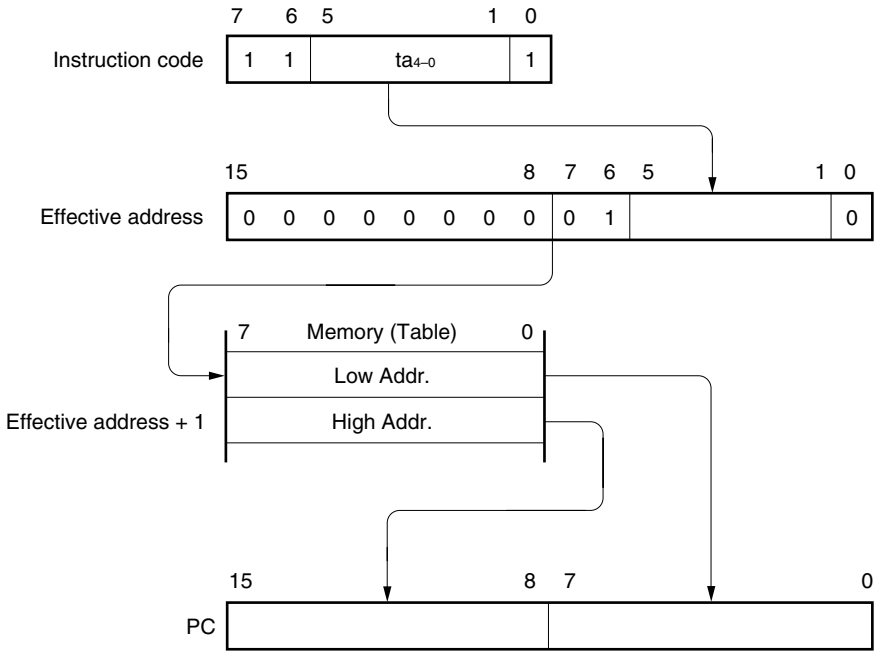
4.3.3 Table indirect addressing

[Function]

The table contents (branch destination address) of the particular location to be addressed by the lower 5-bit immediate data of an instruction code from bit 1 to bit 5 are transferred to the program counter (PC) and branched.

Table indirect addressing is carried out when the CALLT [addr5] instruction is executed. This instruction can refer to the address stored in the memory table 40H to 7FH and branch to all the memory spaces.

[Illustration]



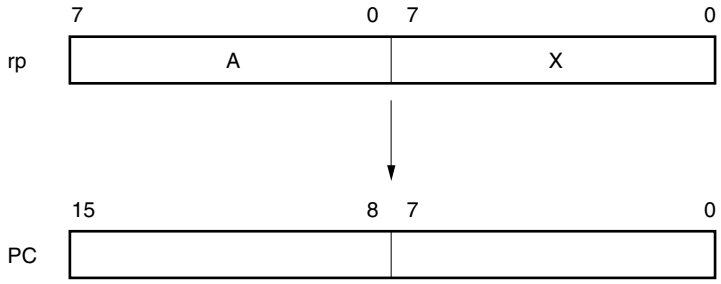
4.3.4 Register addressing

[Function]

The register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



4.4 Operand Address Addressing

The following methods are available to specify the register and memory (addressing) to undergo manipulation during instruction execution.

4.4.1 Direct addressing

[Function]

The memory indicated by immediate data in an instruction word is directly addressed.

[Operand format]

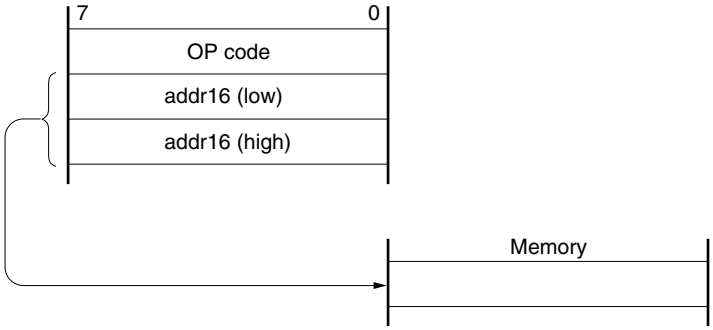
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !FE00H; When setting !addr16 to FE00H

Instruction code	0	0	1	0	1	0	0	1	OP code
	0	0	0	0	0	0	0	0	00H
	1	1	1	1	1	1	1	0	FEH

[Illustration]



4.4.2 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

The fixed space where this addressing is applied to is the 256-byte space FE20H to FF1FH. An internal high-speed RAM and special-function registers (SFRs) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H to FF1FH) where short direct addressing is applied is a part of the total SFR area. In this area, ports which are frequently accessed in a program and a compare register of the timer/event counter are mapped, and these SFRs can be manipulated with a small number of bytes and clocks.

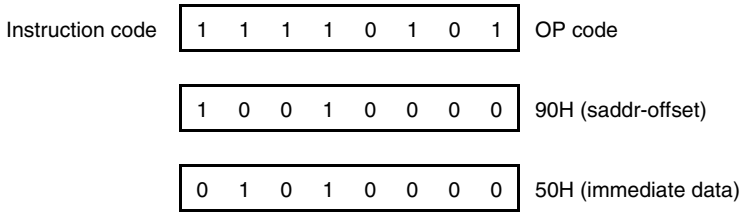
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. Refer to **[Illustration]**.

[Operand format]

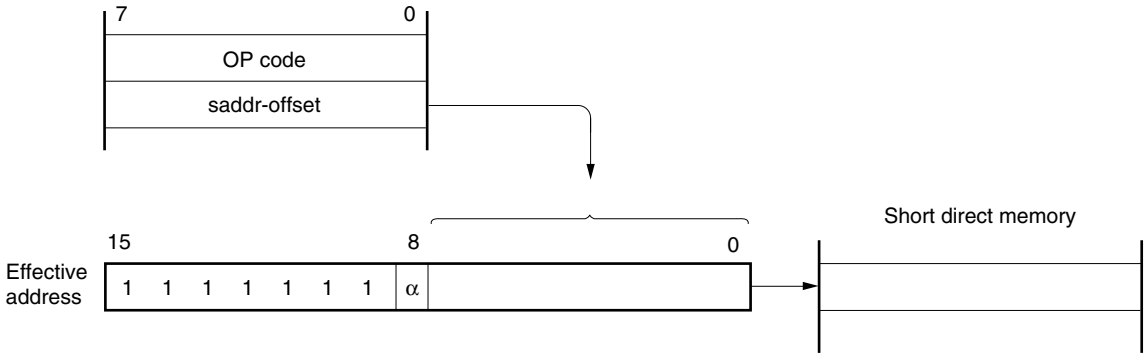
Identifier	Description
saddr	Label or FE20H to FF1FH immediate data
saddrp	Label or FE20H to FF1FH immediate data (even address only)

[Description example]

MOV FE90H, #50H; When setting saddr to FE90H and the immediate data to 50H



[Illustration]



When 8-bit immediate data is 20H to FFH, $\alpha = 0$.
When 8-bit immediate data is 00H to 1FH, $\alpha = 1$.

4.4.3 Special-function register (SFR) addressing

[Function]

Memory-mapped special-function registers (SFRs) are addressed with 8-bit immediate data in an instruction word.

This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. However, SFRs mapped at FF00H to FF1FH can be accessed with short direct addressing.

[Operand format]

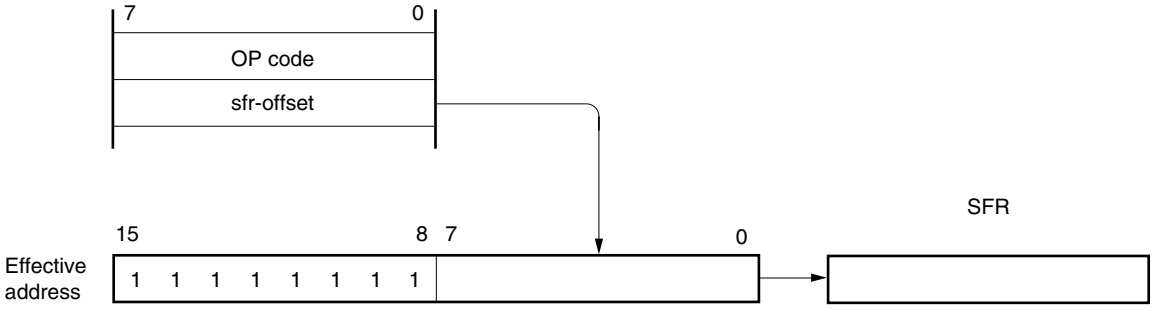
Identifier	Description
sfr	Special-function register name

[Description example]

MOV PM0, A; When selecting PM0 for sfr

Instruction code	1	1	1	0	0	1	1	1
	0	0	1	0	0	0	0	0

[Illustration]



4.4.4 Register addressing

[Function]

General-purpose registers are accessed as operands. The general-purpose register to be accessed is specified with the register specify code and functional name in the instruction code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the instruction code.

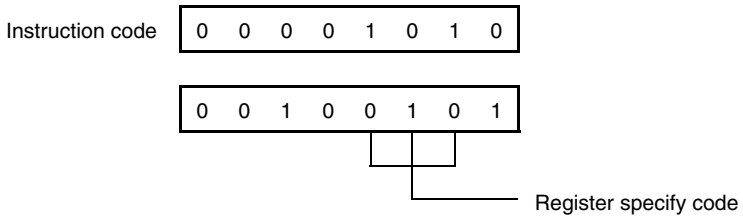
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

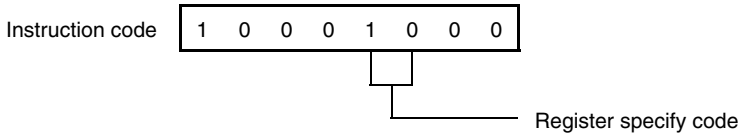
'r' and 'rp' can be described with absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; When selecting the C register for r



INCW DE; When selecting the DE register pair for rp



4.4.5 Register indirect addressing

[Function]

The memory is addressed with the contents of the register pair specified as an operand. The register pair to be accessed is specified with the register pair specify code in the instruction code. This addressing can be carried out for all the memory spaces.

[Operand format]

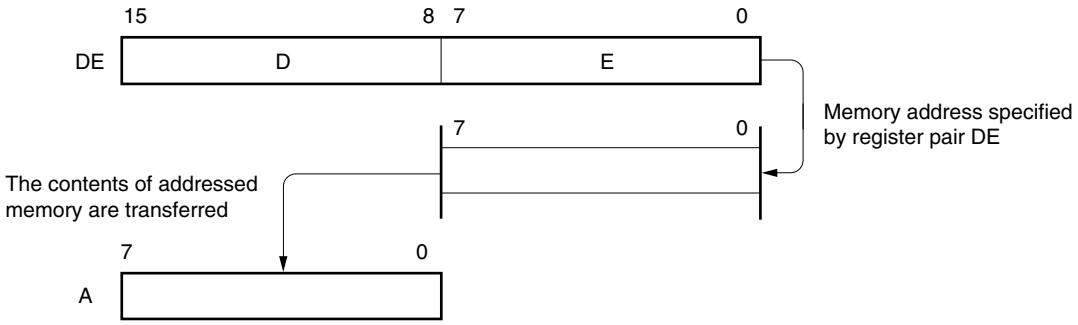
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; When selecting register pair [DE]

Instruction code	0	0	1	0	1	0	1	1

[Illustration]



4.4.6 Based addressing

[Function]

8-bit immediate data is added to the contents of the base register, that is, the HL register pair, and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

Identifier	Description
–	[HL+byte]

[Description example]

MOV A, [HL+10H]; When setting byte to 10H

Instruction code	0	0	1	0	1	1	0	1
	0	0	0	1	0	0	0	0

4.4.7 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call, and RETURN instructions are executed or the register is saved/reset upon generation of an interrupt request.

Stack addressing can be used to address the internal high-speed RAM area only.

[Description example]

In the case of PUSH DE

Instruction code	1	0	1	0	1	0	1	0

CHAPTER 5 PORT FUNCTIONS

5.1 Functions of Ports

The μPD789104A/114A/124A/134A Subseries provides the ports shown in Figure 5-1, enabling various methods of control.

Numerous other functions are provided that can be used in addition to the digital I/O port function. For more information on these additional functions, refer to **CHAPTER 3 PIN FUNCTIONS**.

Figure 5-1. Port Types

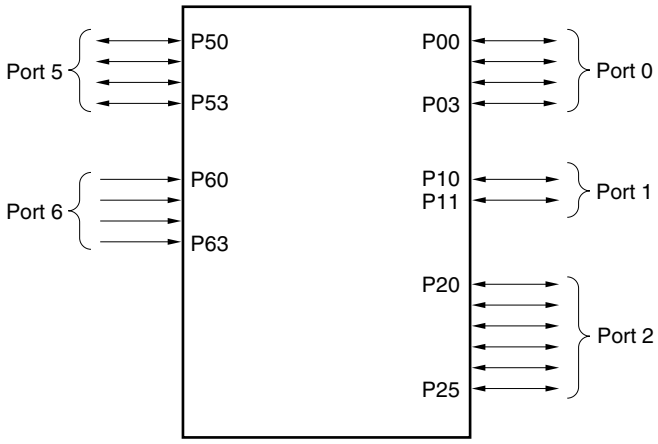


Table 5-1. Port Functions

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0 4-bit I/O port Input/output can be specified in 1-bit units. When used as input port, use of an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P10, P11	I/O	Port 1 2-bit I/O port Input/output can be specified in 1-bit units. When used as input port, use of an on-chip pull-up resistor can be specified by means of pull-up resistor option register 0 (PU0).	Input	–
P20	I/O	Port 2 6-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of pull-up resistor option register B2 (PUB2).	Input	ASCK20/$\overline{\text{SCK20}}$
P21				TxD20/SO20
P22				RxD20/SI20
P23				INTP0/CPT20/$\overline{\text{SS20}}$
P24				INTP1/TO80/TO20
P25				INTP2/TI80
P50 to P53	I/O	Port 5 4-bit N-ch open-drain I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified for mask ROM versions by a mask option.	Input	–
P60 to 63	Input	Port 6 4-bit input-only port	Input	ANI0 to ANI3

5.2 Port Configuration

A port consists of the following hardware.

Table 5-2. Configuration of Port

Item	Configuration
Control register	Port mode register (PM0 to PM2, PM5) Pull-up resistor option register 0 (PU0) Pull-up option register B2 (PUB2)
Port	Total: 20 (input: 4, I/O: 16)
Pull-up resistor	• Mask ROM versions Total: 16 (software control: 12, mask option specification: 4) • Flash memory versions Total: 12 (software control only)

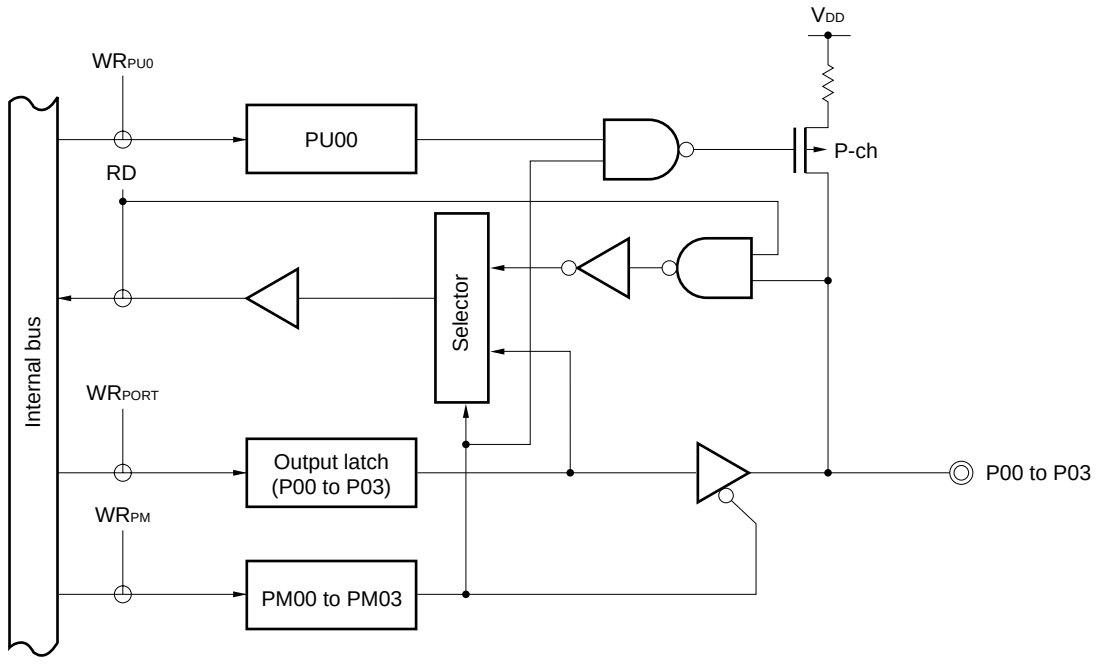
5.2.1 Port 0

This is a 4-bit I/O port with output latches. Port 0 can be set to input or output mode in 1-bit units by using port mode register 0 (PM0). When pins P00 to P03 are used as input port pins, on-chip pull-up resistors can be connected in 4-bit units by using pull-up resistor option register 0 (PU0).

$\overline{\text{RESET}}$ input sets port 0 to input mode.

Figure 5-2 shows the block diagram of port 0.

Figure 5-2. Block Diagram of P00 to P03



PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 0 read signal
WR: Port 0 write signal

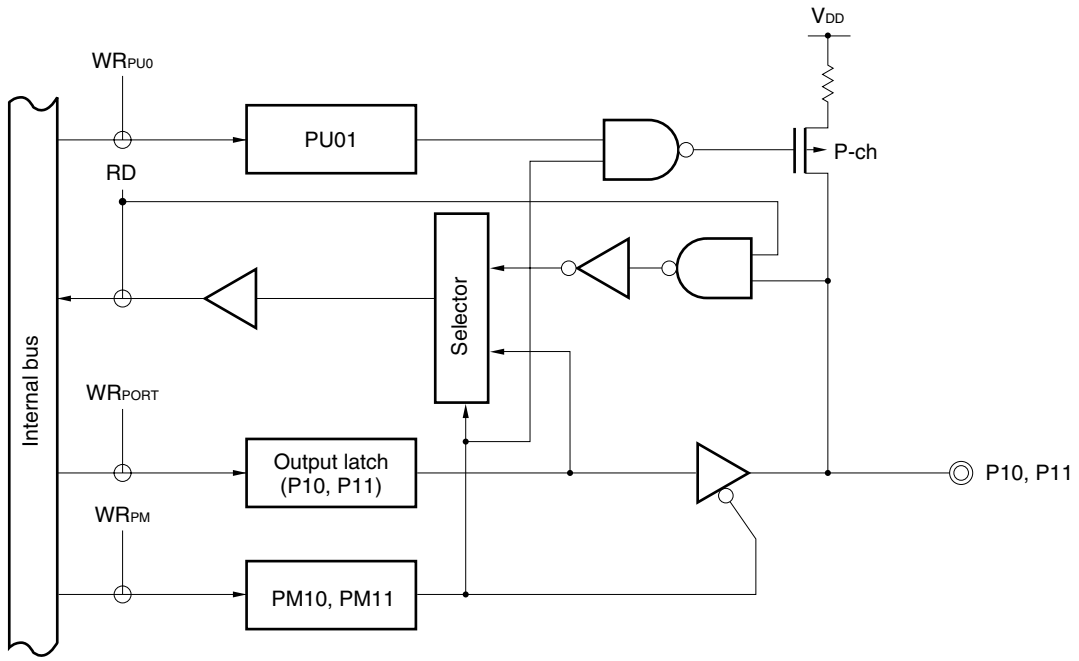
5.2.2 Port 1

This is a 2-bit I/O port with output latches. Port 1 can be set to input or output mode in 1-bit units by using port mode register 1 (PM1). When pins P10 and P11 are used as input port pins, on-chip pull-up resistors can be connected in 2-bit units by using pull-up resistor option register 0 (PU0).

$\overline{\text{RESET}}$ input sets port 1 to input mode.

Figure 5-3 shows the block diagram of port 1.

Figure 5-3. Block Diagram of P10 and P11



PU0: Pull-up resistor option register 0
PM: Port mode register
RD: Port 1 read signal
WR: Port 1 write signal

5.2.3 Port 2

This is a 6-bit I/O port with output latches. Port 2 can be set to input or output mode in 1-bit units by using port mode register 2 (PM2). Use of on-chip pull-up resistors can be specified for pins P20 to P25 in 1-bit units by using pull-up resistor option register B2 (PUB2).

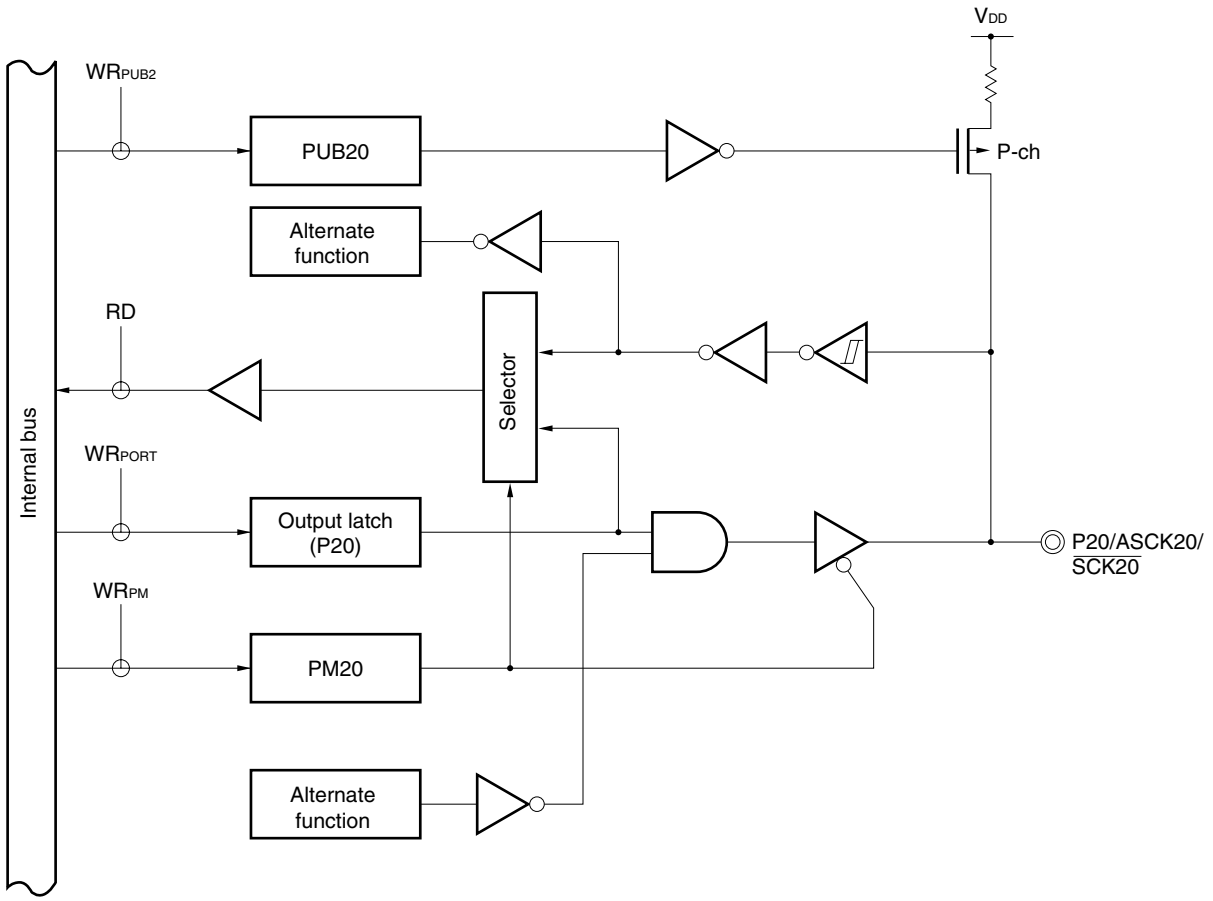
The port is also used as the serial interface data I/O, clock I/O, timer I/O, and external interrupt input.

$\overline{\text{RESET}}$ input sets port 2 to input mode.

Figures 5-4 to 5-7 show block diagrams of port 2.

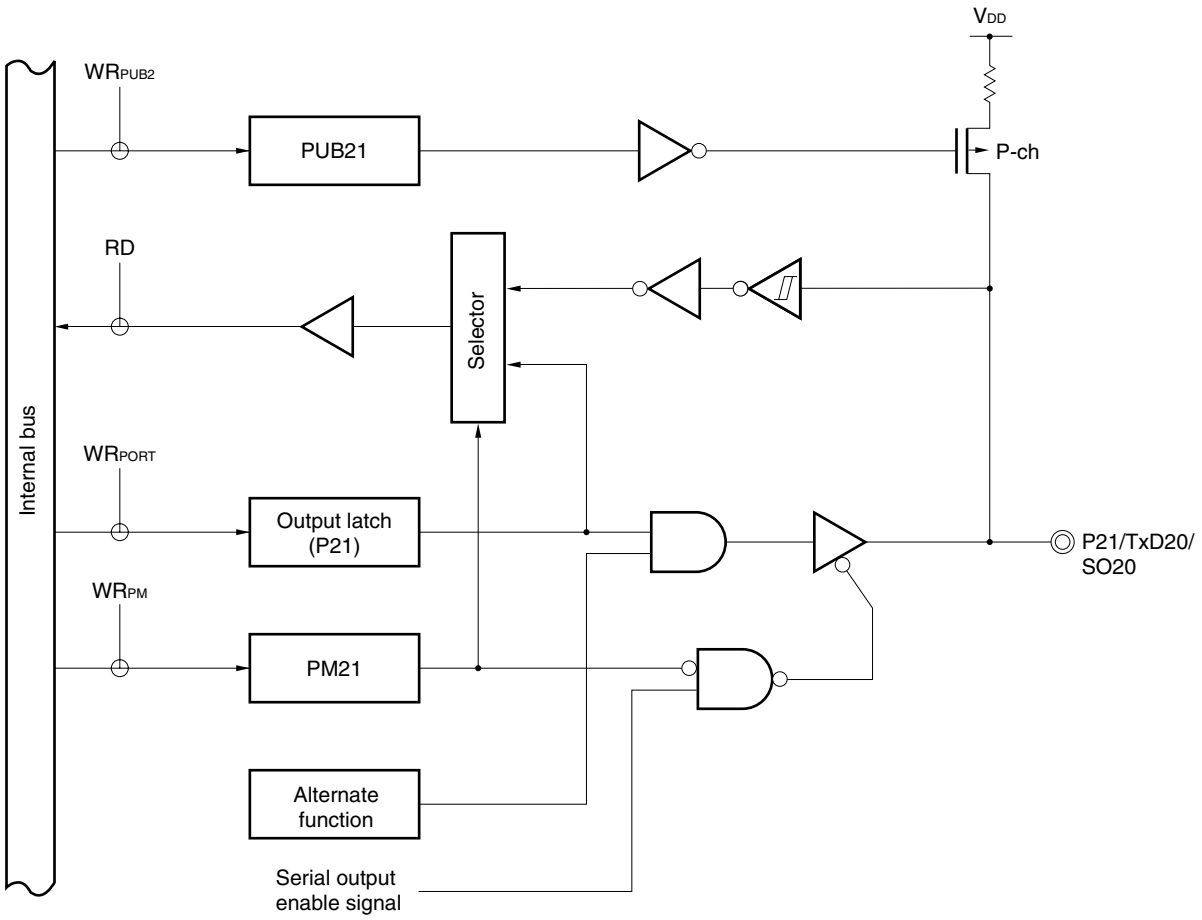
Caution When using the pins of port 2 as the serial interface, the I/O or output latch must be set according to the function to be used. For how to set the latches, see Table 13-2 Serial Interface 20 Operating Mode Settings.

Figure 5-4. Block Diagram of P20



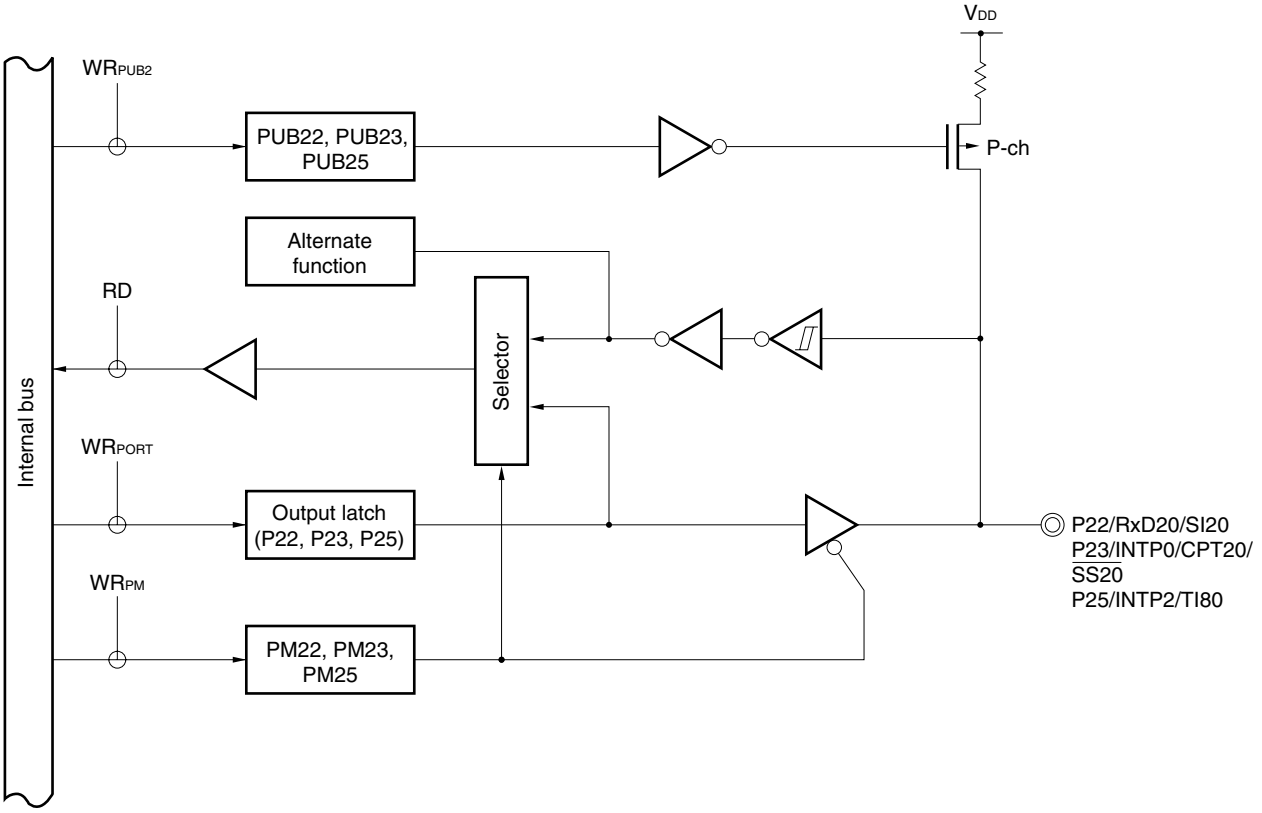
PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Figure 5-5. Block Diagram of P21



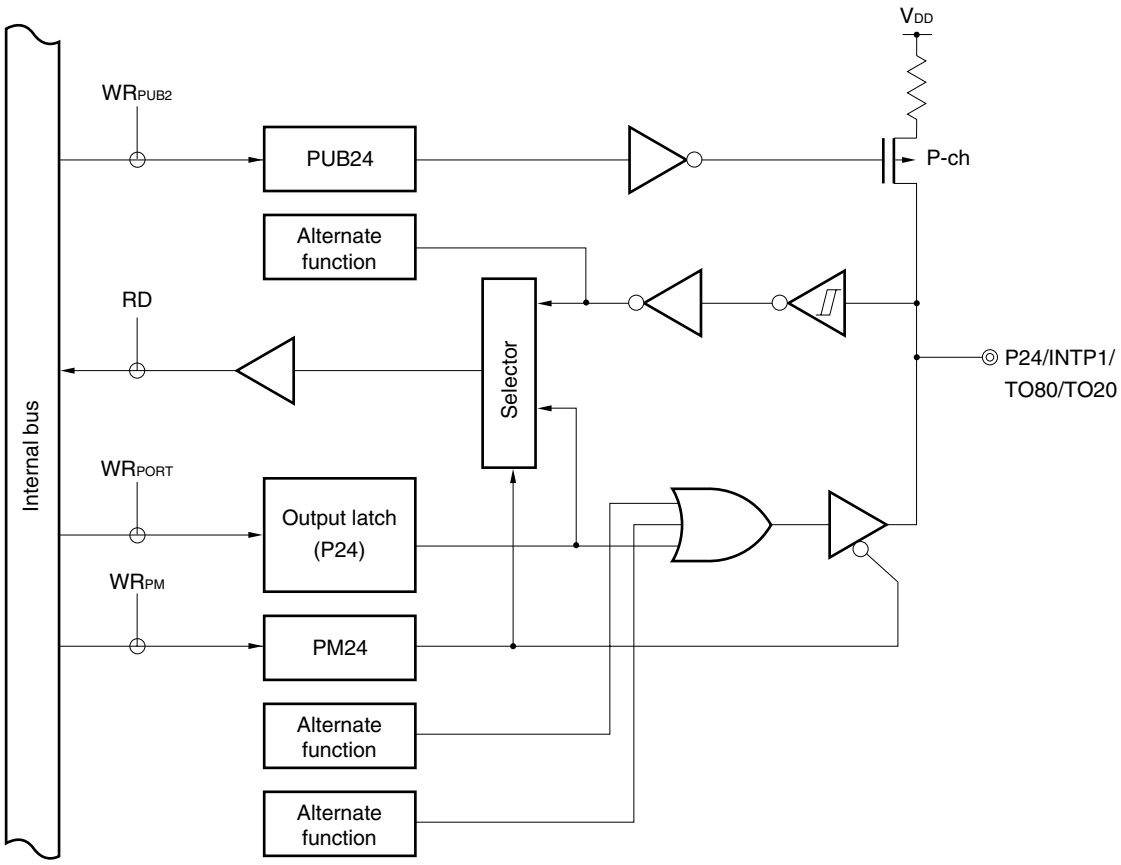
PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Figure 5-6. Block Diagram of P22, P23, and P25



PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

Figure 5-7. Block Diagram of P24



PUB2: Pull-up resistor option register B2
PM: Port mode register
RD: Port 2 read signal
WR: Port 2 write signal

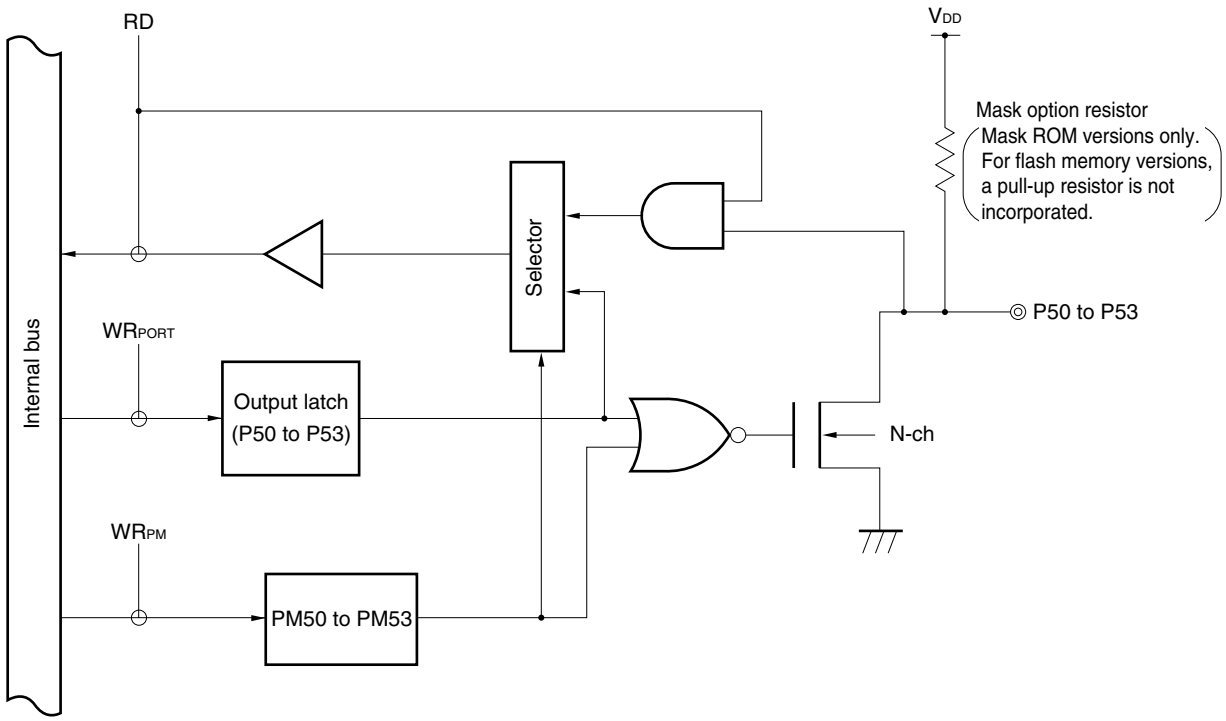
5.2.4 Port 5

This is a 4-bit N-ch open-drain I/O port with output latches. Port 5 can be set to input or output mode in 1-bit units by using port mode register 5 (PM5). For a mask ROM version, whether a pull-up resistor is to be incorporated can be specified by a mask option.

$\overline{\text{RESET}}$ input sets port 5 to input mode.

Figure 5-8 shows a block diagram of port 5.

Figure 5-8. Block Diagram of P50 to P53



PM: Port mode register
RD: Port 5 read signal
WR: Port 5 write signal

Caution When using port 5 of the μPD78F9116A and 78F9136A as an input port, be sure to observe the restrictions listed below.

<1> When V_{DD} = 1.8 to 5.5 V
Use within the range of T_A = 25 to 85°C

<2> When T_A = –40 to +85°C
Use within the range of V_{DD} = 2.7 to 5.5 V

<3> When T_A = –40 to +85°C and V_{DD} = 1.8 to 5.5 V
Issue three consecutive read instructions when reading port 5.

If the above restrictions are not observed, the input value may be read incorrectly.
Note, however, that these restrictions do not apply when port 5 pins are used as output pins, or when the product is other than μPD78F9116A or 78F9136A.

5.2.5 Port 6

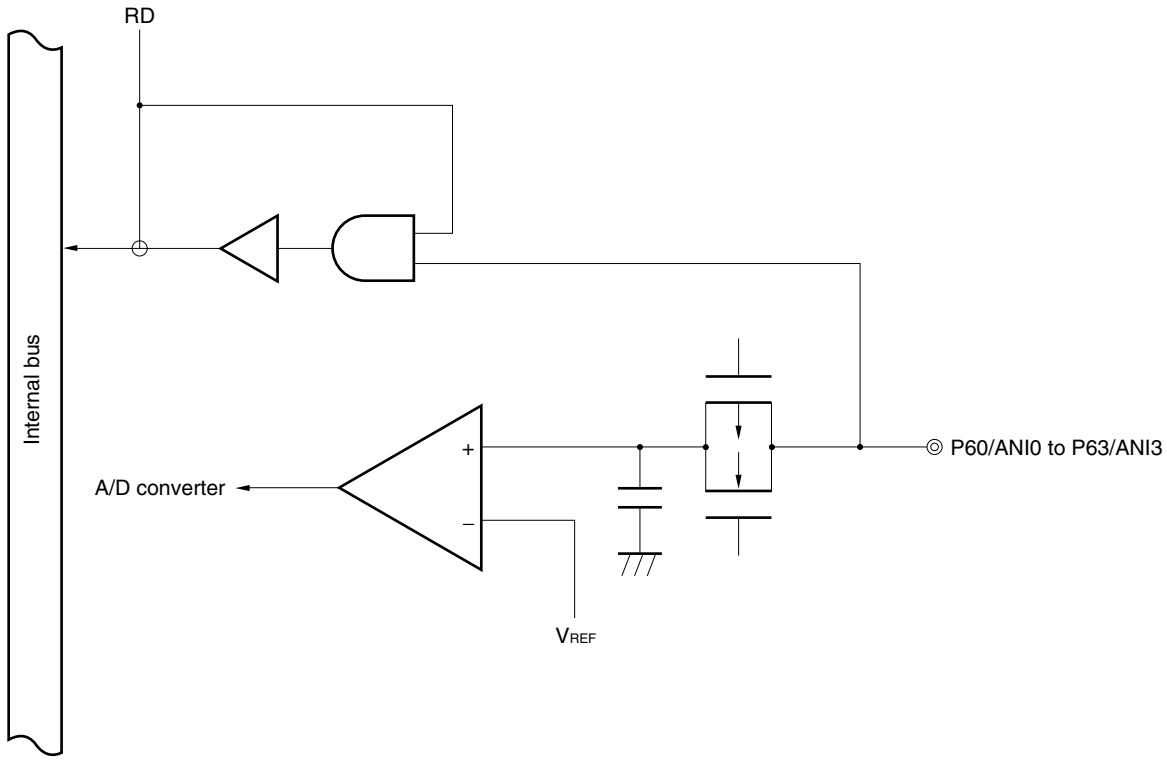
This is a 4-bit input port.

The port is also used for analog input to the A/D converter.

$\overline{\text{RESET}}$ input sets port 6 to input mode.

Figure 5-9 shows a block diagram of port 6.

Figure 5-9. Block Diagram of P60 to P63



5.3 Port Function Control Registers

The following three types of registers control the ports.

- Port mode registers (PM0 to PM2, PM5)
- Pull-up resistor option register 0 (PU0)
- Pull-up resistor option register B2 (PUB2)

(1) Port mode registers (PM0 to PM2, PM5)

These registers are used to set port I/O in 1-bit units.

Port mode registers are independently set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register and output latch according to Table 5-3.

Caution As port 2 has an alternate function as external interrupt input, when the port function output mode is specified and the output level is changed, the interrupt request flag is set. When the output mode is used, therefore, the interrupt mask flag should be set to 1 beforehand.

Table 5-3. Port Mode Register and Output Latch Settings When Using Alternate Functions

Pin Name	Alternate Function		PM××	P××
	Name	I/O		
P23	INTP0	Input	1	×
	CPT20	Input	1	×
P24	INTP1	Input	1	×
	TO80	Output	0	0
	TO20	Output	0	0
P25	INTP2	Input	1	×
	TI80	Input	1	×

Caution When Port 2 is used for serial interface pins, the I/O latch or output latch must be set according to its function. For the setting method, refer to Table 13-2 Serial Interface 20 Operating Mode Settings.

Remark ×: don't care
PM××: Port mode register
P××: Port output latch

Figure 5-10. Port Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	1	1	1	1	1	1	PM11	PM10	FF21H	FFH	R/W
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM5	1	1	1	1	PM53	PM52	PM51	PM50	FF25H	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0 to 2, 5, n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

(2) Pull-up resistor option register 0 (PU0)

Pull-up resistor option register 0 (PU0) sets whether to use on-chip pull-up resistors at each port or not.

At a port where use of on-chip pull-up resistors has been specified by PU0, the pull-up resistors can be internally used only for the bits set in input mode. No on-chip pull-up resistors can be used for the bits set in output mode, in spite of the setting of PU0. On-chip pull-up resistors can also not be used when the pins are used as the alternate-function output pins.

PU0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears PU0 to 00H.

Figure 5-11. Format of Pull-up Resistor Option Register 0

Symbol	7	6	5	4	3	2	<1>	<0>	Address	After reset	R/W
PU0	0	0	0	0	0	0	PU01	PU00	FFF7H	00H	R/W

PU0m	Pm on-chip pull-up resistor selection (m = 0, 1)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

(3) Pull-up resistor option register B2 (PUB2)

This register specifies whether an on-chip pull-up resistor is connected to each pin of port 2. A pin so specified by PUB2 is connected to an on-chip pull-up resistor regardless of the setting of the port mode register.

PUB2 is set with a 1-bit or 8-bit manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 00H.

Figure 5-12. Format of Pull-up Resistor Option Register B2

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
PUB2	0	0	PUB25	PUB24	PUB23	PUB22	PUB21	PUB20	FF32H	00H	R/W

PUB2n	P2n on-chip pull-up resistor selection (n = 0 to 5)
0	On-chip pull-up resistor not used
1	On-chip pull-up resistor used

5.4 Operation of Port Functions

The operation of a port differs depending on whether the port is set in input or output mode, as described below.

5.4.1 Writing to I/O port

(1) In output mode

A value can be written to the output latch of a port by using a transfer instruction. The contents of the output latch can be output from the pins of the port.

Once data is written to the output latch, it is retained until new data is written to the output latch.

(2) In input mode

A value can be written to the output latch by using a transfer instruction. However, the status of the port pin is not changed because the output buffer is off.

Once data is written to the output latch, it is retained until new data is written to the output latch.

Caution A 1-bit memory manipulation instruction is executed to manipulate 1 bit of a port. However, this instruction accesses the port in 8-bit units. When this instruction is executed to manipulate a bit of an I/O port, therefore, the contents of the output latch of the pin that is set in the input mode and not subject to manipulation become undefined.

5.4.2 Reading from I/O port

(1) In output mode

The contents of the output latch can be read by using a transfer instruction. The contents of the output latch are not changed.

(2) In input mode

The status of a pin can be read by using a transfer instruction. The contents of the output latch are not changed.

Caution When using port 5 of μPD78F9116A and 78F9136A as an input port, be sure to observe the restrictions listed below.

<1> When V_{DD} = 1.8 to 5.5 V
Use within the range of T_A = 25 to 85°C

<2> When T_A = –40 to +85°C
Use within the range of V_{DD} = 2.7 to 5.5 V

<3> When T_A = –40 to +85°C and V_{DD} = 1.8 to 5.5 V
Issue three consecutive read instructions when reading port 5.

If the above restrictions are not observed, the input value may be read incorrectly.
Note, however, that these restrictions do not apply when port 5 pins are used as output pins, or when the product is other than μPD78F9116A or 78F9136A.

5.4.3 Arithmetic operation of I/O port

(1) In output mode

An arithmetic operation can be performed on the contents of the output latch. The result of the operation is written to the output latch. The contents of the output latch are output from the port pins.

Once data is written to the output latch, it is retained until new data is written to the output latch.

(2) In input mode

The contents of the output latch become undefined. However, the status of the pin is not changed because the output buffer is off.

Caution A 1-bit memory manipulation instruction is executed to manipulate 1 bit of a port. However, this instruction accesses the port in 8-bit units. When this instruction is executed to manipulate a bit of an I/O port, therefore, the contents of the output latch of the pin that is set in the input mode and not subject to manipulation become undefined.

CHAPTER 6 CLOCK GENERATOR (μPD789104A, 789114A SUBSERIES)

6.1 Function of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware. Oscillation is stopped by executing the STOP instruction.

The system clock oscillator is as follows.

★ • System clock (crystal/ceramic) oscillator

<Expanded-specification products>

This circuit oscillates a clock at a frequency of 1.0 to 10.0 MHz.

<Conventional-specification products>

This circuit oscillates a clock at a frequency of 1.0 to 5.0 MHz.

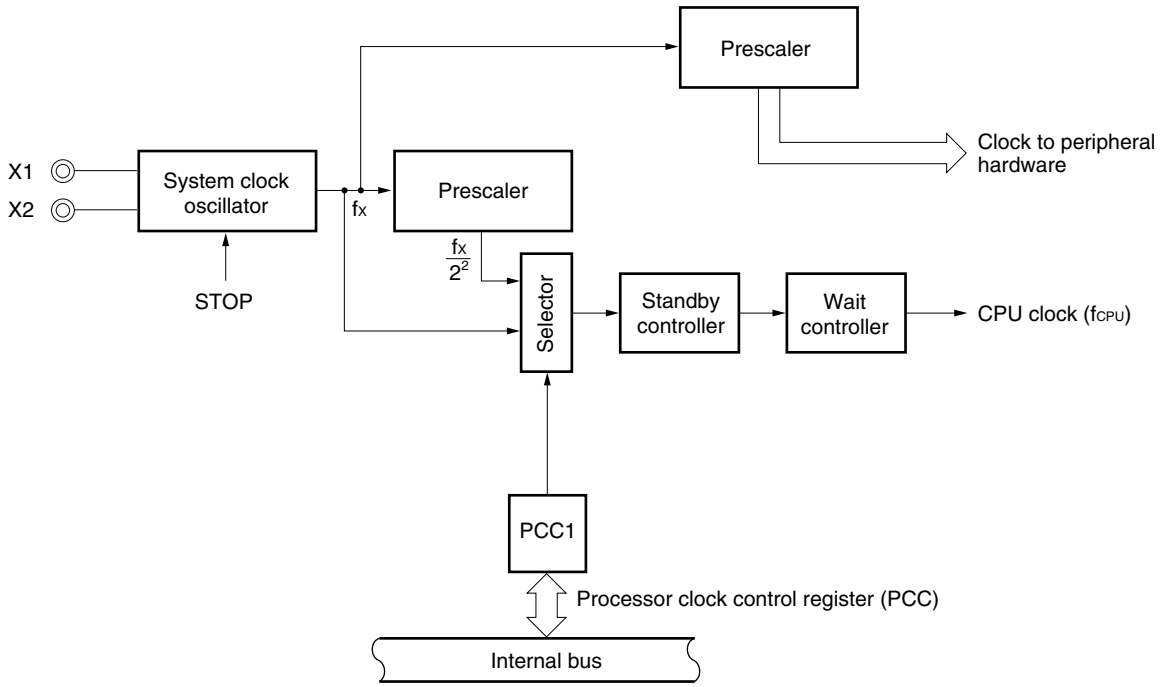
6.2 Configuration of Clock Generator

The clock generator consists of the following hardware.

Table 6-1. Configuration of Clock Generator

Item	Configuration
Control register	Processor clock control register (PCC)
Oscillator	Crystal/ceramic oscillator

Figure 6-1. Block Diagram of Clock Generator



6.3 Register Controlling Clock Generator

The clock generator is controlled by the following register.

- Processor clock control register (PCC)

(1) Processor clock control register (PCC)

PCC sets the CPU clock selection and the division ratio.

PCC is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PCC to 02H.

Figure 6-2. Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	0	0	0	0	0	0	PCC1	0	FFFBH	02H	R/W

★

PCC1	CPU clock (f_{CPU}) selection	Minimum instruction execution time: $2/f_{CPU}$	
		@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation
0	f_X	0.2 μs	0.4 μs
1	$f_X/2^2$	0.8 μs	1.6 μs

Note Expanded-specification products only

Caution Bit 0 and bits 2 to 7 must be set to 0.

Remark f_X: System clock oscillation frequency

6.4 System Clock Oscillator

6.4.1 System clock oscillator

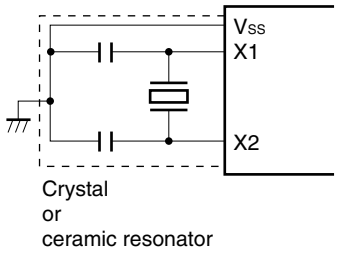
The system clock oscillator is oscillated by the crystal or ceramic resonator connected across the X1 and X2 pins.

An external clock can also be input to the system clock oscillator. In this case, input the clock signal to the X1 pin, and leave the X2 pin open.

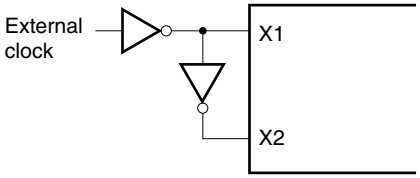
Figure 6-3 shows the external circuit of the system clock oscillator.

Figure 6-3. External Circuit of System Clock Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



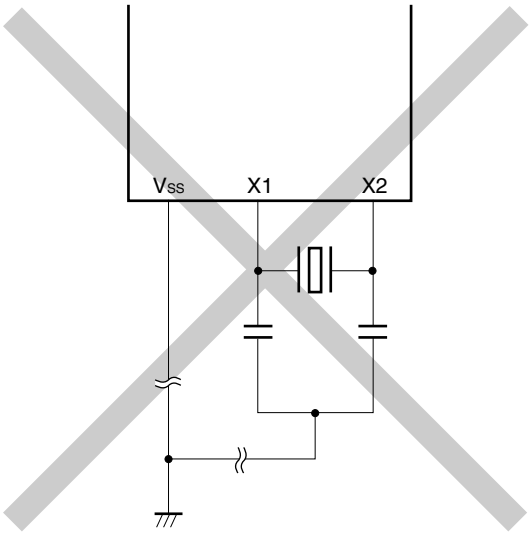
Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Figure 6-4 shows examples of incorrect resonator connection.

Figure 6-4. Examples of Incorrect Resonator Connection (1/2)

(a) Too long wiring



(b) Crossed signal line

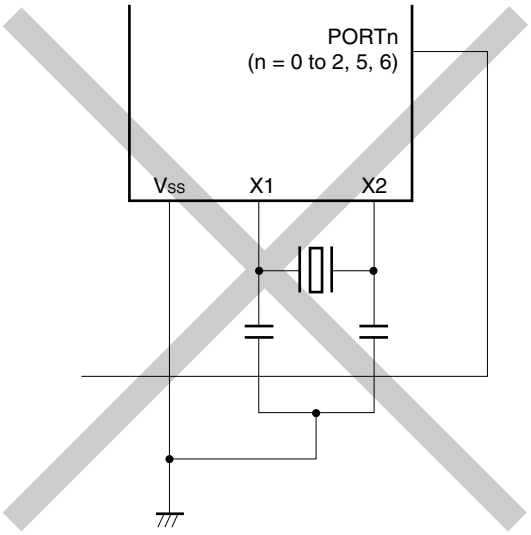
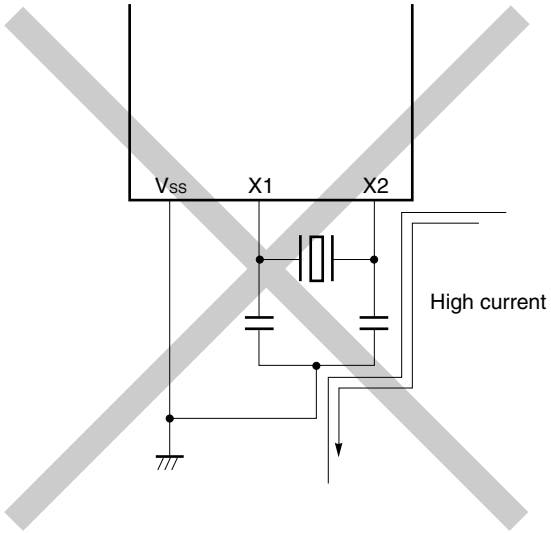
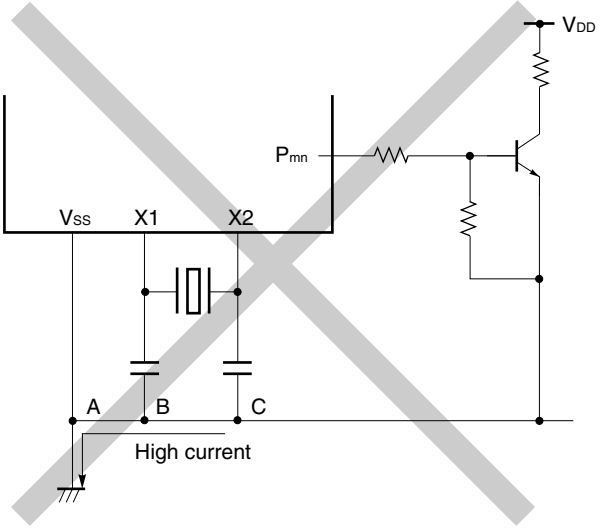


Figure 6-4. Examples of Incorrect Resonator Connection (2/2)

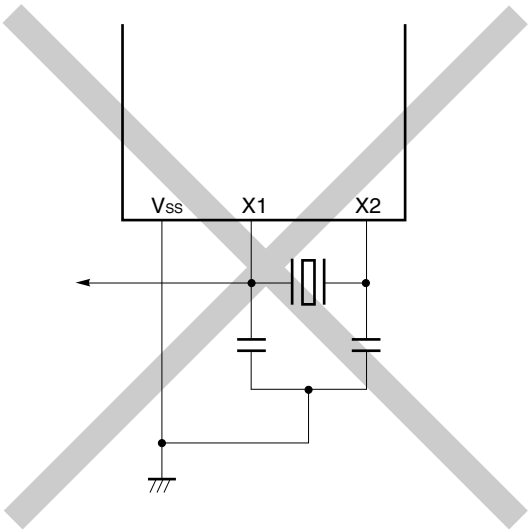
(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(e) Signal is fetched



6.4.2 Divider

The divider divides the output of the system clock oscillator (fx) to generate various clocks.

6.5 Operation of Clock Generator

The clock generator generates the following clocks and controls the operating modes of the CPU, such as the standby mode.

- System clock f_X
- CPU clock f_{CPU}
- Clock to peripheral hardware

The operation of the clock generator is determined by the processor clock control register (PCC), as follows.

★ (a) The slow mode (0.8 μs: at 10.0 MHz operation, 1.6 μs: at 5.0 MHz operation) of the system clock is selected when the $\overline{\text{RESET}}$ signal is generated (PCC = 02H). While a low level is being input to the $\overline{\text{RESET}}$ pin, oscillation of the system clock is stopped.

★ (b) Two types of minimum instruction execution time (0.2 μs and 0.8 μs: at 10.0 MHz operation, 0.4 μs and 1.6 μs: at 5.0 MHz operation) can be selected by setting the PCC register.

(c) Two standby modes, STOP and HALT, can be used.

(d) The clock to the peripheral hardware is supplied by dividing the system clock. The other peripheral hardware is stopped when the system clock is stopped (except the external clock input operation).

6.6 Changing Setting of CPU Clock

6.6.1 Time required for switching CPU clock

The CPU clock can be switched by using bit 1 (PCC1) of the processor clock control register (PCC).

Actually, the specified clock is not switched immediately after the setting of PCC has been changed; the old clock is used for the duration of several instructions after that (refer to **Table 6-2**).

Table 6-2. Maximum Time Required for Switching CPU Clock

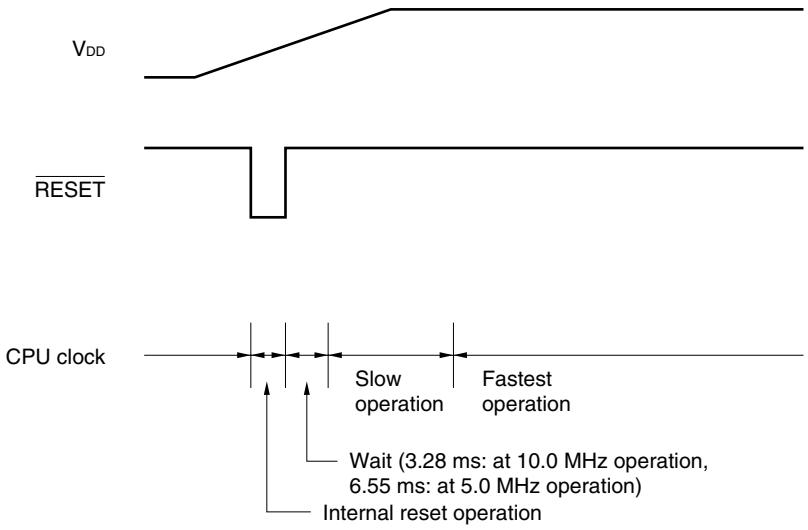
Set Value Before Switching	Set Value After Switching	
PCC1	PCC1	PCC1
	0	1
0		4 clocks
1	2 clocks	

Remark Two clocks are the minimum instruction execution time of the CPU clock before switching.

6.6.2 Switching CPU clock

The following figure illustrates how the CPU clock is switched.

Figure 6-5. Switching CPU Clock



<1> The CPU is reset when the $\overline{\text{RESET}}$ pin is made low on power application. The effect of resetting is released when the $\overline{\text{RESET}}$ pin is later made high, and the system clock starts oscillating. At this time, the time during which oscillation stabilizes (2^{15}/fx) is automatically secured.

After that, the CPU starts instruction execution at the low speed of the system clock (8.0 μs: at 10.0 MHz operation, 1.6 μs: at 5.0 MHz operation).

<2> After the time during which the V_{DD} voltage rises to the level at which the CPU can operate at the highest speed has elapsed, the processor clock control register (PCC) is rewritten so that the highest speed can be selected.

CHAPTER 7 CLOCK GENERATOR (μPD789124A, 789134A SUBSERIES)

7.1 Function of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware. The system clock oscillator is as follows.

- System clock (RC) oscillator
  This circuit oscillates a clock at a frequency of 2.0 to 4.0 MHz. Oscillation can be stopped by executing the STOP instruction.

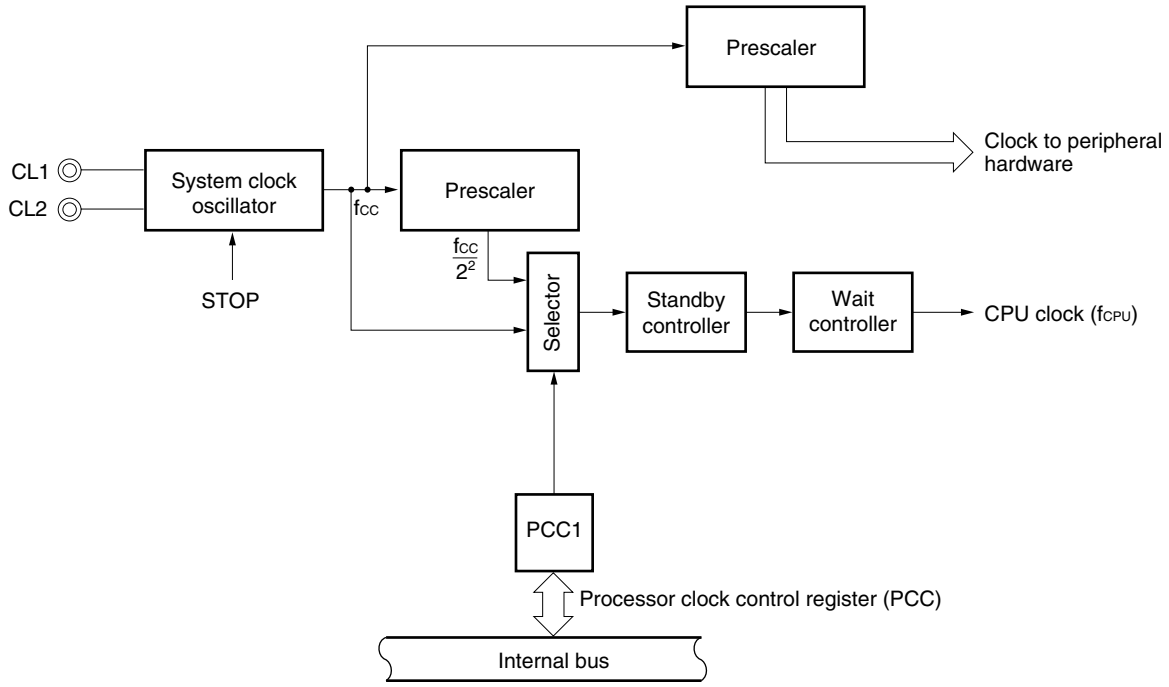
7.2 Configuration of Clock Generator

The clock generator consists of the following hardware.

Table 7-1. Configuration of Clock Generator

Item	Configuration
Control register	Processor clock control register (PCC)
Oscillator	RC oscillator

Figure 7-1. Block Diagram of Clock Generator



7.3 Register Controlling Clock Generator

The clock generator is controlled by the following register.

- Processor clock control register (PCC)

(1) Processor clock control register (PCC)

PCC sets the CPU clock selection and the division ratio.

PCC is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the PCC to 02H.

Figure 7-2. Format of Processor Clock Control Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PCC	0	0	0	0	0	0	PCC1	0	FFFBH	02H	R/W

★

PCC1	CPU clock (f_{CPU}) selection	Minimum instruction execution time: $2/f_{CPU}$
		@ f_{CC} = 4.0 MHz operation
0	f_{CC}	0.5 μs
1	$f_{CC}/2^2$	2.0 μs

Caution Bit 0 and bits 2 to 7 must be set to 0.

Remark f_{CC}: System clock oscillation frequency

7.4 System Clock Oscillator

7.4.1 System clock oscillator

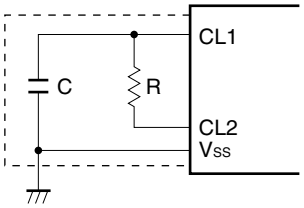
The system clock oscillator is oscillated by the resistor (R) and capacitor (C) (4.0 MHz TYP.) connected across the CL1 and CL2 pins.

An external clock can also be input to the system clock oscillator. In this case, input the clock signal to the CL1 pin, and leave the CL2 pin open.

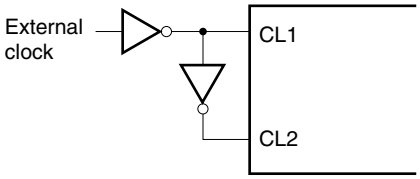
Figure 7-3 shows the external circuit of the system clock oscillator.

Figure 7-3. External Circuit of System Clock Oscillator

(a) RC oscillation



(b) External clock



Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

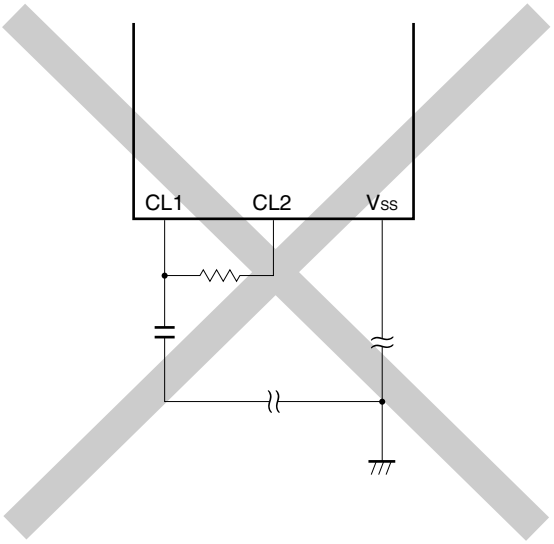
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

7.4.2 Examples of incorrect resonator connection

Figure 7-4 shows examples of incorrect resonator connection.

Figure 7-4. Examples of Incorrect Resonator Connection (1/2)

(a) Too long wiring



(b) Crossed signal line

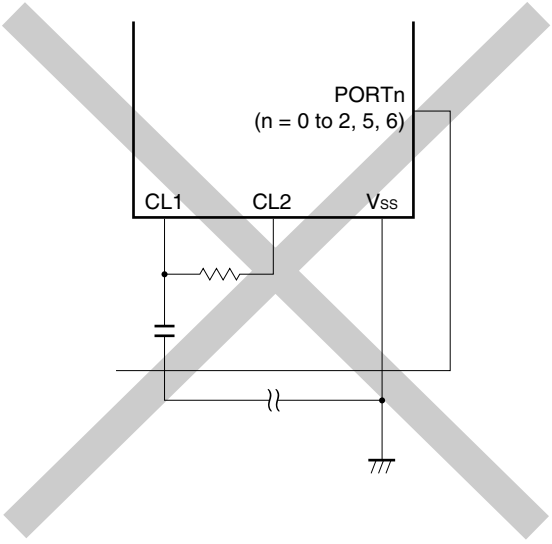
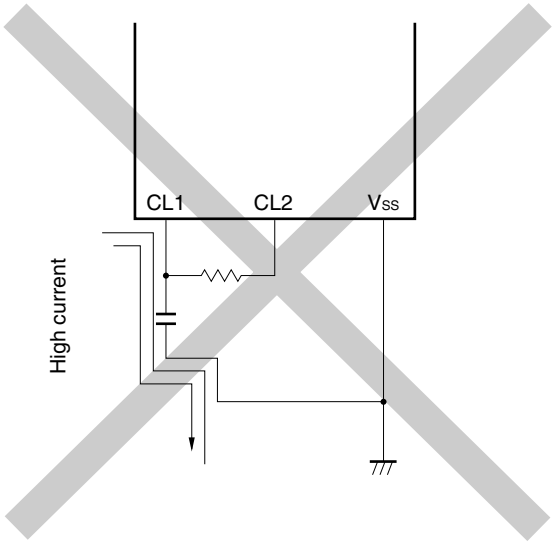
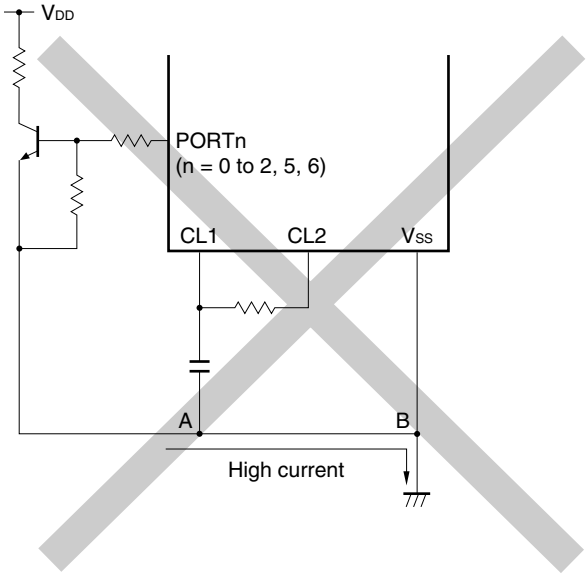


Figure 7-4. Examples of Incorrect Resonator Connection (2/2)

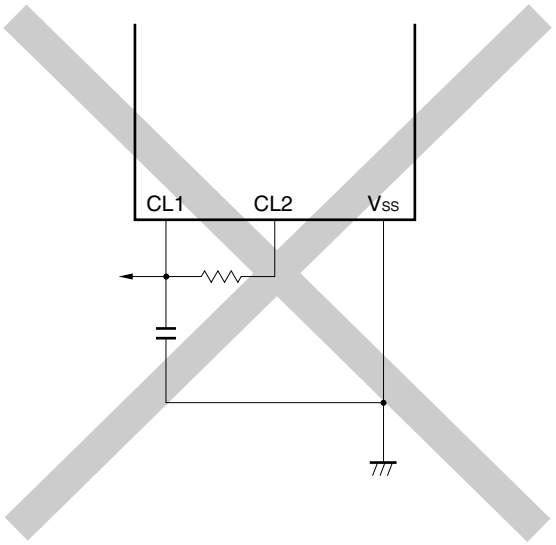
(c) Wiring near high fluctuating current



(d) Current flowing through ground line of oscillator (potential at points A and B fluctuates)



(e) Signal is fetched



7.4.3 Divider

The divider divides the output of the system clock oscillator (f_{CC}) to generate various clocks.

7.5 Operation of Clock Generator

The clock generator generates the following clocks and controls the operating modes of the CPU, such as the standby mode.

- System clock f_{CC}
- CPU clock f_{CPU}
- Clock to peripheral hardware

The operation of the clock generator is determined by the processor clock control register (PCC), as follows.

(a) The slow mode (2.0 μs: at 4.0 MHz operation) of the system clock is selected when the $\overline{\text{RESET}}$ signal is generated (PCC = 02H). While a low level is being input to the $\overline{\text{RESET}}$ pin, oscillation of the system clock is stopped.

★ (b) Two types of minimum instruction execution time (0.5 μs and 2.0 μs: at 4.0 MHz operation) can be selected by setting the PCC register.

(c) Two standby modes, STOP and HALT, can be used.

(d) The clock to the peripheral hardware is supplied by dividing the system clock. The other peripheral hardware is stopped when the system clock is stopped (except the external clock input operation).

7.6 Changing Setting of CPU Clock

7.6.1 Time required for switching CPU clock

The CPU clock can be switched by using bit 1 (PCC1) of the processor clock control register (PCC).

Actually, the specified clock is not switched immediately after the setting of PCC has been changed; the old clock is used for the duration of several instructions after that (refer to **Table 7-2**).

Table 7-2. Maximum Time Required for Switching CPU Clock

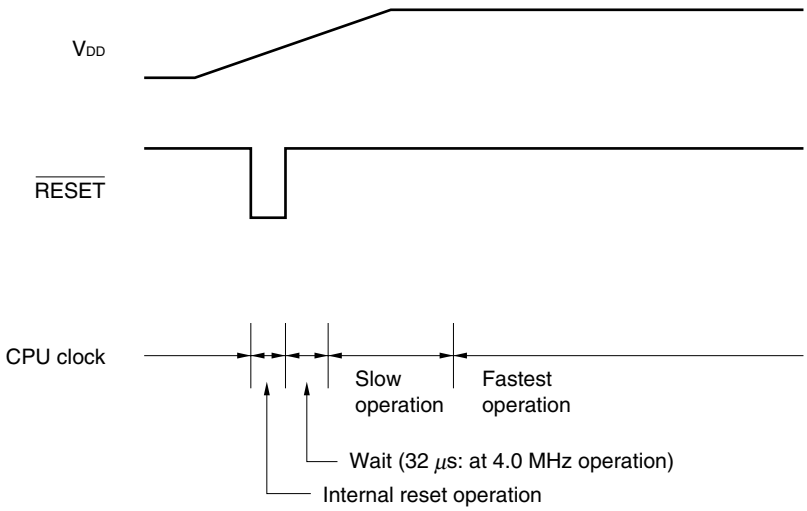
Set Value Before Switching	Set Value After Switching	
PCC1	PCC1	PCC1
	0	1
0		4 clocks
1	2 clocks	

Remark Two clocks are the minimum instruction execution time of the CPU clock before switching.

7.6.2 Switching CPU clock

The following figure illustrates how the CPU clock is switched.

Figure 7-5. Switching CPU Clock



<1> The CPU is reset when the $\overline{\text{RESET}}$ pin is made low on power application. The effect of resetting is released when the $\overline{\text{RESET}}$ pin is later made high, and the system clock starts oscillating. At this time, the time during which oscillation stabilizes ($2^7/f_{CC}$) is automatically secured.

After that, the CPU starts instruction execution at the low speed of the system clock (2.0 μs: at 4.0 MHz operation).

<2> After the time during which the V_{DD} voltage rises to the level at which the CPU can operate at the highest speed has elapsed, the processor clock control register (PCC) is rewritten so that the highest speed can be selected.

CHAPTER 8 16-BIT TIMER 20

The 16-bit timer counter references the free-running counter and provides functions such as timer interrupt and timer output. In addition, the count value can be captured by a capture trigger pin.

8.1 16-Bit Timer 20 Functions

16-bit timer 20 has the following functions.

- Timer interrupt
- Timer output
- Count value capture

(1) Timer interrupt

An interrupt is generated when the count value and compare value match.

(2) Timer output

Timer output control is possible when the count value and compare value match.

(3) Count value capture

The TM20 count value is latched in synchronization with the capture trigger and held.

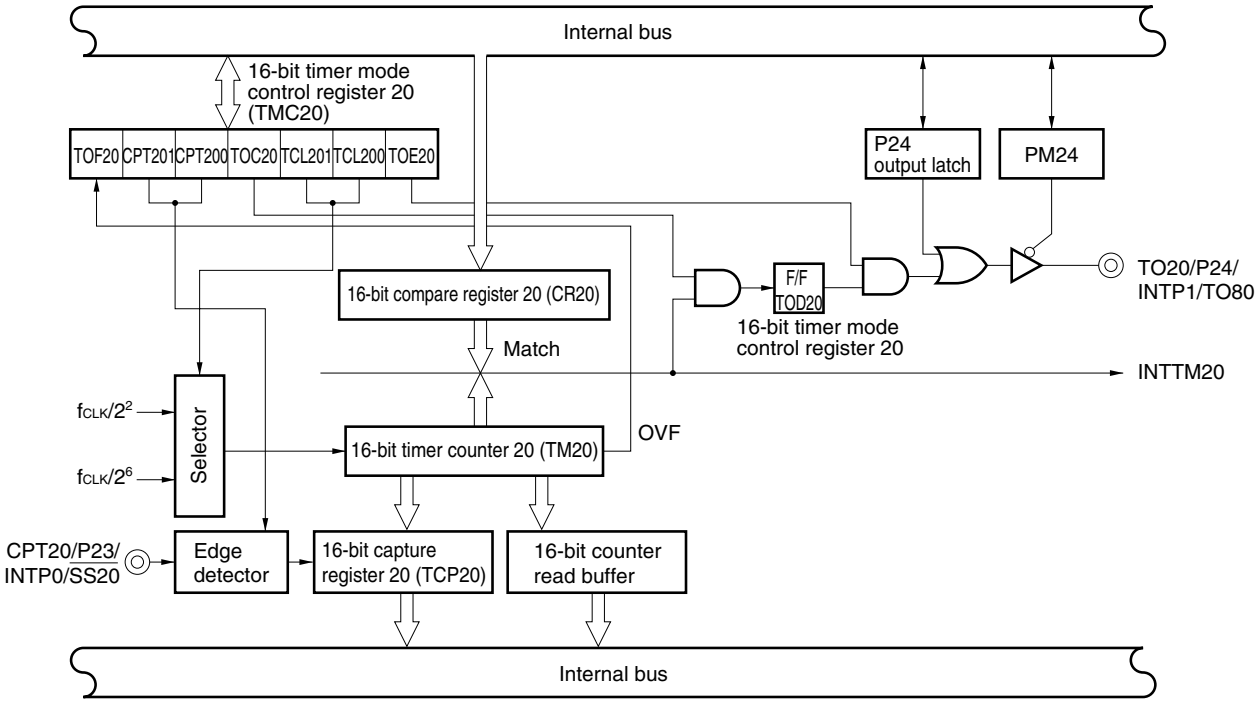
8.2 16-Bit Timer 20 Configuration

16-bit timer 20 consists of the following hardware.

Table 8-1. Configuration of 16-Bit Timer 20

Item	Configuration
Timer counter	16 bits × 1 (TM20)
Registers	Compare register: 16 bits × 1 (CR20) Capture register: 16 bits × 1 (TCP20)
Timer output	1 (TO20)
Control registers	16-bit timer mode control register 20 (TMC20) Port mode register 2 (PM2) Port 2 (P2)

Figure 8-1. Block Diagram of 16-Bit Timer 20



Remark f_{CLK}: f_X or f_{CC}

(1) 16-bit compare register 20 (CR20)

This register compares the value set to CR20 with the count value of 16-bit timer counter 20 (TM20), and when they match, generates an interrupt request (INTTM20).

CR20 is set with a 16-bit memory manipulation instruction. The values 0000H to FFFFH can be set.

$\overline{\text{RESET}}$ input sets this register to FFFFH.

Cautions 1. Although this register is manipulated with a 16-bit memory manipulation instruction, an 8-bit memory manipulation instruction can also be used. When manipulating with an 8-bit memory manipulation instruction, the accessing method should be direct addressing.

2. When rewriting CR20 during a count operation, set CR20 to the interrupt-disabled state using interrupt mask flag register 0 (MK10) beforehand. Also, set the timer output data to inversion disabled using 16-bit timer mode control register 20 (TMC20).

When CR20 is rewritten in the interrupt-enabled state, an interrupt request may occur at the moment of rewrite.

(2) 16-bit timer counter 20 (TM20)

This is a 16-bit register that counts count pulses.

TM20 is read with a 16-bit memory manipulation instruction.

This register is free running during count clock input.

$\overline{\text{RESET}}$ input clears this register to 0000H and after which it resumes free running.

Cautions 1. The count value after releasing stop becomes undefined because the count operation is executed during the oscillation stabilization time.

2. Although this register is manipulated with a 16-bit memory manipulation instruction, an 8-bit memory manipulation instruction can also be used. When manipulating with an 8-bit memory manipulation instruction, the accessing method should be direct addressing.

3. When manipulating with an 8-bit memory manipulation instruction, readout should be performed in the order of lower byte to higher byte and must be performed in pairs.

(3) 16-bit capture register 20 (TCP20)

This is a 16-bit register that captures the contents of 16-bit timer counter 20 (TM20).

TCP20 is set with a 16-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

Caution Although this register is manipulated with a 16-bit memory manipulation instruction, an 8-bit memory manipulation instruction can also be used. When manipulating with an 8-bit memory manipulation instruction, the accessing method should be direct addressing.

(4) 16-bit counter read buffer

This buffer latches the counter value and holds the count value of 16-bit timer counter 20 (TM20).

8.3 Registers Controlling 16-Bit Timer 20

The following three registers control 16-bit timer 20.

- 16-bit timer mode control register 20 (TMC20)
- Port mode register 2 (PM2)
- Port 2 (P2)

(1) 16-bit timer mode control register 20 (TMC20)

16-bit timer mode control register 20 (TMC20) controls the setting of the counter clock, capture edge, etc.

TMC20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC20 to 00H.

Figure 8-2. Format of 16-Bit Timer Mode Control Register 20

Symbol	7	<6>	5	4	3	2	1	<0>	Address	After reset	R/W
TMC20	TOD20	TOF20	CPT201	CPT200	TOC20	TCL201	TCL200	TOE20	FF48H	00H	R/W Note 1

TOD20	Timer output data
0	Timer output of 0
1	Timer output of 1

TOF20	Overflow flag set
0	Clear by reset and software
1	Set by overflow of 16-bit timer

CPT201	CPT200	Capture edge selection
0	0	Capture operation disabled
0	1	Rising edge of CPT20
1	0	Falling edge of CPT20
1	1	Both edges of CPT20

TOC20	Timer output data inversion control
0	Inversion disabled
1	Inversion enabled

★

TCL201	TCL200	16-bit timer counter 20 count clock selection			
			@ f_X = 10.0 MHz Note 2 operation	@ f_X = 5.0 MHz operation	@ f_{CC} = 4.0 MHz operation
0	0	$f_X/2^2$ or $f_{CC}/2^2$	2.5 MHz	1.25 MHz	1.0 MHz
0	1	$f_X/2^6$ or $f_{CC}/2^6$	156.2 kHz	78.1 kHz	62.5 kHz
Other than above		Setting prohibited			

TOE20	16-bit timer 20 output control
0	Output disabled (port mode)
1	Output enabled

Notes 1. Bit 7 is read-only.

2. Expanded-specification products only.

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)

f_{CC}: System clock oscillation frequency (RC oscillation)

(2) Port mode register 2 (PM2)

This register sets the input/output of port 2 in 1-bit units.

To use the P24/TO20/INTP1/TO80 pin for timer output, set the output latch of PM24 and P24 to 0.

PM2 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM2 to FFH.

Figure 8-3. Format of Port Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PM24	P24 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

8.4 16-Bit Timer 20 Operation

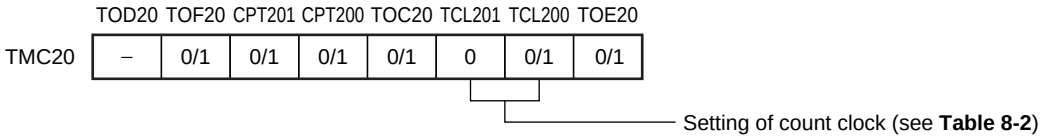
8.4.1 Operation as timer interrupt

★ An interrupt is generated repeatedly each time the free-running counter value reaches the value set to CR20. After interrupt occurs, the counter is not cleared and continues counting. Therefore, the interval time is equivalent to one count clock cycle set by TCL201 and TCL200.

To operate the 16-bit timer 20 as a timer interrupt, the following settings are required.

- Set count values to CR20.
- Set 16-bit timer mode control register 20 (TMC20) as shown in Figure 8-4.

Figure 8-4. Settings of 16-Bit Timer Mode Control Register 20 at Timer Interrupt Operation



Caution If both the CPT201 and CPT200 flags are set to 0, the capture edge becomes setting prohibited.

When the count value of 16-bit timer counter 20 (TM20) coincides with the value set to CR20, counting of TM20 continues and an interrupt request signal (INTTM20) is generated.

Table 8-2 shows the interval time, and Figure 8-5 shows the timing of the timer interrupt operation.

Caution When rewriting CR20 during count operation, be sure to follow the procedure below.
<1> Set CR20 to interrupt disable (by setting bit 7 of interrupt mask flag register 0 (MK0) to 1).
<2> Set inversion control of timer output data to disable (TOC20 = 0)
When CR20 is rewritten in the interrupt-enabled state, an interrupt request may occur at the moment of rewrite.

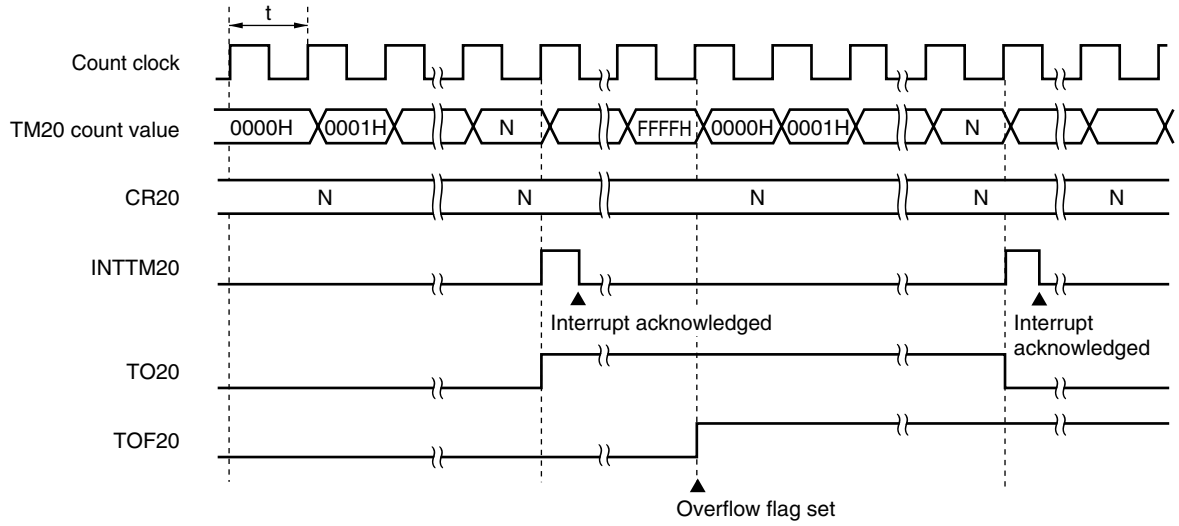
★ **Table 8-2. Interval Time of 16-Bit Timer 20**

TCL201	TCL200	Count Clock				Interval Time			
			@ f_X = 10.0 MHz[Note] Operation	@ f_X = 5.0 MHz Operation	@ f_{CC} = 4.0 MHz Operation		@ f_X = 10.0 MHz[Note] Operation	@ f_X = 5.0 MHz Operation	@ f_{CC} = 4.0 MHz Operation
0	0	$2^2/f_X$ or $2^2/f_{CC}$	0.4 μs	0.8 μs	1.0 μs	$2^{18}/f_X$ or $2^{18}/f_{CC}$	26.2 ms	52.4 ms	65.5 ms
0	1	$2^6/f_X$ or $2^6/f_{CC}$	6.4 μs	12.8 μs	16 μs	$2^{22}/f_X$ or $2^{22}/f_{CC}$	419.4 ms	838.9 ms	1048 ms
Other than above		Setting prohibited							

Note Expanded-specification products only.

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

Figure 8-5. Timing of Timer Interrupt Operation



Remark N = 0000H to FFFFH

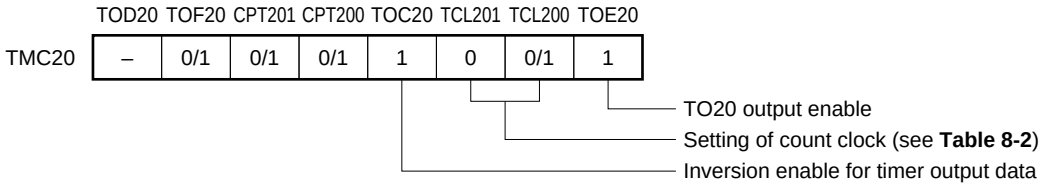
8.4.2 Operation as timer output

★ The timer output is inverted repeatedly each time the free-running counter value reaches the value set to CR20. After the timer output is inverted, the counter is not cleared and continues counting. Therefore, the interval time is equivalent to one count clock cycle set by TCL201 and TCL200.

To operate the 16-bit timer 20 as a timer output, the following settings are required.

- Set P24 to output mode (PM24 = 0).
- Set the P24 output latch to 0.
- Set the count value to CR20.
- Set 16-bit timer mode control register 20 (TMC20) as shown in Figure 8-6.

Figure 8-6. Settings of 16-Bit Timer Mode Control Register 20 for Timer Output Operation

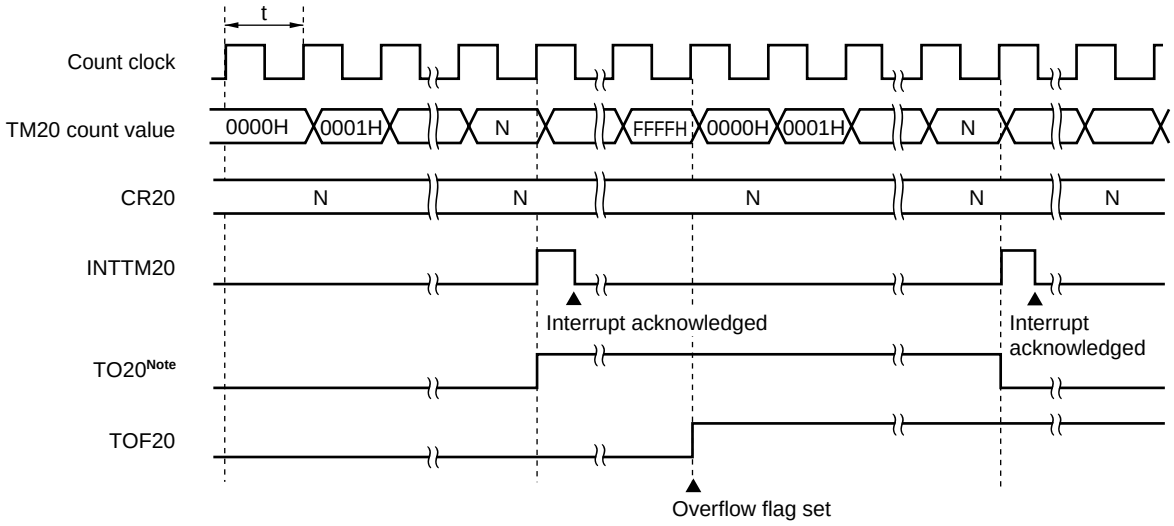


Caution If both the CPT201 flag and CPT200 flag are set to 0, the capture edge becomes operation prohibited.

When the count value of 16-bit timer counter 20 (TM20) matches the value set in CR20, the output status of the TO20/P24/INTP1/TO80 pin is inverted. This enables timer output. At that time, TM20 continues counting and an interrupt request signal (INTTM20) is generated.

Figure 8-7 shows the timing of timer output (refer to **Table 8-2** for the interval time of 16-bit timer 20).

Figure 8-7. Timer Output Timing



Note The TO20 initial value becomes low level while output is enabled (TOE20 = 1).

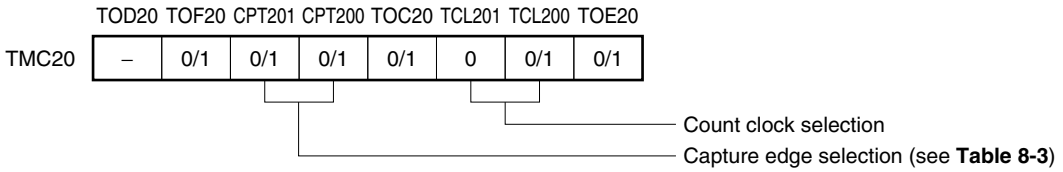
Remark N = 0000H to FFFFH

8.4.3 Capture operation

The capture operation functions to capture and latch the count value of 16-bit timer counter 20 (TM20) in synchronization with a capture trigger.

Set as shown in Figure 8-8 to allow 16-bit timer 20 to start the capture operation.

Figure 8-8. Settings of 16-Bit Timer Mode Control Register 20 for Capture Operation



16-bit capture register 20 (TCP20) starts the capture operation after the CPT20 capture trigger edge has been detected, and latches and holds the count value of 16-bit timer counter 20. TCP20 fetches the count value within 2 clocks and holds the count value until the next capture edge detection.

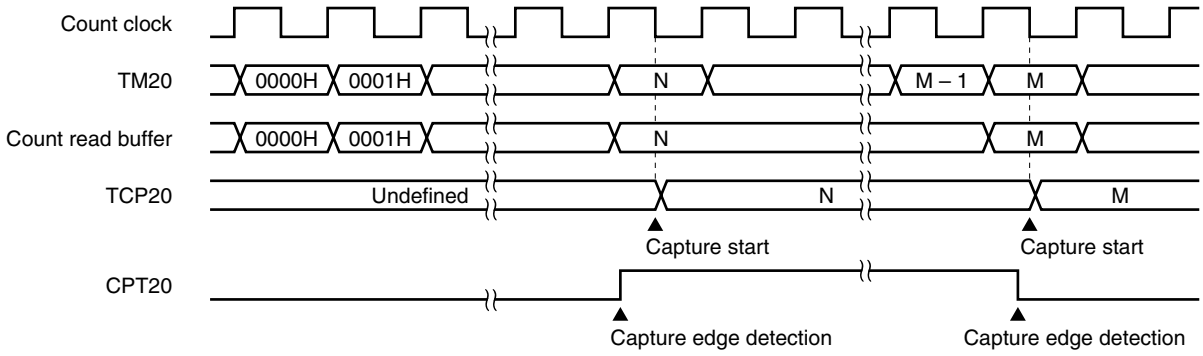
Table 8-3 and Figure 8-9 show the setting contents of the capture edge and the capture operation timing, respectively.

Table 8-3. Settings of Capture Edge

CPT201	CPT200	Capture Edge Selection
0	0	Capture operation prohibited
0	1	CPT20 pin rising edge
1	0	CPT20 pin falling edge
1	1	CPT20 pin both edges

Caution Because TCP20 is rewritten when a capture trigger edge is detected during TCP20 read, disable capture trigger detection during TCP20 read.

Figure 8-9. Capture Operation Timing (Both Edges of CPT20 Pin Are Specified)



Remark N, M = 0000H to FFFFH

8.4.4 16-bit timer counter 20 readout

The count value of 16-bit timer counter 20 (TM20) is read out by a 16-bit manipulation instruction.

TM20 readout is performed via a counter read buffer. The counter read buffer latches the TM20 count value. The buffer operation is then held pending at the CPU clock falling edge after the read signal of the TM20 lower byte rises and the count value is held. The counter read buffer value in the hold state can be read out as the count value.

Cancellation of the pending state is performed at the CPU clock falling edge after the read signal of the TM20 higher byte falls.

$\overline{\text{RESET}}$ input clears TM20 to 0000H and restarts free running.

Figure 8-10 shows the timing of 16-bit timer counter 20 readout.

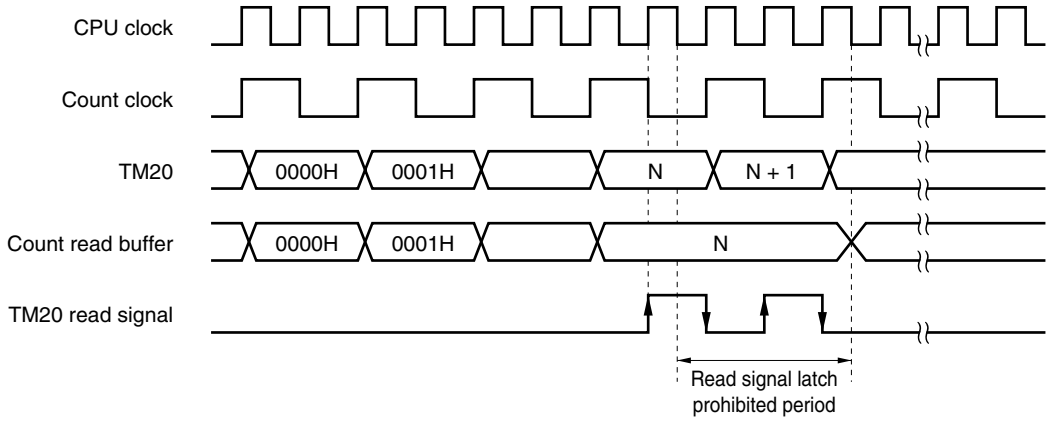
Cautions 1. The count value after releasing stop becomes undefined because the count operation is executed during oscillation stabilization time.

2. Although TM20 is a dedicated 16-bit transfer instruction register, an 8-bit transfer instruction can also be used.

Execute an 8-bit transfer instruction by direct addressing.

3. When using an 8-bit transfer instruction, execute in the order of lower byte to higher byte in pairs. If the only lower byte is read, the pending state of the counter read buffer is not canceled, and if the only higher byte is read, an undefined count value is read.

Figure 8-10. 16-Bit Timer Counter 20 Readout Timing



Remark N = 0000H to FFFFH

★ 8.5 Notes on Using 16-Bit Timer 20

8.5.1 Restrictions on rewriting 16-bit compare register 20

(1) When rewriting the compare register (CR20), be sure to disable interrupts (TMMK20 = 1), and disable inversion control of timer output (TOC20 = 0) first.
If CR20 is rewritten with interrupts enabled, an interrupt request may be generated at the point of rewrite.

(2) The interval time may be double the intended time depending on the timing at which the compare register (CR20) is rewritten. Likewise, the timer output waveform may be shorter or double the intended output.
To avoid this, rewrite using one of the following procedures.

<Prevention method A> Rewriting by 8-bit access

<1> Disable interrupts (TMMK20 = 1), and disable inversion control of timer output (TOC20 = 0).
<2> Rewrite the higher byte of CR20 (16 bits) first.
<3> Next, rewrite the lower byte of CR20 (16 bits).
<4> Clear the interrupt request flag (TMIF20).
<5> After more than half the cycle of the count clock has passed from the start of the interrupt, enable timer interrupts and timer output inversion.

<Program example A> (When count clock = 64/f_X, CPU clock = f_X)

```
TM20_VCT: SET1   TMMK20      ;Timer interrupt disable (6 clocks)
          CLR1   TMC20.3     ;Timer output inversion disable (6 clocks)
          MOV    A,#xxH      ;Higher byte rewrite value setting (6 clocks)
          MOV    !0FF17H,A   ;CR20 higher byte rewriting (8 clocks)
          MOV    A,#yyH      ;Lower byte rewrite value setting (6 clocks)
          MOV    !0FF16H,A   ;CR20 lower byte rewriting (8 clocks)
          CLR1   TMIF20      ;Interrupt request flag clearing (6 clocks)
          CLR1   TMMK20      ;Timer interrupt enable (6 clocks)
          SET1   TMC20.3     ;Timer output inversion enable
```

} More than 32 clocks in total[Note]

Note This is because the INTTM20 signal is set to the high level for a period of half the cycle of the count clock after an interrupt is generated, so the output will be inverted if TOC20 is set to 1 during this period.

<Prevention method B> Rewriting by 16-bit access

<1> Disable interrupts (TMMK20 = 1), and disable inversion control of timer output (TOC20 = 0).

<2> Rewrite CR20 (16 bits).

<3> Wait for more than one cycle of the count clock.

<4> Clear the interrupt request flag (TMIF20).

<5> Enable timer interrupts and timer output inversion

<Program example B> (When count clock = 64/f_X, CPU clock = f_X)

```
TM20_VCT:  SET1   TMMK20      ;Timer interrupt disable
           CLR1   TMC20.3     ;Timer output inversion disable
           MOVW   AX,#xxyyH   ;CR20 rewrite value setting
           MOVW   CR20,AX     ;CR20 rewriting
           NOP
           NOP
             :                ;32 NOP (Wait for 64/fx)Note
           NOP
           NOP
           CLR1   TMIF20      ;Interrupt request flag clearing
           CLR1   TMMK20      ;Timer interrupt enable
           SET1   TMC20.3     ;Timer output inversion enable
```

Note Wait for more than one cycle of the count clock after the instruction rewriting CR20 (MOVW CR20, AX) before clearing the interrupt request flag (TMIF20).

CHAPTER 9 8-BIT TIMER/EVENT COUNTER 80

The 8-bit timer/event counter can be used as an interval timer, external event counter, and for square-wave output and PWM output of arbitrary frequency.

9.1 Functions of 8-Bit Timer/Event Counter 80

8-bit timer/event counter 80 has the following functions.

- Interval timer
- External event counter
- Square-wave output
- PWM output

(1) 8-bit interval timer

When the 8-bit timer/event counter is used as an interval timer, it generates an interrupt at an arbitrary time interval set in advance.

Table 9-1. Interval Time of 8-Bit Timer/Event Counter 80

	Minimum Interval Time	Maximum Interval Time	Resolution
★ At f_X = 10.0 MHz[Note]	$1/f_X$ (100 ns)	$2^8/f_X$ (25.6 μs)	$1/f_X$ (100 ns)
	$2^3/f_X$ (0.8 μs)	$2^{11}/f_X$ (204.8 μs)	$2^3/f_X$ (0.8 μs)
At f_X = 5.0 MHz	$1/f_X$ (200 ns)	$2^8/f_X$ (51.2 μs)	$1/f_X$ (200 ns)
	$2^3/f_X$ (1.6 μs)	$2^{11}/f_X$ (409.6 μs)	$2^3/f_X$ (1.6 μs)
At f_{CC} = 4.0 MHz	$1/f_{CC}$ (250 ns)	$2^8/f_{CC}$ (64 μs)	$1/f_{CC}$ (250 ns)
	$2^3/f_{CC}$ (2.0 μs)	$2^{11}/f_{CC}$ (512 μs)	$2^3/f_{CC}$ (2.0 μs)

Note Expanded-specification products only

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

(2) External event counter

The number of pulses of an externally input signal can be measured.

(3) Square-wave output

A square wave of arbitrary frequency can be output.

Table 9-2. Square-Wave Output Range of 8-Bit Timer/Event Counter 80

	Minimum Pulse Width	Maximum Pulse Width	Resolution
★ At f_X = 10.0 MHz[Note]	1/f_X (100 ns)	$2^8/f_X$ (25.6 μs)	1/f_X (100 ns)
	$2^3/f_X$ (0.8 μs)	$2^{11}/f_X$ (204.8 μs)	$2^3/f_X$ (0.8 μs)
At f_X = 5.0 MHz	1/f_X (200 ns)	$2^8/f_X$ (51.2 μs)	1/f_X (200 ns)
	$2^3/f_X$ (1.6 μs)	$2^{11}/f_X$ (409.6 μs)	$2^3/f_X$ (1.6 μs)
At f_{CC} = 4.0 MHz	1/f_{CC} (250 ns)	$2^8/f_{CC}$ (64 μs)	1/f_{CC} (250 ns)
	$2^3/f_{CC}$ (2.0 μs)	$2^{11}/f_{CC}$ (512 μs)	$2^3/f_{CC}$ (2.0 μs)

Note Expanded-specification products only

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

(4) PWM output

8-bit resolution PWM output can be produced.

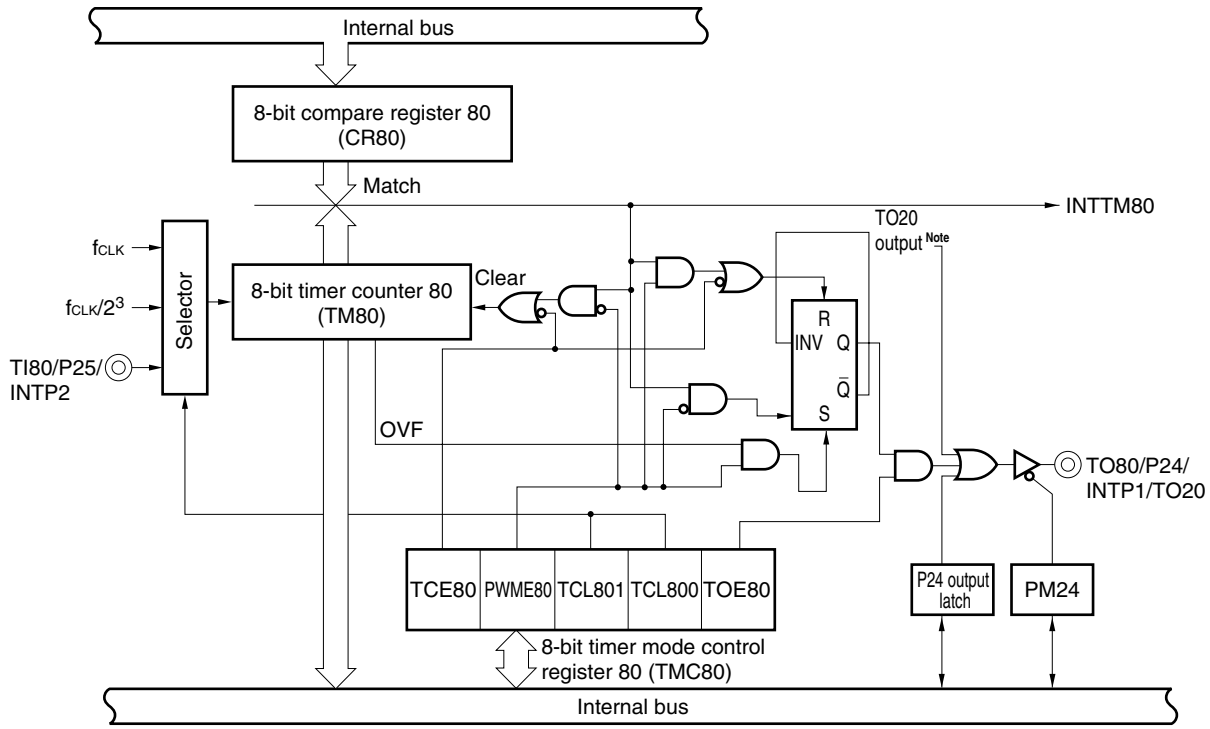
9.2 8-Bit Timer/Event Counter 80 Configuration

8-bit timer/event counter 80 consists of the following hardware.

Table 9-3. 8-Bit Timer/Event Counter 80 Configuration

Item	Configuration
Timer counter	8 bits × 1 (TM80)
Register	Compare register: 8 bits × 1 (CR80)
Timer output	1 (TO80)
Control registers	8-bit timer mode control register 80 (TMC80) Port mode register 2 (PM2) Port 2 (P2)

Figure 9-1. Block Diagram of 8-Bit Timer/Event Counter 80



Note Refer to block diagram of 16-bit timer 20

Remark f_{CLK}: fx or f_{CC}

(1) 8-bit compare register 80 (CR80)

This is an 8-bit register that compares the value set to CR80 with the 8-bit timer counter 80 (TM80) count value, and if they match, generates an interrupt request (INTTM80).

CR80 is set with an 8-bit memory manipulation instruction. The values 00H to FFH can be set.

$\overline{\text{RESET}}$ input makes CR80 undefined.

Cautions 1. When rewriting CR80 in timer counter operation mode (i.e., PWME80 (bit 6 of 8-bit timer mode control register 80 (TMC80)) is set to 0), be sure to stop the timer operation before hand. If CR80 is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. Do not set CR80 to 00H in the PWM output mode (when PWME80 = 1); otherwise, PWM may not be output normally.

(2) 8-bit timer counter 80 (TM80)

This is an 8-bit register used to count count pulses.

TM80 is read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TM80 to 00H.

9.3 Registers Controlling 8-Bit Timer/Event Counter 80

The following three registers are used to control 8-bit timer/event counter 80.

- 8-bit timer mode control register 80 (TMC80)
- Port mode register 2 (PM2)
- Port 2 (P2)

(1) 8-bit timer mode control register 80 (TMC80)

This register enables/stops operation of 8-bit timer counter 80 (TM80), sets the counter clock of TM80, and controls the operation of the output controller of 8-bit timer/event counter 80.

TMC80 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TMC80 to 00H.

Figure 9-2. Format of 8-Bit Timer Mode Control Register 80

Symbol	<7>	<6>	5	4	3	2	1	<0>	Address	After reset	R/W
TMC80	TCE80	PWME80	0	0	0	TCL801	TCL800	TOE80	FF53H	00H	R/W

TCE80	8-bit timer counter 80 operation control
0	Operation stop (TM80 cleared to 0)
1	Operation enable

PWME80	Operation mode selection
0	Timer counter operating mode
1	PWM output operating mode

★

TCL801	TCL800	8-bit timer counter 80 count clock selection			
			@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation	@ f_{CC} = 4.0 MHz operation
0	0	f_X or f_{CC}	10.0 MHz	5.0 MHz	4.0 MHz
0	1	$f_X/2^3$ or $f_{CC}/2^3$	1.25 MHz	625 kHz	500 kHz
1	0	Rising edge of TI80			
1	1	Falling edge of TI80			

TOE80	8-bit timer/event counter 80 output control
0	Output disable (port mode)
1	Output enable

Note Expanded-specification products only

Caution Be sure to set TMC80 after stopping timer operation.

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

(2) Port mode register 2 (PM2)

This register sets port 2 to input/output in 1-bit units.

When using the P24/TO80/INTP1/TO20 pin for timer output, set the output latch of PM24 and P24 to 0. When using it for timer input, set PM24 to 1.

PM2 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM2 to FFH.

Figure 9-3. Format of Port Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PM2n	P2n pin I/O mode selection (n = 0 to 5)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

9.4 Operation of 8-Bit Timer/Event Counter 80

9.4.1 Operation as interval timer

The interval timer repeatedly generates an interrupt at time intervals specified by the count value set to 8-bit compare register 80 (CR80) in advance.

To operate the 8-bit timer/event counter as an interval timer, the following settings are required.

<1> Set 8-bit timer counter 80 (TM80) to operation disabled (by setting TCE80 (bit 7 of 8-bit timer mode control register 80 (TMC80)) to 0).
<2> Set the count clock of 8-bit timer/event counter 80 (refer to **Figure 9-2**)
<3> Set the count value to CR80
<4> Set TM80 to operation enable (TCE80 = 1)

When the count value of 8-bit timer counter 80 (TM80) matches the value set to CR80, the value of TM80 is cleared to 0 and TM80 continues counting. At the same time, an interrupt request signal (INTTM80) is generated.

Tables 9-4 and 9-5 show the interval time, and Figure 9-4 shows the timing of interval timer operation.

Cautions 1. Before rewriting CR80, stop the timer operation once. If CR80 is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If the count clock setting and TM80 operation-enabled are set in TMC80 simultaneously using an 8-bit memory manipulation instruction, an error of more than one clock in one cycle may occur after the timer starts.

Therefore, always follow the above procedure when operating the 8-bit timer/event counter as an interval timer.

★ **Table 9-4. Interval Time of 8-Bit Timer/Event Counter 80 (at f_X = 5.0 MHz, 10.0 MHz Operation)**

TCL801	TCL800	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	$1/f_X$ (100 ns) [200 ns]	$2^8/f_X$ (25.6 μs) [51.2 μs]	$1/f_X$ (100 ns) [200 ns]
0	1	$2^3/f_X$ (0.8 μs) [1.6 μs]	$2^{11}/f_X$ (204.8 μs) [409.6 μs]	$2^3/f_X$ (0.8 μs) [1.6 μs]
1	0	TI80 input cycle	$2^8 \times$ TI80 input cycle	TI80 input edge cycle
1	1	TI80 input cycle	$2^8 \times$ TI80 input cycle	TI80 input edge cycle

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. The values in parentheses ( ) are for operation at f_X = 10.0 MHz (expanded-specification products only).

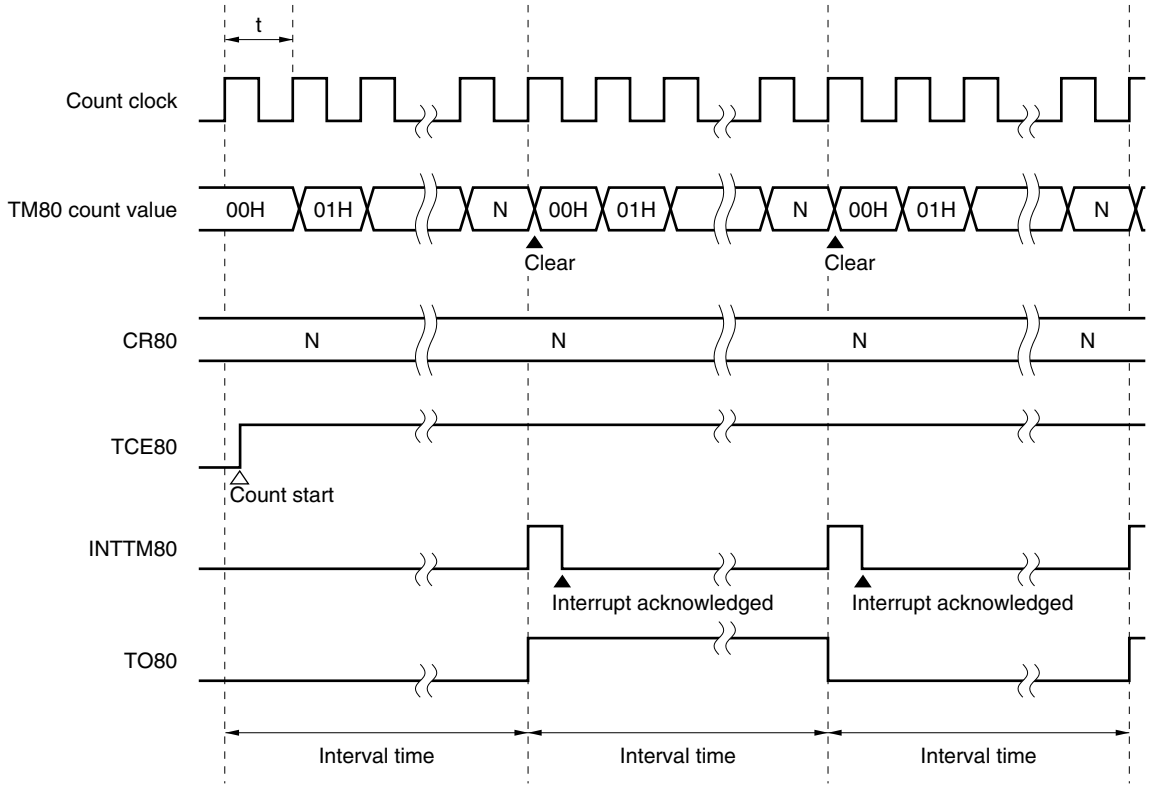
3. The values in square brackets [ ] are for operation at f_X = 5.0 MHz.

Table 9-5. Interval Time of 8-Bit Timer/Event Counter 80 (at f_{CC} = 4.0 MHz Operation)

TCL801	TCL800	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	$1/f_{CC}$ (250 ns)	$2^8/f_{CC}$ (64 μs)	$1/f_{CC}$ (250 ns)
0	1	$2^3/f_{CC}$ (2.0 μs)	$2^{11}/f_{CC}$ (512 μs)	$2^3/f_{CC}$ (2.0 μs)
1	0	TI80 input cycle	$2^8 \times$ TI80 input cycle	TI80 input edge cycle
1	1	TI80 input cycle	$2^8 \times$ TI80 input cycle	TI80 input edge cycle

Remark f_{CC}: System clock oscillation frequency (RC oscillation)

Figure 9-4. Interval Timer Operation Timing



Remark Interval time = (N + 1) × t : N = 00H to FFH

9.4.2 Operation as external event counter

The external event counter counts the number of external clock pulses input to the TI80/P25/INTP2 pin by using 8-bit timer counter 80 (TM80).

To operate 8-bit timer/event counter 80 as an external event counter, the following settings are required.

<1> Set P25 to input mode (PM25 = 1).
<2> Set 8-bit timer counter 80 (TM80) to operation disabled (by setting TCE80 (bit 7 of 8-bit timer mode control register 80 (TMC80)) to 0).
<3> Specify the rising/falling edges of TI80 (refer to **Figure 9-2**), and set TO80 to output disabled (i.e., set TOE80 (bit 0 of TMC80) to 0) and PWM output to disabled (i.e., set PWME80 (bit 6 of TMC80) to 0).
<4> Set the count value to CR80.
<5> Set TM80 to operation enabled (TCE80 = 1).

Each time the valid edge specified by bit 1 (TCL800) of TMC80 is input, the value of 8-bit timer counter 80 (TM80) is incremented.

When the count value of TM80 matches the value set to CR80, the value of TM80 is cleared to 0 and TM80 continues counting. At the same time, an interrupt request signal (INTTM80) is generated.

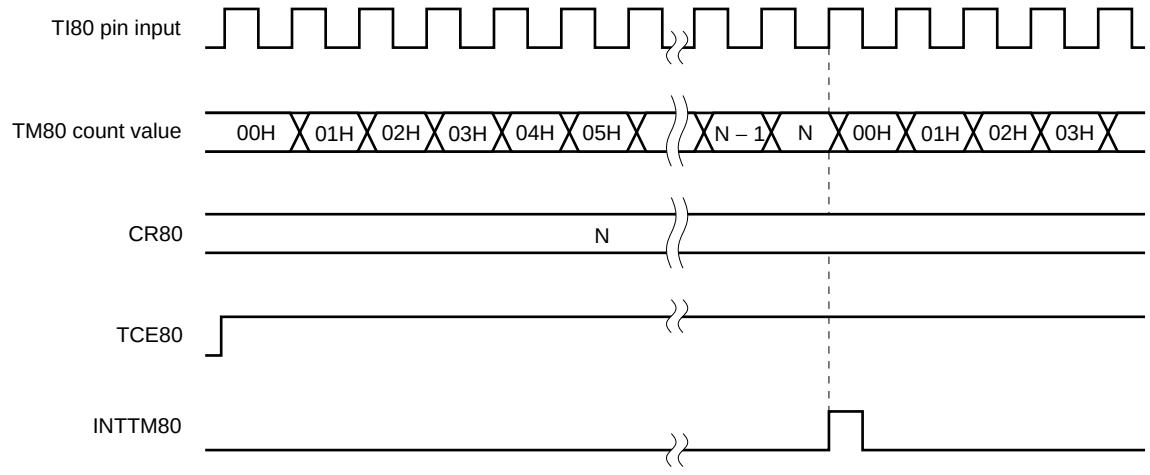
Figure 9-5 shows the timing of the external event counter operation (with the rising edge specified).

Cautions 1. Before rewriting CR80, stop the timer operation once. If CR80 is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If the count clock setting and TM80 operation-enabled are set in TMC80 simultaneously using an 8-bit memory manipulation instruction, an error of more than one clock in one cycle may occur after the timer starts.

Therefore, always follow the above procedure when operating the 8-bit timer/event counter as an external event counter.

Figure 9-5. External Event Counter Operation Timing (with Rising Edge Specified)



Remark N = 00H to FFH

9.4.3 Operation as square-wave output

The 8-bit timer/event counter can output square waves of a given frequency at intervals specified by the count value set to 8-bit compare register 80 (CR80) in advance.

To operate 8-bit timer/event counter 80 as square-wave output, the following settings are required.

<1> Set P24 to output mode (PM24 = 0) and the P24 output latch to 0.
<2> Set 8-bit timer counter 80 (TM80) to operation disabled (TCE80 = 0).
<3> Set the count clock of 8-bit timer/event counter 80 (refer to **Figure 9-2**), TO80 to output enabled (TOE80 = 1), and PWM output to disabled (PWME80 = 0).
<4> Set the count value to CR80.
<5> Set TM80 to operation enabled (TCE80 = 1).

When the count value of 8-bit timer counter 80 (TM80) matches the value set in CR80, the TO80/P24/INTP1/TO20 pin output will be inverted. Through application of this mechanism, square waves of any frequency can be output. As soon as a match occurs, the TM80 value is cleared to 0 and TM80 continues counting. At the same time, an interrupt request signal (INTTM80) is generated.

Square-wave output is cleared (0) when bit 7 (TCE80) of TMC80 is set to 0.

Tables 9-6 and 9-7 show the square-wave output range, and Figure 9-6 shows the timing of square-wave output.

Cautions 1. Before rewriting CR80, stop the timer operation once. If CR80 is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

2. If the count clock setting and TM80 operation-enabled are set in TMC80 simultaneously using an 8-bit memory manipulation instruction, an error of more than one clock in one cycle may occur after the timer starts.

Therefore, always follow the above procedure when operating the 8-bit timer/event counter as square-wave output.

★ **Table 9-6. Square-Wave Output Range of 8-Bit Timer/Event Counter 80 (at f_X = 5.0 MHz, 10.0 MHz Operation)**

TCL801	TCL800	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	$1/f_X$ (100 ns) [200 ns]	$2^8/f_X$ (25.6 μs) [51.2 μs]	$1/f_X$ (100 ns) [200 ns]
0	1	$2^3/f_X$ (0.8 μs) [1.6 μs]	$2^{11}/f_X$ (204.8 μs) [409.6 μs]	$2^3/f_X$ (0.8 μs) [1.6 μs]

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. The values in parentheses ( ) are for operation at f_X = 10.0 MHz (expanded-specification products only).

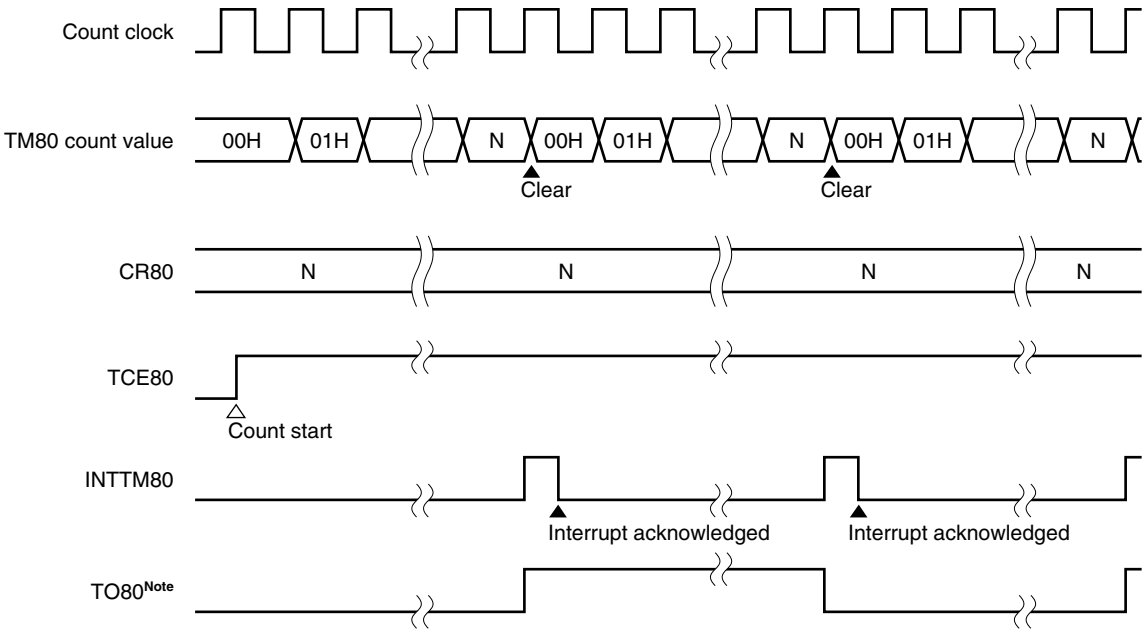
3. The values in square brackets [ ] are for operation at f_X = 5.0 MHz.

Table 9-7. Square-Wave Output Range of 8-Bit Timer/Event Counter 80 (at f_{CC} = 4.0 MHz Operation)

TCL801	TCL800	Minimum Interval Time	Maximum Interval Time	Resolution
0	0	$1/f_{CC}$ (250 ns)	$2^8/f_{CC}$ (64 μs)	$1/f_{CC}$ (250 ns)
0	1	$2^3/f_{CC}$ (2.0 μs)	$2^{11}/f_{CC}$ (512 μs)	$2^3/f_{CC}$ (2.0 μs)

Remark f_{CC}: System clock oscillation frequency (RC oscillation)

Figure 9-6. Square-Wave Output Timing



Note The TO80 initial value becomes low level while output is enabled (TOE80 = 1).

9.4.4 Operation as PWM output

PWM output enables interrupt generation repeatedly at intervals specified by the count value set to 8-bit compare register 80 (CR80) in advance.

To use 8-bit timer/counter 80 for PWM output, the following settings are required.

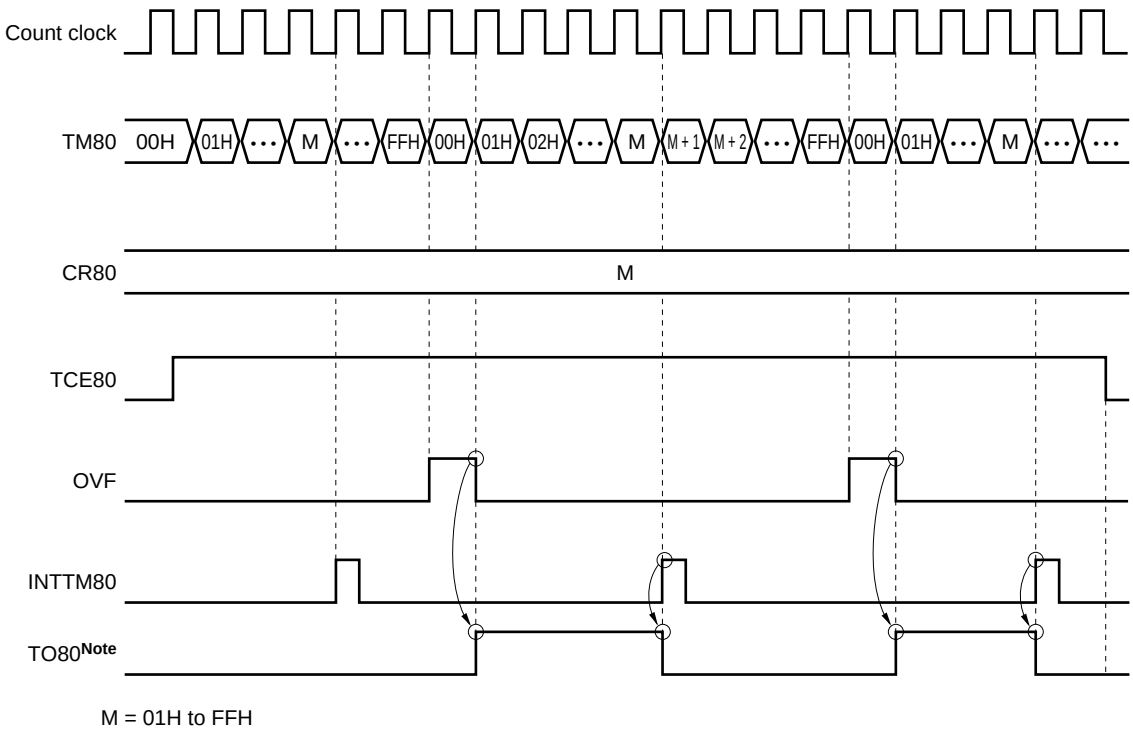
<1> Set P24 to output mode (PM24 = 0) and the P24 output latch to 0.
<2> Set 8-bit timer counter 80 (TM80) to operation disabled (TCE80 = 0).
<3> Set the count clock of 8-bit timer/event counter 80 (refer to **Figure 9-2**), TO80 to output enabled (TOE80 = 1), and PWM output to enabled (PWME80 = 1).
<4> Set the count value to CR80.
<5> Set TM80 to operation enabled (TCE80 = 1).

When the count value of 8-bit timer counter 80 (TM80) matches the value set to CR80, TM80 continues counting, and an interrupt request signal (INTTM80) is generated.

Cautions 1. When CR80 is rewritten during timer operation, a high level may be output for the next cycle (refer to 9.5 (2) Setting of 8-bit compare register 80).

2. If the count clock setting and TM80 operation-enabled are set in TMC80 simultaneously using an 8-bit memory manipulation instruction, an error of more than one clock in one cycle may occur after the timer starts. Therefore, always follow the above procedure when operating 8-bit compare register 80 as a PWM output.

Figure 9-7. PWM Output Timing



M = 01H to FFH

Note The TO80 initial value becomes low level while output is enabled (TOE80 = 1).

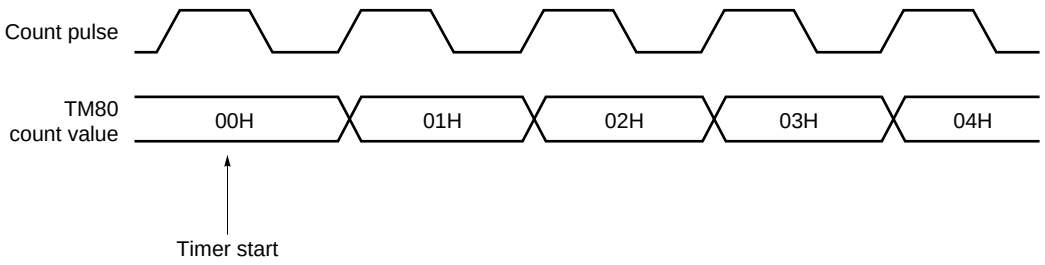
Caution Do not set CR80 to 00H in the PWM output mode; otherwise PWM may not be output normally.

9.5 Notes on Using 8-Bit Timer/Event Counter 80

(1) Error on starting timer

An error of up to 1 clock occurs after the timer is started until a match signal is generated. This is because 8-bit timer counter 80 (TM80) is started asynchronous to the count pulse.

Figure 9-8. Start Timing of 8-Bit Timer Counter

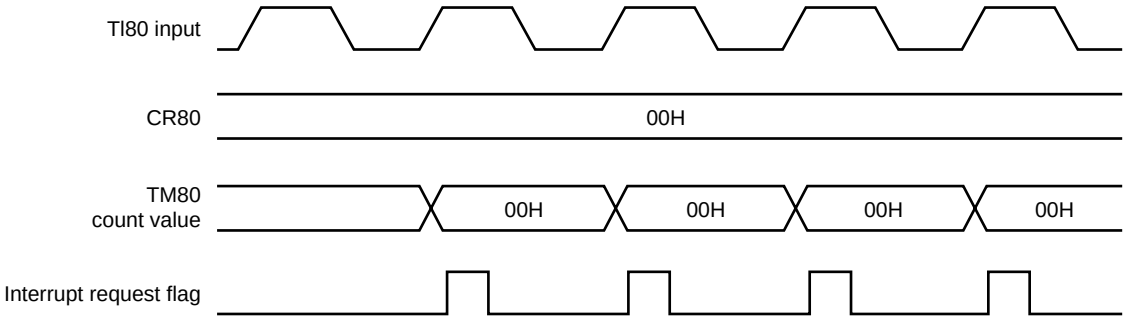


(2) Setting of 8-bit compare register 80

8-bit compare register 80 (CR80) can be set to 00H.

Therefore, one pulse can be counted when the 8-bit timer/event counter operates as an event counter.

Figure 9-9. External Event Counter Operation Timing



Cautions 1. When rewriting CR80 in timer counter operation mode (i.e., PWME80 (bit 6 of 8-bit timer mode control register 80 (TMC80)) is set to 0), be sure to stop the timer operation before hand. If CR80 is rewritten in the timer operation-enabled state, a match interrupt request signal may occur at the moment of rewrite.

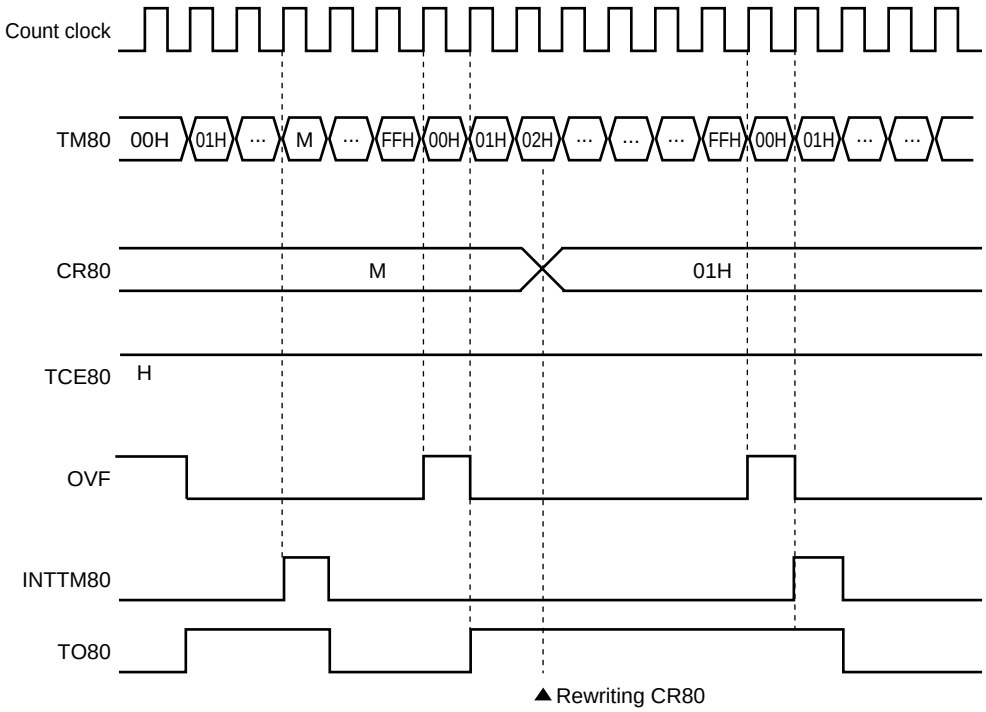
★ **2. If CR80 is rewritten while the timer is operating in PWM output operation mode (PWME80 = 1), a pulse may not be generated just in the cycle immediately after the rewrite.**

3. Do not set CR80 to 00H in the PWM output mode; otherwise PWM may not be output normally.

★ **(3) Operation after rewriting compare register during PWM output**

When 8-bit compare register 80 (CR80) is rewritten during PWM output, a high level may be output for a cycle after rewriting CR80 (count pulse × 256) if the 8-bit compare register 80 value is smaller than the 8-bit timer counter 80 (TM80) value. The timing in this case is shown in Figure 9-10.

Figure 9-10. Timing After Rewriting Compare Register During PWM Output



M = 02H to FFH

★ **(4) Notes on STOP mode setting**

Before executing the STOP instruction, be sure to set the timer to operation stopped (TCE80 = 0).

★ **(5) External event counter start timing**

When the rising edge of TI80 is selected as the count clock, start the timer (TCE80 = 0 → 1) at the timing when TI80 changes to low level. Similarly, when the falling edge of TI80 is selected as the count clock, start the timer (TCE80 = 0 → 1) at the timing when TI80 changes to high level.

CHAPTER 10 WATCHDOG TIMER

The watchdog timer can generate non-maskable interrupts, maskable interrupts and $\overline{\text{RESET}}$ at arbitrary preset intervals.

10.1 Functions of Watchdog Timer

The watchdog timer has the following functions.

- Watchdog timer
- Interval timer

Caution Select the watchdog timer mode or interval timer mode by using the watchdog timer mode register (WDTM).

(1) Watchdog timer

The watchdog timer is used to detect a program loop. When a program loop is detected, a non-maskable interrupt or the $\overline{\text{RESET}}$ signal can be generated.

★ **Table 10-1. Program Loop Detection Time of Watchdog Timer**

Program Loop Detection Time	At f_X = 10.0 MHz[Note] Operation	At f_X = 5.0 MHz Operation	At f_{CC} = 4.0 MHz Operation
$2^{11} \times 1/f_W$	205 μs	410 μs	512 μs
$2^{13} \times 1/f_W$	819 μs	1.64 ms	2.05 ms
$2^{15} \times 1/f_W$	3.28 ms	6.55 ms	8.19 ms
$2^{17} \times 1/f_W$	13.1 ms	26.2 ms	32.8 ms

Note Expanded-specification products only

Remark f_W: f_X or f_{CC}
f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

(2) Interval timer

The interval timer generates an interrupt at a given interval set in advance.

★ **Table 10-2. Interval Time**

Interval Time	At f_X = 10.0 MHz[Note] Operation	At f_X = 5.0 MHz Operation	At f_{CC} = 4.0 MHz Operation
$2^{11} \times 1/f_W$	205 μs	410 μs	512 μs
$2^{13} \times 1/f_W$	819 μs	1.64 ms	2.05 ms
$2^{15} \times 1/f_W$	3.28 ms	6.55 ms	8.19 ms
$2^{17} \times 1/f_W$	13.1 ms	26.2 ms	32.8 ms

Note Expanded-specification products only

Remark f_W: f_X or f_{CC}
f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

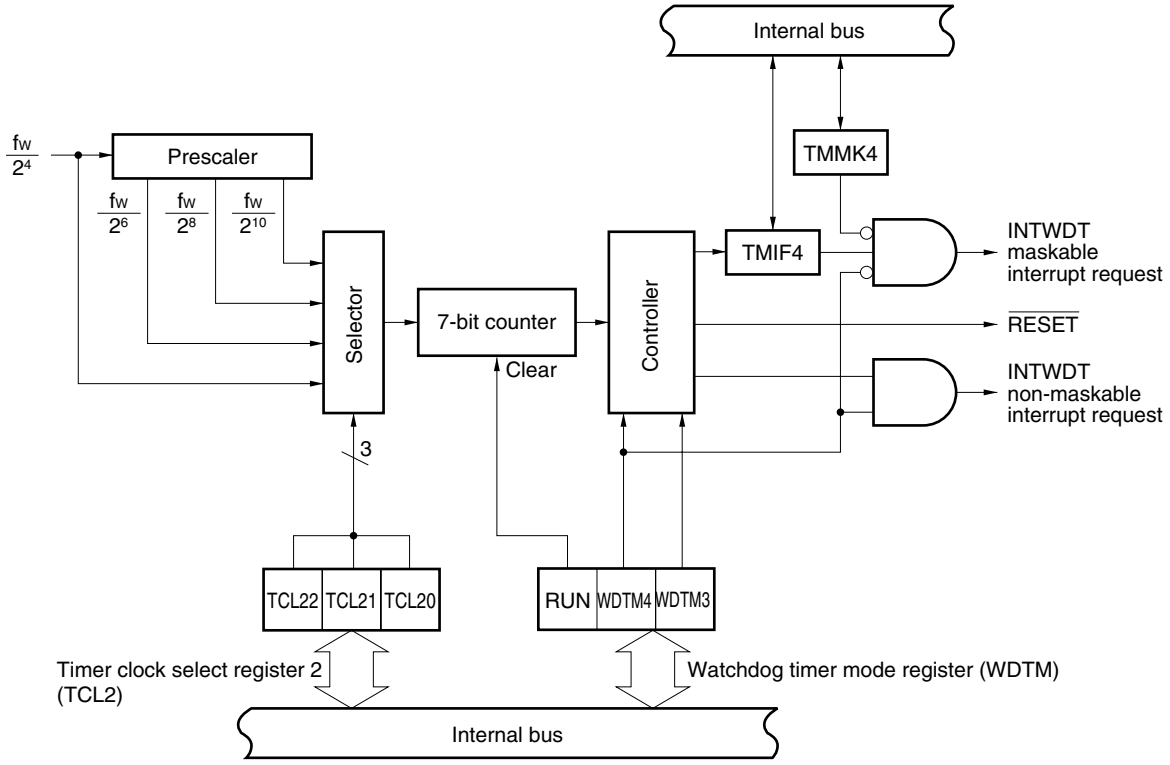
10.2 Configuration of Watchdog Timer

The watchdog timer consists of the following hardware.

Table 10-3. Configuration of Watchdog Timer

Item	Configuration
Control registers	Timer clock select register 2 (TCL2) Watchdog timer mode register (WDTM)

Figure 10-1. Block Diagram of Watchdog Timer



Remark fw: fx or fcc

10.3 Watchdog Timer Control Registers

The following two registers are used to control the watchdog timer.

- Timer clock select register 2 (TCL2)
- Watchdog timer mode register (WDTM)

(1) Timer clock select register 2 (TCL2)

This register sets the watchdog timer count clock.

TCL2 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears TCL2 to 00H.

Figure 10-2. Format of Timer Clock Select Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
TCL2	0	0	0	0	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

★

TCL22	TCL21	TCL20	Watchdog timer count clock selection				Interval time			
				@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation	@ f_{CC} = 4.0 MHz operation		@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation	@ f_{CC} = 4.0 MHz operation
0	0	0	$f_X/2^4$ or $f_{CC}/2^4$	625 kHz	312.5 kHz	250 kHz	$2^{11}/f_X$ or $2^{11}/f_{CC}$	205 μs	410 μs	512 μs
0	1	0	$f_X/2^6$ or $f_{CC}/2^6$	156.2 kHz	78.1 kHz	62.5 kHz	$2^{13}/f_X$ or $2^{13}/f_{CC}$	819 μs	1.64 ms	2.05 ms
1	0	0	$f_X/2^8$ or $f_{CC}/2^8$	39.0 kHz	19.5 kHz	15.6 kHz	$2^{15}/f_X$ or $2^{15}/f_{CC}$	3.28 ms	6.55 ms	8.19 ms
1	1	0	$f_X/2^{10}$ or $f_{CC}/2^{10}$	9.76 kHz	4.88 kHz	3.91 kHz	$2^{17}/f_X$ or $2^{17}/f_{CC}$	13.1 ms	26.2 ms	32.8 ms
Other than above			Setting prohibited							

Note Expanded-specification products only

Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)

f_{CC}: System clock oscillation frequency (RC oscillation)

(2) Watchdog timer mode register (WDTM)

This register sets the operation mode of the watchdog timer, and enables/disables counting of the watchdog timer.

WDTM is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears WDTM to 00H.

Figure 10-3. Format of Watchdog Timer Mode Register

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Selection of operation of watchdog timer[Note 1]
0	Stop counting
1	Clear counter and start counting

WDTM4	WDTM3	Selection of operation mode of watchdog timer[Note 2]
0	0	Operation stop
0	1	Interval timer mode (overflow and maskable interrupt occur)[Note 3]
1	0	Watchdog timer mode 1 (overflow and non-maskable interrupt occur)
1	1	Watchdog timer mode 2 (overflow occurs and reset operation started)

Notes 1. Once RUN has been set (1), it cannot be cleared (0) by software. Therefore, when counting is started, it cannot be stopped by any means other than $\overline{\text{RESET}}$ input.

2. Once WDTM3 and WDTM4 have been set (1), they cannot be cleared (0) by software.

3. The watchdog timer starts operations as an interval timer when RUN is set to 1.

Cautions 1. When the watchdog timer is cleared by setting RUN to 1, the actual overflow time is up to 0.8% shorter than the time set by timer clock select register 2 (TCL2).

2. In watchdog timer mode 1 or 2, set WDTM4 to 1 after confirming TMIF4 (bit 0 of interrupt request flag 0) has been set to 0. When watchdog timer mode 1 or 2 is selected under the condition that TMIF4 is 1, a non-maskable interrupt occurs at the completion of rewriting.

10.4 Operation of Watchdog Timer

10.4.1 Operation as watchdog timer

The watchdog timer operates to detect a program loop when bit 4 (WDTM4) of the watchdog timer mode register (WDTM) is set to 1.

The count clock (program loop detection time interval) of the watchdog timer can be selected by bits 0 to 2 (TCL20 to TCL22) of timer clock select register 2 (TCL2). The watchdog timer is started by setting bit 7 (RUN) of WDTM to 1. Set RUN to 1 within the set program loop detection time interval after the watchdog timer has been started. By setting RUN to 1, the watchdog timer can be cleared and start counting. If RUN is not set to 1, and the program loop detection time is exceeded, the system is reset or a non-maskable interrupt is generated according to the value of bit 3 (WDTM3) of WDTM.

The watchdog timer continues operation in the HALT mode, but stops in the STOP mode. Therefore, set RUN to 1 before entering the STOP mode to clear the watchdog timer, and then execute the STOP instruction.

Caution The actual program loop detection time may be up to 0.8% shorter than the set time.

★ **Table 10-4. Program Loop Detection Time of Watchdog Timer**

TCL22	TCL21	TCL20	Program Loop Detection Time	At f_X = 10.0 MHz[Note] Operation	At f_X = 5.0 MHz Operation	At f_{CC} = 4.0 MHz Operation
0	0	0	$2^{11} \times 1/f_W$	205 μs	410 μs	512 μs
0	1	0	$2^{13} \times 1/f_W$	819 μs	1.64 ms	2.05 ms
1	0	0	$2^{15} \times 1/f_W$	3.28 ms	6.55 ms	8.19 ms
1	1	0	$2^{17} \times 1/f_W$	13.1 ms	26.2 ms	32.8 ms

Note Expanded-specification products only

Remark f_W: f_X or f_{CC}
f_X: System clock oscillation frequency (ceramic/crystal oscillation)
f_{CC}: System clock oscillation frequency (RC oscillation)

10.4.2 Operation as interval timer

When bits 4 and 3 (WDTM4, WDTM3) of the watchdog timer mode register (WDTM) are set to 1, the watchdog timer also operates as an interval timer that repeatedly generates an interrupt at time intervals specified by the count value set in advance.

Select the count clock (or interval time) by setting bits 0 to 2 (TCL20 to TCL22) of timer clock select register 2 (TCL2). The watchdog timer starts operation as an interval timer when the RUN bit (bit 7 of WDTM) is set to 1.

In the interval timer mode, the interrupt mask flag (TMMK4) is valid, and a maskable interrupt (INTWDT) can be generated. The priority of INTWDT is set as the highest of all the maskable interrupts.

The interval timer continues operation in the HALT mode, but stops in the STOP mode. Therefore, set RUN to 1 before entering the STOP mode to clear the interval timer, and then execute the STOP instruction.

Cautions 1. Once bit 4 (WDTM4) of WDTM is set to 1 (when the watchdog timer mode is selected), the interval timer mode is not set, unless the $\overline{\text{RESET}}$ signal is input.

2. The interval time immediately after the setting by WDTM may be up to 0.8% shorter than the set time.

★ **Table 10-5. Interval Time of Interval Timer**

TCL22	TCL21	TCL20	Interval Time	At f_X = 10.0 MHz[Note] Operation	At f_X = 5.0 MHz Operation	At f_{CC} = 4.0 MHz Operation
0	0	0	$2^{11} \times 1/f_W$	205 μs	410 μs	512 μs
0	1	0	$2^{13} \times 1/f_W$	819 μs	1.64 ms	2.05 ms
1	0	0	$2^{15} \times 1/f_W$	3.28 ms	6.55 ms	8.19 ms
1	1	0	$2^{17} \times 1/f_W$	13.1 ms	26.2 ms	32.8 ms

Note Expanded-specification products only

Remark f_W: f_X or f_{CC}

f_X: System clock oscillation frequency (ceramic/crystal oscillation)

f_{CC}: System clock oscillation frequency (RC oscillation)

CHAPTER 11 8-BIT A/D CONVERTER (μPD789104A, 789124A SUBSERIES)

11.1 8-Bit A/D Converter Functions

The 8-bit A/D converter is an 8-bit resolution converter that converts analog inputs into digital signals. This converter can control up to four channels of analog inputs (ANI0 to ANI3).

A/D conversion can only be started by software.

One of analog inputs ANI0 to ANI3 is selected for A/D conversion. A/D conversion is performed repeatedly, with an interrupt request (INTAD0) being issued each time an A/D session is completed.

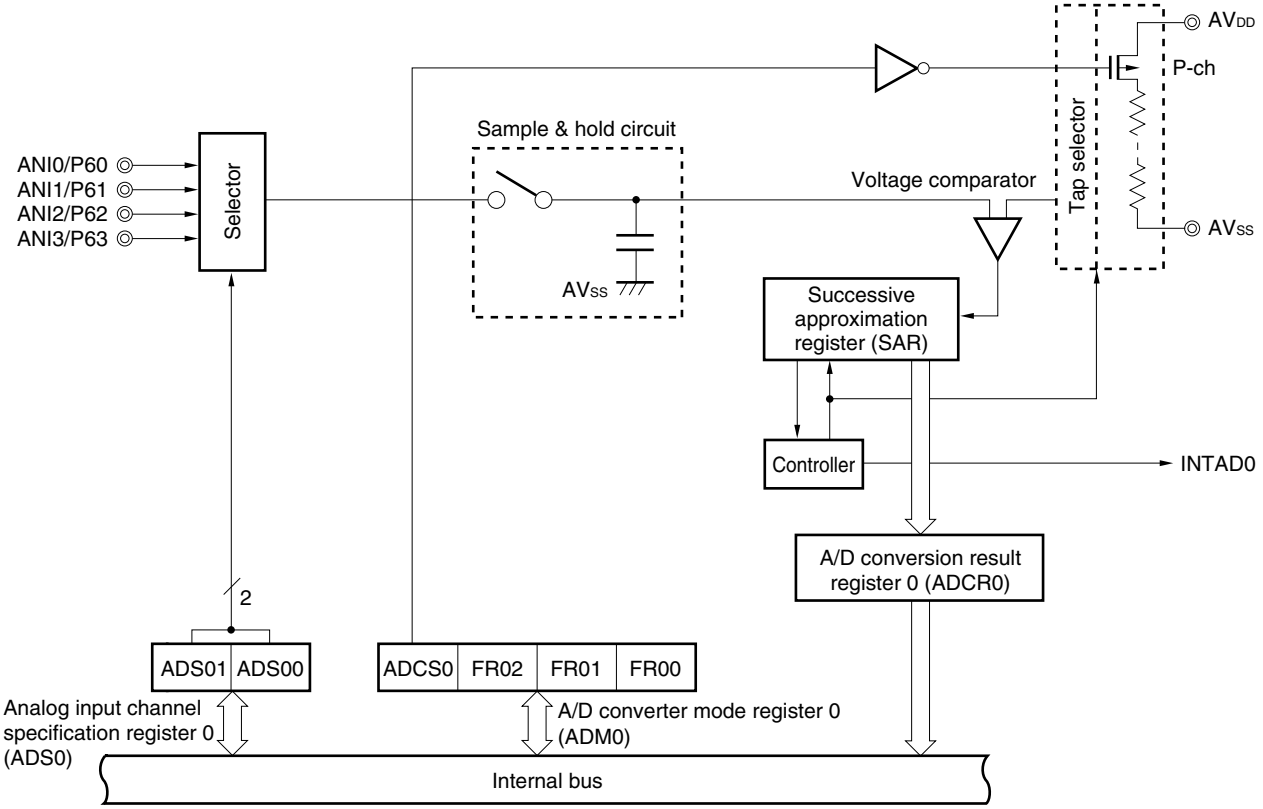
11.2 8-Bit A/D Converter Configuration

The 8-bit A/D converter consists of the following hardware.

Table 11-1. Configuration of 8-Bit A/D Converter

Item	Configuration
Analog input	4 channels (ANI0 to ANI3)
Registers	Successive approximation register (SAR) A/D conversion result register 0 (ADCR0)
Control registers	A/D converter mode register 0 (ADM0) Analog input channel specification register 0 (ADS0)

Figure 11-1. Block Diagram of 8-Bit A/D Converter



(1) Successive approximation register (SAR)

The SAR receives the result of comparing an analog input voltage and a voltage at the voltage tap (comparison voltage), received from the series resistor string, starting from the most significant bit (MSB).

Upon receiving all the bits, down to the least significant bit (LSB), that is, upon the completion of A/D conversion, the SAR sends its contents to A/D conversion result register 0 (ADCR0).

(2) A/D conversion result register 0 (ADCR0)

Each time A/D conversion ends, the conversion result received from the successive approximation register is loaded into ADCR0, which is an 8-bit register that holds the result of A/D conversion.

ADCR0 can be read with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

(3) Sample & hold circuit

The sample & hold circuit samples consecutive analog inputs from the input circuit, one by one, and sends them to the voltage comparator. The sampled analog input voltage is held during A/D conversion.

(4) Voltage comparator

The voltage comparator compares an analog input with the voltage output by the series resistor string.

(5) Series resistor string

The series resistor string is configured between AV_{DD} and AV_{SS}. It generates the reference voltages against which analog inputs are compared.

(6) ANI0 to ANI3 pins

Pins ANI0 to ANI3 are the 4-channel analog input pins for the A/D converter. They are used to receive the analog signals for A/D conversion.

Caution Do not supply pins ANI0 to ANI3 with voltages that fall outside the rated range. If a voltage of AV_{DD} or greater or AV_{SS} or lower (even if within the absolute maximum ratings) is supplied to any of these pins, the conversion value for the corresponding channel will be undefined. Furthermore, the conversion values for the other channels may also be affected.

(7) AV_{SS} pin

The AV_{SS} pin is the ground potential pin for the A/D converter. This pin must be held at the same potential as the V_{SS} pin, even while the A/D converter is not being used.

(8) AV_{DD} pin

The AV_{DD} pin is the analog power supply pin for the A/D converter. This pin must be held at the same potential as the V_{DD} pin, even while the A/D converter is not being used.

11.3 Registers Controlling 8-Bit A/D Converter

The following two registers are used to control the 8-bit A/D converter.

- A/D converter mode register 0 (ADM0)
- Analog input channel specification register 0 (ADS0)

(1) A/D converter mode register 0 (ADM0)

ADM0 specifies the conversion time for analog inputs. It also specifies whether to enable conversion.
ADM0 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears ADM0 to 00H.

Figure 11-2. Format of A/D Converter Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
ADM0	ADCS0	0	FR02	FR01	FR00	0	0	0	FF80H	00H	R/W

ADCS0	A/D conversion control
0	Conversion disabled
1	Conversion enabled

★

FR02	FR01	FR00		A/D conversion time selection[Note 1]		
				@ f_X = 10.0 MHz[Note 2] operation	@ f_X = 5.0 MHz operation	@ f_{CC} = 4.0 MHz operation
0	0	0	144/f_X or 144/f_{CC}	14.4 μs	28.8 μs	36 μs
0	0	1	120/f_X or 120/f_{CC}	12 μs	24 μs	30 μs
0	1	0	96/f_X or 96/f_{CC}	Setting prohibited[Note 3]	19.2 μs	24 μs
1	0	0	72/f_X or 72/f_{CC}	Setting prohibited[Note 3]	14.4 μs	18 μs
1	0	1	60/f_X or 60/f_{CC}	Setting prohibited[Note 3]	12 μs[Note 4]	15 μs
1	1	0	48/f_X or 48/f_{CC}	Setting prohibited[Note 3]	Setting prohibited[Note 3]	Setting prohibited[Note 3]
Other than above			Setting prohibited			

Notes 1. Set the A/D conversion time to satisfy the following specifications.
<Expanded-specification products>
When 4.5 V ≤ V_{DD} ≤ 5.5 V: 12 μs min.
When 2.7 V ≤ V_{DD} < 4.5 V: 14 μs min.
When 1.8 V ≤ V_{DD} < 2.7 V: 28 μs min.
<Conventional-specification products>
When 2.7 V ≤ V_{DD} ≤ 5.5 V: 14 μs min.
When 1.8 V ≤ V_{DD} < 2.7 V: 28 μs min.

2. Expanded-specification products only

3. Setting prohibited because the A/D conversion time does not satisfy the rating shown in **Note 1**.

4. Can be set only for expanded-specification products when 4.5 V ≤ V_{DD} ≤ 5.5 V. Otherwise, setting prohibited.

Cautions 1. The result of conversion performed immediately after bit 7 (ADCS0) is set is undefined.

2. The result of conversion after ADCS0 is cleared may be undefined (for details, refer to 11.5 (5) Timing when A/D conversion result become undefined).

Remark fx: System clock oscillation frequency (ceramic/crystal oscillation)

fcc: System clock oscillation frequency (RC oscillation)

(2) Analog input channel specification register 0 (ADS0)

The ADS0 register specifies the port used to input the analog voltages to be converted to a digital signal.

ADS0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADS0 to 00H.

Figure 11-3. Format of Analog Input Channel Specification Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADS0	0	0	0	0	0	0	ADS01	ADS00	FF84H	00H	R/W

ADS01	ADS00	Analog input channel specification
0	0	ANI0
0	1	ANI1
1	0	ANI2
1	1	ANI3

11.4 8-Bit A/D Converter Operation

11.4.1 Basic operation of 8-bit A/D converter

<1> Select the channel for A/D conversion using analog input channel specification register 0 (ADS0).

<2> The voltage supplied to the selected analog input channel is sampled using the sample & hold circuit.

<3> After sampling continues for a certain period of time, the sample & hold circuit is put on hold to keep the input analog voltage until A/D conversion is completed.

<4> Bit 7 of the successive approximation register (SAR) is set. The tap selector sets the series resistor string voltage tap to half AV_{DD}.

<5> The series resistor string voltage tap is compared with the analog input voltage using the voltage comparator. If the analog input voltage is higher than half AV_{DD}, the MSB of the SAR is left set. If it is lower than half AV_{DD}, the MSB is reset.

<6> Bit 6 of the SAR is set automatically, and comparison shifts to the next stage. The next voltage tap of the series resistor string is selected according to bit 7, which reflects the previous comparison result, as follows.

- Bit 7 = 1: Three quarters of AV_{DD}
- Bit 7 = 0: One quarter of AV_{DD}

The voltage tap is compared with the analog input voltage. Bit 6 is set or reset according to the result of comparison.

- Analog input voltage ≥ voltage tap: Bit 6 = 1
- Analog input voltage < voltage tap: Bit 6 = 0

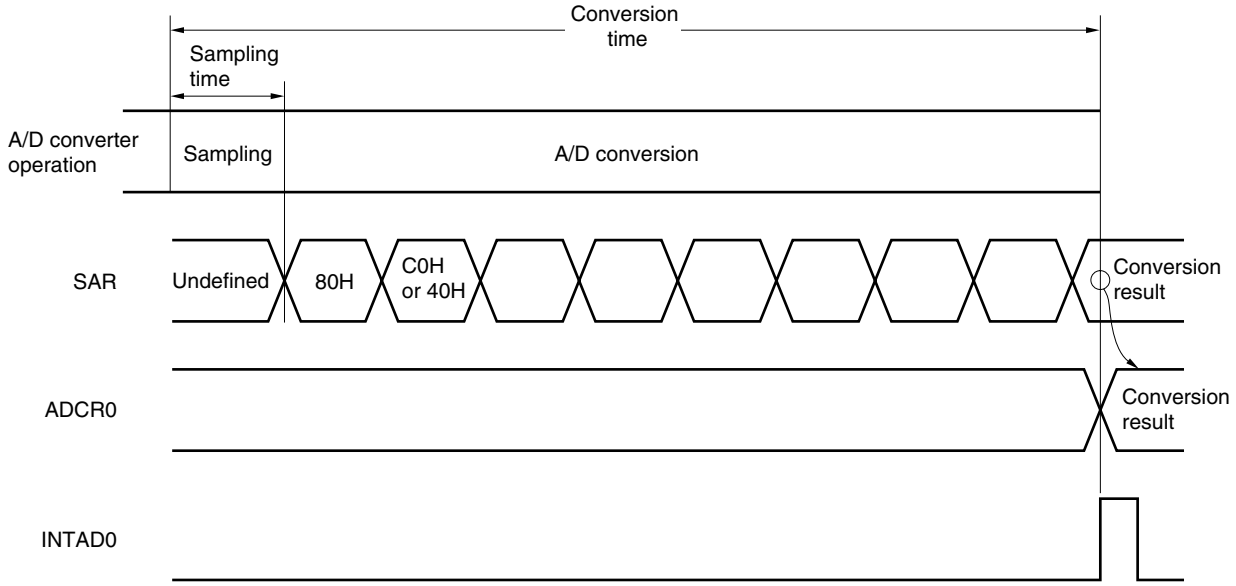
<7> Comparison is repeated until bit 0 of the SAR is reached.

<8> When comparison is completed for all of the 8 bits, a significant digital result is left in the SAR. This value is sent to and latched in A/D conversion result register 0 (ADCR0). At the same time, it is possible to generate an A/D conversion end interrupt request (INTAD0).

Cautions 1. The first A/D conversion value immediately after starting the A/D conversion operation may be undefined.

2. When in standby mode, the A/D converter stops operation.

Figure 11-4. Basic Operation of 8-Bit A/D Converter



A/D conversion continues until bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) is reset (0) by software.

If an attempt is made to write to ADM0 or analog input channel specification register 0 (ADS0) during A/D conversion, the A/D conversion in progress is canceled. In this case, if ADCS0 is set (1), A/D conversion is restarted from the beginning.

$\overline{\text{RESET}}$ input makes A/D conversion result register 0 (ADCR0) undefined.

11.4.2 Input voltage and conversion result

The relationship between the analog input voltage at the analog input pins (ANI0 to ANI3) and the A/D conversion result (A/D conversion result register 0 (ADCR0)) is represented by:

$$ADCR0 = INT\left(\frac{V_{IN}}{AV_{DD}} \times 256 + 0.5\right)$$

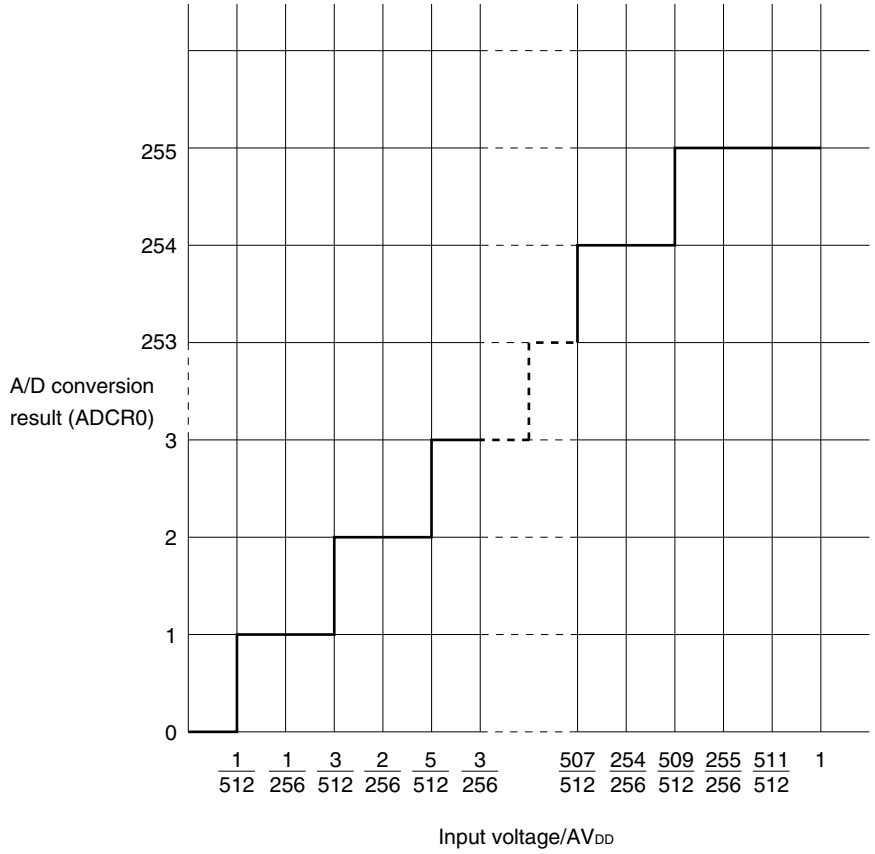
or

$$(ADCR0 - 0.5) \times \frac{AV_{DD}}{256} \leq V_{IN} < (ADCR0 + 0.5) \times \frac{AV_{DD}}{256}$$

INT( ): Function that returns the integer part of the parenthesized value
V_{IN}: Analog input voltage
AV_{DD}: A/D converter supply voltage
ADCR0: Value in A/D conversion result register 0 (ADCR0)

Figure 11-5 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 11-5. Relationship Between Analog Input Voltage and A/D Conversion Result



11.4.3 Operation mode of 8-bit A/D converter

The 8-bit A/D converter is initially in the select mode. In this mode, analog input channel specification register 0 (ADS0) is used to select the analog input channel from ANI0 to ANI3 for A/D conversion.

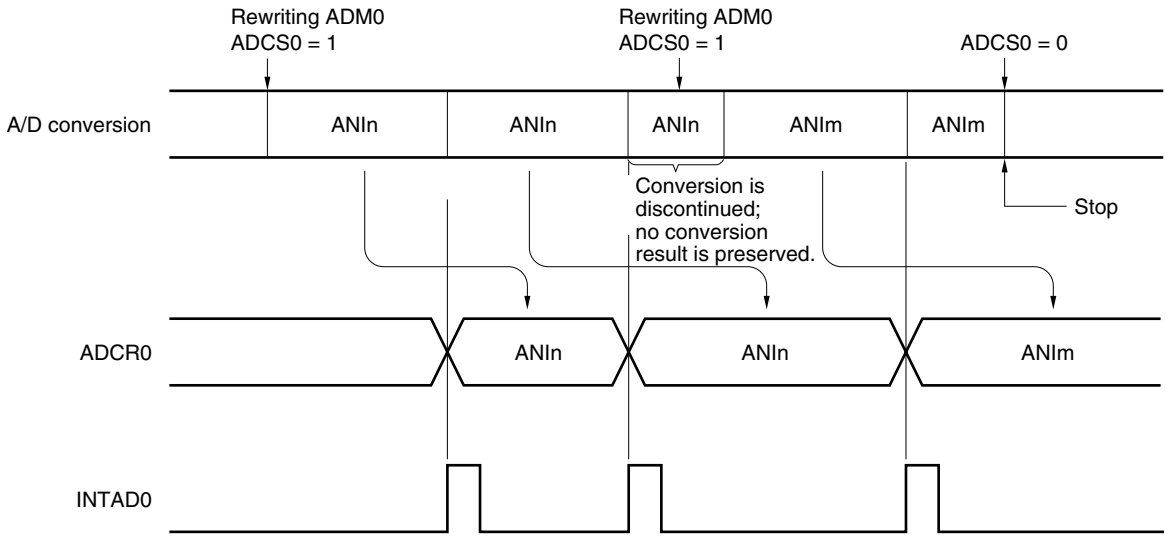
A/D conversion can only be started by software; that is, by setting A/D converter mode register 0 (ADM0).

The A/D conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated.

- **Software-started A/D conversion**

  Setting bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) triggers A/D conversion for the voltage applied to the analog input pin specified by analog input channel specification register 0 (ADS0). Upon completion of A/D conversion, the conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated. Once A/D conversion is activated, and completed, another session of A/D conversion is started. A/D conversion is repeated until new data is written to ADM0. If data where ADCS0 is 1 is written to ADM0 again during A/D conversion, the session of A/D conversion in progress is discontinued, and a new session of A/D conversion begins for the new data. If data where ADCS0 is 0 is written to ADM0 again during A/D conversion, A/D conversion is completely stopped.

Figure 11-6. Software-Started A/D Conversion



Remarks 1. n = 0, 1, 2, 3

2. m = 0, 1, 2, 3

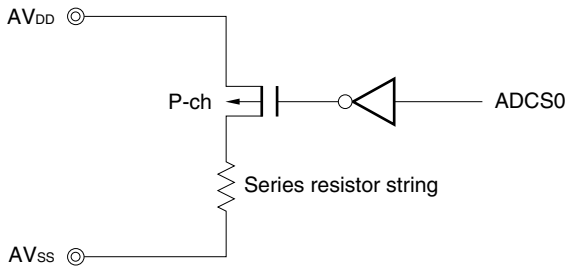
11.5 Notes on Using 8-Bit A/D Converter

(1) Current consumption in the standby mode

When the A/D converter enters the standby mode, it stops operating. Clearing bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 0 can reduce the current consumption.

Figure 11-7 shows how to reduce the current consumption in the standby mode.

Figure 11-7. How to Reduce Current Consumption in Standby Mode



(2) Input range for the ANI0 to ANI3 pins

Be sure to keep the input voltage at ANI0 to ANI3 within the rated values. If a voltage of AVDD or grater or AVSS or lower (even if within the absolute maximum ratings) is input to a conversion channel, the conversion output of the channel becomes undefined, and the conversion output of the other channels may also be affected.

(3) Conflict

<1> Conflict between writing to A/D conversion result register 0 (ADCR0) at the end of conversion and reading from ADCR0

Reading from ADCR0 takes precedence. After reading, the new conversion result is written to ADCR0.

<2> Conflict between writing to ADCR0 at the end of conversion and writing to A/D converter mode register 0 (ADM0) or analog input channel specification register 0 (ADS0)

Writing to ADM0 or ADS0 takes precedence. A request to write to ADCR0 is ignored. No conversion end interrupt request signal (INTAD0) is generated.

(4) Conversion results immediately following start of A/D conversion

The first A/D conversion value immediately following the start of A/D converter operation may be undefined. Be sure to perform processing such as polling the A/D conversion end interrupt request (INTAD0) and discarding the first conversion result.

(5) Timing that makes the A/D conversion result undefined

If the timing of the end of A/D conversion and the timing of the stop of operation of the A/C converter conflict, the A/D conversion value may be undefined. Because of this, be sure to read out the A/D conversion result while the A/D converter is operating. Furthermore, when reading out an A/D conversion result after A/D converter operation has stopped, be sure to have done so by the time the next conversion result is complete.

The conversion result readout timing is shown in Figures 11-8 and 11-9.

Figure 11-8. Conversion Result Readout Timing (When Conversion Result Is Undefined Value)

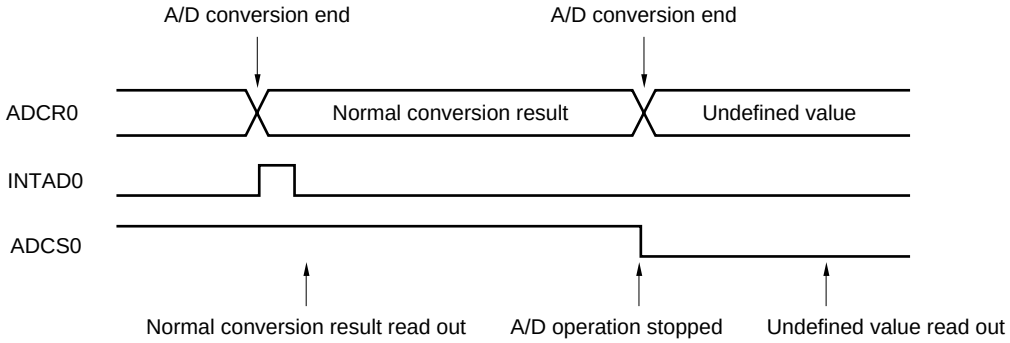
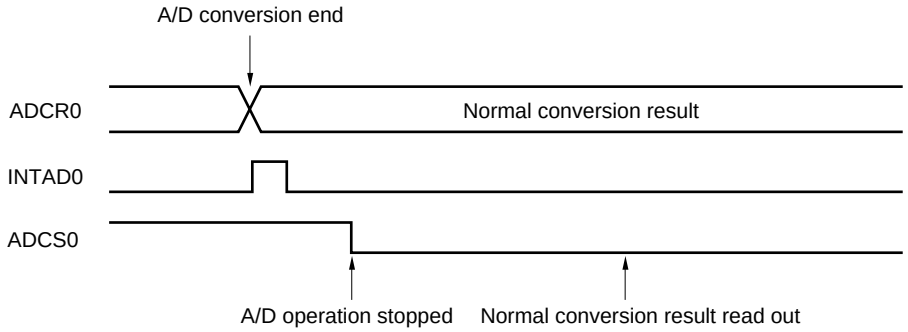


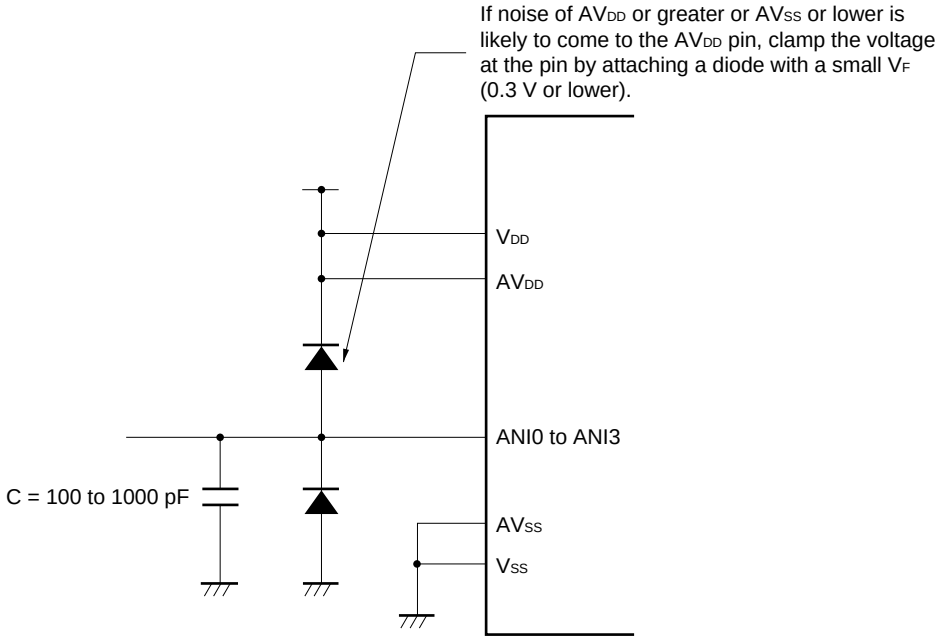
Figure 11-9. Conversion Result Readout Timing (When Conversion Result Is Normal Value)



(6) Noise prevention

To maintain a resolution of 8 bits, watch for noise at the AV_{DD} and ANI0 to ANI3 pins. The higher the output impedance of the analog input source is, the larger the effect by noise. To reduce noise, attach an external capacitor to the relevant pins as shown in Figure 11-10.

Figure 11-10. Analog Input Pin Treatment



(7) ANI0 to ANI3

The analog input pins (ANI0 to ANI3) are alternate-function pins. They are also used as port pins (P60 to P63).

If any of ANI0 to ANI3 has been selected for A/D conversion, do not execute input instructions for the ports; otherwise the conversion resolution may become lower.

If a digital pulse is applied to a pin adjacent to the analog input pin being A/D converted, coupling noise may occur which prevents an A/D conversion result from being attained as expected. Avoid applying a digital pulse to pins adjacent to the analog input pin being A/D converted.

★ **(8) Input impedance of ANI0 to ANI3 pins**

This A/D converter charges the internal sampling capacitor for about 1/10 of the conversion time, and performs sampling.

Therefore at times other than sampling, only the leakage current flows. During sampling, the current for charging the capacitor also flows, so the input impedance fluctuates and has no meaning.

However, to ensure adequate sampling, it is recommend that the output impedance of the analog input source be set to 10 kΩ or lower, or a capacitor of about 100 pF be connected to the ANI0 to ANI3 pins (refer to **Figure 11-10**).

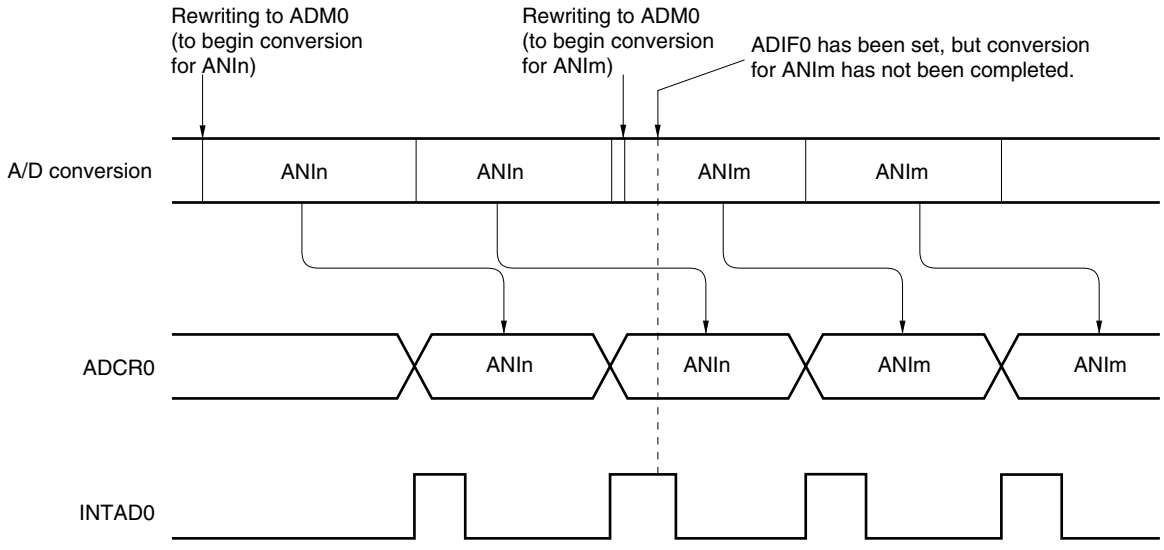
(9) Interrupt request flag (ADIF0)

Changing the contents of A/D converter mode register 0 (ADM0) does not clear the interrupt request flag (ADIF0).

If the analog input pins are changed during A/D conversion, therefore, the conversion result and the conversion end interrupt request flag may reflect the previous analog input immediately before writing to ADM0 occurs. In this case, ADIF0 may appear to be set if it is read-accessed immediately after ADM0 is write-accessed, even when A/D conversion has not been completed for the new analog input.

In addition, when A/D conversion is restarted, ADIF0 must be cleared beforehand.

Figure 11-11. A/D Conversion End Interrupt Request Generation Timing



Remarks 1. n = 0, 1, 2, 3

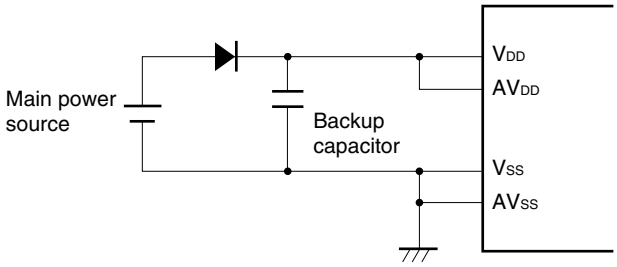
2. m = 0, 1, 2, 3

(10) AV_{DD} pin

The AV_{DD} pin is used to supply power to the analog circuit. It is also used to supply power to the ANI0 to ANI3 input circuit.

Therefore, if the application is designed to be switched to backup power, the AV_{DD} pin must be supplied with the same voltage level as for the V_{DD} pin, as shown in Figure 11-12.

Figure 11-12. AV_{DD} Pin Treatment



(11) Input impedance of the AV_{DD} pin

A series resistor string of several 10 kΩ is connected across the AV_{DD} and AV_{SS} pins.

Therefore, if the output impedance of the reference voltage source is high, this high impedance is eventually connected in parallel with the series resistor string across the AV_{DD} and AV_{SS} pins, leading to a higher reference voltage error.

12.1 10-Bit A/D Converter Functions

The 10-bit A/D converter is a 10-bit resolution converter that converts analog inputs into digital signals. This converter can control up to four channels of analog inputs (ANI0 to ANI3).

A/D conversion can only be started by software.

One of analog inputs ANI0 to ANI3 is selected for A/D conversion. A/D conversion is performed repeatedly, with an interrupt request (INTAD0) being issued each time an A/D session is completed.

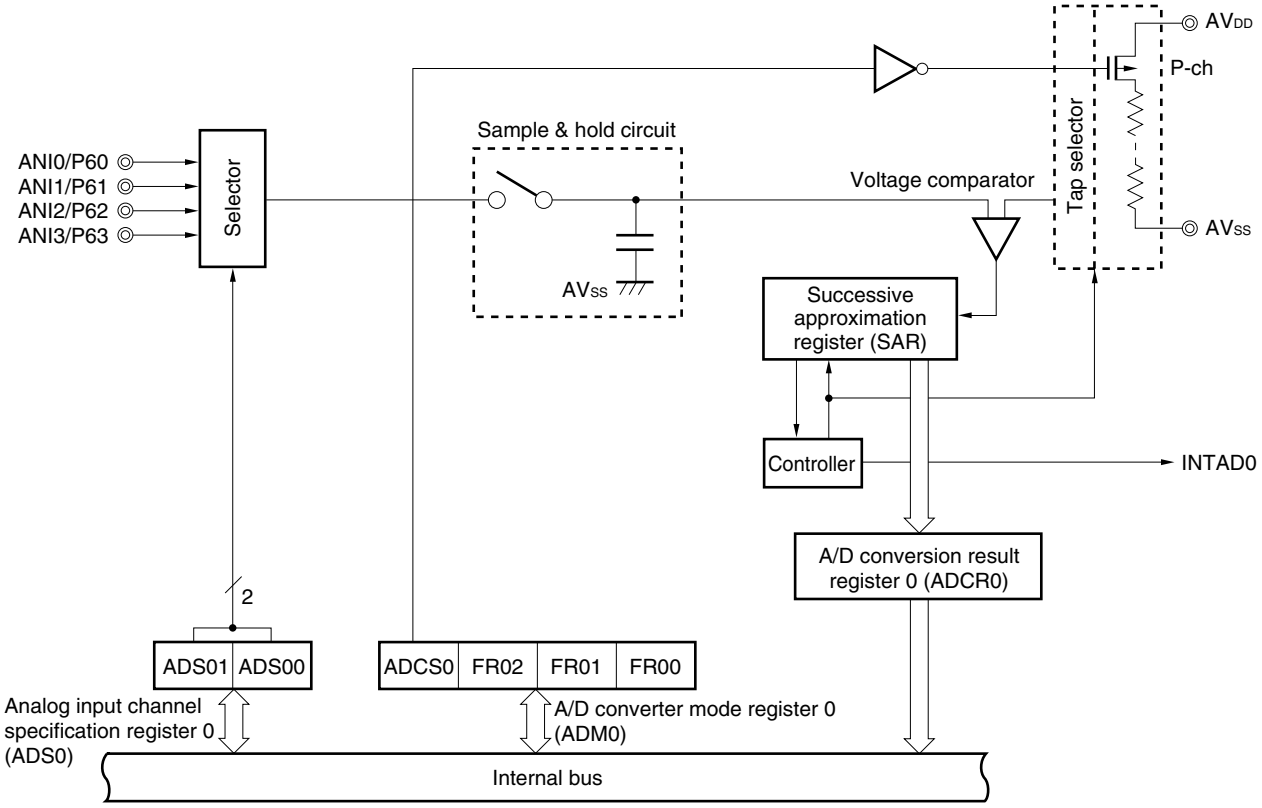
12.2 10-Bit A/D Converter Configuration

The A/D converter consists of the following hardware.

Table 12-1. Configuration of 10-Bit A/D Converter

Item	Configuration
Analog input	4 channels (ANI0 to ANI3)
Registers	Successive approximation register (SAR) A/D conversion result register 0 (ADCR0)
Control registers	A/D converter mode register 0 (ADM0) Analog input channel specification register 0 (ADS0)

Figure 12-1. Block Diagram of 10-Bit A/D Converter



(1) Successive approximation register (SAR)

The SAR receives the result of comparing an analog input voltage and a voltage at the voltage tap (comparison voltage), received from the series resistor string, starting from the most significant bit (MSB).

Upon receiving all the bits, down to the least significant bit (LSB), that is, upon the completion of A/D conversion, the SAR sends its contents to A/D conversion result register 0 (ADCR0).

★ **(2) A/D conversion result register 0 (ADCR0)**

ADCR0 is a 16-bit register that holds the result of A/D conversion. The lower 6 bits are fixed to 0. Each time A/D conversion ends, the conversion result in the successive approximation register is loaded into ADCR0. The results are stored in ADCR0 from the most significant bit.

The higher 8 bits of the conversion result are stored in FF15H and the lower 2 bits of the conversion result are stored in FF14H.

ADCR0 can be read with a 16-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes ADCR0 undefined.

Symbol	FF15H								FF14H								Address	After reset	R/W
ADCR0											0	0	0	0	0	0	FF14H, FF15H	Undefined	R

Caution When using the μPD78F9116A and 78F9116B as flash memory versions of the μPD789101A, 789102A, and 789104A, or the μPD78F9136A and 78F9136B as flash memory versions of the μPD789121A, 789122A, and 789124A, an 8-bit access can be made by ADCR0. However, it is performed only with the object file assembled by the μPD789101A, 789102A, or 789104A, or by the μPD789121A, 789122A, or 789124A, respectively.

(3) Sample & hold circuit

The sample & hold circuit samples consecutive analog inputs from the input circuit, one by one, and sends them to the voltage comparator. The sampled analog input voltage is held during A/D conversion.

(4) Voltage comparator

The voltage comparator compares an analog input with the voltage output by the series resistor string.

(5) Series resistor string

The series resistor string is configured between AV_{DD} and AV_{SS}. It generates the reference voltages against which analog inputs are compared.

(6) ANI0 to ANI3 pins

Pins ANI0 to ANI3 are the 4-channel analog input pins for the A/D converter. They are used to receive the analog signals for A/D conversion.

Caution Do not supply pins ANI0 to ANI3 with voltages that fall outside the rated range. If a voltage of AV_{DD} or greater or AV_{SS} or lower (even if within the absolute maximum ratings) is supplied to any of these pins, the conversion value for the corresponding channel will be undefined. Furthermore, the conversion values for the other channels may also be affected.

(7) AV_{SS} pin

The AV_{SS} pin is the ground potential pin for the A/D converter. This pin must be held at the same potential as the V_{SS} pin, even while the A/D converter is not being used.

(8) AV_{DD} pin

The AV_{DD} pin is the analog power supply pin for the A/D converter. This pin must be held at the same potential as the V_{DD} pin, even while the A/D converter is not being used.

12.3 Registers Controlling 10-Bit A/D Converter

The following two registers are used to control the 10-bit A/D converter.

- A/D converter mode register 0 (ADM0)
- Analog input channel specification register 0 (ADS0)

(1) A/D converter mode register 0 (ADM0)

ADM0 specifies the conversion time for analog inputs. It also specifies whether to enable conversion.

ADM0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears the ADM0 to 00H.

Figure 12-2. Format of A/D Converter Mode Register 0

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
ADM0	ADCS0	0	FR02	FR01	FR00	0	0	0	FF80H	00H	R/W

ADCS0	A/D conversion control
0	Conversion disabled
1	Conversion enabled

★

FR02	FR01	FR00	A/D conversion time selection[Note 1]			
				@ f_X = 10.0 MHz[Note 2] operation	@ f_X = 5.0 MHz operation	@ f_{CC} = 4.0 MHz operation
0	0	0	144/f_X or 144/f_{CC}	14.4 μs	28.8 μs	36 μs
0	0	1	120/f_X or 120/f_{CC}	12 μs	24 μs	30 μs
0	1	0	96/f_X or 96/f_{CC}	Setting prohibited[Note 3]	19.2 μs	24 μs
1	0	0	72/f_X or 72/f_{CC}	Setting prohibited[Note 3]	14.4 μs	18 μs
1	0	1	60/f_X or 60/f_{CC}	Setting prohibited[Note 3]	12 μs[Note 4]	15 μs
1	1	0	48/f_X or 48/f_{CC}	Setting prohibited[Note 3]	Setting prohibited[Note 3]	Setting prohibited[Note 3]
Other than above			Setting prohibited			

Notes 1. Set the A/D conversion time to satisfy the following specifications.

<Expanded-specification products>

When 4.5 V ≤ V_{DD} ≤ 5.5 V: 12 μs min.

When 2.7 V ≤ V_{DD} < 4.5 V: 14 μs min.

When 1.8 V ≤ V_{DD} < 2.7 V: 28 μs min.

<Conventional-specification products>

When 2.7 V ≤ V_{DD} ≤ 5.5 V: 14 μs min.

When 1.8 V ≤ V_{DD} < 2.7 V: 28 μs min.

2. Expanded-specification products only

3. Setting prohibited because the A/D conversion time does not satisfy the rating shown in **Note 1**.

4. Can be set only for expanded-specification products when 4.5 V ≤ V_{DD} ≤ 5.5 V. Otherwise, setting prohibited.

Cautions 1. The result of conversion performed immediately after bit 7 (ADCS0) is set is undefined.

2. The result of conversion after ADCS0 is cleared may be undefined (for details, refer to 12.5 (5) Timing when A/D conversion result becomes undefined).

Remark fx: System clock oscillation frequency (ceramic/crystal oscillation)

fcc: System clock oscillation frequency (RC oscillation)

(2) Analog input channel specification register 0 (ADS0)

The ADS0 register specifies the port used to input the analog voltages to be converted to a digital signal. ADS0 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ADS0 to 00H.

Figure 12-3. Format of Analog Input Channel Specification Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ADS0	0	0	0	0	0	0	ADS01	ADS00	FF84H	00H	R/W

ADS01	ADS00	Analog input channel specification
0	0	ANI0
0	1	ANI1
1	0	ANI2
1	1	ANI3

12.4 10-Bit A/D Converter Operation

12.4.1 Basic operation of 10-bit A/D converter

<1> Select the channel for A/D conversion, using analog input channel specification register 0 (ADS0).

<2> The voltage supplied to the selected analog input channel is sampled using the sample & hold circuit.

<3> After sampling continues for a certain period of time, the sample & hold circuit is put on hold to keep the input analog voltage until A/D conversion is completed.

<4> Bit 9 of the successive approximation A/D conversion register (SAR) is set. The tap selector sets the series resistor string voltage tap to half AV_{DD}.

<5> The series resistor string voltage tap is compared with the analog input voltage using the voltage comparator. If the analog input voltage is higher than half AV_{DD}, the MSB of the SAR is left set. If it is lower than half AV_{DD}, the MSB is reset.

<6> Bit 8 of the SAR is set automatically, and comparison shifts to the next stage. The next voltage tap of the series resistor string is selected according to bit 9, which reflects the previous comparison result, as follows.

- Bit 9 = 1: Three quarters of AV_{DD}
- Bit 9 = 0: One quarter of AV_{DD}

The voltage tap is compared with the analog input voltage. Bit 8 is set or reset according to the result of comparison.

- Analog input voltage ≥ voltage tap: Bit 8 = 1
- Analog input voltage < voltage tap: Bit 8 = 0

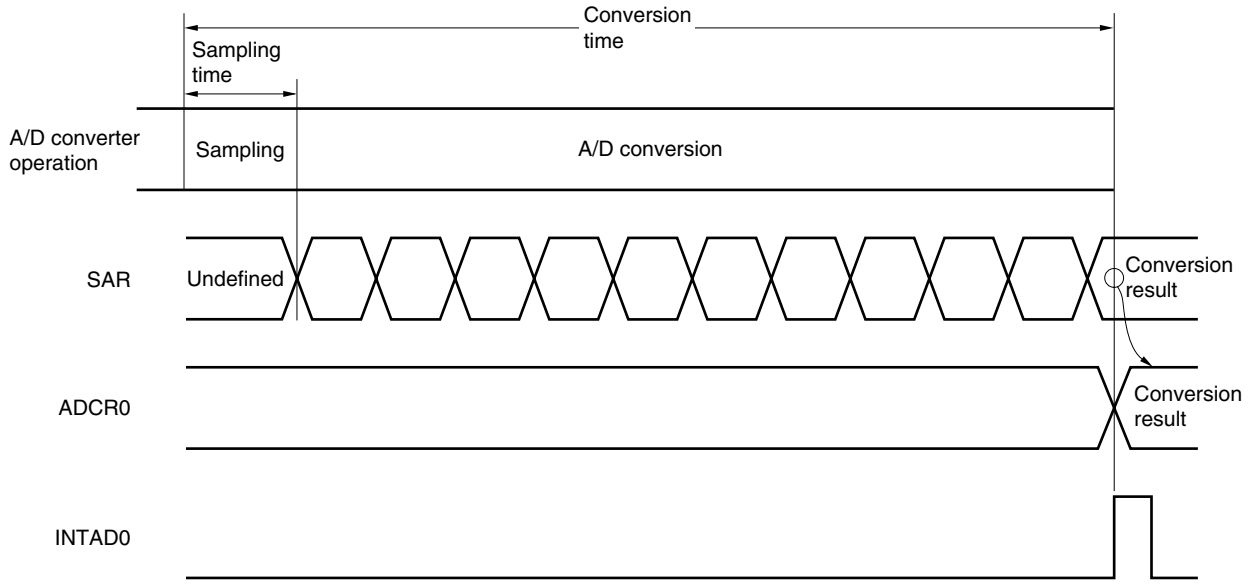
<7> Comparison is repeated until bit 0 of the SAR is reached.

<8> When comparison is completed for all of the 10 bits, a significant digital result is left in the SAR. This value is sent to and latched in A/D conversion result register 0 (ADCR0). At the same time, it is possible to generate an A/D conversion end interrupt request (INTAD0).

Cautions 1. The A/D conversion value immediately after starting the A/D conversion operation may be undefined.

2. When in standby mode, the A/D converter stops operation.

Figure 12-4. Basic Operation of 10-Bit A/D Converter



A/D conversion continues until bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) is reset (0) by software.

If an attempt is made to write to ADM0 or analog input channel specification register 0 (ADS0) during A/D conversion, the A/D conversion in progress is canceled. In this case, A/D conversion is restarted from the beginning, if ADCS0 is set (1).

$\overline{\text{RESET}}$ input makes A/D conversion result register 0 (ADCR0) undefined.

12.4.2 Input voltage and conversion result

The relationship between the analog input voltage at the analog input pins (ANI0 to ANI3) and the A/D conversion result (A/D conversion result register 0 (ADCR0)) is represented by:

$$ADCR0 = INT\left(\frac{V_{IN}}{AV_{DD}} \times 1{,}024 + 0.5\right)$$

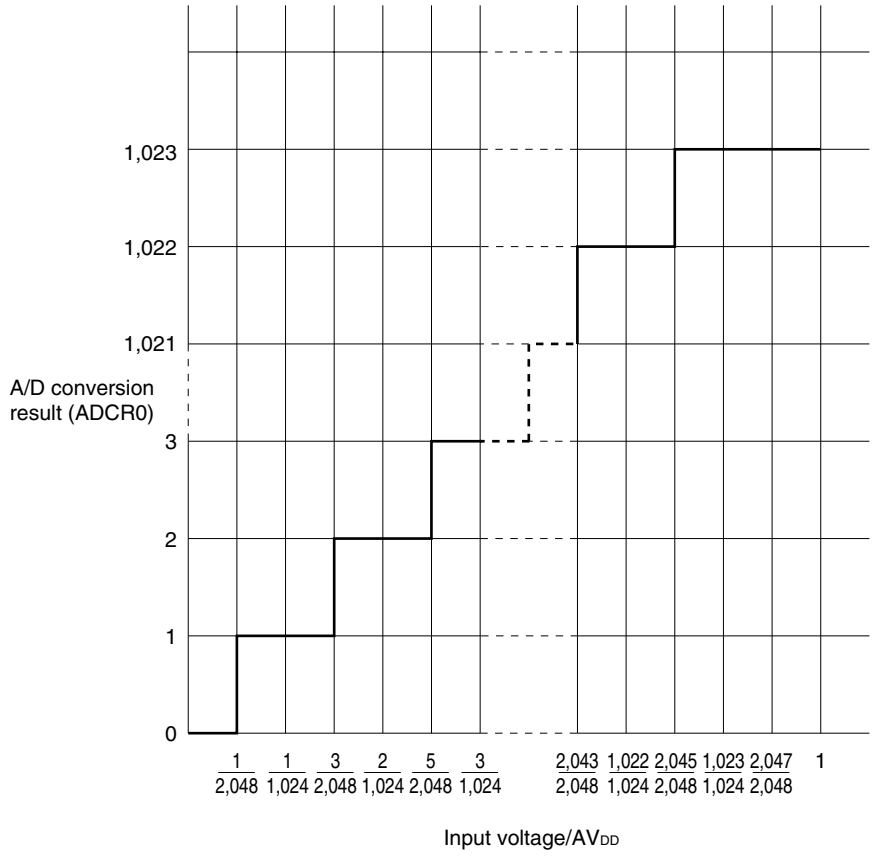
or

$$(ADCR0 - 0.5) \times \frac{AV_{DD}}{1{,}024} \leq V_{IN} < (ADCR0 + 0.5) \times \frac{AV_{DD}}{1{,}024}$$

INT( ): Function that returns the integer part of the parenthesized value
V_{IN}: Analog input voltage
AV_{DD}: A/D converter supply voltage
ADCR0: Value in A/D conversion result register 0 (ADCR0)

Figure 12-5 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 12-5. Relationship Between Analog Input Voltage and A/D Conversion Result



12.4.3 Operation mode of 10-bit A/D converter

The 10-bit A/D converter is initially in the select mode. In this mode, analog input channel specification register 0 (ADS0) is used to select the analog input channel from ANI0 to ANI3 for A/D conversion.

A/D conversion can be started only by software; that is, by setting A/D converter mode register 0 (ADM0).

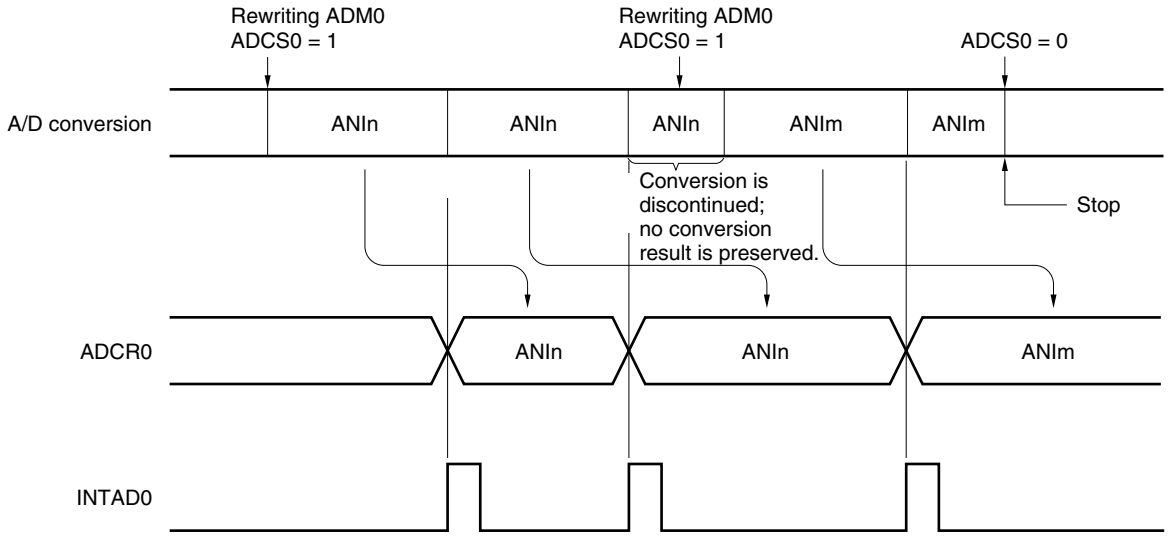
The A/D conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated.

- **Software-started A/D conversion**

  Setting bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) triggers A/D conversion for the voltage applied to the analog input pin specified by analog input channel specification register 0 (ADS0).

  Upon completion of A/D conversion, the conversion result is saved to A/D conversion result register 0 (ADCR0). At the same time, an interrupt request signal (INTAD0) is generated. Once A/D conversion is activated, and completed, another session of A/D conversion is started. A/D conversion is repeated until new data is written to ADM0. If data where ADCS0 is 1 is written to ADM0 again during A/D conversion, the session of A/D conversion in progress is discontinued, and a new session of A/D conversion begins for the new data. If data where ADCS0 is 0 is written to ADM0 again during A/D conversion, A/D conversion is completely stopped.

Figure 12-6. Software-Started A/D Conversion



Remarks 1. n = 0, 1, 2, 3

2. m = 0, 1, 2, 3

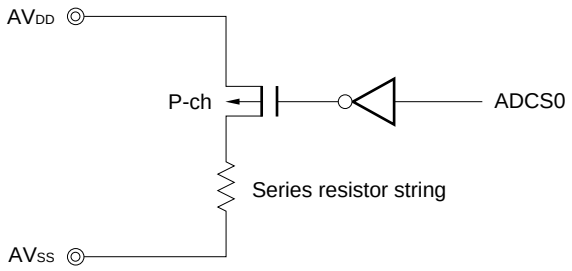
12.5 Notes on Using 10-Bit A/D Converter

(1) Current consumption in the standby mode

When the A/D converter enters the standby mode, it stops operating. Clearing bit 7 (ADCS0) of A/D converter mode register 0 (ADM0) to 0 can reduce the current consumption.

Figure 12-7 shows how to reduce the current consumption in the standby mode.

Figure 12-7. How to Reduce Current Consumption in Standby Mode



(2) Input range for the ANI0 to ANI3 pins

Be sure to keep the input voltage at ANI0 to ANI3 within the rated values. If a voltage of AV_{DD} or greater or AV_{SS} or lower (even if within the absolute maximum ratings) is input a conversion channel, the conversion output of the channel becomes undefined, and the conversion output of the other channels may also be affected.

(3) Conflict

<1> Conflict between writing to A/D conversion result register 0 (ADCR0) at the end of conversion and reading from ADCR0

Reading from ADCR0 takes precedence. After reading, the new conversion result is written to ADCR0.

<2> Conflict between writing to ADCR0 at the end of conversion and writing to A/D converter mode register 0 (ADM0) or analog input channel specification register 0 (ADS0)

Writing to ADM0 or ADS0 takes precedence. A request to write to ADCR0 is ignored. No conversion end interrupt request signal (INTAD0) is generated.

(4) Conversion results immediately following start of A/D conversion

The first A/D conversion value immediately following the start of A/D converter operation may be undefined. Be sure to perform processing such as polling the A/D conversion end interrupt request (INTAD0) and discarding the first conversion result.

(5) Timing that makes the A/D conversion result undefined

If the timing of the end of A/D conversion and the timing of the stop of operation of the A/C converter conflict, the A/D conversion value may be undefined. Because of this, be sure to read out the A/D conversion result while the A/D converter is operating. Furthermore, when reading out an A/D conversion result after A/D converter operation has stopped, be sure to have done so by the time the next conversion result is complete.

The conversion result readout timing is shown in Figures 12-8 and 12-9.

Figure 12-8. Conversion Result Readout Timing (When Conversion Result Is Undefined Value)

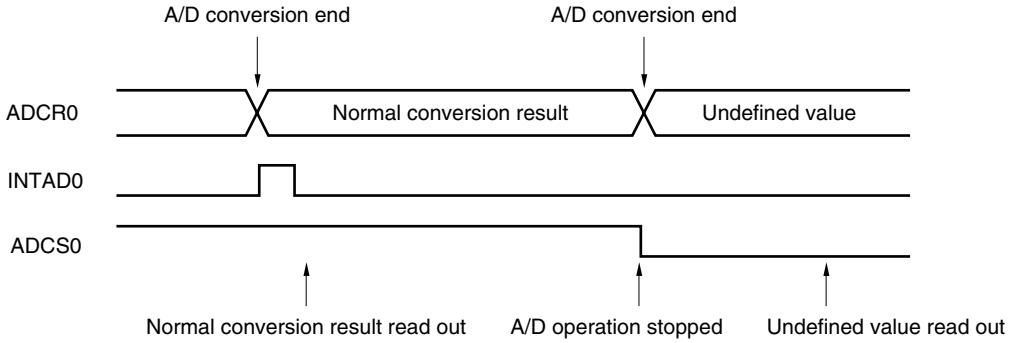
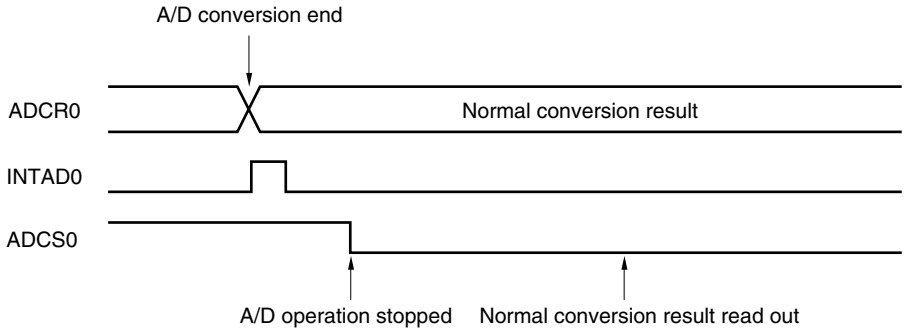


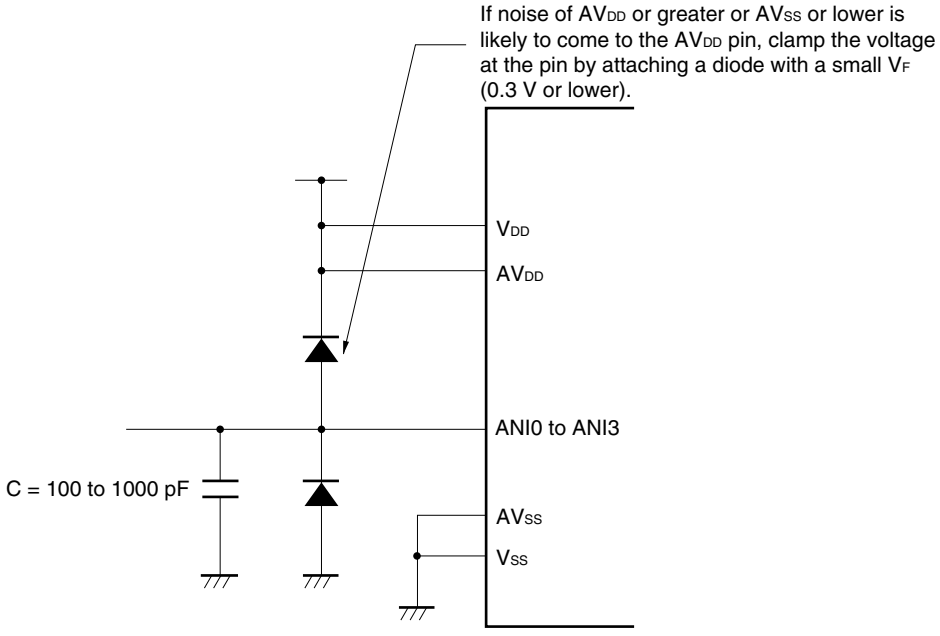
Figure 12-9. Conversion Result Readout Timing (When Conversion Result Is Normal Value)



(6) Noise prevention

To maintain a resolution of 10 bits, watch for noise at the AV_{DD} and ANI0 to ANI3 pins. The higher the output impedance of the analog input source is, the larger the effect by noise is. To reduce noise, attach an external capacitor to the relevant pins as shown in Figure 12-10.

Figure 12-10. Analog Input Pin Treatment



(7) ANI0 to ANI3

The analog input pins (ANI0 to ANI3) are alternate-function pins. They are also used as port pins (P60 to P63).

If any of ANI0 to ANI3 has been selected for A/D conversion, do not execute input instructions for the ports; otherwise, the conversion resolution may become lower.

If a digital pulse is applied to a pin adjacent to the analog input pin being A/D converted, coupling noise may occur which prevents an A/D conversion result from being attained as expected. Avoid applying a digital pulse to pins adjacent to the analog input pin being A/D converted.

★ **(8) Input impedance of ANI0 to ANI3 pins**

This A/D converter charges the internal sampling capacitor for about 1/10 of the conversion time, and performs sampling.

Therefore at times other than sampling, only the leakage current flows. During sampling, the current for charging the capacitor also flows, so the input impedance fluctuates and has no meaning.

However, to ensure adequate sampling, it is recommend that the output impedance of the analog input source be set to 10 kΩ or lower, or a capacitor of about 100 pF be connected to the ANI0 to ANI3 pins (refer to **Figure 12-10**).

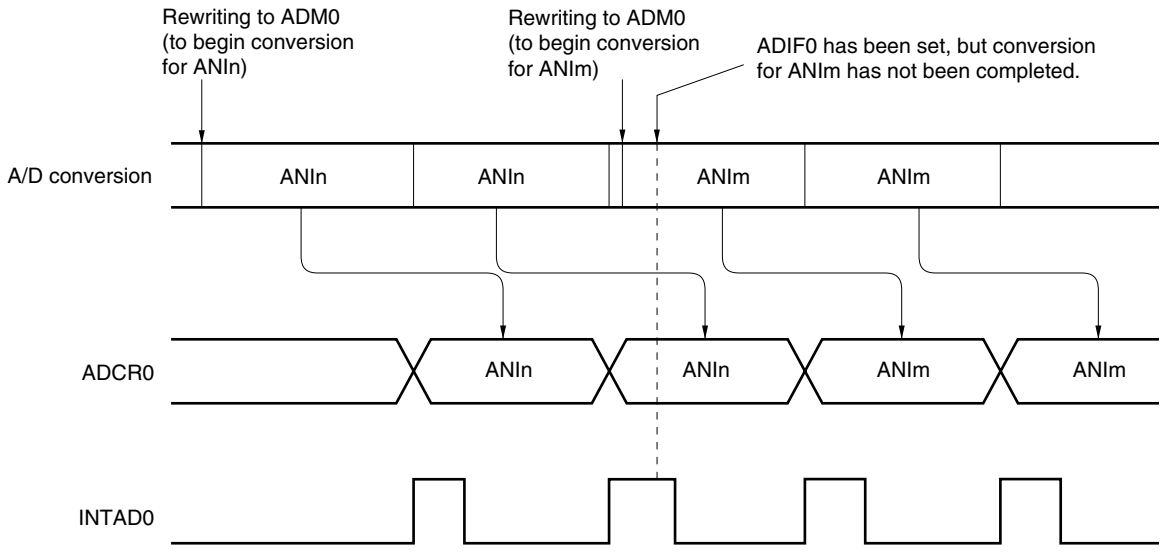
(9) Interrupt request flag (ADIF0)

Changing the contents of A/D converter mode register 0 (ADM0) does not clear the interrupt request flag (ADIF0).

If the analog input pins are changed during A/D conversion, therefore, the conversion result and the conversion end interrupt request flag may reflect the previous analog input immediately before writing to ADM0 occurs. In this case, ADIF0 may appear to be set if it is read-accessed immediately after ADM0 is write-accessed, even when A/D conversion has not been completed for the new analog input.

In addition, when A/D conversion is restarted, ADIF0 must be cleared beforehand.

Figure 12-11. A/D Conversion End Interrupt Request Generation Timing



Remarks 1. n = 0, 1, 2, 3

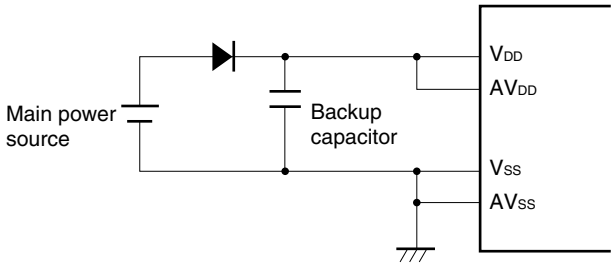
2. m = 0, 1, 2, 3

(10) AV_{DD} pin

The AV_{DD} pin is used to supply power to the analog circuit. It is also used to supply power to the ANI0 to ANI3 input circuit.

Therefore, if the application is designed to be changed to backup power, the AV_{DD} pin must be supplied with the same voltage level as for the V_{DD} pin, as shown in Figure 12-12.

Figure 12-12. AV_{DD} Pin Treatment



(11) Input impedance of the AV_{DD} pin

A series resistor string of several 10 kΩ is connected across the AV_{DD} and AV_{SS} pins.

Therefore, if the output impedance of the reference voltage source is high, this high impedance is eventually connected in parallel with the series resistor string across the AV_{DD} and AV_{SS} pins, leading to a higher reference voltage error.

CHAPTER 13 SERIAL INTERFACE 20

13.1 Functions of Serial Interface 20

Serial interface 20 has the following three modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode

(1) Operation stop mode

This mode is used when serial transfer is not performed. Power consumption is minimized in this mode.

(2) Asynchronous serial interface (UART) mode

This mode is used to transmit and receive the one byte of data that follows a start bit. It supports full-duplex communication.

Serial interface channel 0 contains a dedicated UART baud rate generator, enabling communication over a wide range of baud rates. It is also possible to define baud rates by dividing the frequency of the input clock pulse at the ASCK20 pin.

It is recommended that ceramic/crystal oscillation be used for the system clock in the UART mode. Because the frequency deviation is large in RC oscillation, if an internal clock is selected as the source clock for the baud rate generator, there may be problems in transmit/receive operations.

(3) 3-wire serial I/O mode (switchable between MSB-first and LSB-first transmission)

This mode is used to transmit 8-bit data, using three lines: a serial clock ($\overline{\text{SCK20}}$) line and two serial data lines (SI20 and SO20).

As it supports simultaneous transmission and reception, 3-wire serial I/O mode requires less processing time for data transmission than asynchronous serial interface mode.

Because, in 3-wire serial I/O mode, it is possible to select whether 8-bit data transmission begins with the MSB or LSB, channel 0 can be connected to any device regardless of whether that device is designed for MSB-first or LSB-first transmission.

3-wire serial I/O mode is useful for connecting peripheral I/O circuits and display controllers having conventional clocked serial interfaces, such as those of the 75XL, 78K, and 17K Series devices.

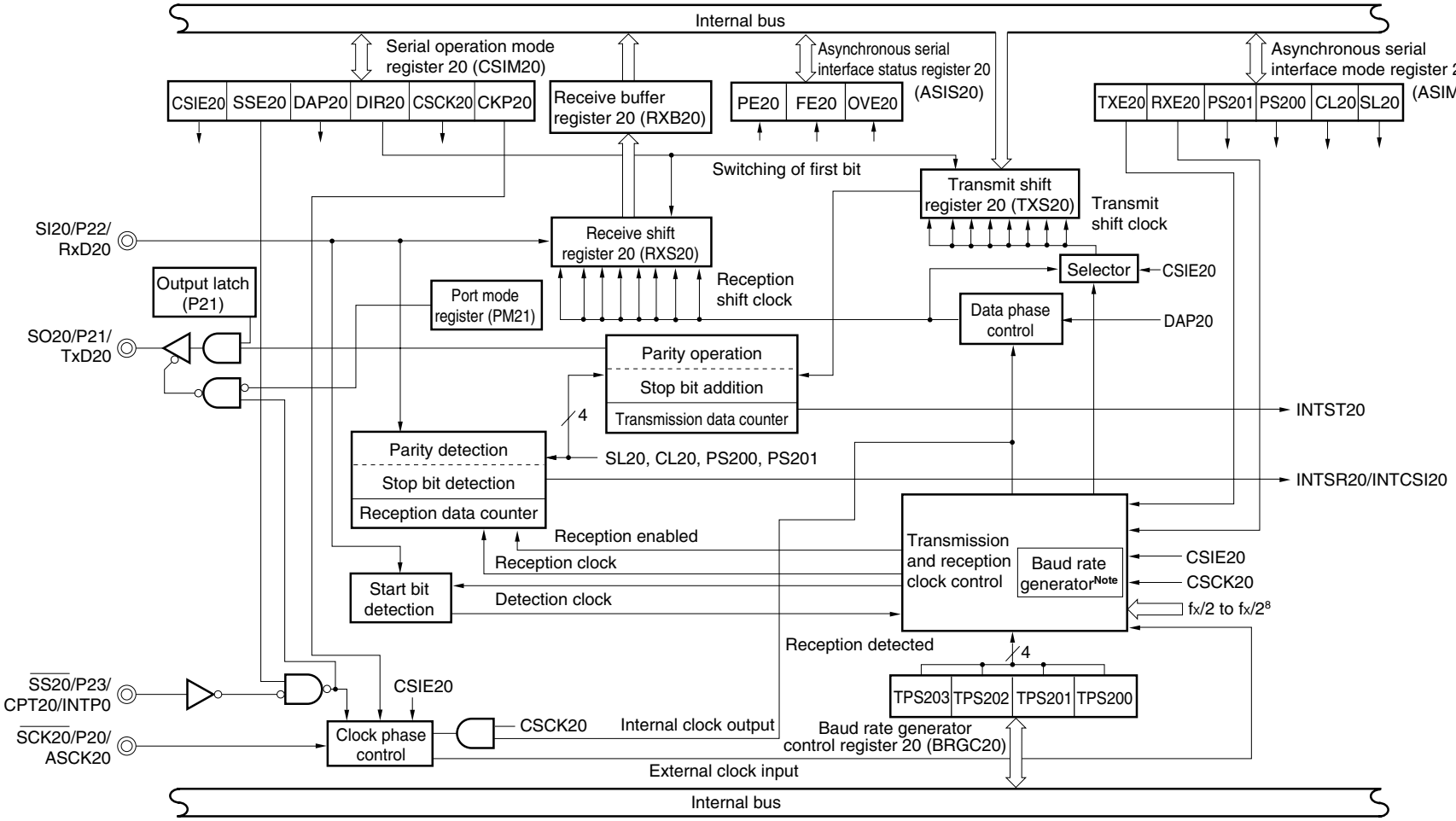
13.2 Serial Interface 20 Configuration

Serial interface 20 consists of the following hardware.

Table 13-1. Configuration of Serial Interface 20

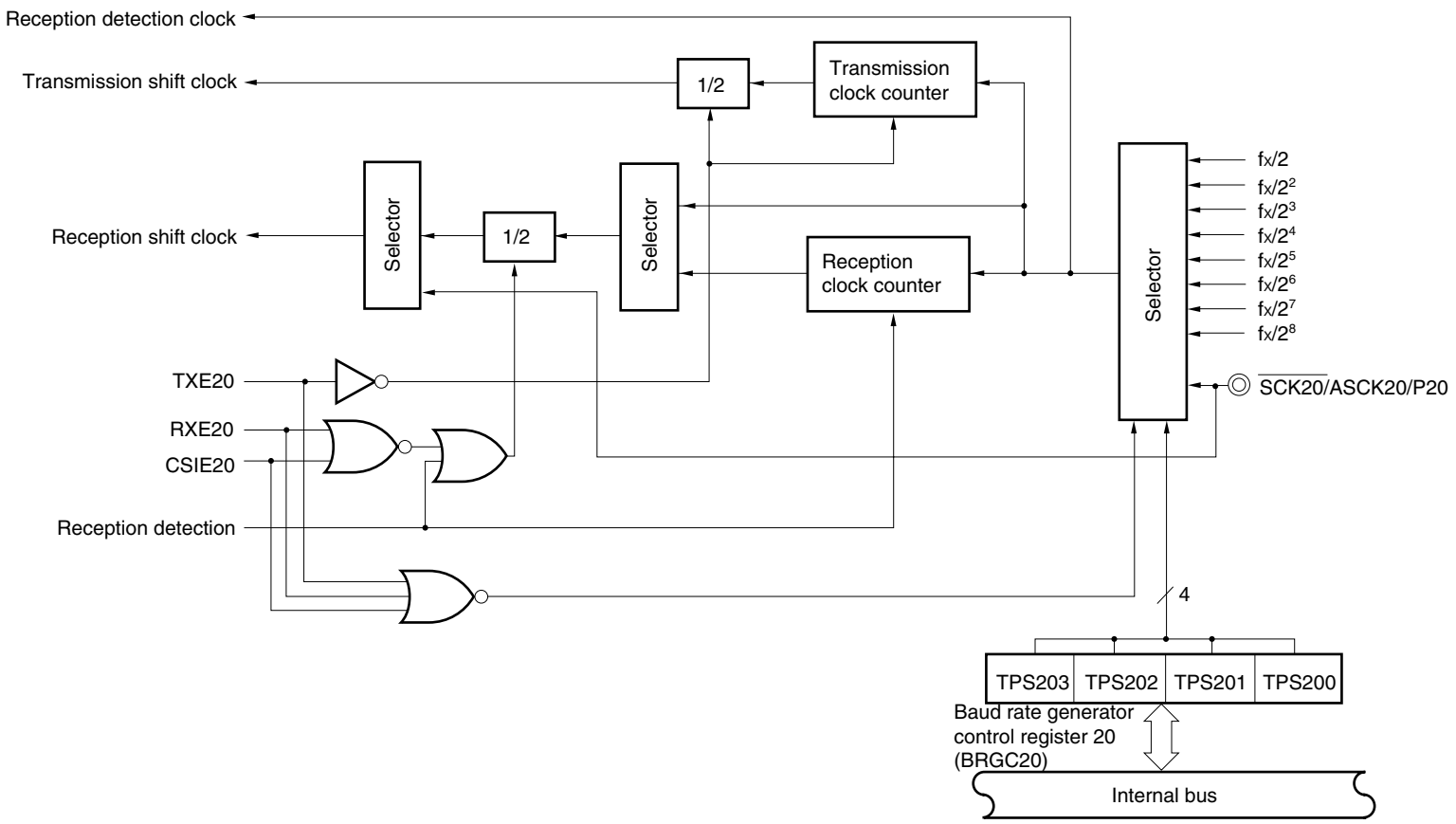
Item	Configuration
Registers	Transmit shift register 20 (TXS20) Receive shift register 20 (RXS20) Receive buffer register 20 (RXB20)
Control registers	Serial operating mode register 20 (CSIM20) Asynchronous serial interface mode register 20 (ASIM20) Asynchronous serial interface status register 20 (ASIS20) Baud rate generator control register 20 (BRGC20) Port mode register 2 (PM2) Port 2 (P2)

★**Figure 13-1. Block Diagram of Serial Interface 20**



Note Refer to **Figure 13-2** for the configuration of the baud rate generator.

Figure 13-2. Baud Rate Generator Block Diagram



(1) Transmit shift register 20 (TXS20)

TXS20 is a register in which transmit data is prepared. The transmit data is output from TXS20 bit-serially.

When the data length is seven bits, bits 0 to 6 of the data in TXS20 will be transmit data. Writing data to TXS20 triggers transmission.

TXS20 can be written with an 8-bit memory manipulation instruction, but cannot be read.

$\overline{\text{RESET}}$ input sets TXS20 to FFH.

Caution Do not write to TXS20 during transmission.

TXS20 and receive buffer register 20 (RXB20) are mapped at the same address, so that any attempt to read from TXS20 results in a value being read from RXB20.

(2) Receive shift register 20 (RXS20)

RXS20 is a register in which serial data, received at the RxD20 pin, is converted to parallel data. Once one entire byte has been received, RXS20 transfers the receive data to receive buffer register 20 (RXB20).

RXS20 cannot be manipulated directly by a program.

(3) Receive buffer register 20 (RXB20)

RXB20 holds receive data. New receive data is transferred from receive shift register 0 (RXS20) per 1 byte of data received.

When the data length is specified as seven bits, the receive data is sent to bits 0 to 6 of RXB20, in which the MSB is always fixed to 0.

RXB20 can be read with an 8-bit memory manipulation instruction, but cannot be written to.

$\overline{\text{RESET}}$ input makes RXB20 undefined.

Caution RXB20 and transmit shift register 20 (TXS20) are mapped at the same address, so that any attempt to write to RXB20 results in a value being written to TXS20.

(4) Transmission controller

The transmission controller controls transmission. For example, it adds start, parity, and stop bits to the data in transmit shift register 20 (TXS20), according to the setting of asynchronous serial interface mode register 20 (ASIM20).

(5) Reception controller

The reception controller controls reception according to the setting of asynchronous serial interface mode register 20 (ASIM20). It also checks for errors, such as parity errors, during reception. If an error is detected, asynchronous serial interface status register 20 (ASIS20) is set according to the status of the error.

13.3 Serial Interface 20 Control Registers

Serial interface 20 is controlled by the following six registers.

- Serial operating mode register 20 (CSIM20)
- Asynchronous serial interface mode register 20 (ASIM20)
- Asynchronous serial interface status register 20 (ASIS20)
- Baud rate generator control register 20 (BRGC20)
- Port mode register 2 (PM2)
- Port 2 (P2)

(1) Serial operating mode register 20 (CSIM20)

CSIM20 is used to make the settings related to 3-wire serial I/O mode.

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM20 to 00H.

Figure 13-3. Format of Serial Operating Mode Register 20

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	3-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

SSE20	$\overline{SS20}$-pin selection	Function of $\overline{SS20}$/P23 pin	Communication status
0	Not used	Port function	Communication enabled
1	Used	0	Communication enabled
		1	Communication disabled

DAP20	3-wire serial I/O mode data phase selection
0	Output at falling edge of $\overline{SCK20}$
1	Output at rising edge of $\overline{SCK20}$

DIR20	First-bit specification
0	MSB
1	LSB

CSCK20	3-wire serial I/O mode clock selection
0	External clock pulse input to $\overline{SCK20}$ pin
1	Output of dedicated baud rate generator

CKP20	3-wire serial I/O mode clock phase selection
0	Clock is active low, and $\overline{SCK20}$ is at high level in the idle state
1	Clock is active high, and $\overline{SCK20}$ is at low level in the idle state

Cautions 1. Bits 4 and 5 must be fixed to 0.

2. CSIM20 must be cleared to 00H if UART mode is selected.

(2) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is used to make the settings related to asynchronous serial interface mode.

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Figure 13-4. Format of Asynchronous Serial Interface Mode Register 20

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stop
1	Transmit operation enable

RXE20	Receive operation control
0	Receive operation stop
1	Receive operation enable

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (no parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Transmit data character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length
0	1 bit
1	2 bits

Cautions 1. Bits 0 and 1 must be fixed to 0.

2. If 3-wire serial I/O mode is selected, ASIM20 must be cleared to 00H.

3. Switch operating modes after halting the serial transmit/receive operation.

Table 13-2. Serial Interface 20 Operating Mode Settings

(1) Operation stopped mode

ASIM20		CSIM20			PM22	P21	PM21	P21	PM20	P20	First Bit	Shift Clock	P22/SI20/RxD20 Pin Function	P21/SO20/TxD20 Pin Function	P20/$\overline{\text{SCK20}}$/ ASCK20 Pin Function
TXE20	RXE20	CSIE20	DIR20	CSCK20											
0	0	0	×	×	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	×Note 1	–	–	P22	P21	P20
Other than above											Setting prohibited				

(2) 3-wire serial I/O mode

ASIM20		CSIM20			PM22	P21	PM21	P21	PM20	P20	First Bit	Shift Clock	P22/SI20/RxD20 Pin Function	P21/SO20/TxD20 Pin Function	P20/$\overline{\text{SCK20}}$/ ASCK20 Pin Function
TXE20	RXE20	CSIE20	DIR20	CSCK20											
0	0	1	0	0	×Note 1	×Note 2	0	1	1	×	MSB	External clock	SI20Note 2	SCK20(CMOS output)	$\overline{\text{SCK20}}$ input
				1					0	1		Internal clock			$\overline{\text{SCK20}}$ output
		1	1	0					1	×	LSB	External clock			$\overline{\text{SCK20}}$ input
				1					0	1		Internal clock			$\overline{\text{SCK20}}$ output
Other than above											Setting prohibited				

(3) Asynchronous serial interface mode

ASIM20		CSIM20			PM22	P21	PM21	P21	PM20	P20	First Bit	Shift Clock	P22/SI20/RxD20 Pin Function	P21/SO20/TxD20 Pin Function	P20/$\overline{\text{SCK20}}$/ ASCK20 Pin Function
TXE20	RXE20	CSIE20	DIR20	CSCK20											
1	0	0	0	0	×Note 1	×Note 1	0	1	1	×	LSB	External clock	P22	TxD20 (CMOS output)	ASCK20 input
									×Note 1	×Note 1		Internal clock			P20
0	1	0	0	0	1	×	×Note 1	×Note 1	1	×		External clock	RD20	P21	ASCK20 input
									×Note 1	×Note 1		Internal clock			P20
1	1	0	0	0	1	×	0	1	1	×		External clock		TxD20 (CMOS output)	ASCK20 input
									×Note 1	×Note 1		Internal clock			P20
Other than above											Setting prohibited				

Notes 1. These pins can be used for port functions.

2. When only transmission is used, these pins can be used as P22 (CMOS I/O).

Remark ×: don't care.

(3) Asynchronous serial interface status register 20 (ASIS20)

ASIS20 is used to display the type of a reception error, if it occurs while asynchronous serial interface mode is set.

ASIS20 is read with a 1-bit or 8-bit memory manipulation instruction.

The contents of ASIS20 are undefined in 3-wire serial I/O mode.

$\overline{\text{RESET}}$ input clears ASIS20 to 00H.

Figure 13-5. Format of Asynchronous Serial Interface Status Register 20

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASIS20	0	0	0	0	0	PE20	FE20	OVE20	FF71H	00H	R

PE20	Parity error flag
0	No parity error has occurred.
1	A parity error has occurred (when the transmission parity and reception parity do not match).

FE20	Framing error flag
0	No framing error has occurred.
1	A framing error has occurred (when no stop bit is detected).Note 1

OVE20	Overrun error flag
0	No overrun error has occurred.
1	An overrun error has occurred.Note 2 (Before data was read from the reception buffer register, the subsequent reception sequence was completed.)

Notes 1. Even when the stop bit length is set to 2 bits by setting bit 2 (SL20) of asynchronous serial interface mode register 20 (ASIM20), the stop bit detection in the case of reception is performed with 1 bit.

2. Be sure to read receive buffer register 20 (RXB20) when an overrun error occurs. If not, every time the data is received an overrun error will occur.

(4) Baud rate generator control register 20 (BRGC20)

BRGC20 is used to specify the serial clock for the serial interface.

BRGC20 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BRGC20 to 00H.

★ **Figure 13-6. Format of Baud Rate Generator Control Register 20**

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BRGC20	TPS203	TPS202	TPS201	TPS200	0	0	0	0	FF73H	00H	R/W

TPS203	TPS202	TPS201	TPS200	Selection of source clock for baud rate generator			n
					@ f_X = 10.0 MHz[Note 1] operation	@ f_X = 5.0 MHz operation	
0	0	0	0	$f_X/2$	5.0 MHz	2.5 MHz	1
0	0	0	1	$f_X/2^2$	2.5 MHz	1.25 MHz	2
0	0	1	0	$f_X/2^3$	1.25 MHz	625 kHz	3
0	0	1	1	$f_X/2^4$	625 kHz	313 kHz	4
0	1	0	0	$f_X/2^5$	313 kHz	156 kHz	5
0	1	0	1	$f_X/2^6$	156 kHz	78.1 kHz	6
0	1	1	0	$f_X/2^7$	78.1 kHz	39.1 kHz	7
0	1	1	1	$f_X/2^8$	39.1 kHz	19.5 kHz	8
1	0	0	0	External clock pulse input at the ASCK20 pin[Note 2]			–
Other than above				Setting prohibited			

Notes 1. Expanded-specification products only

2. An external clock can only be used in UART mode.

Cautions 1. When writing to BRGC20 is performed during a communication operation, the output of baud rate generator is disrupted and communications cannot be performed normally. Be sure not to write to BRGC20 during communication operations.

2. Be sure not to select n = 1 when f_X > 2.5 MHz in UART mode because n = 1 exceeds the rating of the baud rate.

3. Be sure not to select n = 2 when f_X > 5.0 MHz in UART mode because n = 2 exceeds the rating of the baud rate.

4. Be sure not to select n = 1 when f_X > 5.0 MHz in 3-wire serial I/O mode because n = 1 exceeds the rating of the serial clock.

5. When the external input clock is selected, set port mode register 2 (PM2) in input mode.

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. n: Value specified in TPS200 to TPS203 ($1 \leq n \leq 8$)

The baud rate transmit/receive clock to be generated is either a signal divided from the system clock, or a signal divided from the clock input from the ASCK20 pin.

(a) Generation of baud rate UART transmit/receive clock by means of system clock

The transmit/receive clock is generated by dividing the system clock. The baud rate generated from the system clock is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_X}{2^{n+1} \times 8} \text{ [bps]}$$

f_X: System clock oscillation frequency (ceramic/crystal oscillation)

n: Values in Figure 13-6 specified by the setting in TPS200 to TPS203 ($2 \leq n \leq 8$)

★ **Table 13-3. Example of Relationship Between System Clock and Baud Rate**

Baud Rate (bps)	f_X = 10.0 MHz[Note]			f_X = 5.0 MHz			f_X = 4.9152 MHz		
	n	BRGC20 Setting	Error (%)	n	BRGC20 Setting	Error (%)	n	BRGC20 Setting	Error (%)
1,200	–	–	1.73	8	70H	1.73	8	70H	0
2,400	8	70H		7	60H		7	60H	
4,800	7	60H		6	50H		6	50H	
9,600	6	50H		5	40H		5	40H	
19,200	5	40H		4	30H		4	30H	
38,400	4	30H		3	20H		3	20H	
76,800	3	20H		2	10H		2	10H	

Note Expanded-specification products only.

Cautions 1. Be sure not to select n = 1 when f_X > 2.5 MHz because n = 1 exceeds the rating of the baud rate.

2. Be sure not to select n = 2 when f_X > 5.0 MHz because n = 2 exceeds the rating of the baud rate.

(b) Generation of baud rate UART transmit/receive clock by means of external clock from ASCK20 pin

The transmit/receive clock is generated by dividing the clock input from the ASCK20 pin. The baud rate generated from the clock input from the ASCK20 pin is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_{ASCK}}{16} \text{ [bps]}$$

f_{ASCK}: Frequency of clock pulse received at the ASCK20 pin

Table 13-4. Relationship Between ASCK20 Pin Input Frequency and Baud Rate (When BRGC20 Is Set to 80H)

Baud Rate (bps)	ASCK20 Pin Input Frequency (kHz)
75	1.2
150	2.4
300	4.8
600	9.6
1,200	19.2
2,400	38.4
4,800	76.8
9,600	153.6
19,200	307.2
31,250	500.0
38,400	614.4

★ **(c) Generation of serial clock from system clock in 3-wire serial I/O mode**

The serial clock is generated by dividing the system clock. The serial clock frequency is estimated by using the following expression. BRGC20 does not need to be set when an external serial clock is input to the $\overline{SCK20}$ pin.

$$\text{Serial clock frequency} = \frac{f_X}{2^{n+1}} \text{ [Hz]}$$

f_X: System clock oscillation frequency

n: Value determined by the settings of TPS200 to TPS203 as shown in Figure 13-6 ($1 \leq n \leq 8$)

13.4 Operation of Serial Interface 20

Serial interface 20 provides the following three modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode

13.4.1 Operation stop mode

In the operation stop mode, serial transfer is not executed; therefore, the power consumption can be reduced. The P20/$\overline{\text{SCK20}}$/ASCK20, P21/SO20/TxD20, and P22/SI20/RxD20 pins can be used as normal I/O port pins.

(1) Register setting

Operation stop mode is set by serial operating mode register 20 (CSIM20) and asynchronous serial interface mode register 20 (ASIM20).

(a) Serial operating mode register 20 (CSIM20)

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM20 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	Operation control in 3-wire serial I/O mode
0	Operation disabled
1	Operation enabled

Caution Be sure to clear bits 4 and 5 to 0.

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

RXE20	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

Caution Be sure to clear bits 0 and 1 to 0.

13.4.2 Asynchronous serial interface (UART) mode

In this mode, the one-byte data following the start bit is transmitted/received and thus full-duplex communication is possible.

This device incorporates a UART-dedicated baud rate generator that enables communication at the desired transfer rate from many options. In addition, the baud rate can also be defined by dividing the clock input to the ASCK pin.

The UART-dedicated baud rate generator also can output the 31.25 kbps baud rate that complies with the MIDI standard.

It is recommended that ceramic/crystal oscillation be used for the system clock in the UART mode. Because the frequency deviation is large in RC oscillation, if an internal clock is selected as the source clock for the baud rate generator, there may be problems in transmit/receive operations.

(1) Register setting

The UART mode is set by serial operating mode register 20 (CSIM20), asynchronous serial interface mode register 20 (ASIM20), asynchronous serial interface status register 20 (ASIS20), baud rate generator control register 20 (BRGC20), port mode register 2 (PM2), and port 2 (P2).

(a) Serial operating mode register 20 (CSIM20)

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears CSIM20 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	3-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

SSE20	$\overline{\text{SS20}}$-pin selection	Function of $\overline{\text{SS20}}$/P23 pin	Communication status
0	Not used	Port function	Communication enabled
1	Used	0	Communication enabled
		1	Communication disabled

DAP20	3-wire serial I/O mode data phase selection
0	Output at falling edge of $\overline{\text{SCK20}}$
1	Output at rising edge of $\overline{\text{SCK20}}$

DIR20	First-bit specification
0	MSB
1	LSB

CSCK20	3-wire serial I/O mode clock selection
0	External clock pulse input to $\overline{\text{SCK20}}$ pin
1	Output of dedicated baud rate generator

CKP20	3-wire serial I/O mode clock phase selection
0	Clock is active low, and $\overline{\text{SCK20}}$ is high level in the idle state
1	Clock is active high, and $\overline{\text{SCK20}}$ is low level in the idle state

Cautions 1. Bits 4 and 5 must be fixed to 0.

★ **2. When UART mode is selected, clear CSIM20 to 00H.**

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

RXE20	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (no parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length specification
0	1 bit
1	2 bits

Cautions 1. Be sure to clear bits 0 and 1 to 0.

2. Switch operating modes after halting the serial transmit/receive operation.

(c) Asynchronous serial interface status register 20 (ASIS20)

ASIS20 is read with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIS20 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASIS20	0	0	0	0	0	PE20	FE20	OVE20	FF71H	00H	R

PE20	Parity error flag
0	No parity error has occurred.
1	A parity error has occurred (when the transmission parity and reception parity do not match).

FE20	Framing error flag
0	No framing error has occurred.
1	A framing error has occurred (when no stop bit is detected).[Note 1]

OVE20	Overrun error flag
0	No overrun error has occurred.
1	An overrun error has occurred.[Note 2] (Before data was read from the reception buffer register, the subsequent reception sequence was completed.)

Notes 1. Even when the stop bit length is set to 2 bits by setting bit 2 (SL20) of asynchronous serial interface mode register 20 (ASIM20), the stop bit detection in the case of reception is performed with 1 bit.

2. Be sure to read receive buffer register 20 (RXB20) when an overrun error occurs. If not, every time the data is received an overrun error will occur.

(d) Baud rate generator control register 20 (BRGC20)

BRGC20 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BRGC20 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BRGC20	TPS203	TPS202	TPS201	TPS200	0	0	0	0	FF73H	00H	R/W

★

TPS203	TPS202	TPS201	TPS200	Selection of source clock for baud rate generator			n
					@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation	
0	0	0	0	$f_X/2$	5.0 MHz	2.5 MHz	1
0	0	0	1	$f_X/2^2$	2.5 MHz	1.25 MHz	2
0	0	1	0	$f_X/2^3$	1.25 MHz	625 kHz	3
0	0	1	1	$f_X/2^4$	625 kHz	313 kHz	4
0	1	0	0	$f_X/2^5$	313 kHz	156 kHz	5
0	1	0	1	$f_X/2^6$	156 kHz	78.1 kHz	6
0	1	1	0	$f_X/2^7$	78.1 kHz	39.1 kHz	7
0	1	1	1	$f_X/2^8$	39.1 kHz	19.5 kHz	8
1	0	0	0	External clock input to ASCK20 pin			–
Other than above				Setting prohibited			

Note Expanded-specification products only

Cautions 1. When writing to BRGC20 is performed during a communication operation, the output of baud rate generator is disrupted and communications cannot be performed normally. Be sure not to write to BRGC20 during communication operations.

2. Be sure not to select n = 1 when f_X > 2.5 MHz because n = 1 exceeds the rating of the baud rate.

3. Be sure not to select n = 2 when f_X > 5.0 MHz because n = 2 exceeds the rating of the baud rate.

4. When the external input clock is selected, set port mode register 2 (PM2) to input mode.

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. n: Values specified by the setting in TPS200 to TPS203 ($1 \leq n \leq 8$)

The baud rate transmit/receive clock to be generated is either a signal divided from the system clock, or a signal divided from the clock input from the ASCK20 pin.

(i) Generation of baud rate transmit/receive clock by means of system clock

The transmit/receive clock is generated by dividing the system clock. The baud rate generated from the system clock is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_X}{2^{n+1} \times 8} \text{ [bps]}$$

f_X: System clock oscillation frequency (ceramic/crystal oscillation)

n: Values in the above table specified by the setting in TPS200 to TPS203 ($2 \leq n \leq 8$)

★ **Table 13-5. Example of Relationship Between System Clock and Baud Rate**

Baud Rate (bps)	f_X = 10.0 MHz[Note]			f_X = 5.0 MHz			f_X = 4.9152 MHz		
	n	BRGC20 Setting	Error (%)	n	BRGC20 Setting	Error (%)	n	BRGC20 Setting	Error (%)
1,200	–	–	1.73	8	70H	1.73	8	70H	0
2,400	8	70H		7	60H		7	60H	
4,800	7	60H		6	50H		6	50H	
9,600	6	50H		5	40H		5	40H	
19,200	5	40H		4	30H		4	30H	
38,400	4	30H		3	20H		3	20H	
76,800	3	20H		2	10H		2	10H	

Note Expanded-specification products only.

Cautions 1. Be sure not to select n = 1 when f_X > 2.5 MHz because n = 1 exceeds the rating of the baud rate.

2. Be sure not to select n = 2 when f_X > 5.0 MHz because n = 2 exceeds the rating of the baud rate.

(ii) Generation of baud rate transmit/receive clock by means of external clock from ASCK20 pin

The transmit/receive clock is generated by dividing the clock input from the ASCK20 pin. The baud rate generated from the clock input from the ASCK20 pin is estimated by using the following expression.

$$[\text{Baud rate}] = \frac{f_{ASCK}}{16} \text{ [bps]}$$

f_{ASCK}: Frequency of clock input to ASCK20 pin

Table 13-6. Relationship Between ASCK20 Pin Input Frequency and Baud Rate (When BRGC20 Is Set to 80H)

Baud Rate (bps)	ASCK20 Pin Input Frequency (kHz)
75	1.2
150	2.4
300	4.8
600	9.6
1,200	19.2
2,400	38.4
4,800	76.8
9,600	153.6
19,200	307.2
31,250	500.0
38,400	614.4

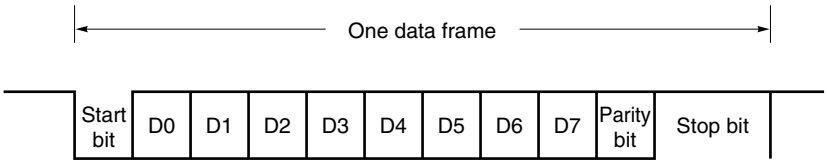
(2) Communication operation

(a) Data format

The transmit/receive data format is as shown in Figure 13-7. One data frame consists of a start bit, character bits, parity bit and stop bit(s).

The specification of character bit length, parity selection, and specification of stop bit length for each data frame is carried out using asynchronous serial interface mode register 20 (ASIM20).

Figure 13-7. Asynchronous Serial Interface Transmit/Receive Data Format



- Start bits ..... 1 bit
- Character bits..... 7 bits/8 bits
- Parity bits..... Even parity/odd parity/0 parity/no parity
- Stop bits ..... 1 bit/2 bits

When 7 bits is selected as the number of character bits, only the lower 7 bits (bits 0 to 6) are valid; in transmission the most significant bit (bit 7) is ignored, and in reception the most significant bit (bit 7) is always “0”.

The serial transfer rate is selected by baud rate generator control register 20 (BRGC20).

If a serial data receive error occurs, the receive error contents can be determined by reading the status of asynchronous serial interface status register 20 (ASIS20).

(b) Parity types and operation

The parity bit is used to detect a bit error in the communication data. Normally, the same kind of parity bit is used on the transmitting side and the receiving side. With even parity and odd parity, a "1" bit (odd number) error can be detected. With 0 parity and no parity, an error cannot be detected.

(i) Even parity

- **At transmission**

  The transmission operation is controlled so that the number of bits with a value of "1" in the transmit data including parity bit is even. The parity bit value should be as follows.

  The number of bits with a value of "1" is an odd number in transmit data: 1
  The number of bits with a value of "1" is an even number in transmit data: 0

- **At reception**

  The number of bits with a value of "1" in the receive data including parity bit is counted, and if the number is odd, a parity error is generated.

(ii) Odd parity

- **At transmission**

  Opposite to even parity, the transmission operation is controlled so that the number of bits with a value of "1" in the transmit data including parity bit is odd. The parity bit value should be as follows.

  The number of bits with a value of "1" is an odd number in transmit data: 0
  The number of bits with a value of "1" is an even number in transmit data: 1

- **At reception**

  The number of bits with a value of "1" in the receive data including parity bit is counted, and if the number is even, a parity error is generated.

(iii) 0 Parity

When transmitting, the parity bit is set to "0" irrespective of the transmit data.
At reception, a parity bit check is not performed. Therefore, a parity error does not occur, irrespective of whether the parity bit is set to "0" or "1".

(iv) No parity

A parity bit is not added to the transmit data. At reception, data is received assuming that there is no parity bit. Since there is no parity bit, a parity error does not occur.

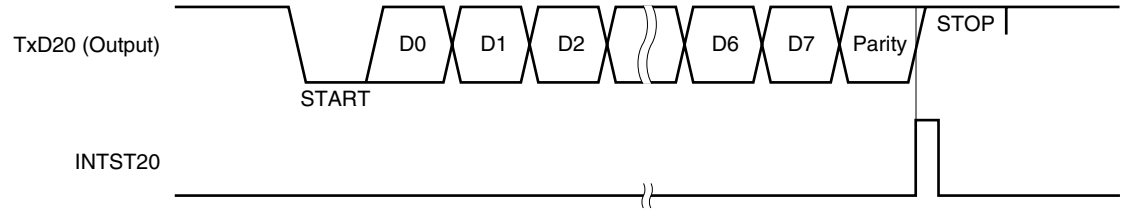
(c) Transmission

A transmit operation is started by writing transmit data to transmit shift register 20 (TXS20). The start bit, parity bit and stop bit(s) are added automatically.

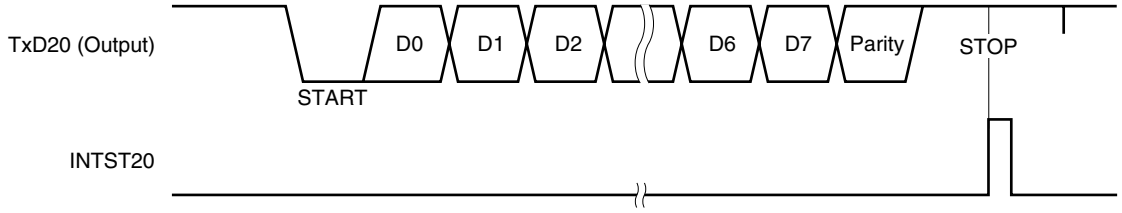
When the transmit operation starts, the data in TXS20 is shifted out, and when TXS20 is empty, a transmission completion interrupt (INTST20) is generated.

Figure 13-8. Asynchronous Serial Interface Transmission Completion Interrupt Timing

(a) Stop bit length: 1



(b) Stop bit length: 2



Caution Do not rewrite asynchronous serial interface mode register 20 (ASIM20) during a transmit operation. If the ASIM20 register is rewritten during transmission, subsequent transmission may not be performed (the normal state is restored by $\overline{\text{RESET}}$ input).

It is possible to determine whether transmission is in progress by software by using a transmission completion interrupt (INTST20) or the interrupt request flag (STIF20) set by INTST20.

(d) Reception

When bit 6 (RXE20) of asynchronous serial interface mode register 20 (ASIM20) is set (1), a receive operation is enabled and sampling of the RxD20 pin input is performed.

RxD20 pin input sampling is performed using the serial clock specified by BRGC20.

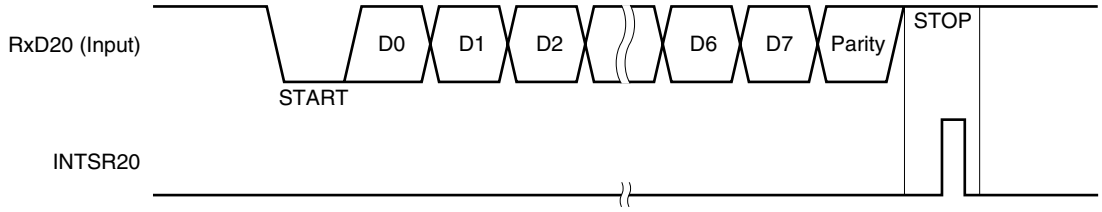
When the RxD20 pin input becomes low, the 3-bit counter starts counting, and when half the time determined by the specified baud rate has passed, the data sampling start timing signal is output. If the RxD20 pin input sampled again as a result of this start timing signal is low, it is identified as a start bit, the 3-bit counter is initialized and starts counting, and data sampling is performed. When character data, a parity bit and one stop bit are detected after the start bit, reception of one frame of data ends.

When one frame of data has been received, the receive data in the shift register is transferred to receive buffer register 20 (RXB20), and a reception completion interrupt (INTSR20) is generated.

If an error occurs, the receive data in which the error occurred is still transferred to RXB20, and INTSR20 is generated.

If the RXE20 bit is reset (0) during the receive operation, the receive operation is stopped immediately. In this case, the contents of RXB20 and asynchronous serial interface status register 20 (ASIS20) are not changed, and INTSR20 is not generated.

Figure 13-9. Asynchronous Serial Interface Reception Completion Interrupt Timing



Caution Be sure to read receive buffer register 20 (RXB20) even if a receive error occurs. If RXB20 is not read, an overrun error will occur when the next data is received, and the receive error state will continue indefinitely.

(e) Receive errors

The following three errors may occur during a receive operation: a parity error, framing error, or overrun error. The data reception result error flag is set in asynchronous serial interface status register 20 (ASIS20). Receive error causes are shown in Table 13-7.

It is possible to determine what kind of error occurred during reception by reading the contents of ASIS20 in the reception error interrupt servicing (refer to **Table 13-7** and **Figure 13-10**).

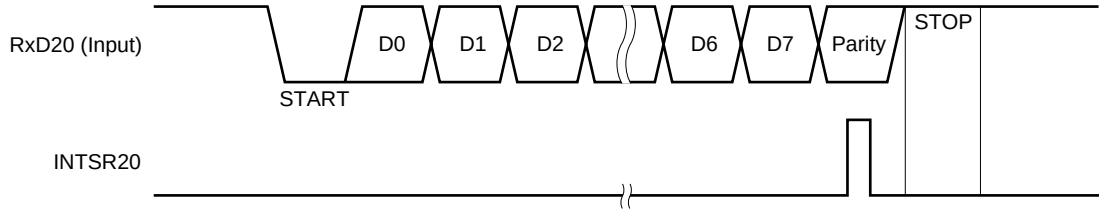
The contents of ASIS20 are reset (0) by reading receive buffer register 20 (RXB20) or receiving the next data (if there is an error in the next data, the corresponding error flag is set).

Table 13-7. Receive Error Causes

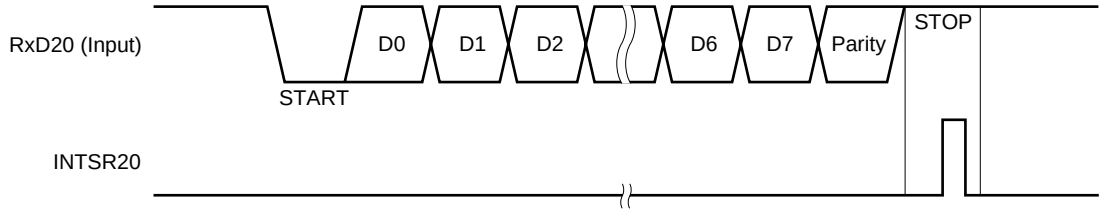
Receive Errors	Cause
Parity error	Transmission-time parity specification and receive data parity do not match
Framing error	Stop bit not detected
Overrun error	Reception of next data is completed before data is read from receive register buffer

Figure 13-10. Receive Error Timing

(a) Parity error occurred



(b) Framing error or overrun error occurred



Cautions 1. The contents of the ASIS20 register are reset (0) by reading receive buffer register 20 (RXB20) or receiving the next data. To ascertain the error contents, read ASIS20 before reading RXB20.

2. Be sure to read receive buffer register 20 (RXB20) even if a receive error occurs. If RXB20 is not read, an overrun error will occur when the next data is received, and the receive error state will continue indefinitely.

★ **(f) Reading receive data**

When the reception completion interrupt (INTSR20) occurs, receive data can be read by reading the value of receive buffer register 20 (RXB20).

To read the receive data stored in receive buffer register 20 (RXB20), read while reception is enabled (RXE20 = 1).

Remark However, if it is necessary to read receive data after reception has stopped (RXE20 = 0), read using either of the following methods.

(a) Read after setting RXE20 = 0 after waiting for one cycle or more of the source clock selected by BRGC20.
(b) Read after bit 2 (DIR20) of serial operating mode register 20 (CSIM20) is set (1).

Program example of (a) (BRGC20 = 00H (source clock = $f_X/2$))

```
INTRXE:                 ;<Reception completion interrupt routine>
        NOP             ;2 clocks
        CLR1 RXE20      ;Reception stopped
        MOV  A, RXB20   ;Read receive data
```

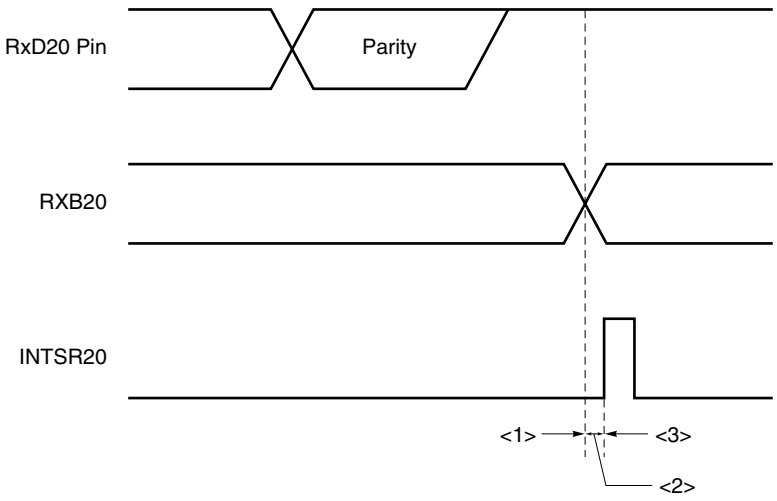
Program example of (b)

```
INTRXE:                 ;<Reception completion interrupt routine>
        SET1 CSIM20.2   ;DIR20 flag is set to LSB first
        CLR1 RXE20      ;Reception stopped
        MOV  A, RXB20   ;Read receive data
```

(3) UART mode cautions

(a) When bit 7 (TXE20) of asynchronous serial interface mode register 20 (ASIM20) is cleared during transmission, be sure to set transmit shift register 20 (TXS20) to FFH, then set TXE20 to 1 before executing the next transmission.

(b) When bit 6 (RXE20) of asynchronous serial interface mode register 20 (ASIM20) is cleared during reception, receive buffer register 20 (RXB20) and receive completion interrupt 20 (INTSR20) are as follows.



When RXE20 is set to 0 at the time indicated by <1>, RXB20 holds the previous data and does not generate INTSR20.
When RXE20 is set to 0 at the time indicated by <2>, RXB20 renews the data and does not generate INTSR20.
When RXE20 is set to 0 at the time indicated by <3>, RXB20 renews the data and generates INTSR20.

13.4.3 3-wire serial I/O mode

The 3-wire serial I/O mode is useful for connection of peripheral I/Os and display controllers, etc. that incorporate a conventional clocked serial interface, such as the 75XL Series, 78K Series, and 17K Series.

Communication is performed using three lines: the serial clock ($\overline{SCK20}$), serial output (SO20), and serial input (SI20).

(1) Register setting

3-wire serial I/O mode settings are performed using serial operating mode register 20 (CSIM20), asynchronous serial interface mode register 20 (ASIM20), baud rate generator control register 20 (BRGC20), port mode register 2 (PM2), and port 2 (P2).

(a) Serial operating mode register 20 (CSIM20)

CSIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{RESET}$ input clears CSIM20 to 00H.

Symbol	<7>	6	5	4	3	2	1	0	Address	After reset	R/W
CSIM20	CSIE20	SSE20	0	0	DAP20	DIR20	CSCK20	CKP20	FF72H	00H	R/W

CSIE20	3-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

SSE20	$\overline{SS20}$-pin selection	Function of $\overline{SS20}$/P23 pin	Communication status
0	Not used	Port function	Communication enabled
1	Used	0	Communication enabled
		1	Communication disabled

DAP20	3-wire serial I/O mode data phase selection
0	Output at falling edge of $\overline{SCK20}$
1	Output at rising edge of $\overline{SCK20}$

DIR20	First-bit specification
0	MSB
1	LSB

CSCK20	3-wire serial I/O mode clock selection
0	External clock pulse input to $\overline{SCK20}$ pin
1	Output of dedicated baud rate generator

CKP20	3-wire serial I/O mode clock phase selection
0	Clock is active low, and $\overline{SCK20}$ is at high level in the idle state
1	Clock is active high, and $\overline{SCK20}$ is at low level in the idle state

Caution Bits 4 and 5 must be fixed to 0.

(b) Asynchronous serial interface mode register 20 (ASIM20)

ASIM20 is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears ASIM20 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM20	TXE20	RXE20	PS201	PS200	CL20	SL20	0	0	FF70H	00H	R/W

TXE20	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

RXE20	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

PS201	PS200	Parity bit specification
0	0	No parity
0	1	Always add 0 parity at transmission. Parity check is not performed at reception (no parity error is generated).
1	0	Odd parity
1	1	Even parity

CL20	Character length specification
0	7 bits
1	8 bits

SL20	Transmit data stop bit length specification
0	1 bit
1	2 bits

Cautions 1. Be sure to clear bits 0 and 1 to 0.

2. When the 3-wire serial I/O mode is selected, ASIM20 must be cleared to 00H.

3. Switching operation modes must be performed after the serial transmit/receive operation is halted.

(c) Baud rate generator control register 20 (BRGC20)

BRGC20 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears BRGC20 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
BRGC20	TPS203	TPS202	TPS201	TPS200	0	0	0	0	FF73H	00H	R/W

★

TPS203	TPS202	TPS201	TPS200	Selection of source clock for baud rate generator			n
					@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation	
0	0	0	0	$f_X/2$	5.0 MHz	2.5 MHz	1
0	0	0	1	$f_X/2^2$	2.5 MHz	1.25 MHz	2
0	0	1	0	$f_X/2^3$	1.25 MHz	625 kHz	3
0	0	1	1	$f_X/2^4$	625 kHz	313 kHz	4
0	1	0	0	$f_X/2^5$	313 kHz	156 kHz	5
0	1	0	1	$f_X/2^6$	156 kHz	78.1 kHz	6
0	1	1	0	$f_X/2^7$	78.1 kHz	39.1 kHz	7
0	1	1	1	$f_X/2^8$	39.1 kHz	19.5 kHz	8
Other than above				Setting prohibited			

Note Expanded-specification products only

Cautions 1. When writing to BRGC20 is performed during a communication operation, the baud rate generator output is disrupted and communication cannot be performed normally. Be sure not to write to BRGC20 during communication operations.

★ **2. Be sure not to select n = 1 when f_X > 5.0 MHz in 3-wire serial I/O mode because n = 1 exceeds the rating of the serial clock.**

Remarks 1. f_X: System clock oscillation frequency (ceramic/crystal oscillation)

2. n: Values specified by TPS200 to TPS203 ($1 \leq n \leq 8$)

If the internal clock is used as the serial clock for the 3-wire serial I/O mode, set the TPS200 to TPS203 bits to set the frequency of the serial clock. To obtain the frequency to be set, use the following formula. When the serial clock is input from off-chip, setting BRGC20 is not necessary.

$$\text{Serial clock frequency} = \frac{f_X}{2^{n+1}} \text{ [Hz]}$$

f_X: System clock oscillation frequency (ceramic/crystal oscillation)

n: Values in the above table specified by the setting in TPS200 to TPS203 ($1 \leq n \leq 8$)

(2) Communication operation

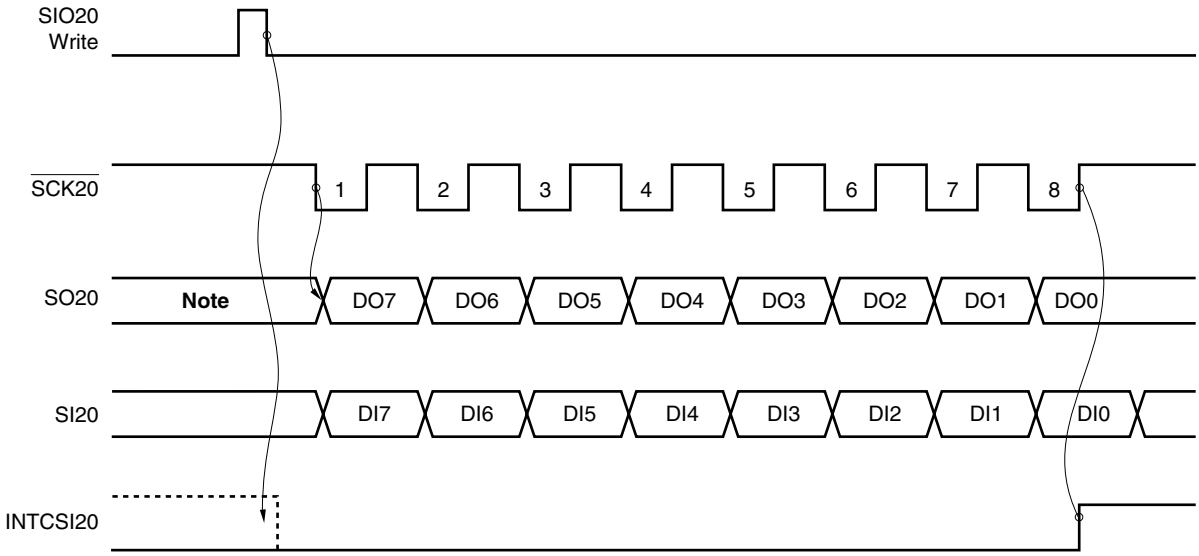
In the 3-wire serial I/O mode, data transmission/reception is performed in 8-bit units. Data is transmitted/received bit by bit in synchronization with the serial clock.

The transmit shift register (TXS20/SIO20) and receive shift register (RXS20) shift operations are performed in synchronization with the fall of the serial clock ($\overline{SCK20}$). Then transmit data is held in the SO20 latch and output from the SO20 pin. Also, receive data input to the SI0 pin is latched in the receive buffer register (RXB20/SIO20) on the rise of $\overline{SCK20}$.

At the end of an 8-bit transfer, the operation of TXS20/SIO20 or RXS20 stops automatically, and an interrupt request signal (INTCSI20) is generated.

Figure 13-11. 3-Wire Serial I/O Mode Timing (1/7)

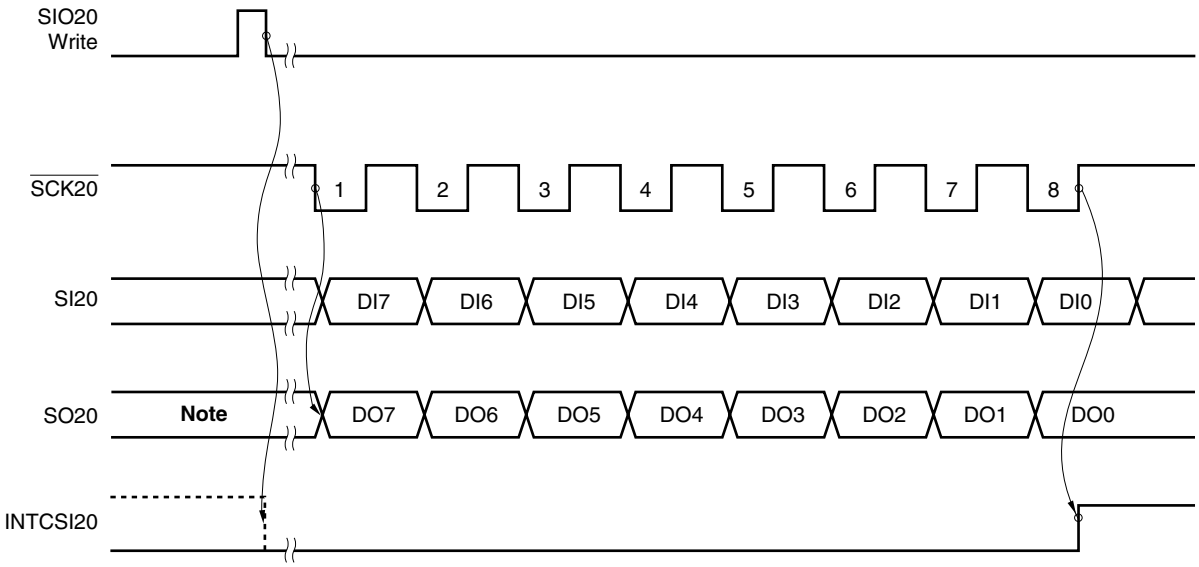
(i) Master operation timing (when DAP20 = 0, CKP20 = 0, SSE20 = 0)



Note The value of the last bit previously output is output.

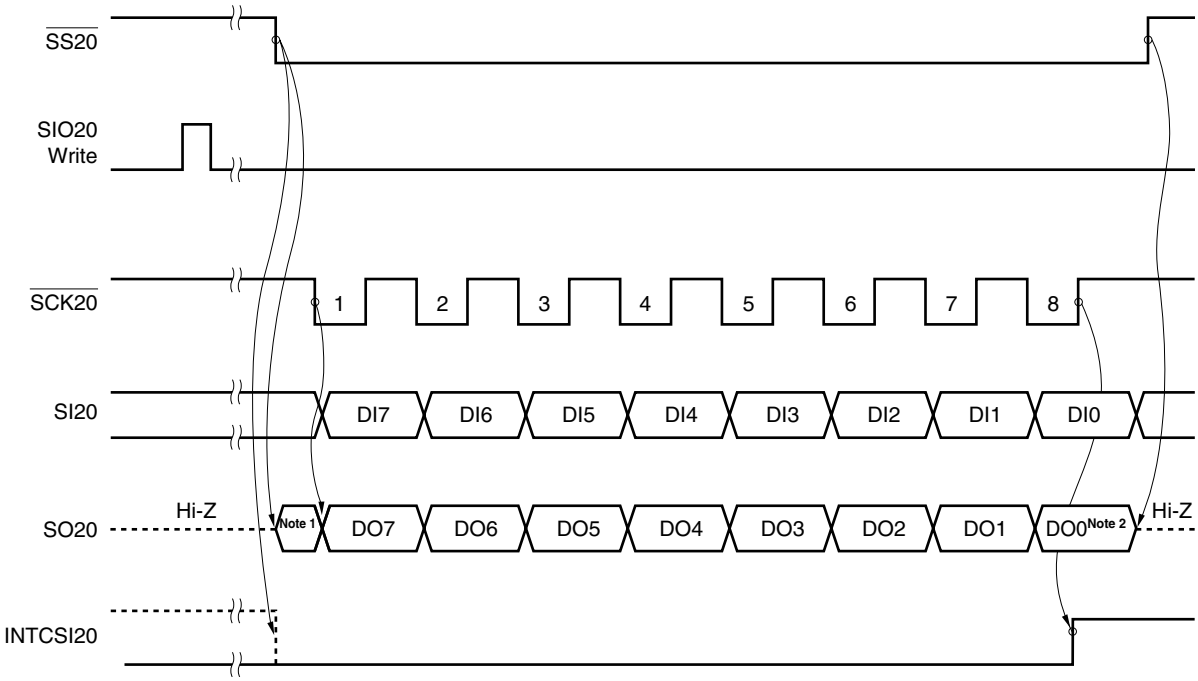
Figure 13-11. 3-Wire Serial I/O Mode Timing (2/7)

(ii) Slave operation timing (when DAP20 = 0, CKP20 = 0, SSE20 = 0)



Note The value of the last bit previously output is output.

(iii) Slave operation (when DAP20 = 0, CKP20 = 0, SSE20 = 1)

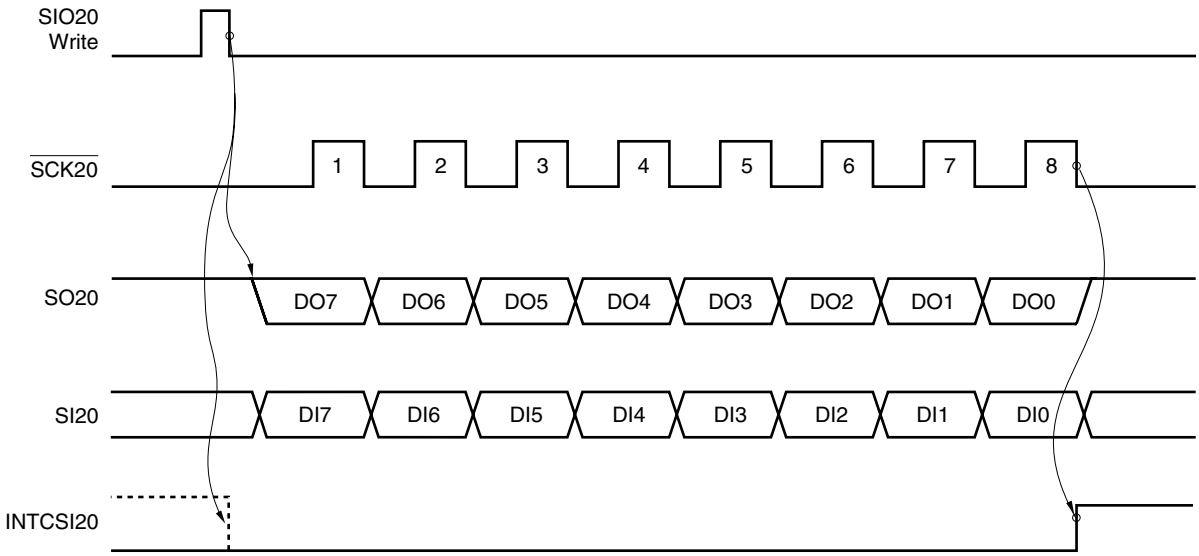


Notes 1. The value of the last bit previously output is output.

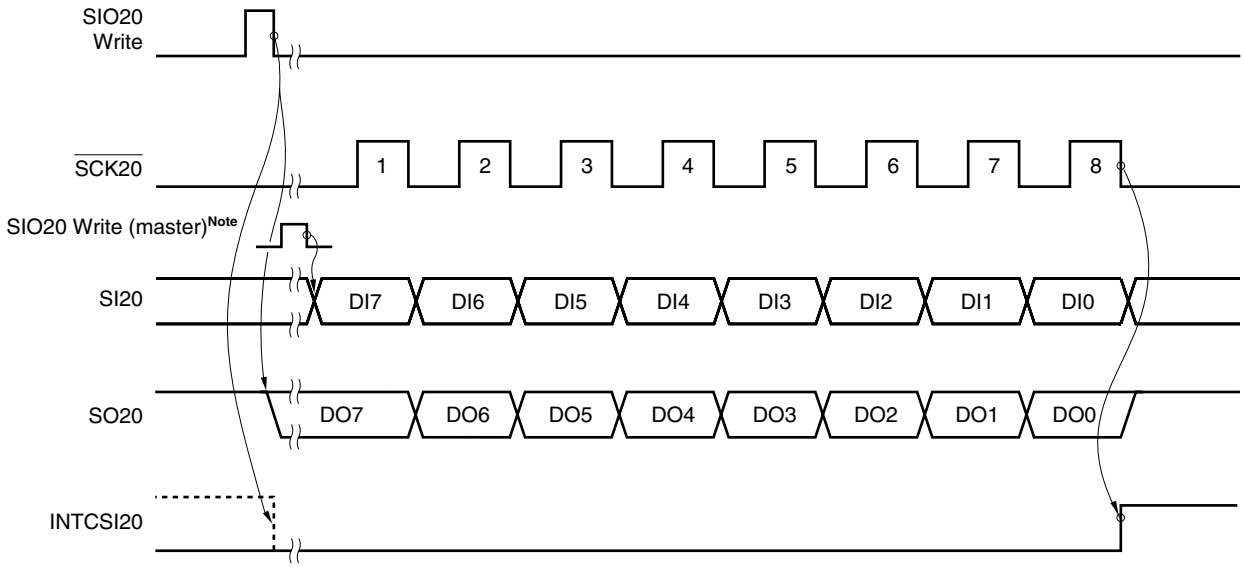
2. DO0 is output until $\overline{SS20}$ rises.
When $\overline{SS20}$ is high, SO20 is in a high-impedance state.

Figure 13-11. 3-Wire Serial I/O Mode Timing (3/7)

(iv) Master operation (when DAP20 = 0, CKP20 = 1, SSE20 = 0)



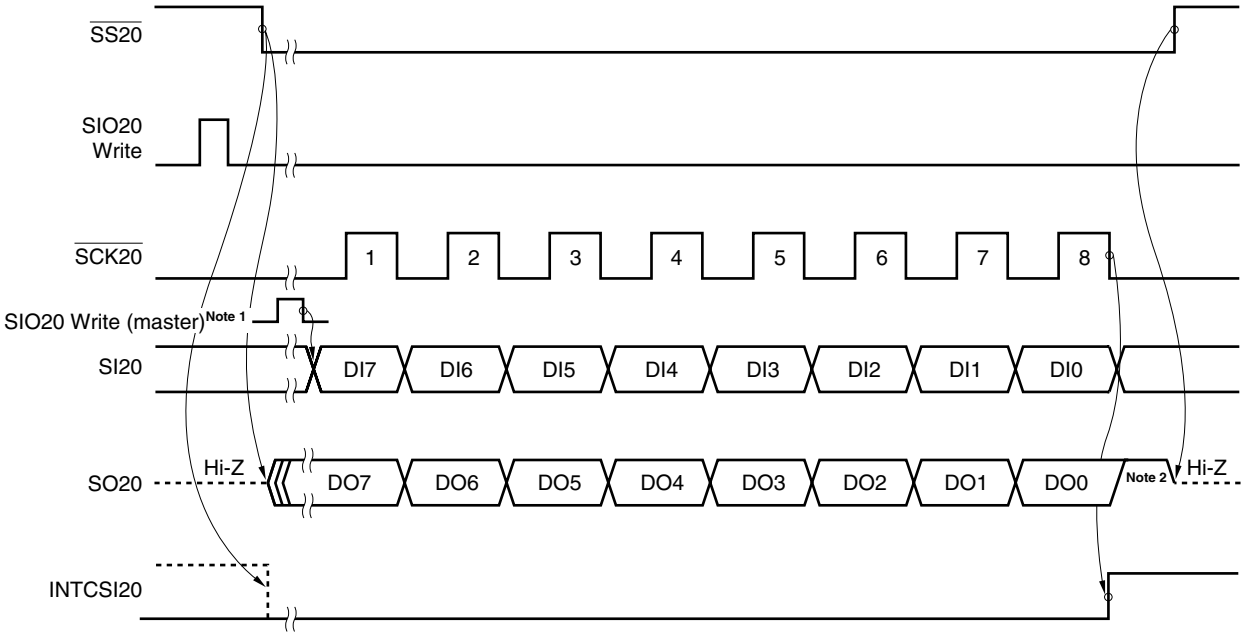
(v) Slave operation (when DAP20 = 1, CKP20 = 1, SSE20 = 0)



Note The data of SI20 is loaded at the first rising edge of $\overline{\text{SCK20}}$. Make sure that the master outputs the first bit before the first rising of $\overline{\text{SCK20}}$.

Figure 13-11. 3-Wire Serial I/O Mode Timing (4/7)

(vi) Slave operation (when DAP20 = 0, CKP20 = 1, SSE20 = 1)



Notes 1. The data of SI20 is loaded at the first rising edge of $\overline{\text{SCK20}}$. Make sure that the master outputs the first bit before the first rising of $\overline{\text{SCK20}}$.

2. SO20 is high until $\overline{\text{SS20}}$ rises after completion of DO0 output. When $\overline{\text{SS20}}$ is high, SO20 is in a high-impedance state.

(vii) Master operation (when DAP20 = 1, CKP20 = 0, SSE20 = 0)

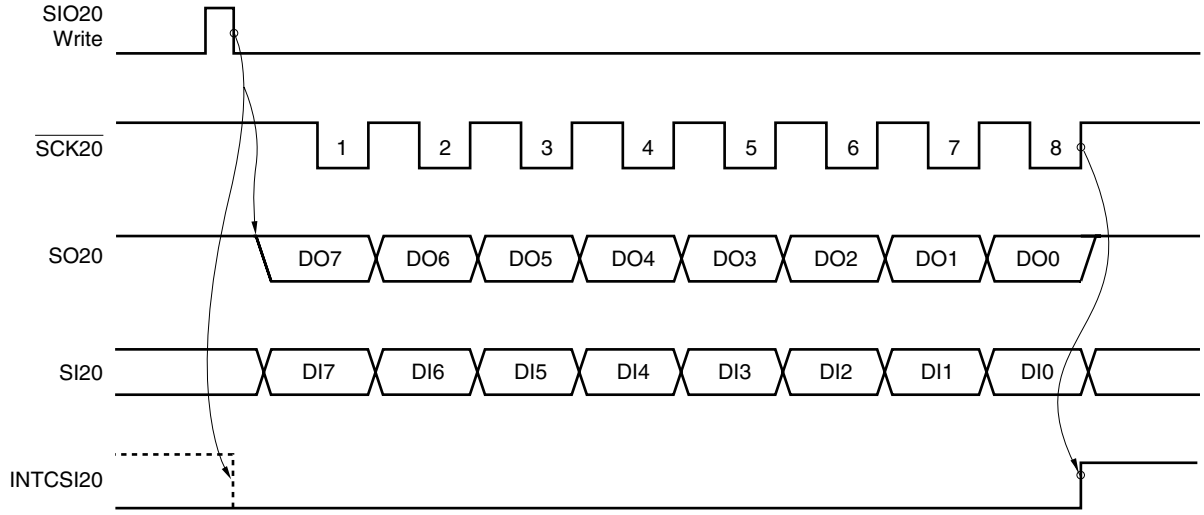
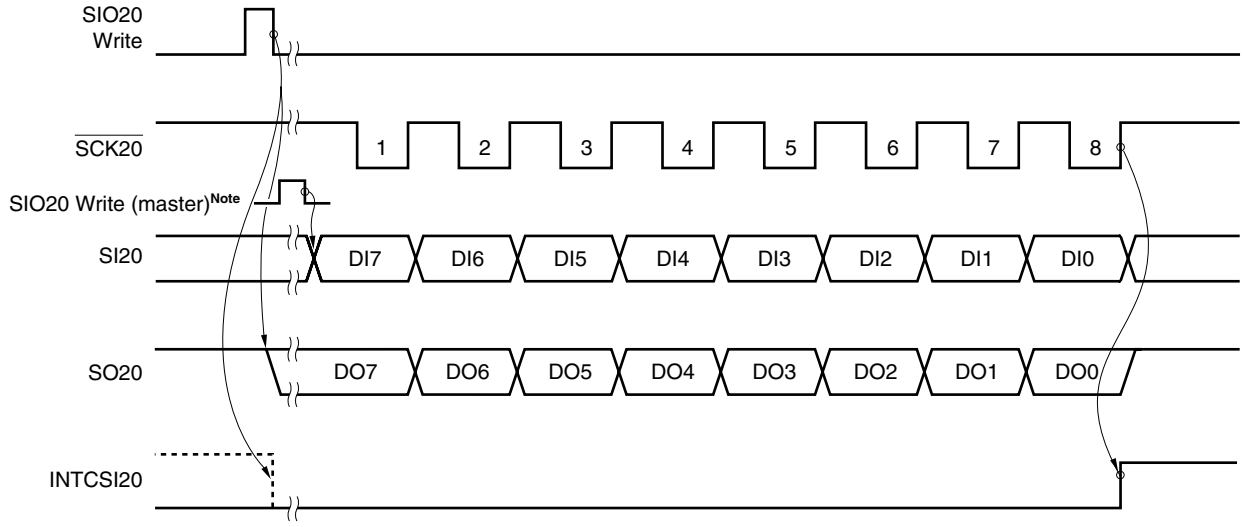


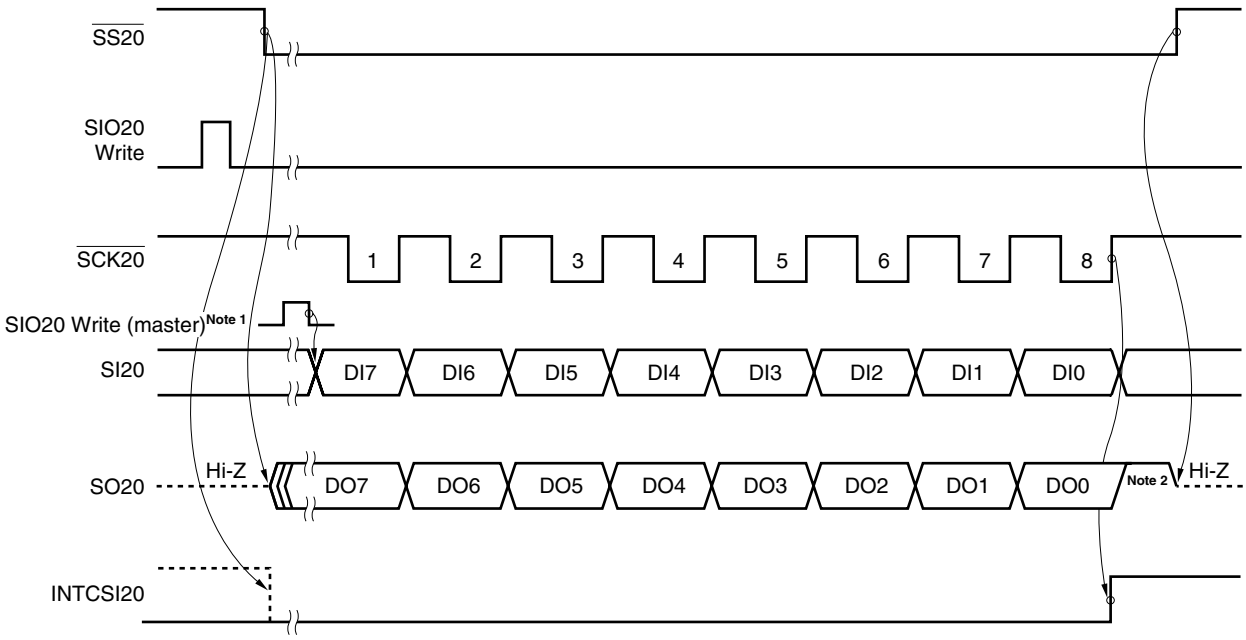
Figure 13-11. 3-Wire Serial I/O Mode Timing (5/7)

(viii) Slave operation (when DAP20 = 1, CKP20 = 0, SSE20 = 0)



Note The data of SI20 is loaded at the first falling edge of $\overline{SCK20}$. Make sure that the master outputs the first bit before the first falling of $\overline{SCK20}$.

(ix) Slave operation (when DAP20 = 1, CKP20 = 0, SSE20 = 1)

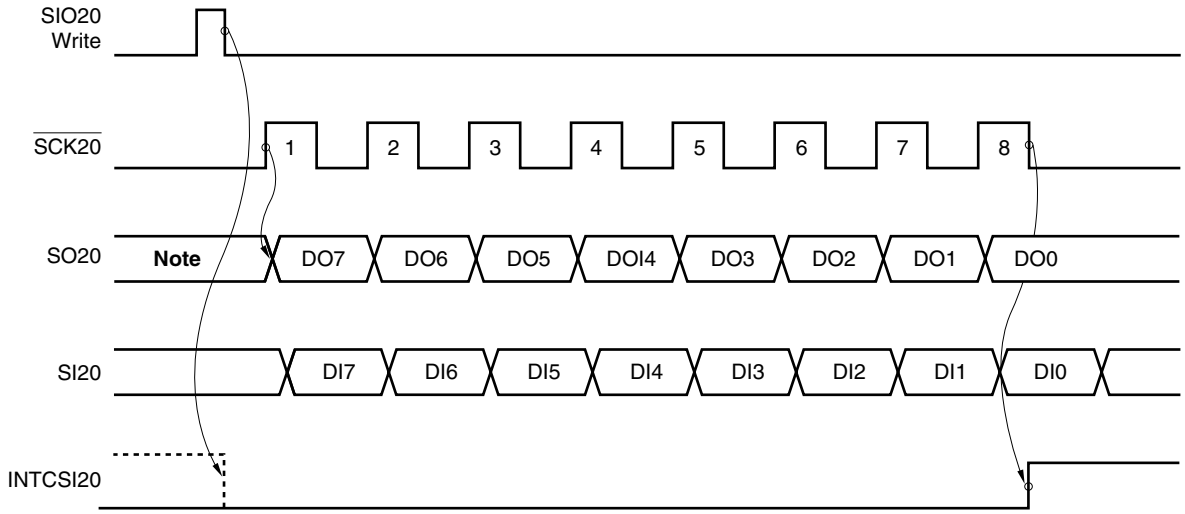


Notes 1. The data of SI20 is loaded at the first falling edge of $\overline{SCK20}$. Make sure that the master outputs the first bit before the first falling of $\overline{SCK20}$.

2. SO20 is high until $\overline{SS20}$ rises after completion of DO0 output. When $\overline{SS20}$ is high, SO20 is in a high-impedance state.

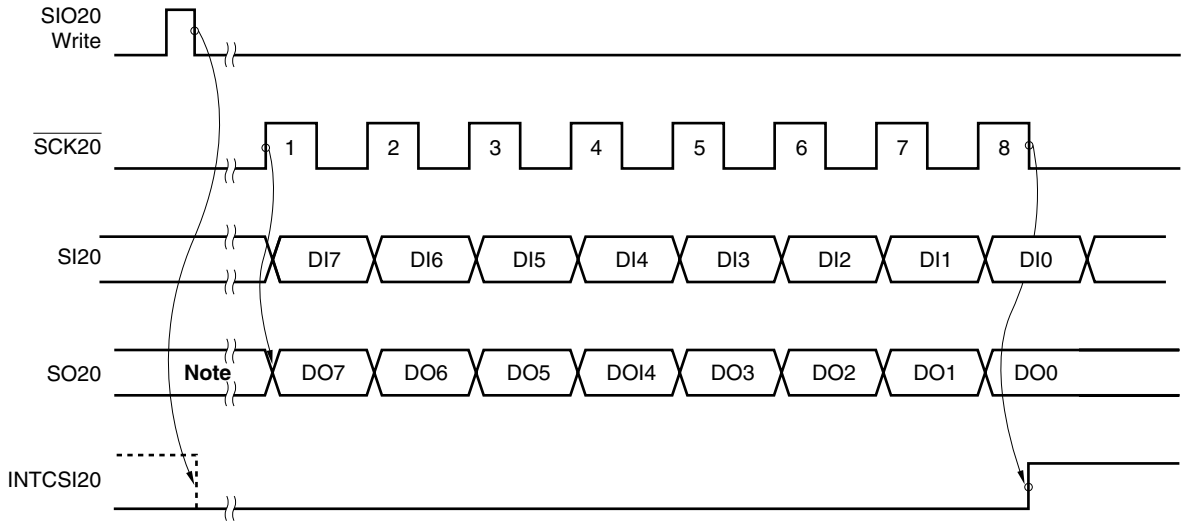
Figure 13-11. 3-Wire Serial I/O Mode Timing (6/7)

(x) Master operation (when DAP20 = 1, CKP20 = 1, SSE20 = 0)



Note The value of the last bit previously output is output.

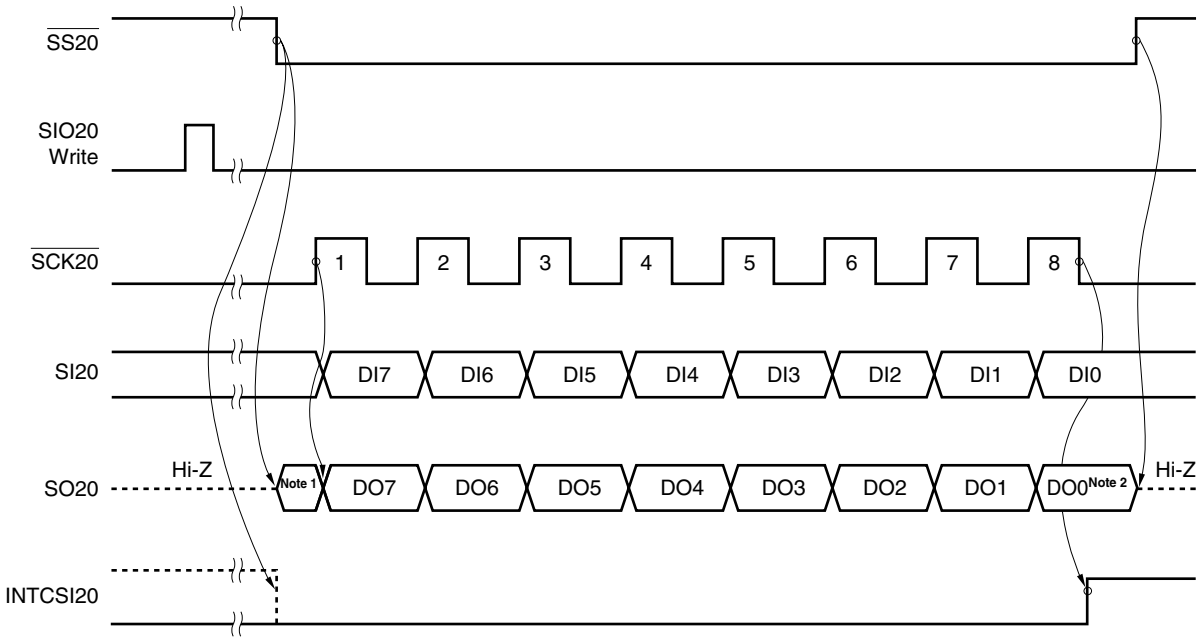
(xi) Slave operation (when DAP20 = 1, CKP20 = 1, SSE20 = 0)



Note The value of the last bit previously output is output.

Figure 13-11. 3-Wire Serial I/O Mode Timing (7/7)

(xii) Slave operation (when DAP20 = 1, CKP20 = 1, SSE20 = 1)



Notes 1. The value of the last bit previously output is output.

2. DO0 is output until $\overline{SS20}$ rises.
When $\overline{SS20}$ is high, SO20 is in a high-impedance state.

(3) Transfer start

Serial transfer is started by setting transfer data to the transmit shift register (TXS20/SIO20) when the following two conditions are satisfied.

- Serial operating mode register 20 (CSIM20) bit 7 (CSIE20) = 1
- Internal serial clock is stopped or $\overline{SCK20}$ is a high level after 8-bit serial transfer.

Caution If CSIE20 is set to "1" after data is written to TXS20/SIO20, transfer does not start.

Termination of 8-bit transfer stops the serial transfer automatically and generates an interrupt request signal (INTCSI20).

CHAPTER 14 MULTIPLIER

14.1 Multiplier Function

The multiplier has the following function.

- Calculation of 8 bits × 8 bits = 16 bits

14.2 Multiplier Configuration

(1) 16-bit multiplication result storage register 0 (MUL0)

This register stores the 16-bit result of multiplication.

This register holds the result of multiplication after 16 CPU clocks have elapsed.

MUL0 is set with a 16-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input makes this register undefined.

Caution Although this register is manipulated with a 16-bit memory manipulation instruction, it can also be manipulated with an 8-bit memory manipulation instruction. When using an 8-bit memory manipulation instruction, however, access the register by means of direct addressing.

(2) Multiplication data registers A and B (MRA0 and MRB0)

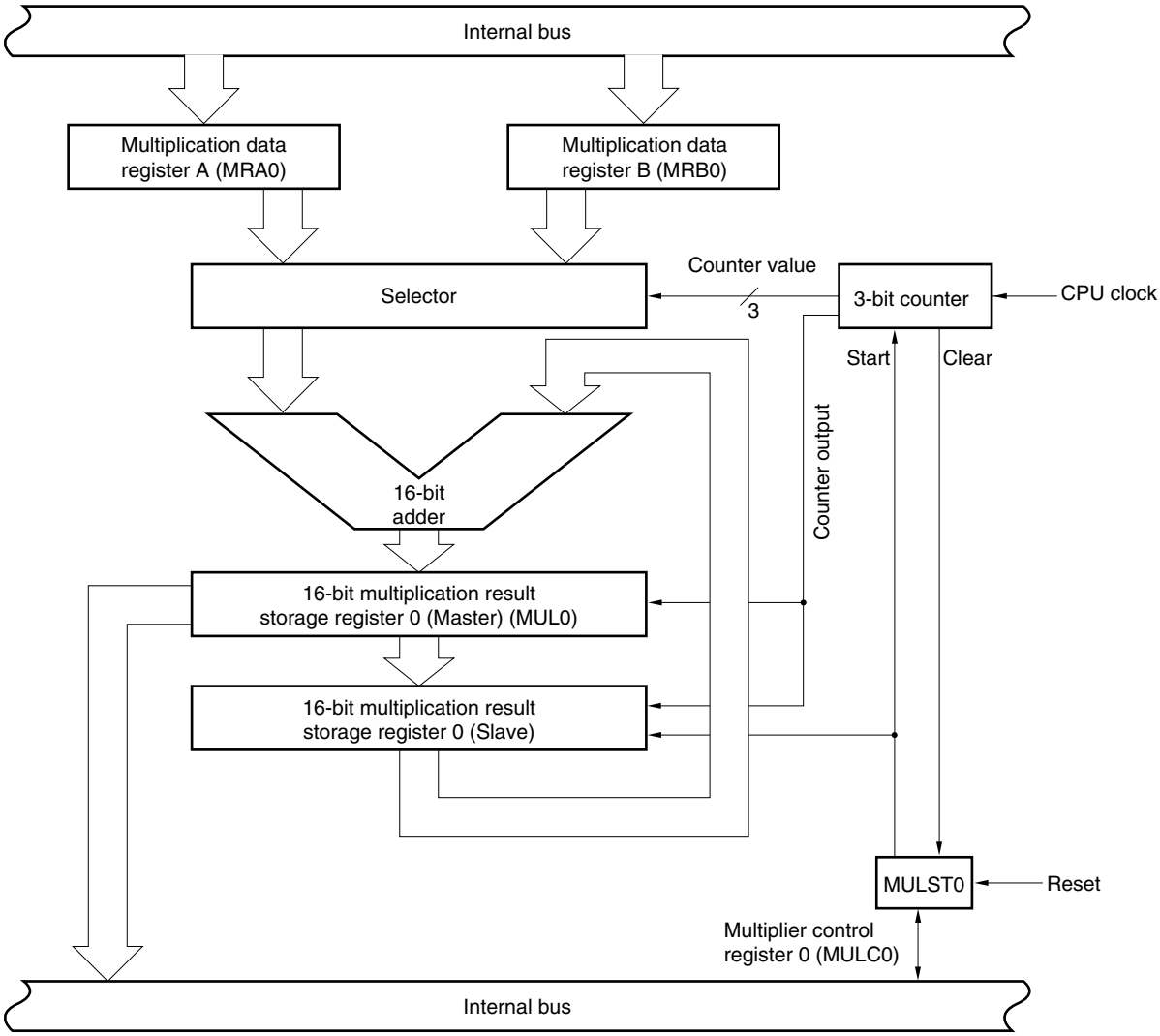
These are 8-bit multiplication data storage registers. The multiplier multiplies the values of MRA0 and MRB0.

MRA0 and MRB0 are set with a 1-bit or 8-bit memory manipulation instructions.

$\overline{\text{RESET}}$ input makes these registers undefined.

Figure 14-1 shows the block diagram of the multiplier.

Figure 14-1. Block Diagram of Multiplier



14.3 Multiplier Control Register

The multiplier is controlled by the following register.

- Multiplier control register 0 (MULC0)

MULC0 indicates the operating status of the multiplier after operation, as well as controls the multiplier.
MULC0 is set with a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input clears this register to 00H.

Figure 14-2. Format of Multiplier Control Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
MULC0	0	0	0	0	0	0	0	MULST0	FFD2H	00H	R/W

MULST0	Multiplier operation start control bit	Operating status of multiplier
0	Stop operation after resetting counter to 0.	Operation stopped
1	Enable operation	Operation in progress

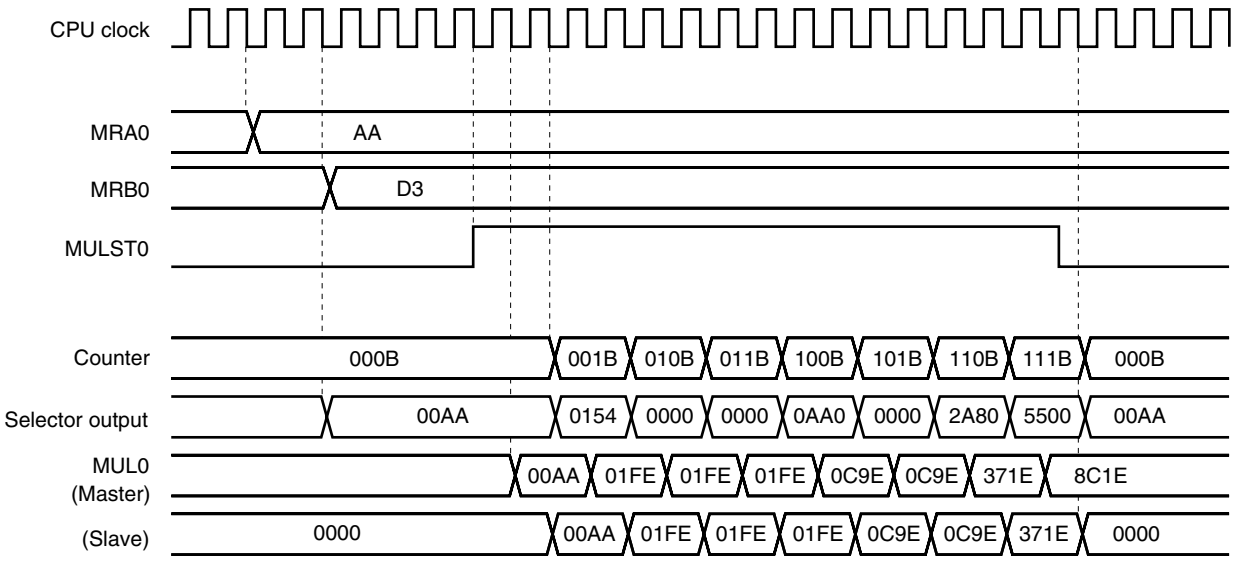
Caution Be sure to clear bits 1 to 7 to 0.

14.4 Multiplier Operation

The multiplier of the μPD789104A/114A/124A/134A Subseries can execute the calculation of 8 bits × 8 bits = 16 bits. Figure 14-3 shows the operation timing of the multiplier where MRA0 is set to AAH and MRB0 is set to D3H.

<1> Counting is started by setting MULST0.
<2> The data generated by the selector is added to the data of MUL0 at each CPU clock, and the counter value is incremented by one.
<3> If MULST0 is cleared when the counter value is 111B, the operation is stopped. At this time, MUL0 holds the data.
<4> While MULST0 is low, the counter and slave are cleared.

Figure 14-3. Multiplier Operation Timing



CHAPTER 15 INTERRUPT FUNCTIONS

15.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Non-maskable interrupt

This interrupt is acknowledged unconditionally. It does not undergo interrupt priority control and is given top priority over all other interrupt requests.

A standby release signal is generated.

There is one non-maskable interrupt source, which is from the watchdog timer.

(2) Maskable interrupt

These interrupts undergo mask control. If two or more interrupts with the same priority are simultaneously generated, each interrupt has a predetermined priority as shown in Table 15-1.

A standby release signal is generated.

There are nine maskable interrupt sources: three external interrupts and six internal interrupts.

15.2 Interrupt Sources and Configuration

There are total of 10 non-maskable and maskable interrupt sources (refer to **Table 15-1**).

Table 15-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSR20	End of serial interface 20 UART reception	Internal	000CH	(B)
		INTCSI20	End of serial interface 20 3-wire transfer			
	5	INTST20	End of serial interface 20 UART transmission		000EH	
	6	INTTM80	Generation of 8-bit timer/event counter 80 match signal		0010H	
	7	INTTM20	Generation of 16-bit timer 20 match signal		0012H	
	8	INTAD0	A/D conversion completion signal		0014H	

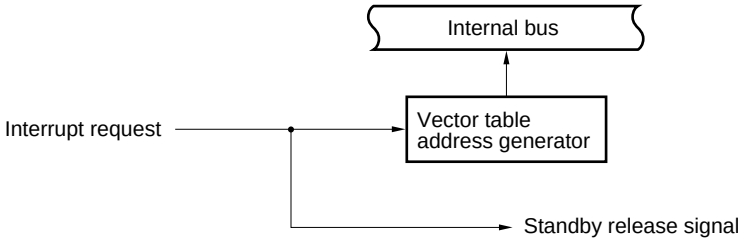
Notes 1. Priority is the priority applicable when two or more maskable interrupts are simultaneously generated. 0 is the highest priority and 8 is the lowest priority.

2. Basic configuration types A to C correspond to A to C in Figure 15-1.

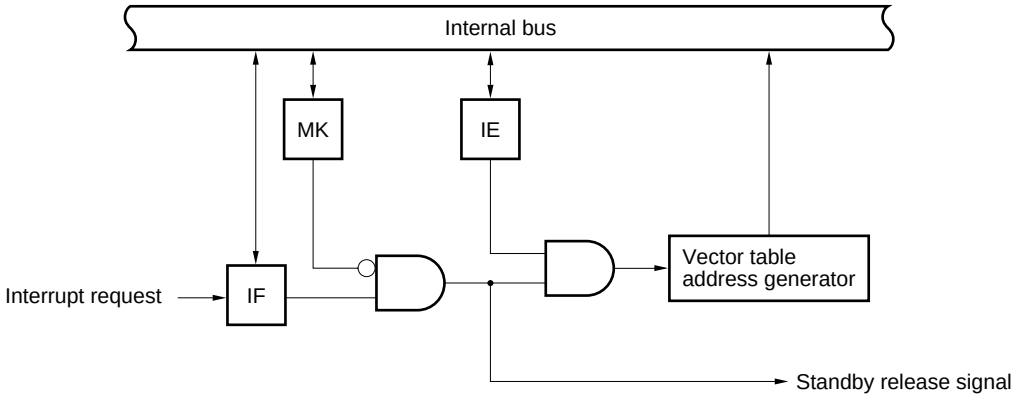
Remark As the interrupt source of the watchdog timer (INTWDT), either a non-maskable interrupt or a maskable interrupt (internal) can be selected.

Figure 15-1. Basic Configuration of Interrupt Function

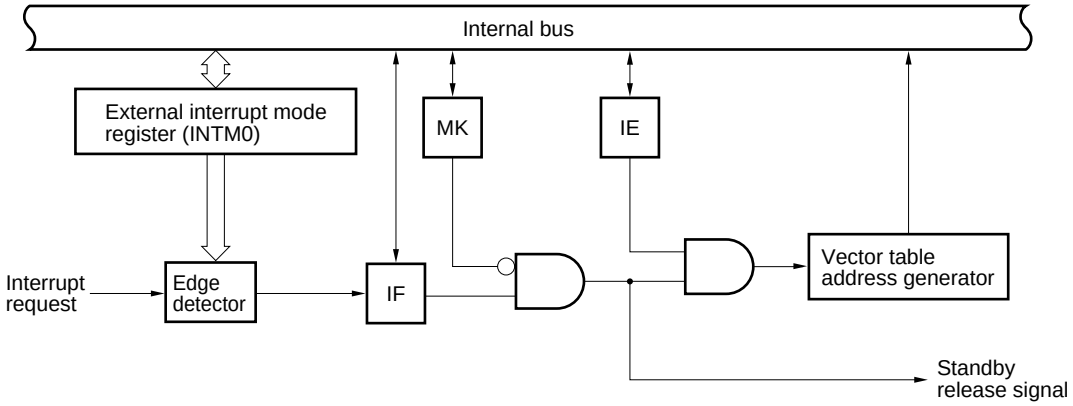
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



IF: Interrupt request flag

IE: Interrupt enable flag

MK: Interrupt mask flag

15.3 Interrupt Function Control Registers

The following four registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0, IF1)
- Interrupt mask flag registers (MK0, MK1)
- External interrupt mode register (INTM0)
- Program status word (PSW)

Table 15-2 gives a listing of interrupt request flag and interrupt mask flag names corresponding to interrupt requests.

Table 15-2. Flags Corresponding to Interrupt Request Signals

Interrupt Request Signal Name	Interrupt Request Flag	Interrupt Mask Flag
INTWDT	TMIF4	TMMK4
INTP0	PIF0	PMK0
INTP1	PIF1	PMK1
INTP2	PIF2	PMK2
INTSR20/INTCSI20	SRIF20	SRMK20
INTST20	STIF20	STMK20
INTTM80	TMIF80	TMMK80
INTTM20	TMIF20	TMMK20
INTAD0	ADIF0	ADMK0

(1) Interrupt request flag registers (IF0, IF1)

The interrupt request flag is set to 1 when the corresponding interrupt request is generated or an instruction is executed. It is cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon $\overline{\text{RESET}}$ input.

IF0 and IF1 are set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears these registers to 00H.

Figure 15-2. Format of Interrupt Request Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
IF0	TMIF20	TMIF80	STIF20	SRIF20	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W

Symbol	7	6	5	4	3	2	1	<0>	Address	After reset	R/W
IF1	0	0	0	0	0	0	0	ADIF0	FFE1H	00H	R/W

××IF×	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request signal is generated; interrupt request state

Cautions 1. TMIF4 flag is R/W enabled only when the watchdog timer is used as an interval timer. If watchdog timer mode 1 and 2 are used, set the TMIF4 flag to 0.

2. Because port 2 has an alternate function as the external interrupt input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

★ **3. When an interrupt is acknowledged, the interrupt request flag is automatically cleared and the interrupt routine is entered.**

(2) Interrupt mask flag registers (MK0, MK1)

The interrupt mask flag is used to enable/disable the corresponding maskable interrupt servicing.

MK0 and MK1 are set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets these registers to FFH.

Figure 15-3. Format of Interrupt Mask Flag Register

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>	Address	After reset	R/W
MK0	TMMK20	TMMK80	STMK20	SRMK20	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W

Symbol	7	6	5	4	3	2	1	<0>	Address	After reset	R/W
MK1	1	1	1	1	1	1	1	ADMK0	FFE5H	FFH	R/W

××MK×	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Cautions 1. If the TMMK4 flag is read when the watchdog timer is used in watchdog timer mode 1 and 2, its value becomes undefined.

2. Because port 2 has an alternate function as the external interrupt input, when the output level is changed by specifying the output mode of the port function, an interrupt request flag is set. Therefore, the interrupt mask flag should be set to 1 before using the output mode.

(3) External interrupt mode register 0 (INTM0)

This register is used to set the valid edge of INTP0 to INTP2.

INTM0 is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input clears INTM0 to 00H.

Figure 15-4. Format of External Interrupt Mode Register 0

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
INTM0	ES21	ES20	ES11	ES10	ES01	ES00	0	0	FFECH	00H	R/W

ES21	ES20	INTP2 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES11	ES10	INTP1 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES01	ES00	INTP0 valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

Cautions 1. Be sure to clear bits 0 and 1 to 0.

2. Before setting the INTM0 register, be sure to set the corresponding interrupt mask flag (××MK× = 1) to disable interrupts. After setting the INTM0 register, clear the interrupt request flag (××IF× = 0), then clear the interrupt mask flag (××MK× = 0), which will enable interrupts.

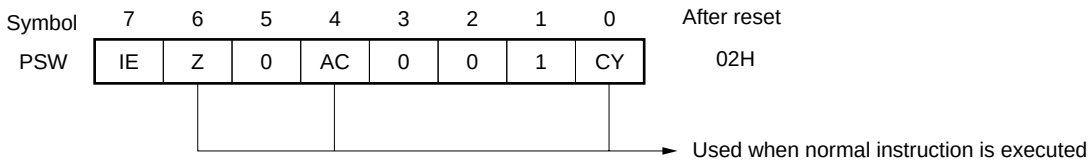
(4) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for interrupt requests. The IE flag used to set maskable interrupt enable/disable is mapped to the PSW.

This register can be read/written in 8-bit units and can carry out operations using bit manipulation and dedicated instructions (EI, DI). When a vectored interrupt request is acknowledged, the PSW is automatically saved into a stack, and the IE flag is reset to 0. It is restored from the stack by the RETI and POP PSW instructions.

$\overline{\text{RESET}}$ input sets the PSW to 02H.

Figure 15-5. Program Status Word Configuration



IE	Interrupt acknowledgment enable/disable
0	Disabled
1	Enabled

15.4 Interrupt Servicing Operation

15.4.1 Non-maskable interrupt request acknowledgment operation

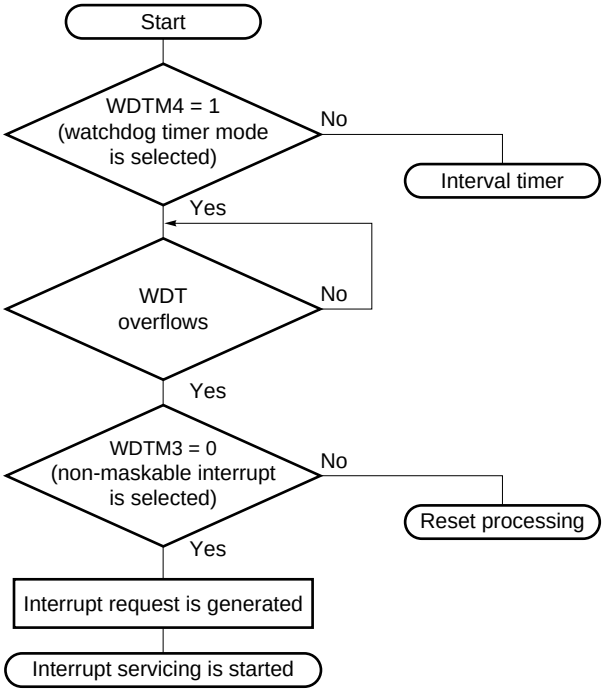
A non-maskable interrupt request is unconditionally acknowledged even when interrupts are disabled. It is not subject to interrupt priority control and takes precedence over all other interrupts.

When a non-maskable interrupt request is acknowledged, the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, the contents of the vector table are loaded to the PC, and then program execution branches.

Figure 15-6 shows the flowchart from non-maskable interrupt request generation to acknowledgment. Figure 15-7 shows the timing of non-maskable interrupt request acknowledgment. Figure 15-8 shows the acknowledgment operation if multiple non-maskable interrupts are generated.

Caution During non-maskable interrupt servicing program execution, do not input another non-maskable interrupt request; if it is input, the servicing program will be interrupted and the new interrupt request will be acknowledged.

Figure 15-6. Flowchart from Non-Maskable Interrupt Request Generation to Acknowledgment



WDTM: Watchdog timer mode register

WDT: Watchdog timer

Figure 15-7. Timing of Non-Maskable Interrupt Request Acknowledgment

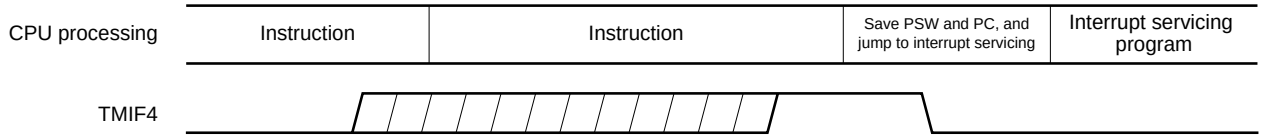
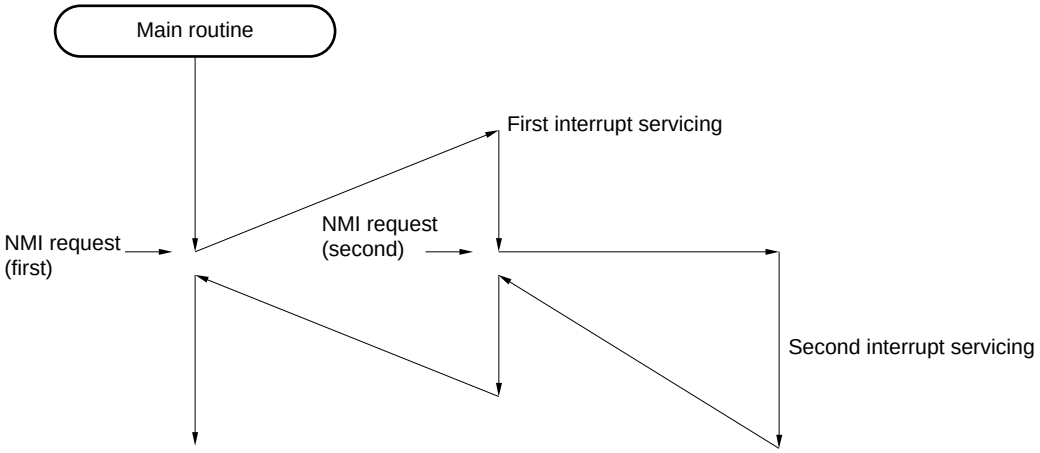


Figure 15-8. Acknowledging Non-Maskable Interrupt Request



15.4.2 Maskable interrupt request acknowledgment operation

A maskable interrupt request can be acknowledged when the interrupt request flag is set to 1 and the corresponding interrupt mask flag is cleared to 0. A vectored interrupt request is acknowledged in the interrupt enabled status (when the IE flag is set to 1).

The time required to start the interrupt servicing after a maskable interrupt request has been generated is shown in Table 15-3.

Refer to Figures 15-10 and 15-11 for the interrupt request acknowledgment timing.

Table 15-3. Time from Generation of Maskable Interrupt Request to Servicing

Minimum Time	Maximum Time[Note]
9 clocks	19 clocks

Note The wait time is maximum when an interrupt request is generated immediately before the BT or BF instruction.

Remark 1 clock: $\frac{1}{f_{CPU}}$ (f_{CPU}: CPU clock)

When two or more maskable interrupt requests are generated at the same time, they are acknowledged starting from the interrupt request assigned the highest priority.

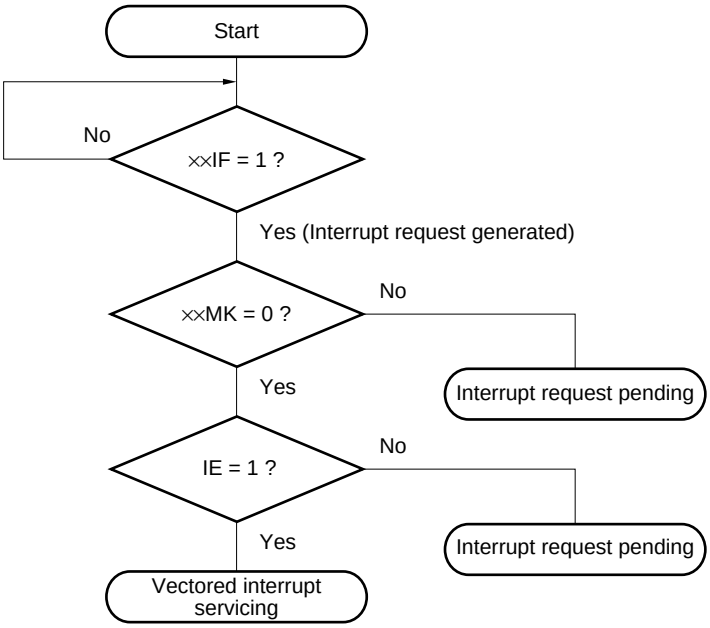
A pending interrupt is acknowledged when the status in which it can be acknowledged is set.

Figure 15-9 shows the algorithm of acknowledging interrupt requests.

When a maskable interrupt request is acknowledged, the contents of the PSW and PC are saved to the stack in that order, the IE flag is reset to 0, and the data in the vector table determined for each interrupt request is loaded to the PC, and execution branches.

To return from interrupt servicing, use the RETI instruction.

Figure 15-9. Interrupt Acknowledgment Program Algorithm

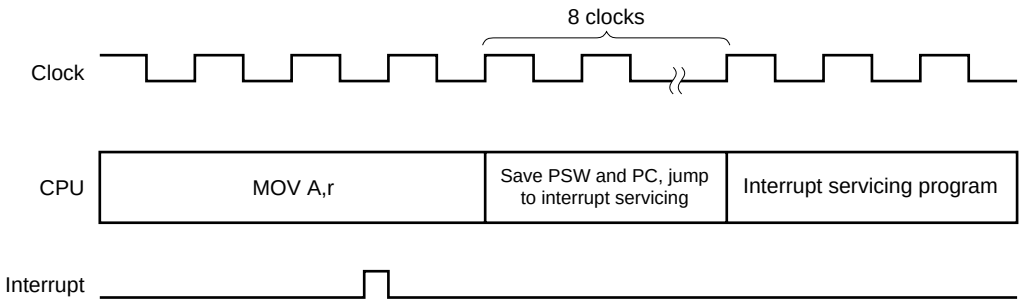


××IF: Interrupt request flag

××MK: Interrupt mask flag

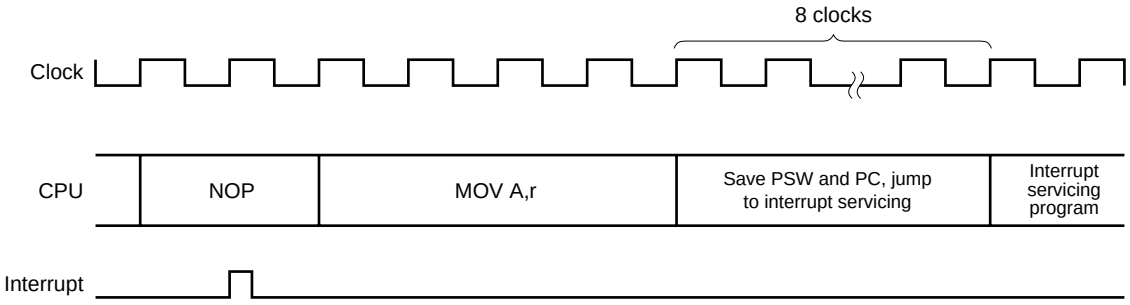
IE: Flag to control maskable interrupt request acknowledgment (1 = Enable, 0 = Disable)

Figure 15-10. Interrupt Request Acknowledgment Timing (Example of MOV A,r)



If an interrupt request flag (××IF) is set before instruction clock n (n = 4 to 10) under execution becomes n – 1, the interrupt is acknowledged after the instruction under execution is complete. Figure 15-10 shows an example of the interrupt request acknowledgment timing for an 8-bit data transfer instruction MOV A,r. Since this instruction is executed for 4 clocks, if an interrupt occurs for 3 clocks after the execution starts, the interrupt acknowledgment processing is performed after the MOV A,r instruction is completed.

Figure 15-11. Interrupt Request Acknowledgment Timing (When Interrupt Request Flag Is Generated at Last Clock During Instruction Execution)



If an interrupt request flag (××IF) is set at the last clock of the instruction, the interrupt acknowledgment processing starts after the next instruction is executed.

Figure 15-11 shows an example of the interrupt acknowledgment timing for an interrupt request flag that is set at the second clock of NOP (2-clock instruction). In this case, the MOV A,r instruction after the NOP instruction is executed, and then the interrupt acknowledgment processing is performed.

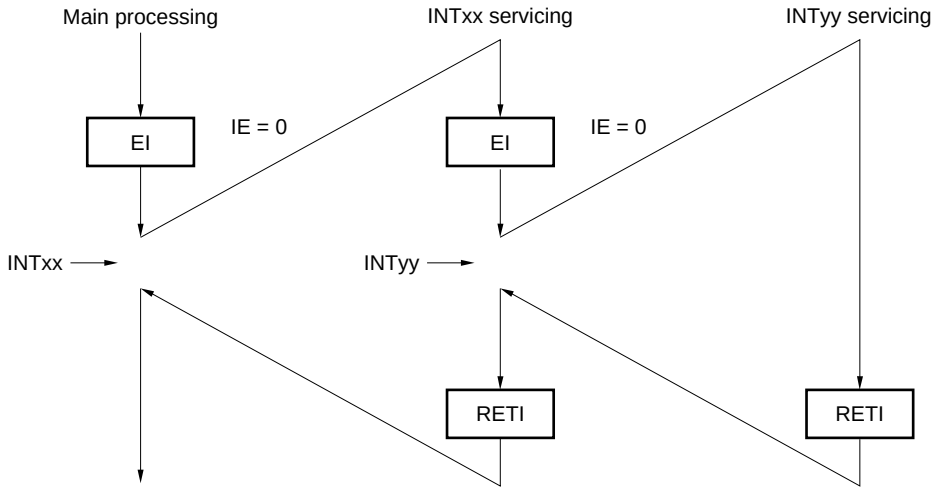
Caution Interrupt requests are held pending while the interrupt request flag register (IF0, IF1) or the interrupt mask flag register (MK0, MK1) is being accessed.

15.4.3 Multiple interrupt servicing

Multiple interrupt servicing, in which an interrupt is acknowledged while another interrupt is being serviced, can be executed by priority. When the priority is controlled by the default priority and two or more interrupts are generated at the same time, interrupt servicing is performed according to the priority assigned to each interrupt request in advance (refer to **Table 15-1**).

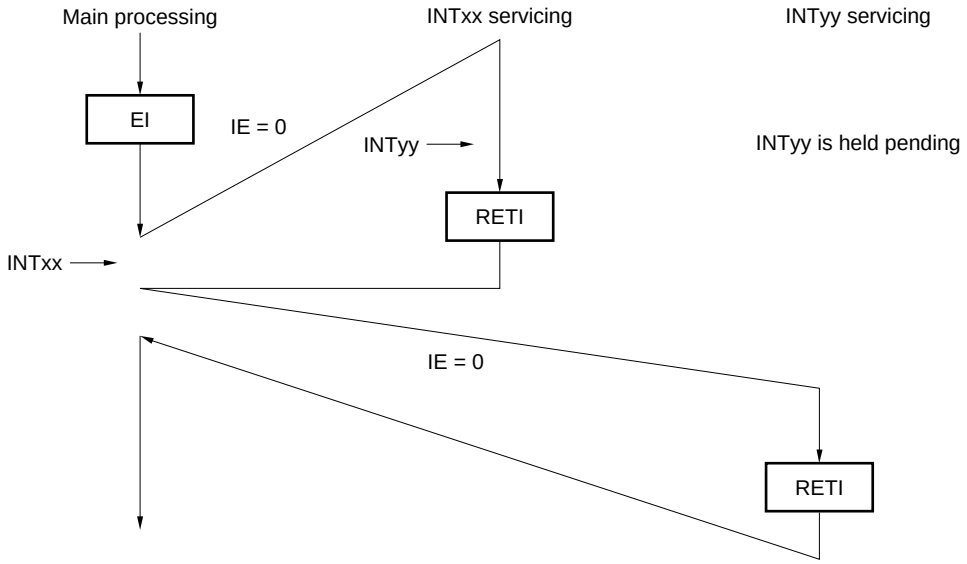
Figure 15-12. Example of Multiple Interrupt Servicing

Example 1. Multiple interrupts are acknowledged



During interrupt INTxx servicing, interrupt request INTyy is acknowledged, and multiple interrupt servicing occurs. The EI instruction is issued before each interrupt request acknowledgment, and the interrupt request acknowledgment enabled state is set.

Example 2. Multiple interrupt servicing does not occur because interrupts are not enabled



Because interrupts are not enabled in interrupt INTxx servicing (the EI instruction is not issued), interrupt request INTyy is not acknowledged, and a multiple interrupt servicing does not occur. The INTyy request is held pending and acknowledged after the INTxx servicing is performed.

IE = 0: Interrupt request acknowledgment disabled

15.4.4 Interrupt request hold

Some instructions may hold the acknowledgment of an instruction request pending until completion of the execution of the next instruction even if the interrupt request (maskable interrupt, non-maskable interrupt, and external interrupt) is generated during the execution. The following shows such instructions (interrupt request hold instructions).

- Manipulation instruction for the interrupt request flag registers (IF0, IF1)
- Manipulation instruction for the interrupt mask flag registers (MK0, MK1)

CHAPTER 16 STANDBY FUNCTION

16.1 Standby Function and Configuration

16.1.1 Standby function

The standby function is used to reduce the power consumption of the system and can be effected in the following two modes.

(1) HALT mode

This mode is set when the HALT instruction is executed. The HALT mode stops the operation clock of the CPU. The system clock oscillator continues oscillating. This mode does not reduce the power consumption as much as the STOP mode, but is useful for resuming processing immediately when an interrupt request is generated, or for intermittent operations.

(2) STOP mode

This mode is set when the STOP instruction is executed. The STOP mode stops the main system clock oscillator and stops the entire system. The power consumption of the CPU can be substantially reduced in this mode.

The low voltage of the data memory (V_{DD} = 1.8 V) can be held. Therefore, this mode is useful for holding the contents of the data memory at an extremely low current consumption.

The STOP mode can be released by an interrupt request, so that this mode can be used for intermittent operations. However, some time is required until the system clock oscillator stabilizes after the STOP mode has been released. If processing must be resumed immediately by using an interrupt request, therefore, use the HALT mode.

In both modes, the previous contents of the registers, flags, and data memory before setting the standby mode are all held. In addition, the statuses of the output latches of the I/O ports and output buffers are also retained.

Caution To set the STOP mode, be sure to stop the operations of the peripheral hardware, and then execute the STOP instruction.

16.1.2 Standby function control register (μPD789104A, 789114A Subseries)

The wait time after the STOP mode is released upon interrupt request until the oscillation stabilizes is controlled by the oscillation stabilization time select register (OSTS)[Note].

OSTS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets OSTS to 04H. However, the oscillation stabilization time after $\overline{\text{RESET}}$ input is $2^{15}/f_X$, instead of $2^{17}/f_X$.

Note μPD789104A and 789114A Subseries only.

The μPD789124A and 789134A Subseries do not provide an oscillation stabilization time select register. The oscillation stabilization time of the μPD789124A and 789134A Subseries is fixed to $2^7/f_{CC}$.

Figure 16-1. Format of Oscillation Stabilization Time Select Register

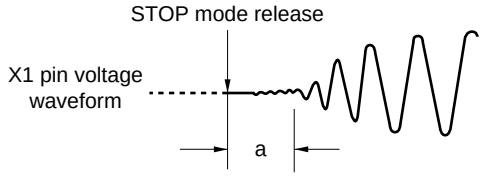
Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

★

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				@ f_X = 10.0 MHz[Note] operation	@ f_X = 5.0 MHz operation
0	0	0	$2^{12}/f_X$	409 μs	819 μs
0	1	0	$2^{15}/f_X$	3.28 ms	6.55 ms
1	0	0	$2^{17}/f_X$	13.1 ms	26.2 ms
Other than above			Setting prohibited		

Note Expanded-specification products only

Caution The wait time after the STOP mode is released when using a ceramic/crystal oscillator does not include the time from STOP mode release to clock oscillation start (“a” in the figure below), regardless of whether STOP mode was released by $\overline{\text{RESET}}$ input or by interrupt generation.



Remark f_X: System clock oscillation frequency (ceramic/crystal oscillation)

16.2 Operation of Standby Function

16.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction.

The operation status in the HALT mode is shown in the following table.

Table 16-1. HALT Mode Operating Status

Item	HALT Mode Operating Status
Clock generator	System clock can be oscillated. Clock supply to CPU stops.
CPU	Operation stopped
Port (output latch)	Holds status before setting the HALT mode.
16-bit timer 20	Operable
8-bit timer/event counter 80	Operable
Watchdog timer	Operable
Serial interface 20	Operable
A/D converter	Operation stopped
Multiplier	Operation stopped
External interrupt	Operable[Note]

Note Maskable interrupt that is not masked

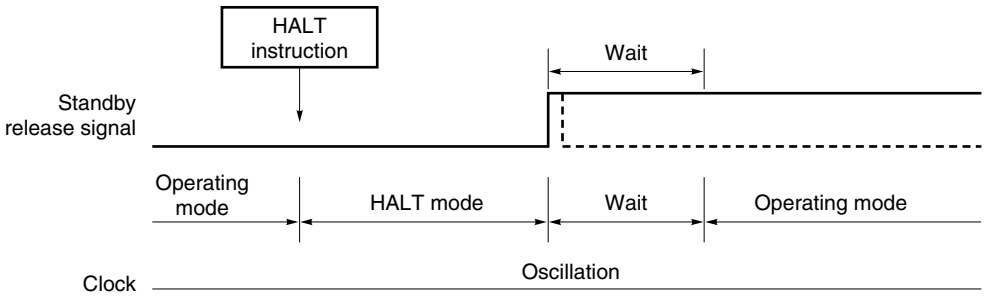
(2) Releasing HALT mode

The HALT mode can be released by the following three sources.

(a) Releasing by unmasked interrupt request

The HALT mode is released by an unmasked interrupt request. In this case, if the interrupt request is able to be acknowledged, vectored interrupt servicing is performed. If interrupts are disabled, the instruction at the next address is executed.

Figure 16-2. Releasing HALT Mode by Interrupt



Remarks 1. The broken lines indicate the case where the interrupt request that has released the standby mode is acknowledged.

2. The wait time is as follows:

- When vectored interrupt servicing is performed: 9 to 10 clocks
- When vectored interrupt servicing is not performed: 1 to 2 clocks

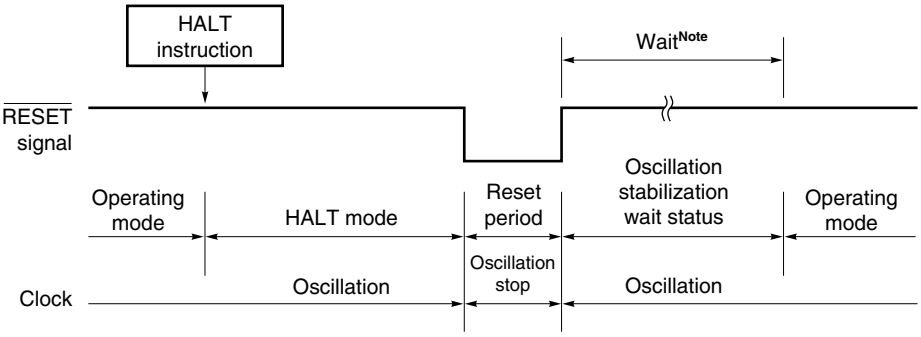
(b) Releasing by non-maskable interrupt request

The HALT mode is released regardless of whether interrupts are enabled or disabled, and vectored interrupt servicing is performed.

(c) Releasing by $\overline{\text{RESET}}$ input

When the HALT mode is released by the $\overline{\text{RESET}}$ signal, execution branches to the reset vector address in the same manner as an ordinary reset operation, and program execution is started.

Figure 16-3. Releasing HALT Mode by $\overline{\text{RESET}}$ Input



Note In the μPD789104A and 789114A Subseries,
2^{15}/fx: 6.55 ms (at fx = 5.0 MHz operation), 3.28 ms (at fx = 10.0 MHz operation)
In the μPD789124A and 789134A Subseries,
2^{7}/fcc: 32 μs (at fcc = 4.0 MHz operation)

Remark fx: System clock oscillation frequency (ceramic/crystal oscillation)
fcc: System clock oscillation frequency (RC oscillation)

Table 16-2. Operation After Release of HALT Mode

Releasing Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction is executed
	0	1	Interrupt servicing is executed
	1	×	HALT mode is held
Non-maskable interrupt request	–	×	Interrupt servicing is executed
$\overline{\text{RESET}}$ input	–	–	Reset processing

×: don't care

16.2.2 STOP mode

(1) Setting and operation status of STOP mode

The STOP mode is set by executing the STOP instruction.

Caution Because the standby mode can be released by an interrupt request signal, the standby mode is released as soon as it is set if there is an interrupt source whose interrupt request flag is set and interrupt mask flag is reset. When the STOP mode is set, therefore, the HALT mode is set immediately after the STOP instruction has been executed, the wait time set by the oscillation stabilization time select register (OSTS) elapses, and then an operation mode is set.

The operation status in the STOP mode is shown in the following table.

Table 16-3. STOP Mode Operating Status

Item	STOP Mode Operating Status
Clock generator	System clock oscillation stopped
CPU	Operation stopped
Port (output latch)	Holds the status before setting the STOP mode
16-bit timer 20	Operation stopped
8-bit timer/event counter 80	Operable[Note 1]
Watchdog timer	Operation stopped
Serial interface 20	Operable[Note 2]
A/D converter	Operation stopped
Multiplier	Operation stopped
External interrupt	Operable[Note 3]

Notes 1. Operation is possible only when TI80 is selected as the count clock.

2. Operation is possible in both 3-wire serial I/O and UART modes while an external clock is being used.

3. Maskable interrupt that is not masked

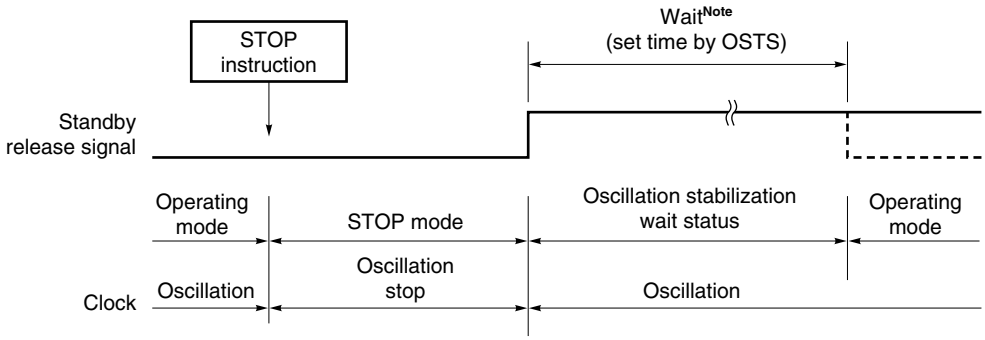
(2) Releasing STOP mode

The STOP mode can be released by the following two sources.

(a) Releasing by unmasked interrupt request

The STOP mode can be released by an unmasked interrupt request. In this case, if the interrupt is able to be acknowledged, vectored interrupt servicing is performed, after the oscillation stabilization time has elapsed. If interrupts are disabled, the instruction at the next address is executed.

Figure 16-4. Releasing STOP Mode by Interrupt



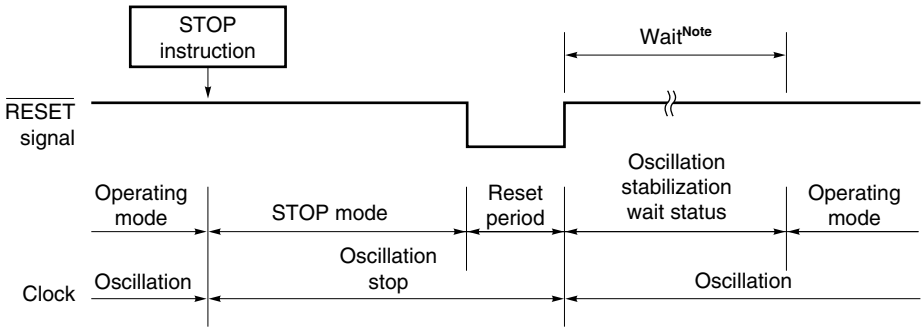
Note OSTS is not provided in the μPD789124A and 789134A Subseries, and the wait time is fixed to $2^7/f_{CC}$.

Remark The broken lines indicate the case where the interrupt request that has released the standby mode is acknowledged.

(b) Releasing by $\overline{\text{RESET}}$ input

When the STOP mode is released by the $\overline{\text{RESET}}$ signal, the reset operation is performed after the oscillation stabilization time has elapsed.

Figure 16-5. Releasing STOP Mode by $\overline{\text{RESET}}$ Input



Note In the μPD789104A and 789114A Subseries,

2^{15}/fx: 6.55 ms (at fx = 5.0 MHz operation), 3.28 ms (at fx = 10.0 MHz operation)

In the μPD789124A and 789134A Subseries,

2^{7}/fcc: 32 μs (at fcc = 4.0 MHz operation)

Remark fx: System clock oscillation frequency (ceramic/crystal oscillation)

fcc: System clock oscillation frequency (RC oscillation)

Table 16-4. Operation After Release of STOP Mode

Releasing Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction is executed
	0	1	Interrupt servicing is executed
	1	×	STOP mode is held
$\overline{\text{RESET}}$ input	–	–	Reset processing

×: don't care

CHAPTER 17 RESET FUNCTION

The following two operations are available to generate reset signals.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by program loop time detection with watchdog timer

External and internal resets have no functional differences. In both cases, program execution starts at addresses 0000H and 0001H by reset signal input.

When a low level is input to the $\overline{\text{RESET}}$ pin or the watchdog timer overflows, a reset is applied and each hardware item is set to the status shown in Table 17-1. Each pin is high impedance during reset input or during the oscillation stabilization time just after reset clear.

When a high level is input to the $\overline{\text{RESET}}$ pin, the reset is cleared and program execution is started after the oscillation stabilization time has elapsed. The reset applied by the watchdog timer overflow is automatically cleared after reset, and program execution is started after the oscillation stabilization time has elapsed (refer to **Figures 17-2** to **17-4**).

Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.

2. When the STOP mode is cleared by reset, the STOP mode contents are held during reset input. However, the port pins become high impedance.

Figure 17-1. Block Diagram of Reset Function

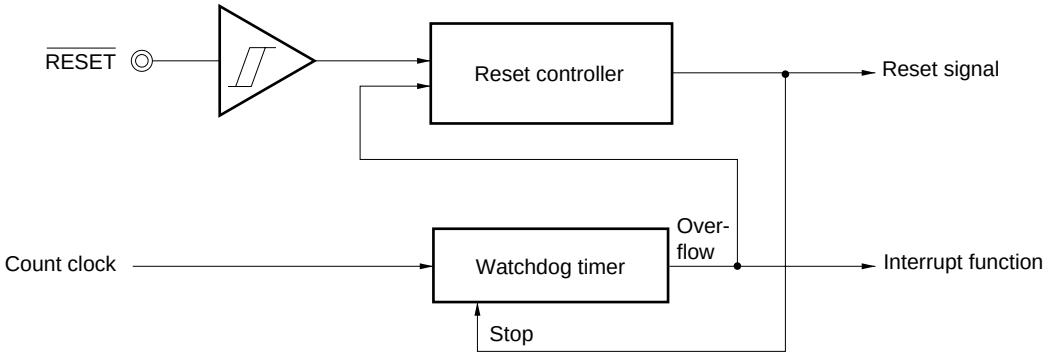


Figure 17-2. Reset Timing by $\overline{\text{RESET}}$ Input

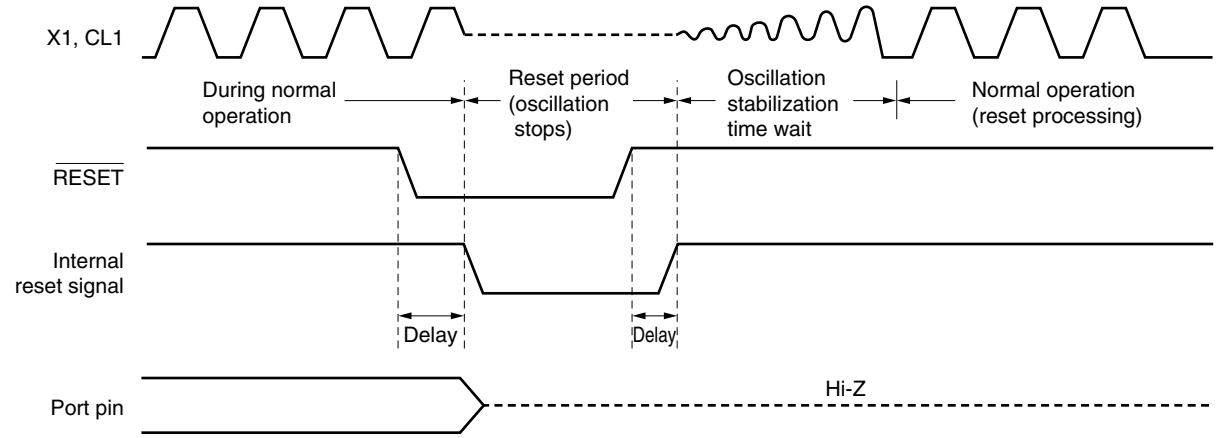


Figure 17-3. Reset Timing by Overflow in Watchdog Timer

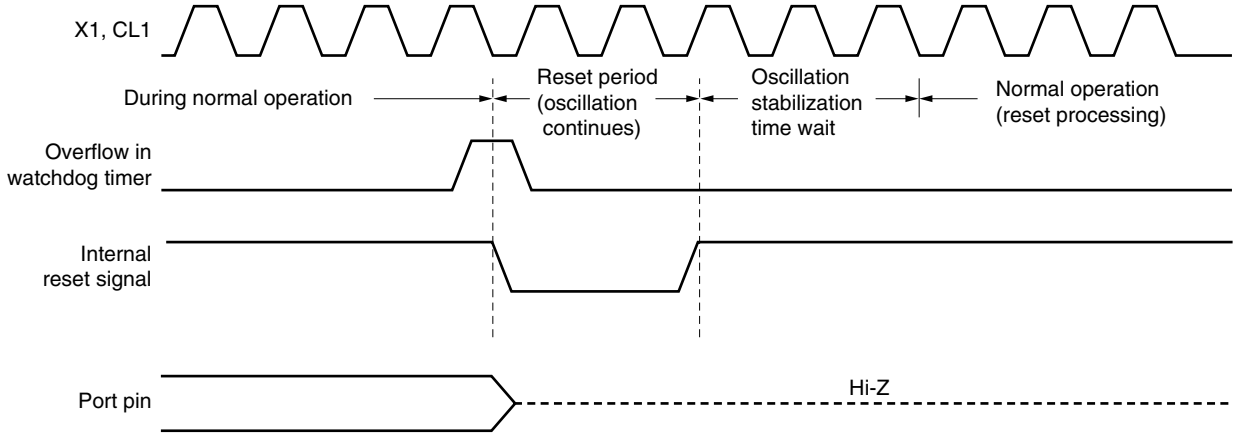


Figure 17-4. Reset Timing by $\overline{\text{RESET}}$ Input in STOP Mode

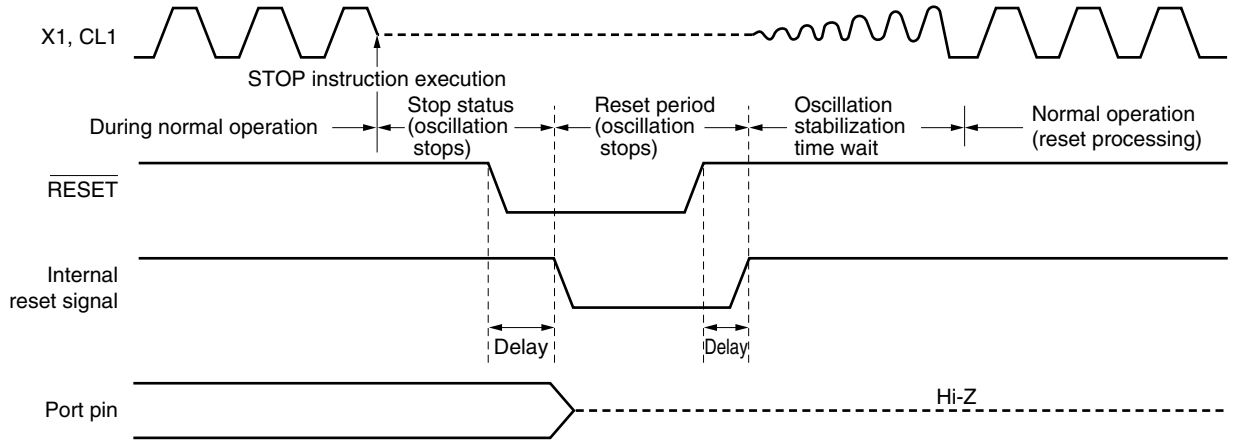


Table 17-1. Hardware Status After Reset (1/2)

Hardware		Status After Reset
Program counter (PC)[Note 1]		The contents of reset vector tables (0000H and 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Ports (P0 to P2, P5) (output latch)		00H
Port mode registers (PM0 to PM2, PM5)		FFH
Pull-up resistor option register 0 (PU0)		00H
Pull-up resistor option register B2 (PUB2)		00H
Processor clock control register (PCC)		02H
Oscillation stabilization time select register (OSTS)[Note 3]		04H
16-bit timer 20	Timer counter (TM20)	0000H
	Compare register (CR20)	FFFFH
	Mode control register (TMC20)	00H
	Capture register (TPC20)	Undefined
8-bit timer/event counter 80	Timer counter (TM80)	00H
	Compare register (CR80)	Undefined
	Mode control register (TMC80)	00H
Watchdog timer	Timer clock select register (TCL2)	00H
	Mode register (WDTM)	00H
A/D converter	Mode register (ADM0)	00H
	Input channel specification register (ADS0)	00H
	Conversion result register (ADCR0)	Undefined
Serial interface 20	Mode register (CSIM20)	00H
	Asynchronous serial interface mode register (ASIM20)	00H
	Asynchronous serial interface status register (ASIS20)	00H
	Baud rate generator control register (BRGC20)	00H
	Transmit shift register (TXS20)	FFH
	Receive buffer register (RXB20)	Undefined

Notes 1. During reset input and oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined.
All other hardware remains unchanged after reset.

2. If the reset signal is input in the standby mode, the status before reset is retained even after reset.

3. μPD789104A, 789114A Subseries only

Table 17-1. Hardware Status After Reset (2/2)

Hardware		Status After Reset
Multiplier	16-bit multiplication result storage register (MUL0)	Undefined
	Data register A (MRA0)	Undefined
	Data register B (MRB0)	Undefined
	Control register (MULC0)	00H
Interrupts	Request flag register (IF0, IF1)	00H
	Mask flag register (MK0, MK1)	FFH
	External interrupt mode register (INTM0)	00H

★ CHAPTER 18 μPD78F9116A, 78F9116B, 78F9136A, 78F9136B

The μPD78F9116A and 78F9116B are versions with flash memory instead of the internal ROM of the mask ROM versions in the μPD789104A and 789114A Subseries. The μPD78F9136A and 78F9136B are versions with flash memory instead of the internal ROM of the mask ROM versions in the μPD789124A and 789134A Subseries. The differences between the flash memory and the mask ROM versions are shown in Table 18-1.

Table 18-1. Differences Between Flash Memory and Mask ROM Versions

Item		Flash Memory	Mask ROM		
		μPD78F9116A μPD78F9116B	μPD789101A μPD789111A	μPD789102A μPD789112A	μPD789104A μPD789114A
		μPD78F9136A μPD78F9136B	μPD789121A μPD789131A	μPD789122A μPD789132A	μPD789124A μPD789134A
Internal memory	ROM	16 KB (flash memory)	2 KB	4 KB	8 KB
	High-speed RAM	256 bytes			
Pull-up resistors		12 (software control only)	16 (software control: 12, mask option specification: 4)		
V_{PP} pin		Provided	Not provided		
Electrical specifications		Refer to the relevant electrical specifications chapter.			

Cautions 1. There are differences in noise immunity and noise radiation between the flash memory versions and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM versions.

2. A/D conversion result register 0 (ADCR0) is manipulated by an 8-bit memory manipulation instruction or a 16-bit memory manipulation instruction, when used as an 8-bit A/D converter (μPD789104A, 789124A Subseries) or 10-bit A/D converter (μPD789114A, 789134A Subseries), respectively.

However, if the μPD78F9116A and 78F9116B are used as the flash memory versions of the μPD789101A, 789102A, and 789104A, ADCR0 can be manipulated by an 8-bit memory manipulation instruction, providing an object file has been assembled in the μPD789101A, 789102A, 789104A. If the μPD78F9136A and 78F9136B are used as the flash memory versions of the μPD789121A, 789122A, and 789124A, ADCR0 can be manipulated by an 8-bit memory manipulation instruction, providing an object file has been assembled in the μPD789121A, 789122A, or 789124A.

18.1 Flash Memory Characteristics

Flash memory programming is performed by connecting a dedicated flash programmer (Flashpro III (part no. FL-PR3, PG-FP3)/Flashpro IV (part no. FL-PR4, PG-FP4)) to the target system with the flash memory mounted on the target system (on-board programming). A flash memory writing adapter (program adapter), which is a target board used exclusively for programming, is also provided.

Remark FL-PR3, FL-PR4, and the program adapter are products of Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Programming using flash memory has the following advantages.

- Software can be modified after the microcontroller is solder-mounted on the target system.
- Distinguishing software facilities low-quantity, varied model production
- Easy data adjustment when starting mass production

18.1.1 Programming environment

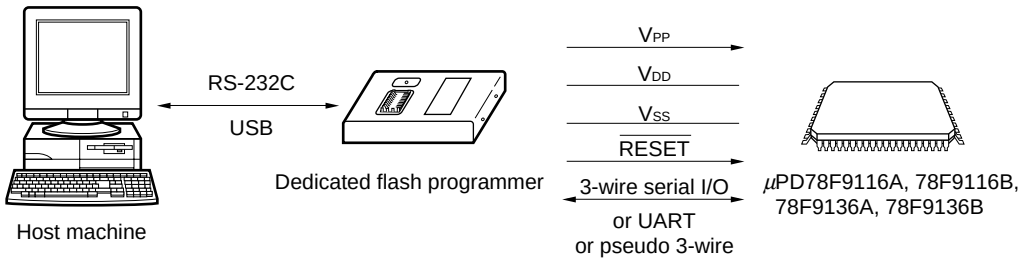
The following shows the environment required for μPD78F9116A, 78F9116B, 78F9136A, and 78F9136B flash memory programming.

When Flashpro III (part no. FL-PR3, PG-FP3) or Flashpro IV (Part no. FL-PR4, PG-FP4) is used as a dedicated flash programmer, a host machine is required to control the dedicated flash programmer. Communication between the host machine and flash programmer is performed via RS-232C/USB (Rev. 1.1).

For details, refer to the manuals for Flashpro III/Flashpro IV.

Remark USB is supported by Flashpro IV only.

Figure 18-1. Environment for Writing Program to Flash Memory



18.1.2 Communication mode

Use the communication mode shown in Table 18-2 or 18-3 to perform communication between the dedicated flash programmer and the μPD78F9116A, 78F9116B, 78F9136A, or 78F9136B.

Table 18-2. Communication Mode List (μPD78F9116A, 78F9136A)

Communication Mode	TYPE Setting[Note 1]					Pins Used[Note 2]	Number of V_{PP} Pulses
	COMM PORT	SIO Clock	CPU Clock	Flash Clock	Multiple Rate		
3-wire serial I/O (SIO3)	SIO ch-0 (3-wire, sync.)	100 Hz to 1.25 MHz[Note 3]	Optional	1 to 5 MHz[Note 3]	1.0	$\overline{SCK20}$/ASCK20/P20 SO20/TxD20/P21 SI20/RxD20/P22	0
UART (UART0)	UART ch-0	4800 to 76800 bps[Note 3, 4]	Optional[Note 5]	4.91 or 5 MHz[Note 3]	1.0	TxD20/SO20/P21 RxD20/SI20/P22	8
Pseudo 3-wire	Port A (pseudo 3-wire)	100 Hz to 1 MHz[Note 3]	Optional	1 to 5 MHz[Note 3]	1.0	P00 P01 P02	12

Table 18-3. Communication Mode List (μPD78F9116B, 78F9136B)

Communication Mode	TYPE Setting[Note 1]					Pins Used[Note 2]	Number of V_{PP} Pulses
	COMM PORT	SIO Clock	CPU Clock	Flash Clock	Multiple Rate		
3-wire serial I/O	SIO ch-0 (3-wire, sync.)	100 Hz to 1.25 MHz[Note 3]	Optional	1 to 10 MHz[Note 3]	1.0	$\overline{SCK20}$/ASCK20/P20 SO20/TxD20/P21 SI20/RxD20/P22	0
	SIO ch-1 (3-wire, sync.)					P00 P01 P02	1
UART	UART ch-0	4800 to 76800 bps[Note 3, 4]	Optional[Note 5]	4.91, 5, or 10 MHz[Note 3]	1.0	TxD20/SO20/P21 RxD20/SI20/P22	8

Notes 1. Selection items for TYPE settings on the dedicated flash programmer (Flashpro III/Flashpro IV).

2. When the system shifts to the flash memory programming mode, all the pins that are not used for flash memory programming are in the same status as that immediately after reset. If the external device connected to each port does not recognize the status of the port immediately after reset, pins require appropriate processing, such as connecting to V_{DD} or V_{SS} via a resistor.

3. The possible setting range differs depending on the voltage. For details, refer to the relevant electrical specifications chapter.

4. Because signal wave slew also affects UART communication, in addition to the baud rate error, thoroughly evaluate the slew.

5. Only for Flashpro IV. However, when using Flashpro III, be sure to select the clock of the resonator on the board. UART cannot be used with the clock supplied by Flashpro III.

Caution Be sure to select the communication mode according to the number of V_{PP} pulses shown in Table 18-2 or 18-3.

Figure 18-2. Communication Mode Selection Format

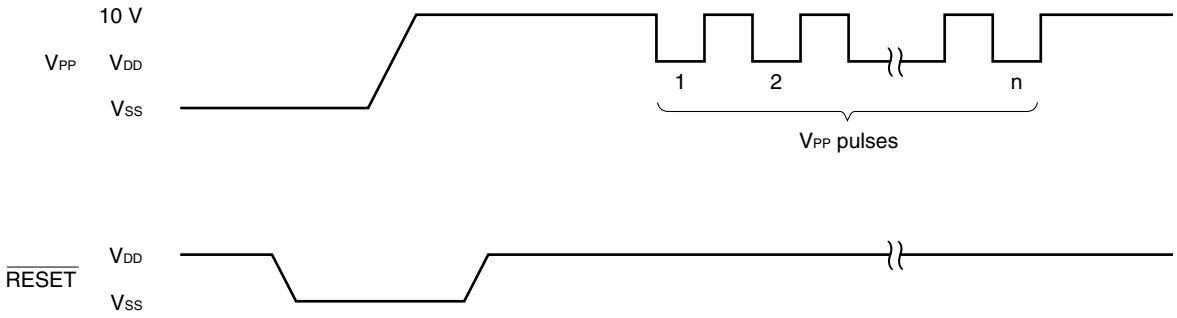
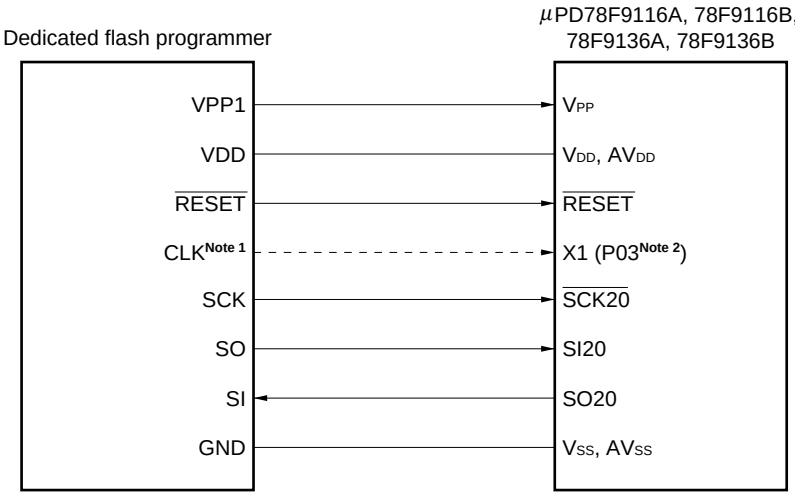
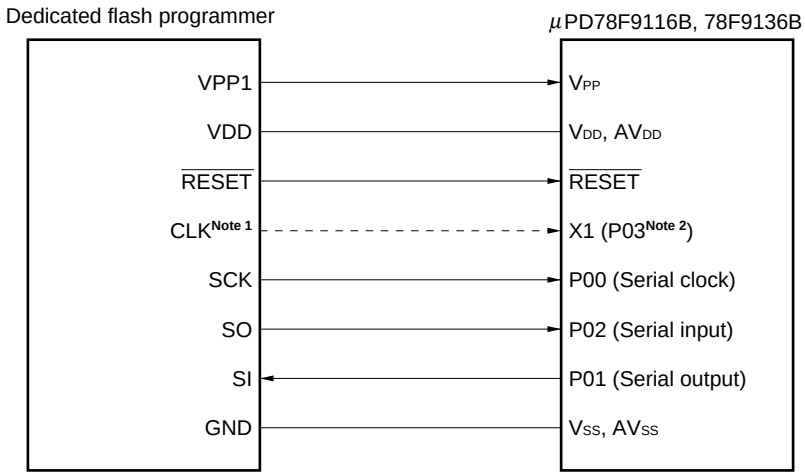


Figure 18-3. Example of Connection with Dedicated Flash Programmer (1/2)

(a) 3-wire serial I/O mode (SIO ch-0)



(b) 3-wire serial I/O mode (SIO ch-1) (μPD78F9116B, 78F9136B only)



Notes 1. Connect this pin when the system clock is supplied by the dedicated flash programmer. When a resonator has already been connected to the X1 pin, the CLK pin does not need to be connected.

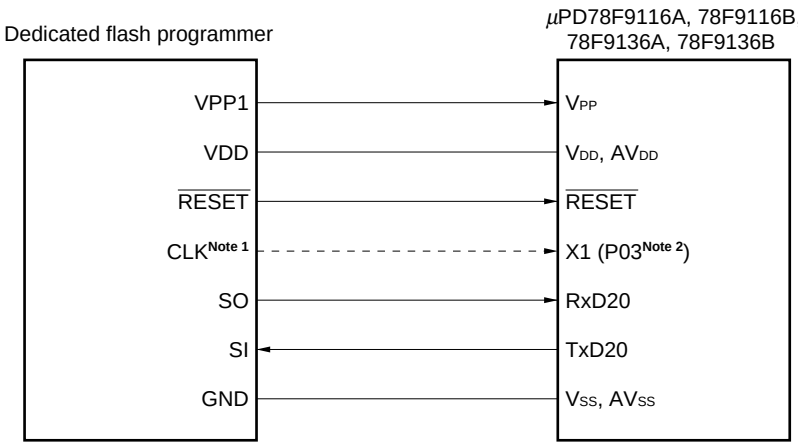
2. μPD78F9136A, 78F9136B only

Cautions 1. The V_{DD} pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the V_{DD} pin, supply voltage before starting programming.

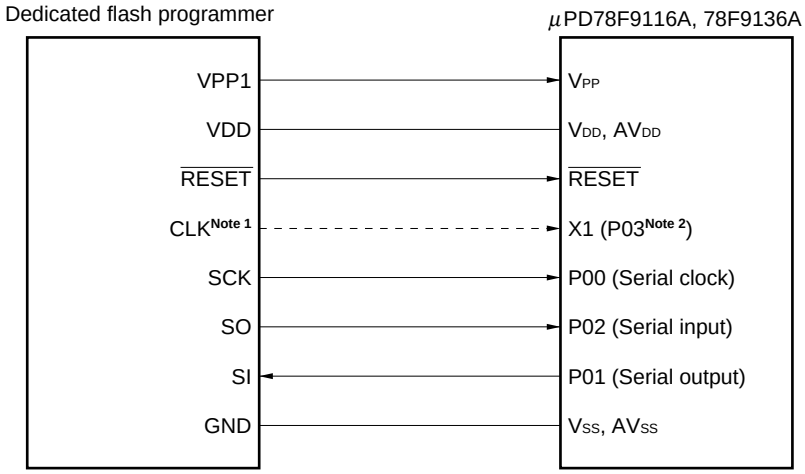
2. In the μPD78F9136A and 78F9136B, use the P03 pin as the pin for system clock input from the dedicated flash programmer.

Figure 18-3. Example of Connection with Dedicated Flash Programmer (2/2)

(c) UART mode



(d) Pseudo 3-wire mode (μPD78F9116A, 78F9136A only)



Notes 1. Connect this pin when the system clock is supplied by the dedicated flash programmer. When a resonator has already been connected to the X1 pin, the CLK pin does not need to be connected.

2. μPD78F9136A, 78F9136B only

Cautions 1. The V_{DD} pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the V_{DD} pin, supply voltage before starting programming.

2. In the μPD78F9136A and 78F9136B, use the P03 pin as the pin for system clock input from the dedicated flash programmer.

If Flashpro III/Flashpro IV is used as the dedicated flash programmer, the following signals are generated for the μPD78F9116A, 78F9116B, 78F9136A, and 78F9136B. For details, refer to the manual of Flashpro III/Flashpro IV.

Table 18-4. Pin Connection List

Signal Name	I/O	Pin Function	Pin Name	3-Wire Serial I/O	UART	Pseudo 3-Wire
VPP1	Output	Write voltage	V_{PP}	◎	◎	◎
VPP2	–	–	–	×	×	×
VDD	I/O	V_{DD} voltage generation/ voltage monitoring	V_{DD}/AV_{DD}	◎ Note 1	◎ Note 1	◎ Note 1
GND	–	Ground	V_{SS}/AV_{SS}	◎	◎	◎
CLK	Output	Clock output	X1 (P03 Note 2)	○	○	○
RESET	Output	Reset signal	$\overline{RESET}$	◎	◎	◎
SI	Input	Reception signal	SO20/P01/TxD20	◎	◎	◎
SO	Output	Transmit signal	SI20/P02/RxD20	◎	◎	◎
SCK	Output	Transfer clock	SCK20/P00	◎	×	◎
HS	–	–	–	×	×	×

Notes 1. V_{DD} voltage must be supplied before programming is started.

2. μPD78F9136A, 78F9136B only

Remark ◎: Pin must be connected.

○: If the signal is supplied on the target board, pin does not need to be connected.

×: Pin does not need to be connected.

18.1.3 On-board pin processing

When performing programming on the target system, provide a connector on the target system to connect the dedicated flash programmer.

An on-board function that allows switching between normal operation mode and flash memory programming mode may be required in some cases.

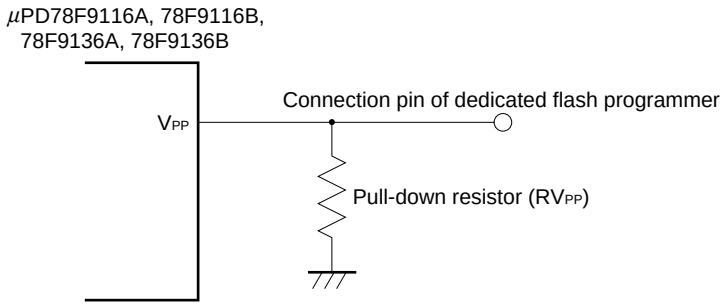
<V_{PP} pin>

In normal operation mode, input 0 V to the V_{PP} pin. In flash memory programming mode, a write voltage of 10.0 V (TYP.) is supplied to the V_{PP} pin, so perform the following.

(1) Connect a pull-down resistor (RV_{PP} = 10 kΩ) to the V_{PP} pin.
(2) Use the jumper on the board to switch the V_{PP} pin input to either the programmer or directly to GND.

A V_{PP} pin connection example is shown below.

Figure 18-4. V_{PP} Pin Connection Example



<Serial interface pins>

The following shows the pins used by the serial interface.

<μPD78F9116A, 78F9136A>

Serial Interface	Pins Used
3-wire serial I/O	$\overline{SCK20}$, SO20, SI20
UART	TxD20, RxD20
Pseudo 3-wire	P00, P01, P02

<μPD78F9116B, 78F9136B>

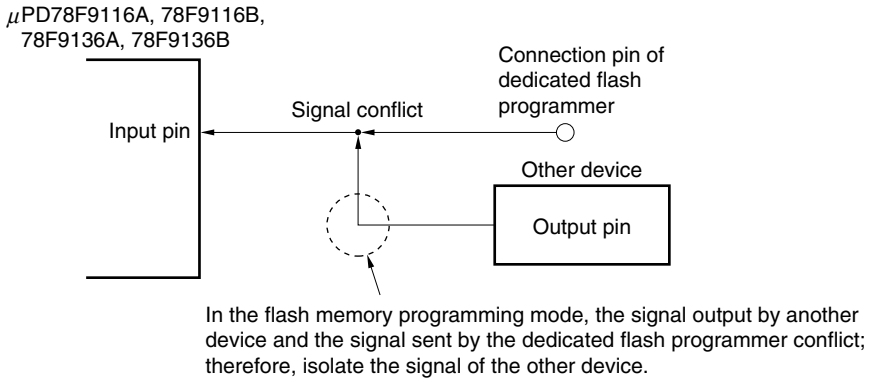
Serial Interface	Pins Used
3-wire serial I/O	$\overline{SCK20}$, SO20, SI20
	P00, P01, P02
UART	TxD20, RxD20

When connecting the dedicated flash programmer to a serial interface pin that is connected to another device on-board, signal conflict or abnormal operation of the other device may occur. Care must therefore be taken with such connections.

(1) Signal conflict

If the dedicated flash programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a signal conflict occurs. To prevent this, isolate the connection with the other device or set the other device to the output high impedance status.

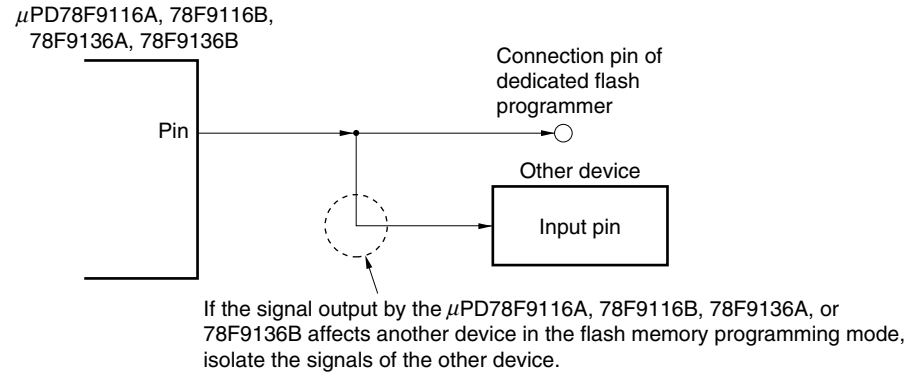
Figure 18-5. Signal Conflict (Input Pin of Serial Interface)

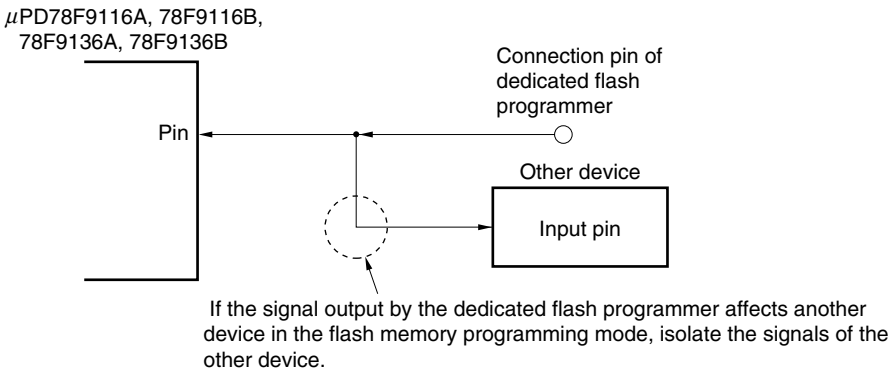


(2) Abnormal operation of other device

If the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), a signal is output to the device, and this may cause an abnormal operation. To prevent this abnormal operation, isolate the connection with the other device or set so that the input signals to the other device are ignored.

Figure 18-6. Abnormal Operation of Other Device



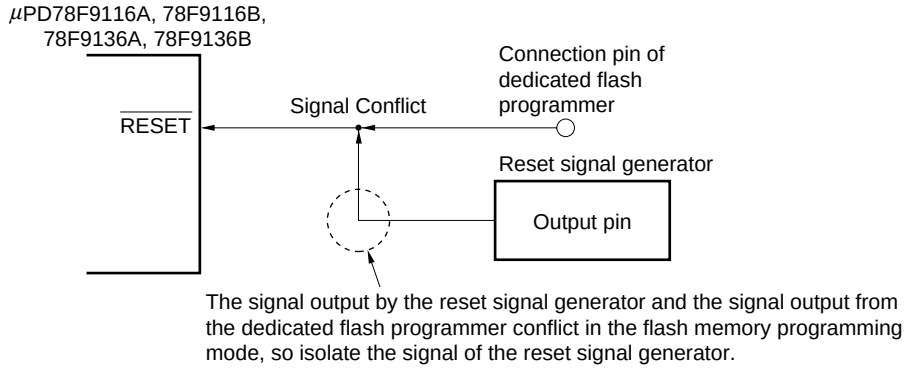


<$\overline{\text{RESET}}$ pin>

If the reset signal of the dedicated flash programmer is connected to the $\overline{\text{RESET}}$ pin connected to the reset signal generator on-board, a signal conflict occurs. To prevent this, isolate the connection with the reset signal generator.

If the reset signal is input from the user system in the flash memory programming mode, a normal programming operation cannot be performed. Therefore, do not input reset signals from other than the dedicated flash programmer.

Figure 18-7. Signal Conflict ($\overline{\text{RESET}}$ Pin)



<Port pins>

When the flash memory programming mode is set, all the pins other than those that communicate with the flash programmer are in the same status as immediately after reset.

If the external device does not recognize initial statuses such as the output high impedance status, therefore, connect the external device to V_{DD} or V_{SS}.

<Oscillation pins>

When using the on-board clock, connect X1 and X2 as required in the normal operation mode.

When using the clock output of the flash programmer, connect it directly to X1, disconnecting the main resonator on-board, and leave the X2 pin open.

<Power supply>

When using the power supply output of the flash programmer, connect the V_{DD} and V_{SS} pins to VDD and GND of the flash programmer, respectively.

When using the on-board power supply, connect it as required in the normal operation mode. Because the flash programmer monitors the voltage, however, VDD of the flash programmer must be connected.

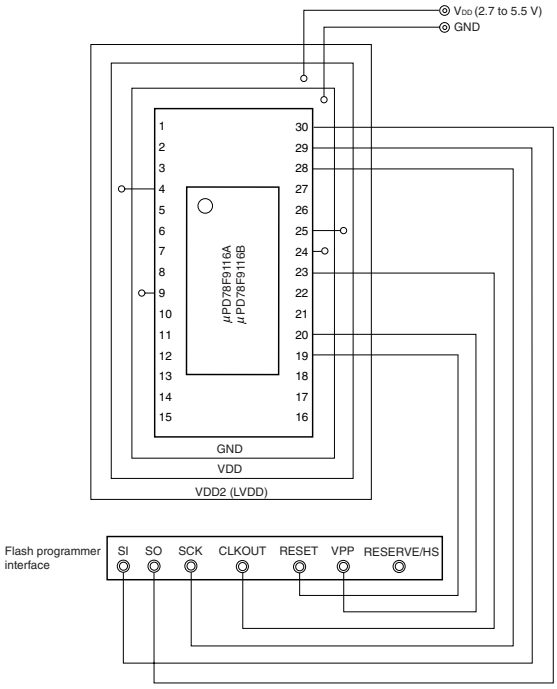
For the other power pins (AV_{DD} and A_{SS}), supply the same power supply as in the normal operation mode.

18.1.4 Connection when using flash memory writing adapter

The following shows an example of the recommended connection when using the flash memory writing adapter.

Figure 18-8. Example of Flash Memory Writing Adapter Connection When Using 3-Wire Serial I/O Mode (SIO-ch0)

(a) μPD78F9116A, 78F9116B



(b) μPD78F9136A, 78F9136B

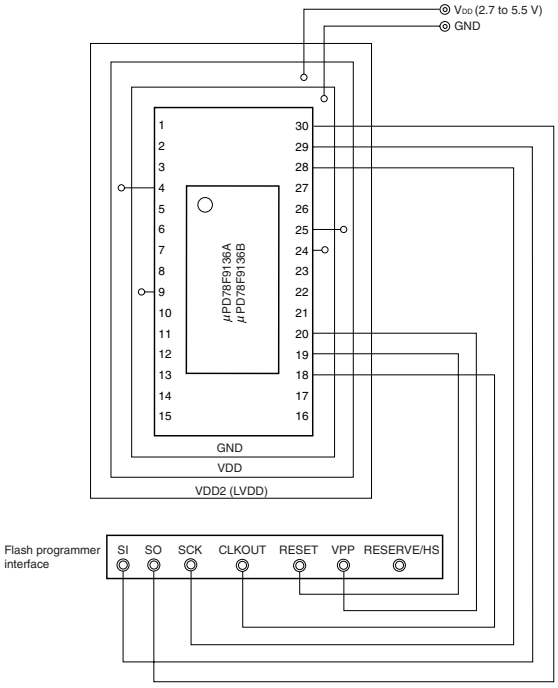
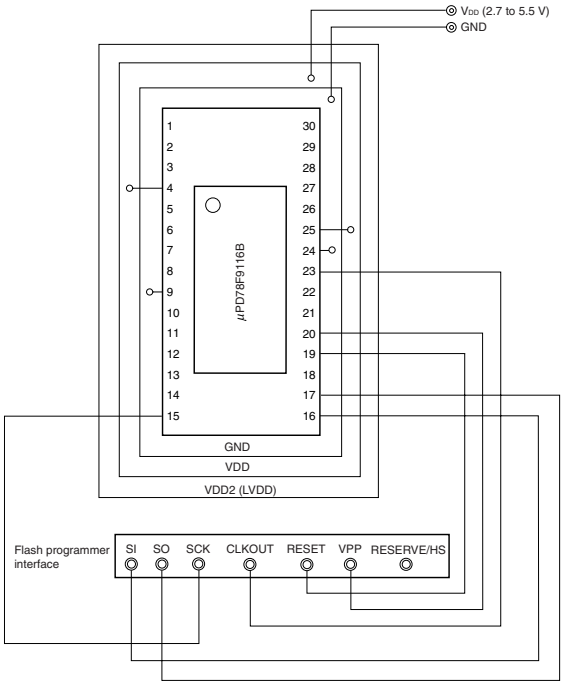


Figure 18-9. Example of Flash Memory Writing Adapter Connection When Using 3-Wire Serial I/O Mode (SIO-ch1)

(a) μPD78F9116B



(b) μPD78F9136B

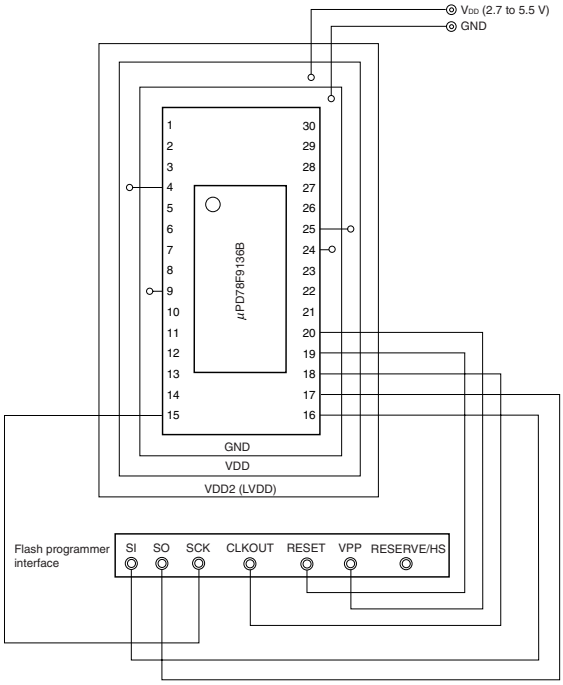
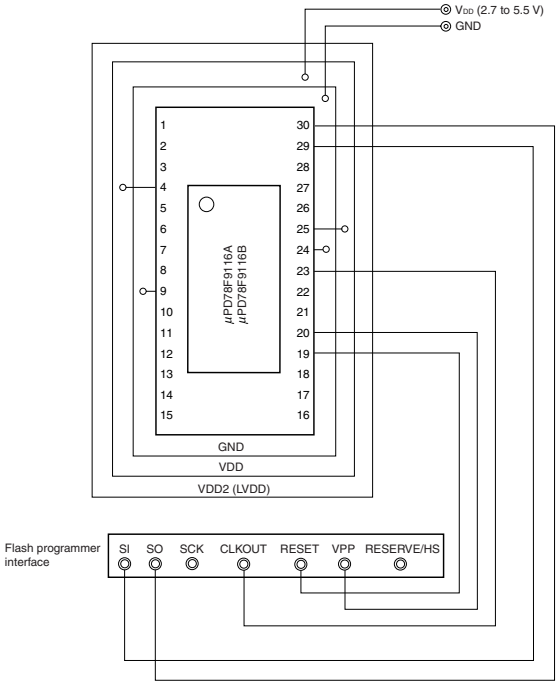


Figure 18-10. Example of Flash Memory Writing Adapter Connection When Using UART Mode

(a) μPD78F9116A, 78F9116B



(b) μPD78F9136A, 78F9136B

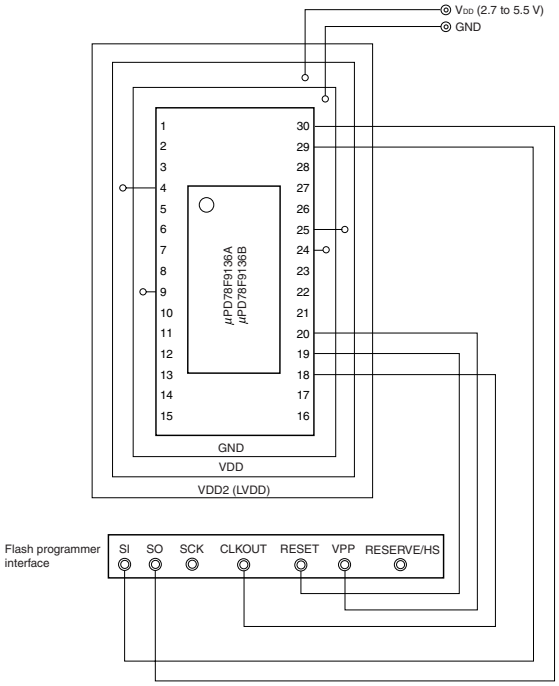
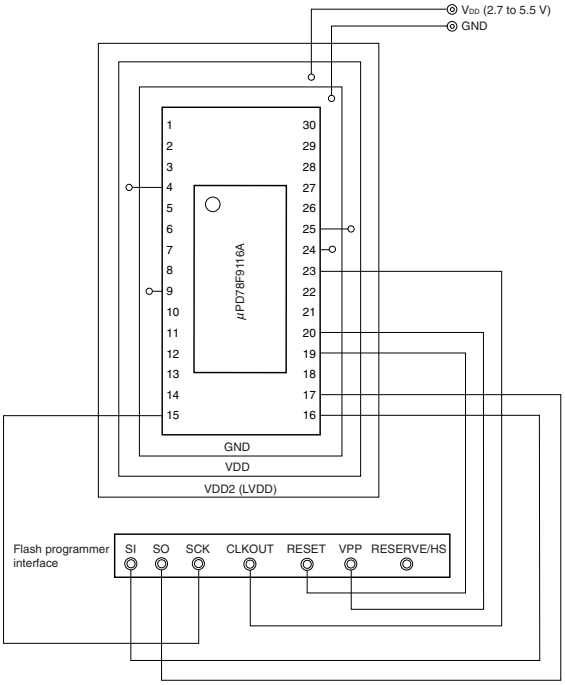
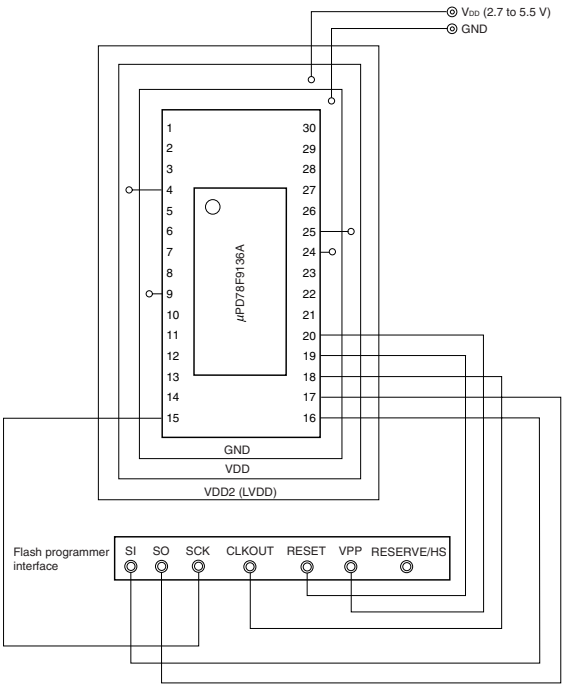


Figure 18-11. Example of Flash Memory Writing Adapter Connection When Using Pseudo 3-Wire Mode

(a) μPD78F9116A



(b) μPD78F9136A



CHAPTER 19 MASK OPTION (MASK ROM VERSION)

Table 19-1. Selection of Mask Option for Pins

Pin	Mask Option
P50 to P53	On-chip pull-up resistor can be specified in 1-bit units.

For P50 to P53 (port 5), an on-chip pull-up resistor can be specified by the mask option. The mask option is specified in 1-bit units.

Caution The flash memory versions do not provide the on-chip pull-up resistor function.

CHAPTER 20 INSTRUCTION SET

This chapter lists the instruction set of the μPD789104A/114A/124A/134A Subseries. For details of the operation and machine language (instruction code) of each instruction, refer to the **78K/0S Series Instructions User's Manual (U11047E)**.

20.1 Operation

20.1.1 Operand identifiers and description methods

Operands are described in the "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Uppercase letters and the symbols #, !, $, and [ ] are keywords and are described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $ and [ ] symbols.

For the operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 20-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special-function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or labels FE20H to FF1FH Immediate data or labels (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or labels (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or labels (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

Remark Refer to **Table 4-3 Special-Function Register List** for the symbols of the special-function registers.

20.1.2 Description of “operation” column

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Flag indicating non-maskable interrupt servicing in progress
( ):	Memory contents indicated by address or register contents in parentheses
×H, ×L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
∀:	Exclusive logical sum (exclusive OR)
¯:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

20.1.3 Description of “flag operation” column

(Blank):	Unchanged
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is restored

20.2 Operation List

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r[Note 1]	2	4	A ← r			
	r, A[Note 1]	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL+byte]	2	6	A ← (HL+byte)			
	[HL+byte], A	2	6	(HL+byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r[Note 2]	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ sfr			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL+byte]	2	8	A ↔ (HL+byte)			

Notes 1. Except r = A.

2. Except r = A, X.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp[Note]	1	4	AX ← rp			
	rp, AX[Note]	1	4	rp ← AX			
XCHW	AX, rp[Note]	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL+byte]	2	6	A, CY ← A + (HL+byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL+byte]	2	6	A, CY ← A + (HL+byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL+byte]	2	6	A, CY ← A – (HL+byte)	×	×	×

Note Only when rp = BC, DE, or HL.

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL+byte]	2	6	A, CY ← A – (HL+byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL+byte]	2	6	A ← A ∧ (HL+byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL+byte]	2	6	A ← A ∨ (HL+byte)	×		
XOR	A, #byte	2	4	A ← A ∀ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∀ byte	×		
	A, r	2	4	A ← A ∀ r	×		
	A, saddr	2	4	A ← A ∀ (saddr)	×		
	A, !addr16	3	8	A ← A ∀ (addr16)	×		
	A, [HL]	1	6	A ← A ∀ (HL)	×		
	A, [HL+byte]	2	6	A ← A ∀ (HL+byte)	×		

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL+byte]	2	6	A – (HL+byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
ROL	A, 1	1	2	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
RORC	A, 1	1	2	(CY ← A_0, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operands	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CALL	!addr16	3	6	$(SP - 1) \leftarrow (PC + 3)_H$, $(SP - 2) \leftarrow (PC + 3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP - 2$			
CALLT	[addr5]	1	8	$(SP - 1) \leftarrow (PC + 1)_H$, $(SP - 2) \leftarrow (PC + 1)_L$, $PC_H \leftarrow$ (00000000, addr5 + 1), $PC_L \leftarrow$ (00000000, addr5), $SP \leftarrow SP - 2$			
RET		1	6	$PC_H \leftarrow (SP + 1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP + 2$			
RETI		1	8	$PC_H \leftarrow (SP + 1)$, $PC_L \leftarrow (SP)$, PSW $\leftarrow (SP + 2)$, $SP \leftarrow SP + 3$, NMIS $\leftarrow 0$	R	R	R
PUSH	PSW	1	2	$(SP - 1) \leftarrow$ PSW, $SP \leftarrow SP - 1$			
	rp	1	4	$(SP - 1) \leftarrow rp_H$, $(SP - 2) \leftarrow rp_L$, $SP \leftarrow SP - 2$			
POP	PSW	1	4	PSW $\leftarrow (SP)$, $SP \leftarrow SP + 1$	R	R	R
	rp	1	6	$rp_H \leftarrow (SP + 1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP + 2$			
MOVW	SP, AX	2	8	$SP \leftarrow$ AX			
	AX, SP	2	6	AX $\leftarrow$ SP			
BR	!addr16	3	6	PC $\leftarrow$ addr16			
	$addr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8			
	AX	1	6	$PC_H \leftarrow$ A, $PC_L \leftarrow$ X			
BC	$addr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if CY = 0			
BZ	$saddr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if Z = 1			
BNZ	$saddr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if Z = 0			
BT	saddr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if (saddr.bit) = 1			
	sfr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if sfr.bit = 1			
	A.bit, $addr16	3	8	PC $\leftarrow$ PC + 3 + jdisp8 if A.bit = 1			
	PSW.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if PSW.bit = 1			
BF	saddr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if (saddr.bit) = 0			
	sfr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if sfr.bit = 0			
	A.bit, $addr16	3	8	PC $\leftarrow$ PC + 3 + jdisp8 if A.bit = 0			
	PSW.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if PSW.bit = 0			
DBNZ	B, $addr16	2	6	B $\leftarrow$ B $-$ 1, then PC $\leftarrow$ PC + 2 + jdisp8 if B $\neq 0$			
	C, $addr16	2	6	C $\leftarrow$ C $-$ 1, then PC $\leftarrow$ PC + 2 + jdisp8 if C $\neq 0$			
	saddr, $addr16	3	8	(saddr) $\leftarrow$ (saddr) $-$ 1, then PC $\leftarrow$ PC + 3 + jdisp8 if (saddr) $\neq 0$			
NOP		1	2	No Operation			
EI		3	6	IE $\leftarrow$ 1 (Enable Interrupt)			
DI		3	6	IE $\leftarrow$ 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

20.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV[Note] XCH[Note] ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											
[HL+byte]		MOV											

Note Except r = A.

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	saddrp	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	
rp	MOVW	MOVW[Note]				INCW DECW PUSH POP
saddrp		MOVW				
SP		MOVW				

Note Only when rp = BC, DE, or HL.

(3) Bit manipulation instructions

SET1, CLR1, NOT1, BT, BF

1st Operand \ 2nd Operand	$addr16	None
A.bit	BT BF	SET1 CLR1
sfr.bit	BT BF	SET1 CLR1
saddr.bit	BT BF	SET1 CLR1
PSW.bit	BT BF	SET1 CLR1
[HL].bit		SET1 CLR1
CY		SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLT, BR, BC, BNC, BZ, BNZ, DBNZ

2nd Operand / 1st Operand	AX	!addr16	[addr5]	$addr16
Basic instructions	BR	CALL BR	CALLT	BR BC BNC BZ BNZ
Compound instructions				DBNZ

(5) Other instructions

RET, RETI, NOP, EI, DI, HALT, STOP

★ CHAPTER 21 ELECTRICAL SPECIFICATIONS (μPD78910xA, 78911xA, 78910xA(A), 78911xA(A)) (EXPANDED-SPECIFICATION PRODUCTS)

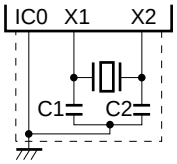
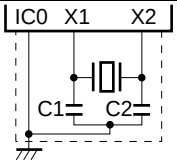
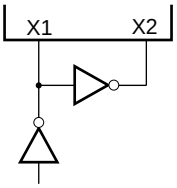
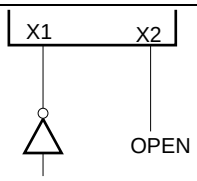
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
			With an on-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78910xA, 78911xA	–10	mA
		Total for all pins		–30	mA
		Per pin	μPD78910xA(A), 78911xA(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	μPD78910xA, 78911xA	30	mA
		Total for all pins		160	mA
		Per pin	μPD78910xA(A), 78911xA(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		10	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		10	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		10	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	45		500	ns
			V_{DD} = 3.0 to 5.5 V	75		500	ns
			V_{DD} = 1.8 to 5.5 V	85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use a resonator that stabilizes oscillation during the oscillation wait time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

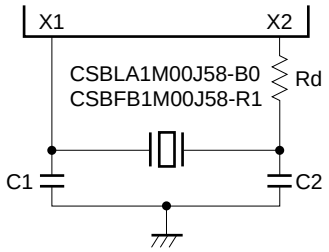
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

Ceramic resonator (T_A = –40 to +85°C)
(μPD78910xA, 78911xA, 78910xA(A), 78911xA(A)) (Expanded-specification products)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSBLA1M00J58-B0[Note]	1.0	100	100	2.1	5.5	Rd = 2.2 kΩ
	CSBFB1M00J58-R1[Note]						
	CSTCC2M00G56-R0	2.0	–	–	1.8		On-chip capacitor version
	CSTLS2M00G56-B0						
	CSTCR4M00G53-R0	4.0					
	CSTLS4M00GG53-B0						
	CSTCR4M19G53-R0	4.194					
	CSTLS4M19GG53-B0						
	CSTCR4M91G53-R0	4.915					
	CSTLS4M91GG53-B0						
	CSTCR5M00G53-R0	5.0					
	CSTLS5M00GG53-B0						
	CSTCR6M00G53-R0	6.0					
	CSTLS6M00GG53-B0						
	CSTCE8M00G52-R0	8.0					
	CSTLS8M00G53-B0						
	CSTCE8M38G52-R0	8.388					
	CSTLS8M38G53-B0						
	CSTCE10M0G52-R0	10.0					
	CSTLS10M00G53-B0						

Note A limiting resistor (Rd = 2.2 kΩ) is required when the CSBLA1M00J58-B0 and CSBFB1M00J58-R1 (1.0 MHz) of Murata Mfg. Co., Ltd. are used as ceramic resonators (see the figure below). A limiting resistor is not necessary when other recommended resonators are used.



Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer. If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the μPD78910xA, 78911xA, 78910xA(A), and 78911xA(A) so that the internal operating conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78910xA, 78911xA				–1	mA
		Total for all pins					–15	mA
		Per pin	μPD78910xA(A), 78911xA(A)				–1	mA
		Total for all pins					–11	mA
Output current, low	I_{OL}	Per pin	μPD78910xA, 78911xA				10	mA
		Total for all pins					80	mA
		Per pin	μPD78910xA(A), 78911xA(A)				3	mA
		Total for all pins					60	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
			With on-chip pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78910xA, 78911xA)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78910xA(A), 78911xA(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78910xA, 78911xA)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78910xA(A), 78911xA(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than X1, X2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than X1, X2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63		50	100	200	kΩ
Mask option pull-up resistance	R_2	V_I = 0 V, P50 to P53		10	30	60	kΩ
Power supply current	I_{DD1} Note 2	10.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10% Note 4		3.2	8.0	mA
		6.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10% Note 4		2.0	4.7	mA
		5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.8	3.2	mA
			V_{DD} = 3.0 V ±10% Note 5		0.45	0.9	mA
			V_{DD} = 2.0 V ±10% Note 5		0.25	0.45	mA
	I_{DD2} Note 2	10.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10% Note 4		1.5	3.0	mA
		6.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10% Note 4		0.9	1.8	mA
		5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		0.8	1.6	mA
			V_{DD} = 3.0 V ±10% Note 5		0.3	0.6	mA
			V_{DD} = 2.0 V ±10% Note 5		0.15	0.3	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			V_{DD} = 2.0 V ±10%		0.05	5.0	μA
	I_{DD4} Note 3	10.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ±10% Note 4		4.4	10.3	mA
		6.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ±10% Note 4		3.2	7.0	mA
		5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	5.5	mA
			V_{DD} = 3.0 V ±10% Note 5		1.65	3.2	mA
			V_{DD} = 2.0 V ±10% Note 5		1.25	2.7	mA

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by the mask option) and when port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

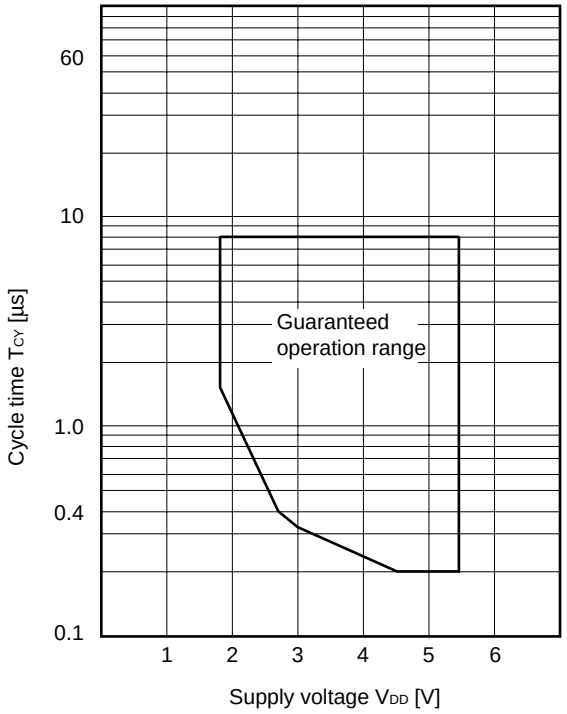
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 4.5 to 5.5 V	0.2		8	μs
		V_{DD} = 3.0 to 5.5 V	0.33		8	μs
		V_{DD} = 2.7 to 5.5 V	0.4		8	μs
		V_{DD} = 1.8 to 5.5 V	1.6		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 – 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 – 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

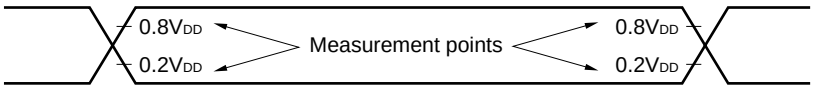
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

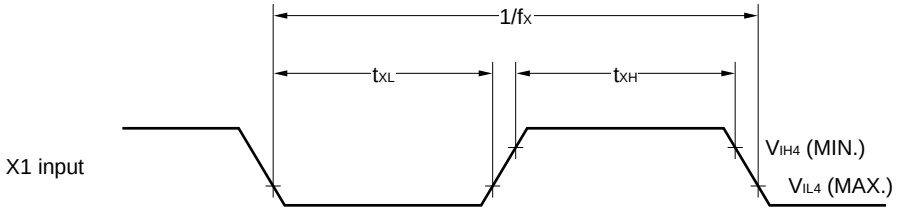
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

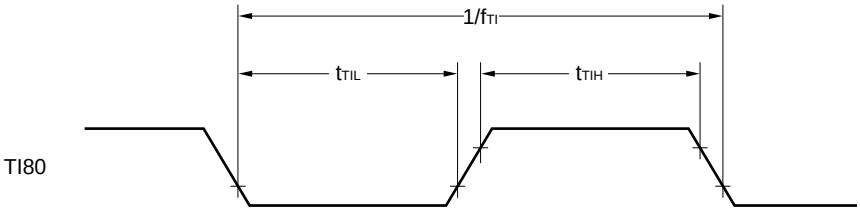
AC Timing Measurement Points (Excluding X1 Input)



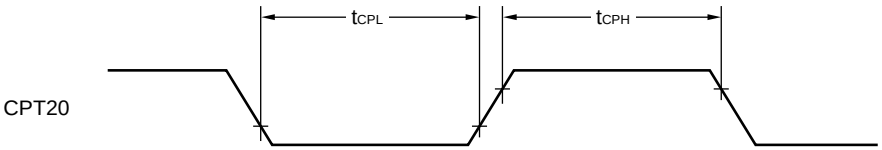
Clock Timing



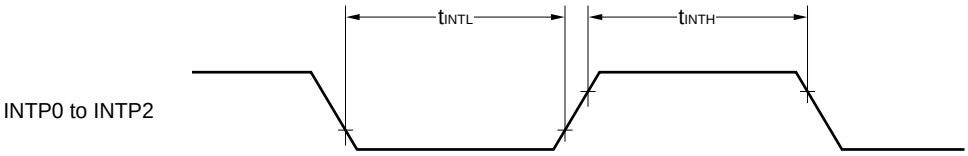
TI Timing



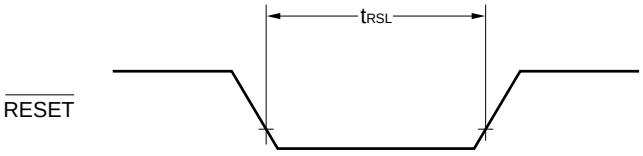
Capture Input Timing



Interrupt Input Timing

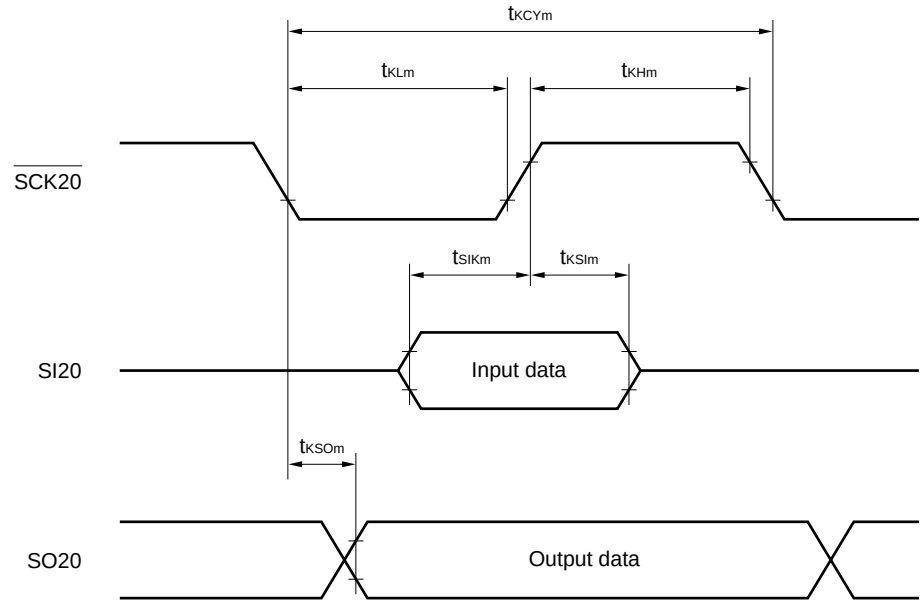


$\overline{\text{RESET}}$ Input Timing



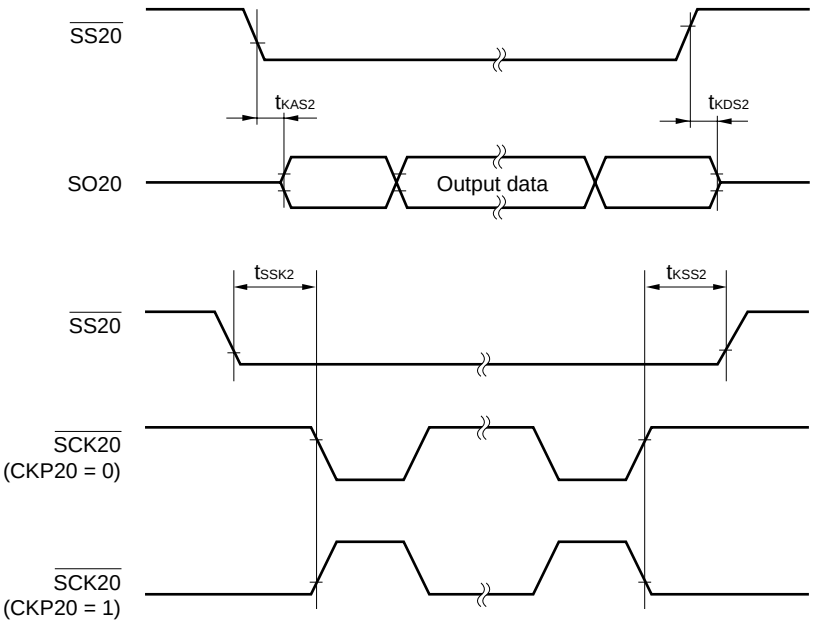
Serial Transfer Timing

3-wire serial I/O mode:

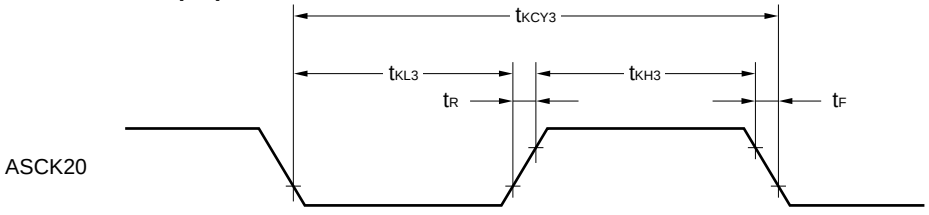


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78910xA, 78910xA(A))

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	Bits
Overall error[Notes 1, 2]		V_{DD} = 2.7 to 5.5 V		±0.4	±0.6	%FSR
		V_{DD} = 1.8 to 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	V_{DD} = 4.5 to 5.5 V	12		100	μs
		V_{DD} = 2.7 to 5.5 V	14		100	μs
		V_{DD} = 1.8 to 5.5 V	28		100	μs
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.2%).

2. This value is indicated as a ratio to the full-scale value (%FSR).

10-Bit A/D Converter Characteristics (μPD78911xA, 78911xA(A))

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ V_{DD} ≤ 5.5 V	12		100	μs
		2.7 V ≤ V_{DD} < 4.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

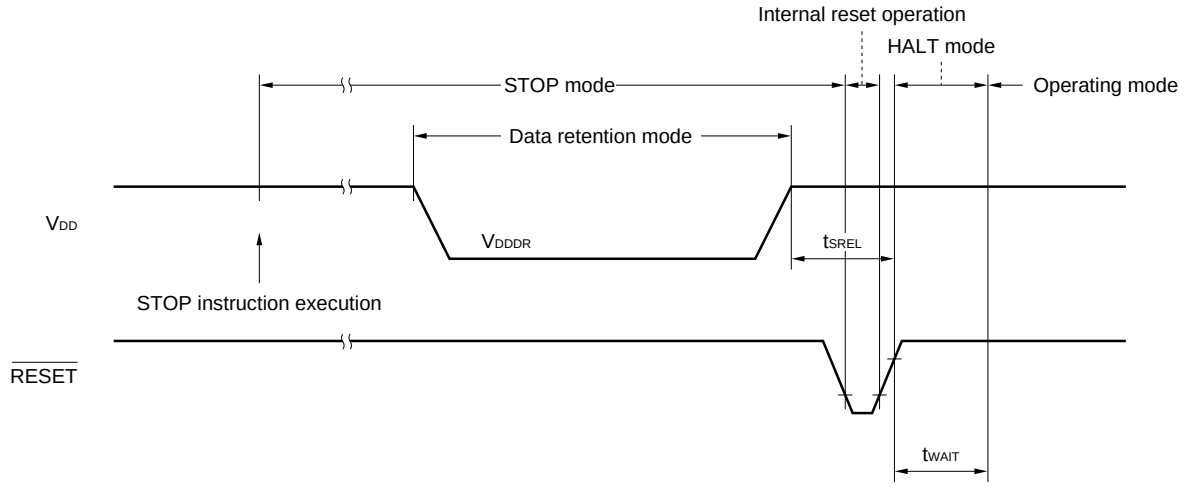
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

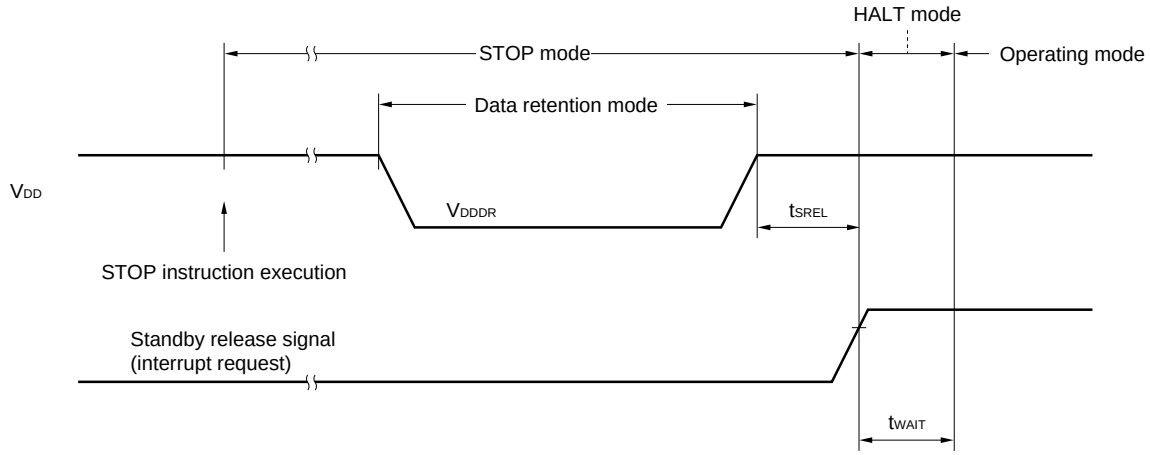
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



★ CHAPTER 22 ELECTRICAL SPECIFICATIONS (μPD78910xA, 78911xA, 78910xA(A), 78911xA(A)) (CONVENTIONAL-SPECIFICATION PRODUCTS)

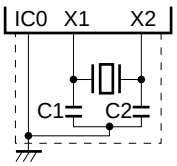
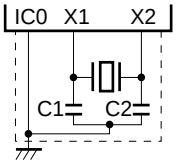
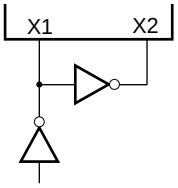
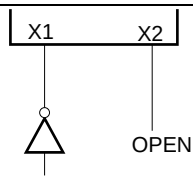
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
			With an on-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78910xA, 78911xA	–10	mA
		Total for all pins		–30	mA
		Per pin	μPD78910xA(A), 78911xA(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	μPD78910xA, 78911xA	30	mA
		Total for all pins		160	mA
		Per pin	μPD78910xA(A), 78911xA(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use a resonator that stabilizes oscillation during the oscillation wait time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

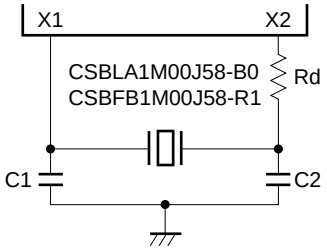
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

Ceramic resonator (T_A = –40 to +85°C)
(μPD78910xA, 78911xA, 78910xA(A), 78911xA(A)) (Conventional-specification products)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSBLA1M00J58-B0[Note]	1.0	100	100	2.1	5.5	Rd = 2.2 kΩ
	CSBFB1M00J58-R1[Note]						
	CSTCC2M00G56-R0	2.0	–	–	1.8		On-chip capacitor version
	CSTLS2M00G56-B0						
	CSTCR4M00G53-R0	4.0					
	CSTLS4M00GG53-B0						
	CSTCR4M19G53-R0	4.194					
	CSTLS4M19GG53-B0						
	CSTCR4M91G53-R0	4.915					
	CSTLS4M91GG53-B0						
	CSTCR5M00G53-R0	5.0					
	CSTLS5M00GG53-B0						

Note A limiting resistor (Rd = 2.2 kΩ) is required when the CSBLA1M00J58-B0 and CSBFB1M00J58-R1 (1.0 MHz) of Murata Mfg. Co., Ltd. are used as ceramic resonators (see the figure below). A limiting resistor is not necessary when other recommended resonators are used.



Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer. If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the μPD78910xA, 78911xA, 78910xA(A), and 78911xA(A) so that the internal operating conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78910xA, 78911xA				–1	mA
		Total for all pins					–15	mA
		Per pin	μPD78910xA(A), 78911xA(A)				–1	mA
		Total for all pins					–11	mA
Output current, low	I_{OL}	Per pin	μPD78910xA, 78911xA				10	mA
		Total for all pins					80	mA
		Per pin	μPD78910xA(A), 78911xA(A)				3	mA
		Total for all pins					60	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
			With on-chip pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78910xA, 78911xA)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78910xA(A), 78911xA(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78910xA, 78911xA)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78910xA(A), 78911xA(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than X1, X2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than X1, X2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63		50	100	200	kΩ
Mask option pull-up resistance	R_2	V_I = 0 V, P50 to P53		10	30	60	kΩ
Power supply current	I_{DD1} Note 2	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.8	3.2	mA
			V_{DD} = 3.0 V ±10% Note 5		0.45	0.9	mA
			V_{DD} = 2.0 V ±10% Note 5		0.25	0.45	mA
	I_{DD2} Note 2	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		0.8	1.6	mA
			V_{DD} = 3.0 V ±10% Note 5		0.3	0.6	mA
			V_{DD} = 2.0 V ±10% Note 5		0.15	0.3	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			V_{DD} = 2.0 V ±10%		0.05	5.0	μA
	I_{DD4} Note 3	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	5.5	mA
			V_{DD} = 3.0 V ±10% Note 5		1.65	3.2	mA
			V_{DD} = 2.0 V ±10% Note 5		1.25	2.7	mA

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by the mask option) and when port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

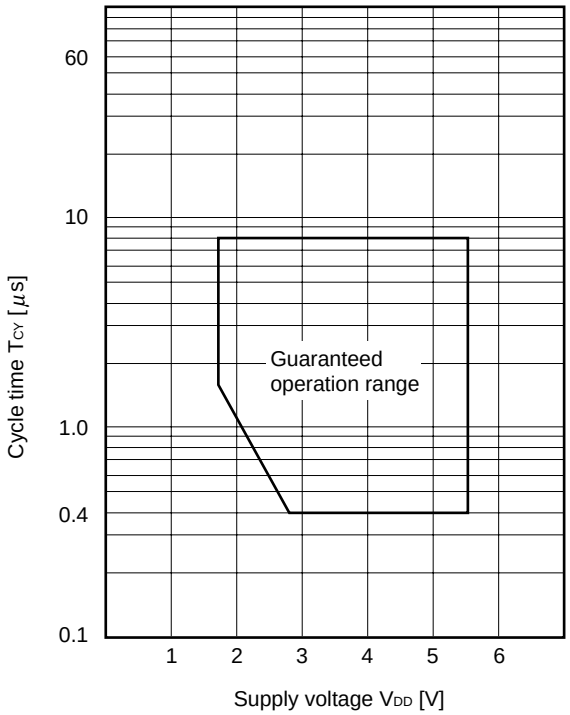
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
		V_{DD} = 1.8 to 5.5 V	1.6		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 – 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 – 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (for $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

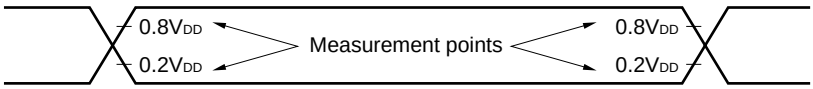
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

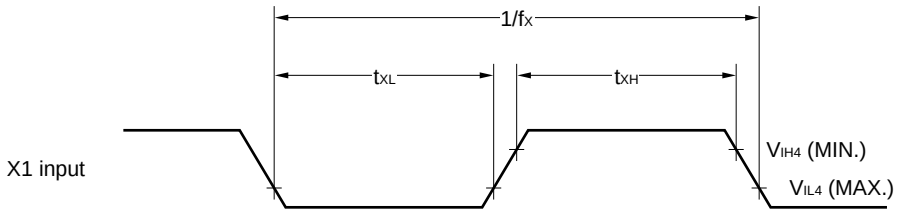
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

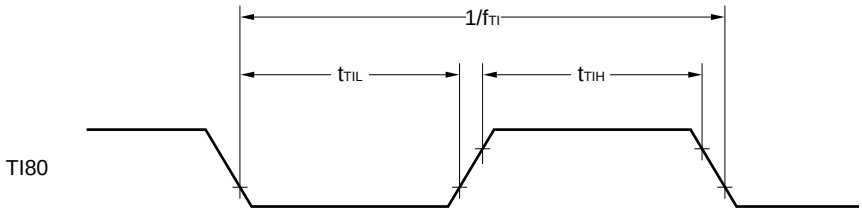
AC Timing Measurement Points (Excluding X1 Input)



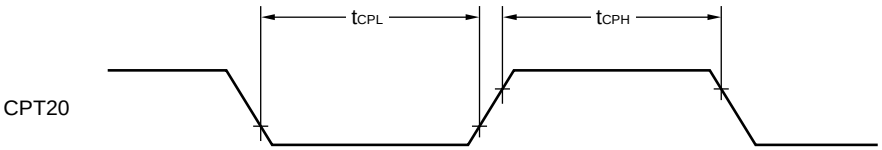
Clock Timing



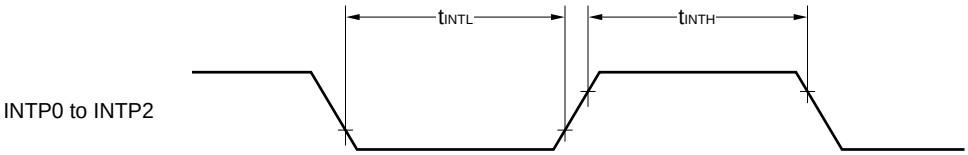
TI Timing



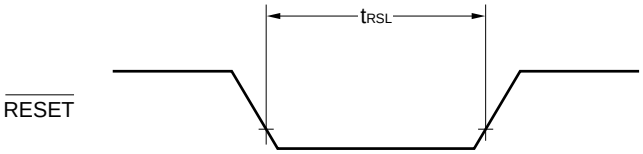
Capture Input Timing



Interrupt Input Timing

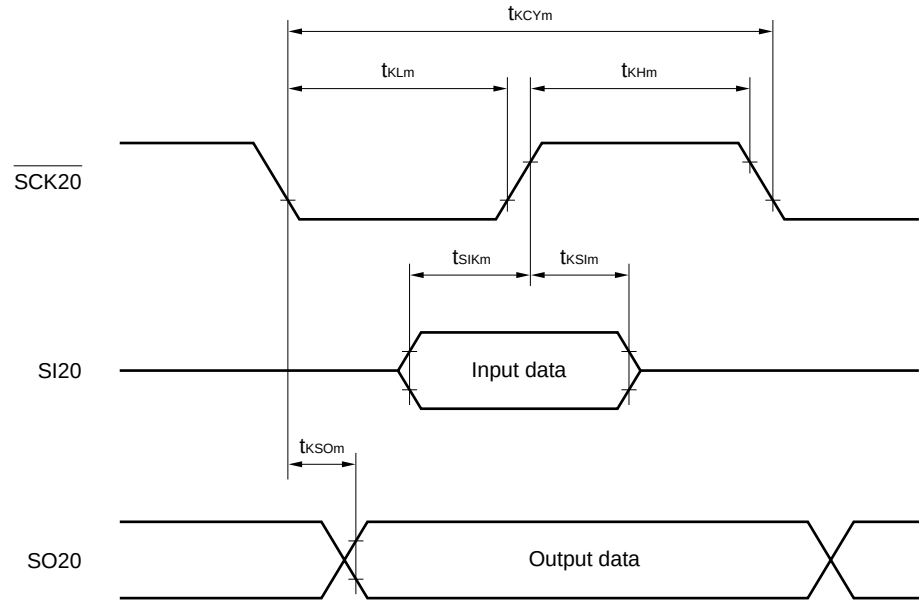


$\overline{\text{RESET}}$ Input Timing



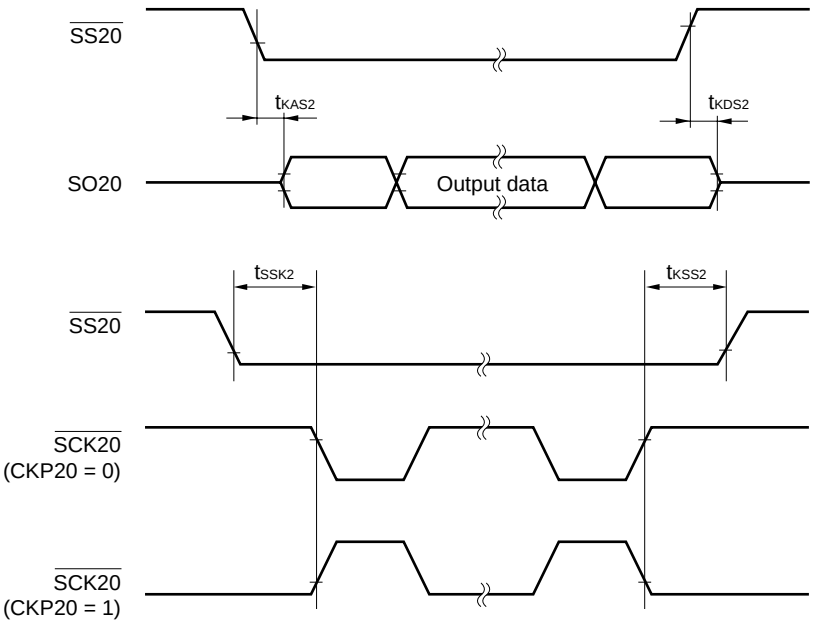
Serial Transfer Timing

3-wire serial I/O mode:

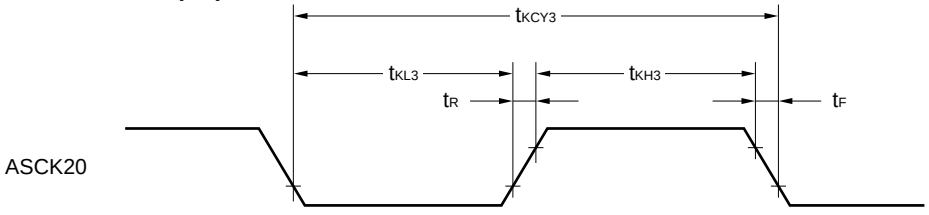


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78910xA, 78910xA(A))

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	Bits
Overall error[Notes 1, 2]		V_{DD} = 2.7 to 5.5 V		±0.4	±0.6	%FSR
		V_{DD} = 1.8 to 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	V_{DD} = 2.7 to 5.5 V	14		100	μs
		V_{DD} = 1.8 to 5.5 V	28		100	μs
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.2%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

10-Bit A/D Converter Characteristics (μPD78911xA, 78911xA(A))

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	2.7 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

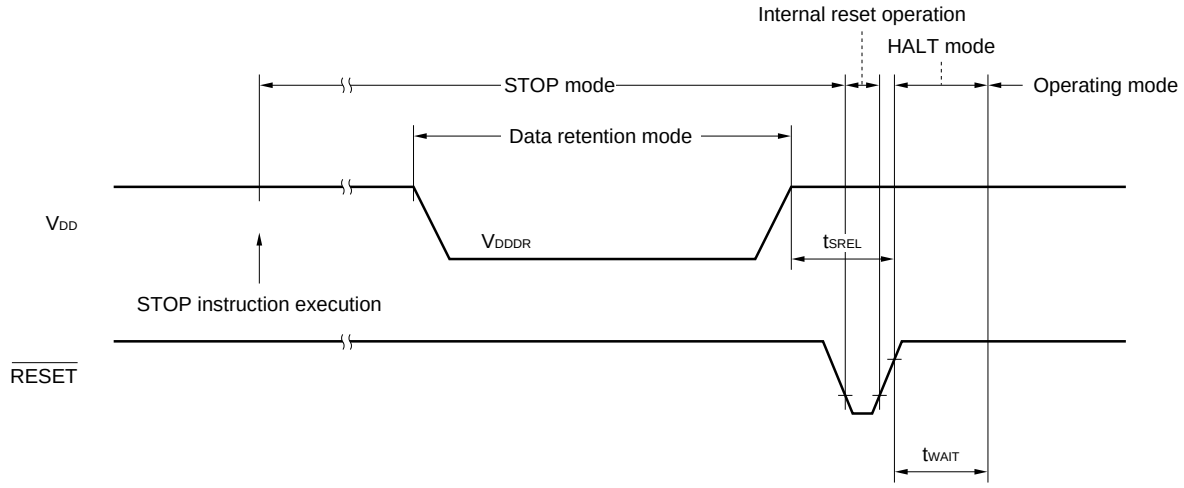
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

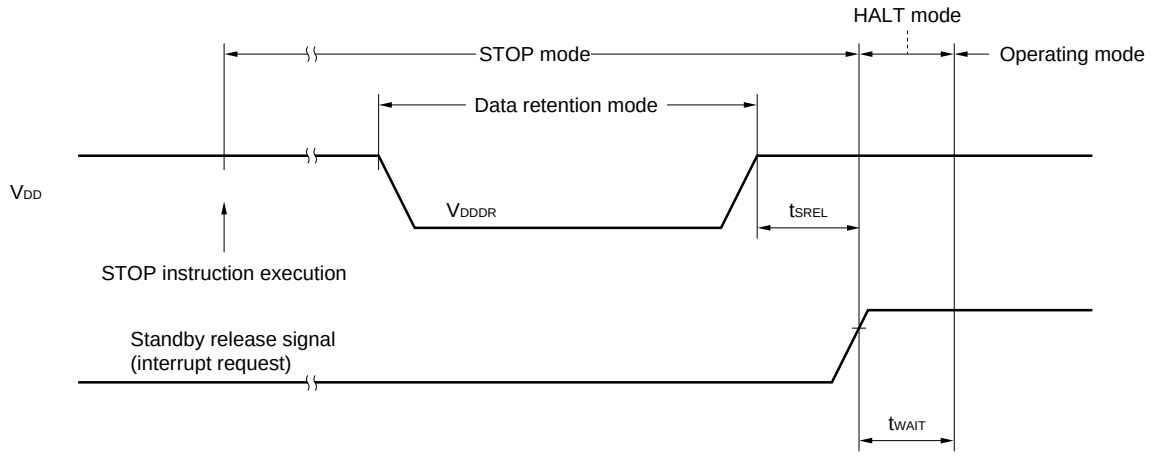
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



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CHAPTER 23 ELECTRICAL SPECIFICATIONS
(μPD78910xA(A1), 78911xA(A1), 78910xA(A2), 78911xA(A2))

Absolute Maximum Ratings (T_A = 25°C)

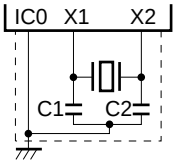
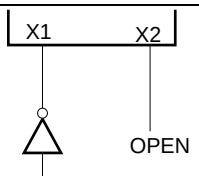
Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
			With an on-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78910xA(A1), 78911xA(A1)	–4	mA
		Total for all pins		–14	mA
		Per pin	μPD78910xA(A2), 78911xA(A2)	–2	mA
		Total for all pins		–6	mA
Output current, low	I_{OL}	Per pin	μPD78910xA(A1), 78911xA(A1)	5	mA
		Total for all pins		80	mA
		Per pin	μPD78910xA(A2), 78911xA(A2)	2	mA
		Total for all pins		40	mA
Operating ambient temperature	T_A	μPD78910xA(A1), 78911xA(A1)		–40 to +110	°C
		μPD78910xA(A2), 78911xA(A2)		–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)),
–40 to +125°C (μPD78910xA(A2), 78911xA(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use a resonator that stabilizes oscillation during the oscillation wait time.

Cautions 1. When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Use a ceramic resonator that is guaranteed by the resonator manufacturer to operate under the following conditions.

μPD78910xA(A1), 78911xA(A1): T_A = 110°C
μPD78910xA(A2), 78911xA(A2): T_A = 125°C

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)), –40 to +125°C (μPD78910xA(A2), 78911xA(A2))) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78910xA(A1), 78911xA(A1)				–1	mA
		Total for all pins					–7	mA
		Per pin	μPD78910xA(A2), 78911xA(A2)				–1	mA
		Total for all pins					–3	mA
Output current, low	I_{OL}	Per pin	μPD78910xA(A1), 78911xA(A1)				1.6	mA
		Total for all pins					40	mA
		Per pin	μPD78910xA(A2), 78911xA(A2)				1.6	mA
		Total for all pins					20	mA
Input voltage, high	V_{IH1}	Pins other than described below			0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain		0.7V_{DD}		10	V
			With on-chip pull-up resistor		0.7V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{RESET}$, P20 to P25			0.8V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2			V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below			0		0.3V_{DD}	V
	V_{IL2}	P50 to P53			0		0.3V_{DD}	V
	V_{IL3}	$\overline{RESET}$, P20 to P25			0		0.2V_{DD}	V
	V_{IL4}	X1, X2			0		0.1	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA			V_{DD} – 2.0			V
	V_{OH2}	I_{OH} = –100 μA			V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA				2.0	V
			I_{OL} = 400 μA				1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA				1.0	V
Input leakage current, high	I_{LIH1}	Pins other than X1, X2, or P50 to P53		$V_I = V_{DD}$			10	μA
	I_{LIH2}	X1, X2					20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)		V_I = 10 V			80	μA
Input leakage current, low	I_{LIL1}	Pins other than X1, X2, or P50 to P53		V_I = 0 V			–10	μA
	I_{LIL2}	X1, X2					–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)					–10[Note]	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$					10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V					–10	μA

Note When pull-up resistors are not connected to P50 to P53 (specified by the mask option) and when port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)), –40 to +125°C (μPD78910xA(A2), 78911xA(A2))) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63	50	100	300	kΩ
Mask option pull-up resistance	R_2	V_I = 0 V, P50 to P53	10	30	100	kΩ
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF) Note 3		1.8	8.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF) Note 3		0.8	5.0	mA
	I_{DD3} Note 1	STOP mode		0.1	1000	μA
	I_{DD4} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF) Note 3		3.0	10	mA

Notes 1. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

3. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

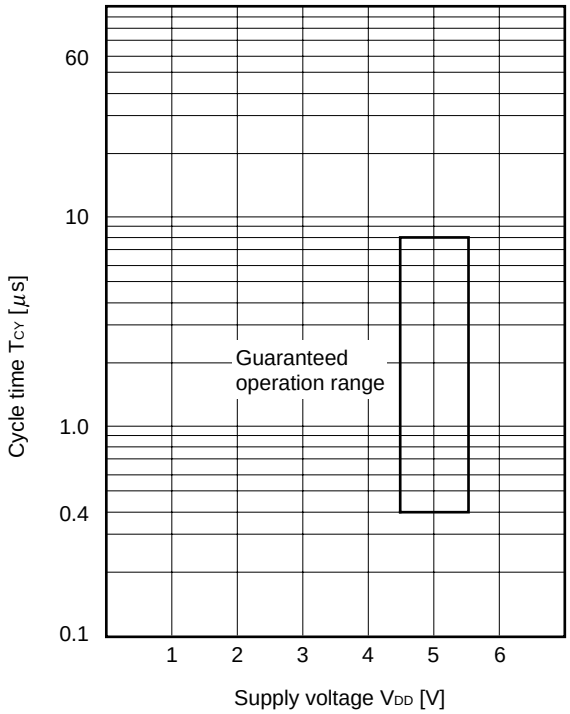
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)), –40 to +125°C (μPD78910xA(A2), 78911xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}		0.4		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
TI80 input frequency	f_{TI}		0		4	MHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)), –40 to +125°C (μPD78910xA(A2), 78911xA(A2)))

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}				120	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}				240	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}		100			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}		400			ns

Note R and C are the load resistance and load capacitance of the SO output line.

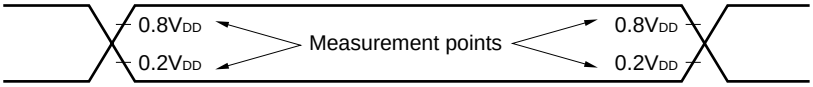
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

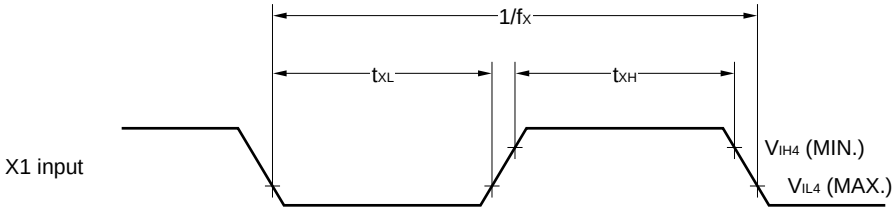
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		800			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

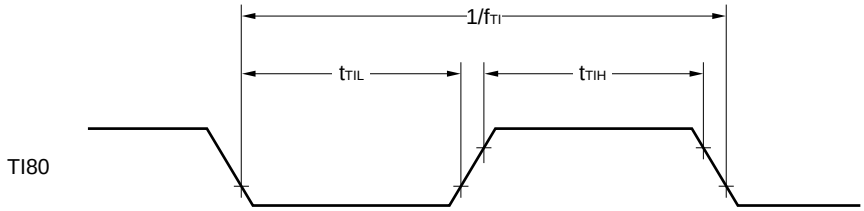
AC Timing Measurement Points (Excluding X1 Input)



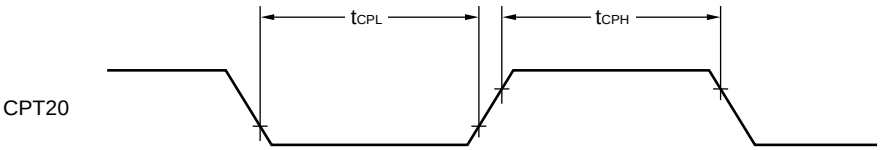
Clock Timing



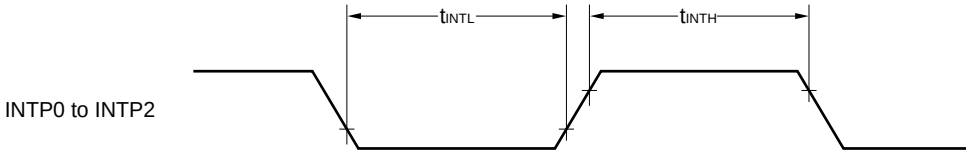
TI Timing



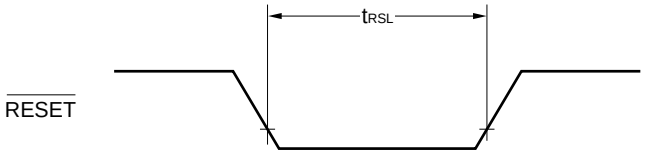
Capture Input Timing



Interrupt Input Timing

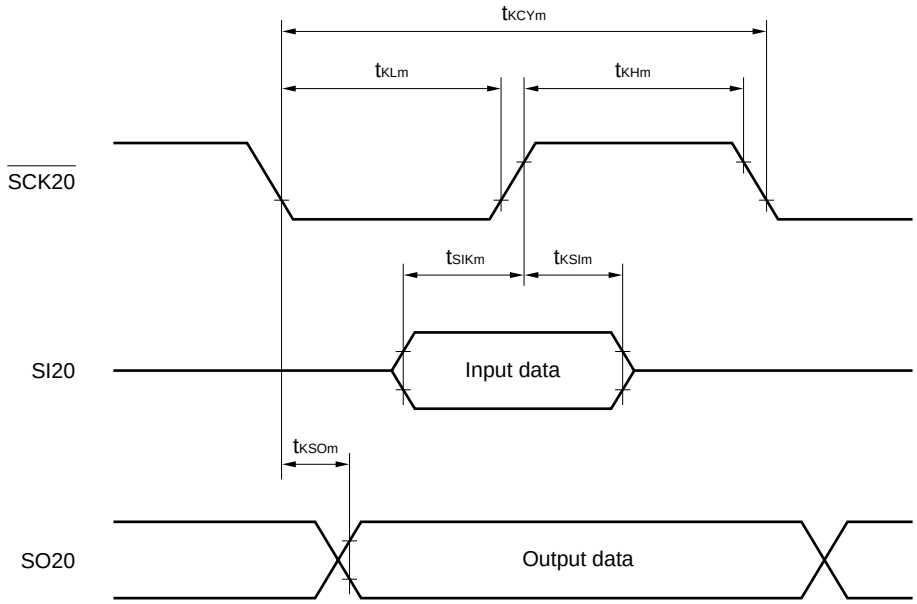


$\overline{\text{RESET}}$ Input Timing



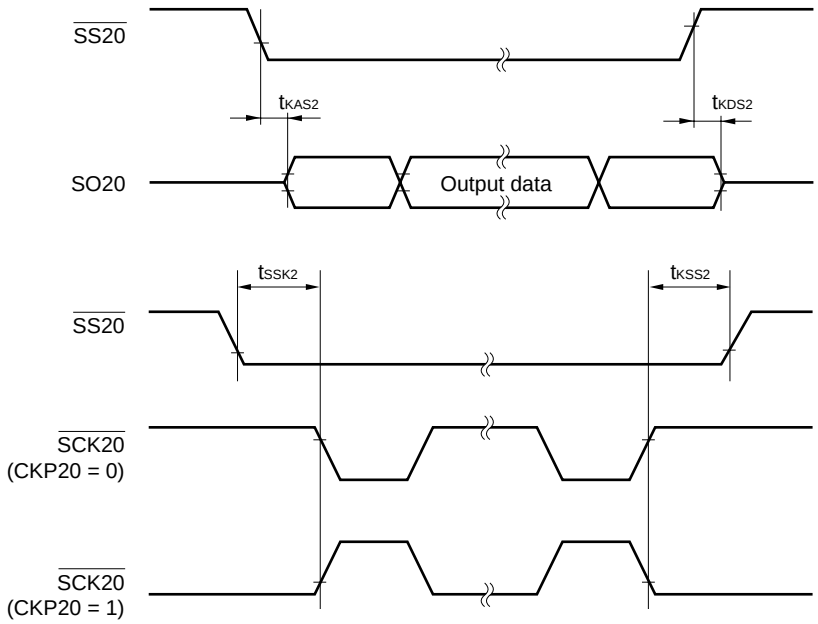
Serial Transfer Timing

3-wire serial I/O mode:

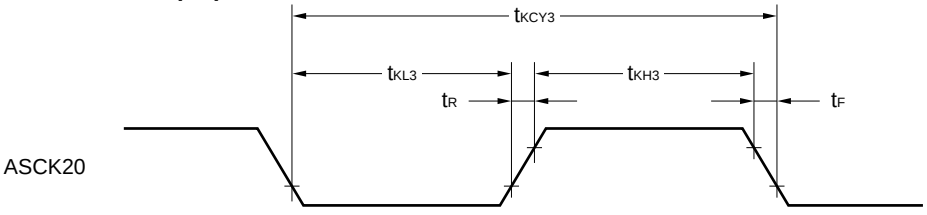


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78910xA(A1), 78910xA(A2) only)

(AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 to +110°C (μPD78910xA(A1)), –40 to +125°C (μPD78910xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	Bits
Overall error[Notes 1, 2]				±0.4	±1.0	%FSR
Conversion time	t_{CONV}		14		28	μs
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.2%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

10-Bit A/D Converter Characteristics (μPD78911xA(A1), 78911xA(A2) only)

(AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 to +110°C (μPD78911xA(A1)), –40 to +125°C (μPD78911xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]				±0.4	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Notes 1, 2]					±0.6	%FSR
Full-scale error[Notes 1, 2]					±0.6	%FSR
Integral linearity error[Note 1]	ILE				±4.5	LSB
Differential linearity error[Note 1]	DLE				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +110°C (μPD78910xA(A1), 78911xA(A1)), –40 to +125°C (μPD78910xA(A2), 78911xA(A2)))

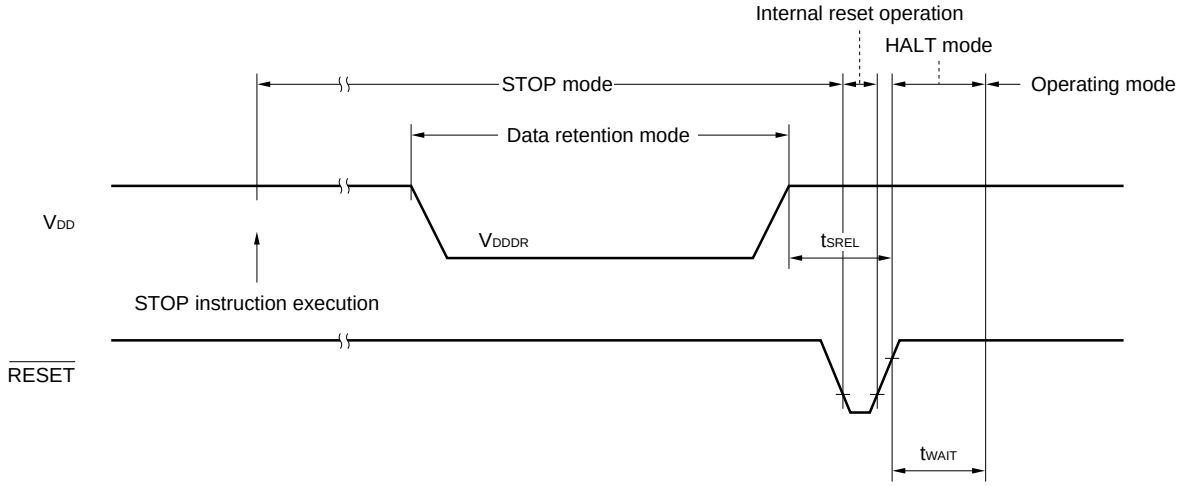
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

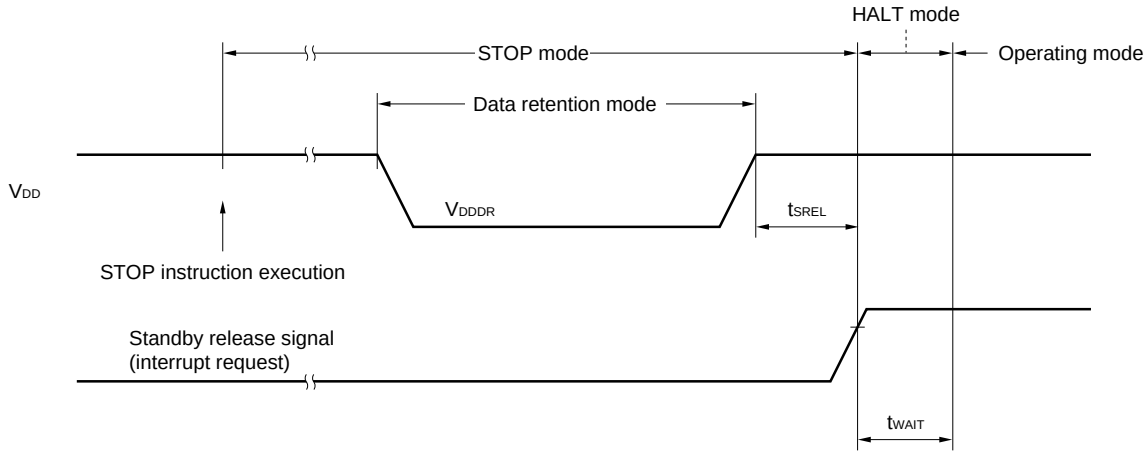
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

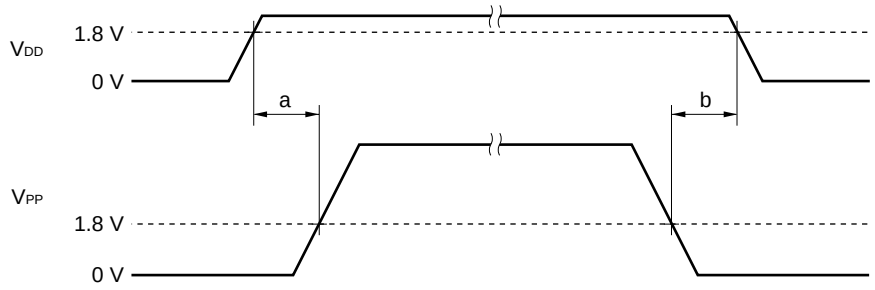


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78F9116B	–10	mA
		Total for all pins		–30	mA
		Per pin	μPD78F9116B(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	μPD78F9116B	30	mA
		Total for all pins		160	mA
		Per pin	μPD78F9116B(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

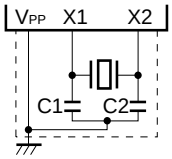
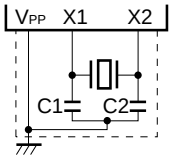
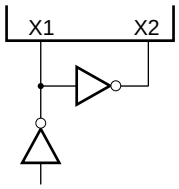
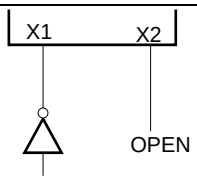
- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see a in the figure below).
- When supply voltage drops
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see b in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	
External clock		X1 input frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	45		500	ns
			V_{DD} = 3.0 to 5.5 V	75		500	ns
			V_{DD} = 1.8 to 5.5 V	85		500	ns
		X1 input frequency (f_X)Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use a resonator that stabilizes oscillation during the oscillation wait time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

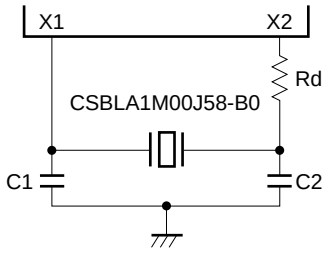
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

Ceramic resonator (T_A = –40 to +85°C) (μPD78F9116B, 78F9116B(A))

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd. (Standard products)	CSBLA1M00J58-B0[Note]	1.0	100	100	2.0	5.5	Rd = 2.2 kΩ
	CSTCC2M00G56-R0	2.0	–	–			On-chip capacitor version
	CSTCR4M00G53-R0	4.0					
	CSTLS4M00G53-B0						
	CSTCR5M00G53-R0	5.0			2.1		
	CSTLS5M00G53-B0						
	CSTCR6M00G53-R0	6.0					
	CSTLS6M00G53-B0				2.2		
	CSTCE8M38G52-R0	8.388			2.0		
	CSTLS8M38G53-B0				2.2		
	CSTCE10M0G52-R0	10.0			2.1		
	CSTLS10M0G53-B0				2.4		
Murata Mfg. Co., Ltd. (Low-voltage drive type)	CSTCR4M00G53U-R0	4.0	–	–	1.8	5.5	On-chip capacitor version
	CSTLS4M00G53093-B0						
	CSTCR5M00G53U-R0	5.0					
	CSTLS5M00G53U-B0						
	CSTCR6M00G53093-R0	6.0			1.9		
	CSTLS6M00G53U-B0						
	CSTLS8M38G53193-B0	8.0			2.0		
	CSTLS10M0G53U-B0	10.0					

Note A limiting resistor (Rd = 2.2 kΩ) is required when the CSBLA1M00J58-B0 (1.0 MHz) of Murata Mfg. Co., Ltd. is used as the ceramic resonator (see the figure below). A limiting resistor is not necessary when other recommended resonators are used.



Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer. If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the μPD78F9116B and 78F9116B(A) so that the internal operating conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78F9116B				–1	mA
		Total for all pins					–15	mA
		Per pin	μPD78F9116B(A)				–1	mA
		Total for all pins					–11	mA
Output current, low	I_{OL}	Per pin	μPD78F9116B				10	mA
		Total for all pins					80	mA
		Per pin	μPD78F9116B(A)				3	mA
		Total for all pins					60	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78F9116B)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78F9116B(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78F9116B)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78F9116B(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than X1, X2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than X1, X2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63		50	100	200	kΩ
Power supply current	I_{DD1} Note 2	10.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10% Note 4		10.0	20.0	mA
		6.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10% Note 4		6.0	12.0	mA
		5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		4.0	10.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.0	2.5	mA
			V_{DD} = 2.0 V ±10% Note 5		0.8	2.0	mA
	I_{DD2} Note 2	10.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10% Note 4		1.2	6.0	mA
		6.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10% Note 4		0.9	2.8	mA
		5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		0.6	2.5	mA
			V_{DD} = 3.0 V ±10% Note 5		0.3	2.0	mA
			V_{DD} = 2.0 V ±10% Note 5		0.2	1.5	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA
	I_{DD4} Note 3	10.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ±10% Note 4		11.0	22.5	mA
		6.0 MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ±10% Note 4		7.0	14.5	mA
		5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		5.0	12.5	mA
			V_{DD} = 3.0 V ±10% Note 5		2.0	5.0	mA
			V_{DD} = 2.0 V ±10% Note 5		1.8	4.5	mA

Notes 1. When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
		V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
		V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		V_{DD} = 1.8 to 5.5 V	1.0		1.25	MHz
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (@ 5.0 MHz operation)			21	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (@ 5.0 MHz operation)			21	mA
Erase current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.2	0.2	0.2	s
Total erase time	t_{era}				20	s
Rewrite count		Erase/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

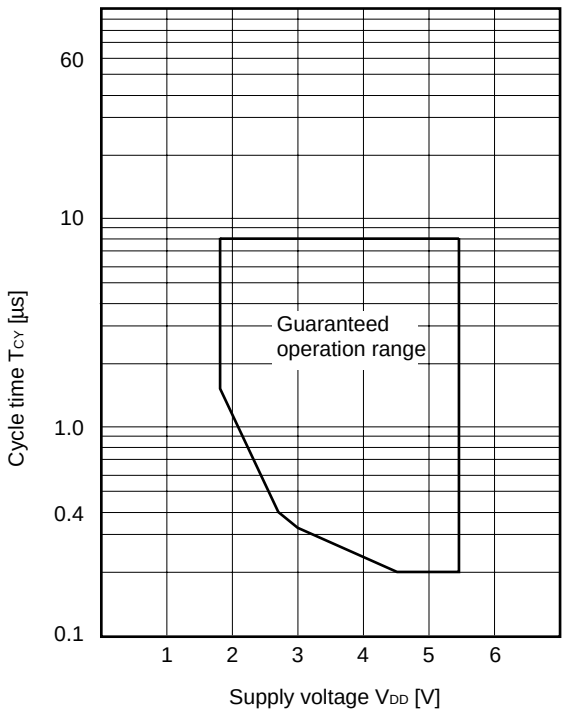
Note The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 4.5 to 5.5 V	0.2		8	μs
		V_{DD} = 3.0 to 5.5 V	0.33		8	μs
		V_{DD} = 2.7 to 5.5 V	0.4		8	μs
		V_{DD} = 1.8 to 5.5 V	1.6		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 - 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (for $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
$\overline{SS20}$ setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
$\overline{SS20}$ hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

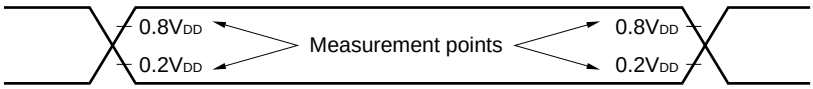
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

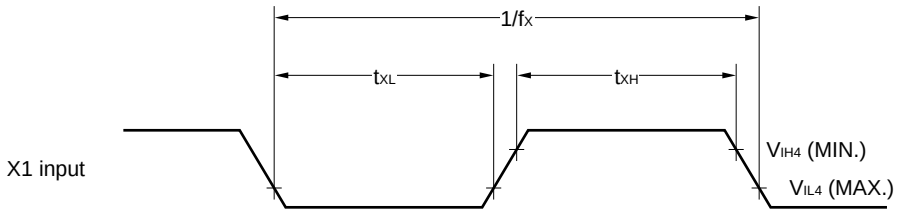
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

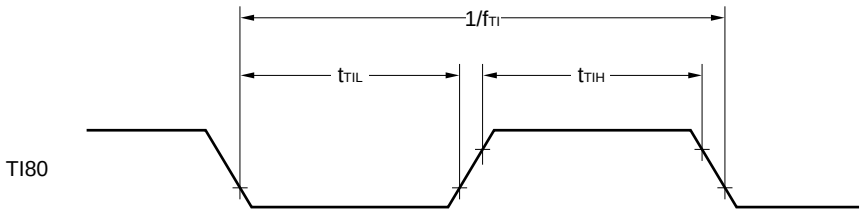
AC Timing Measurement Points (Excluding X1 Input)



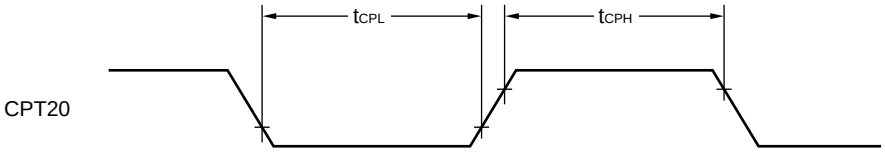
Clock Timing



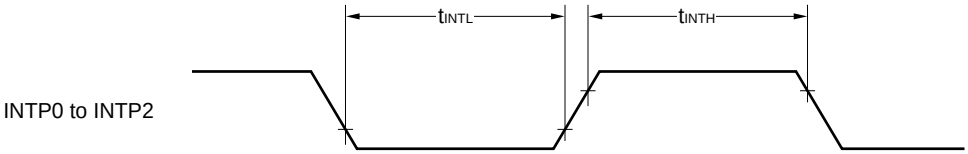
TI Timing



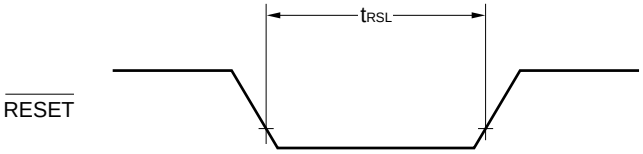
Capture Input Timing



Interrupt Input Timing

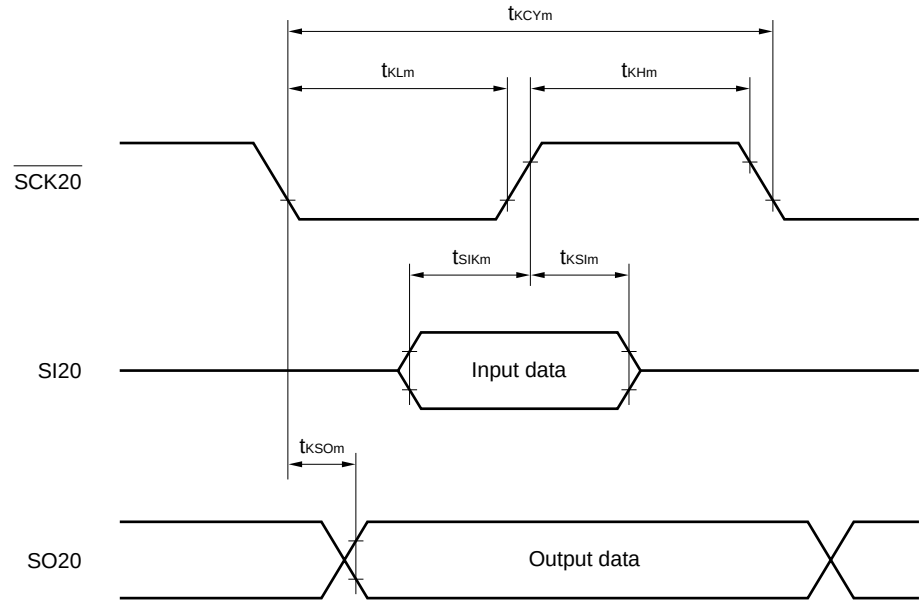


$\overline{\text{RESET}}$ Input Timing



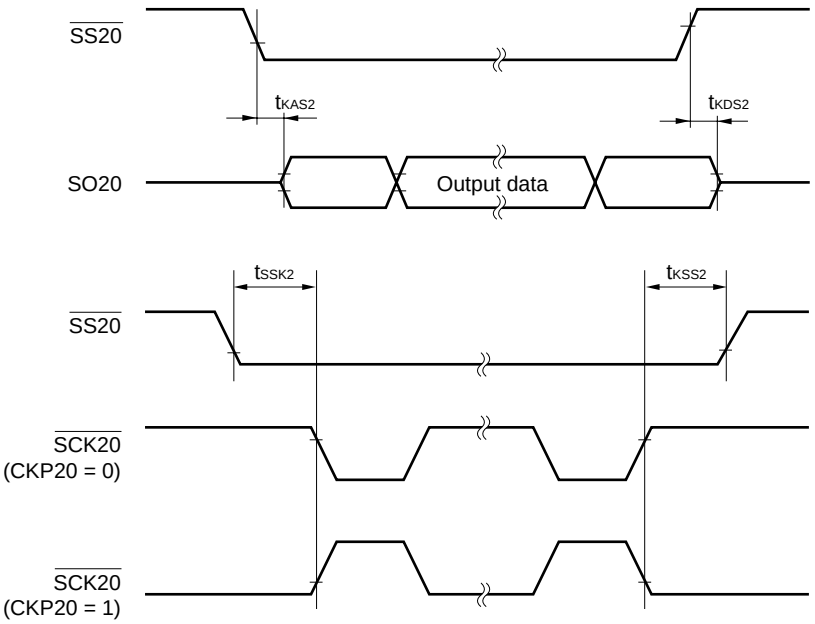
Serial Transfer Timing

3-wire serial I/O mode:

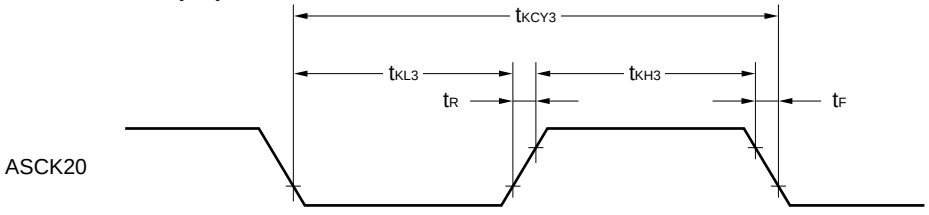


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ V_{DD} ≤ 5.5 V	12		100	μs
		2.7 V ≤ V_{DD} < 4.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

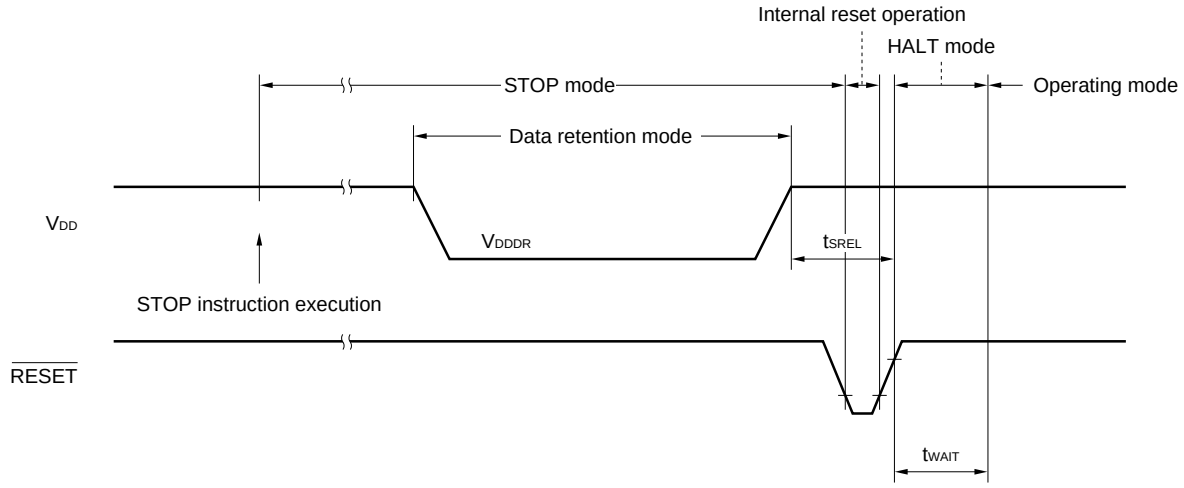
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

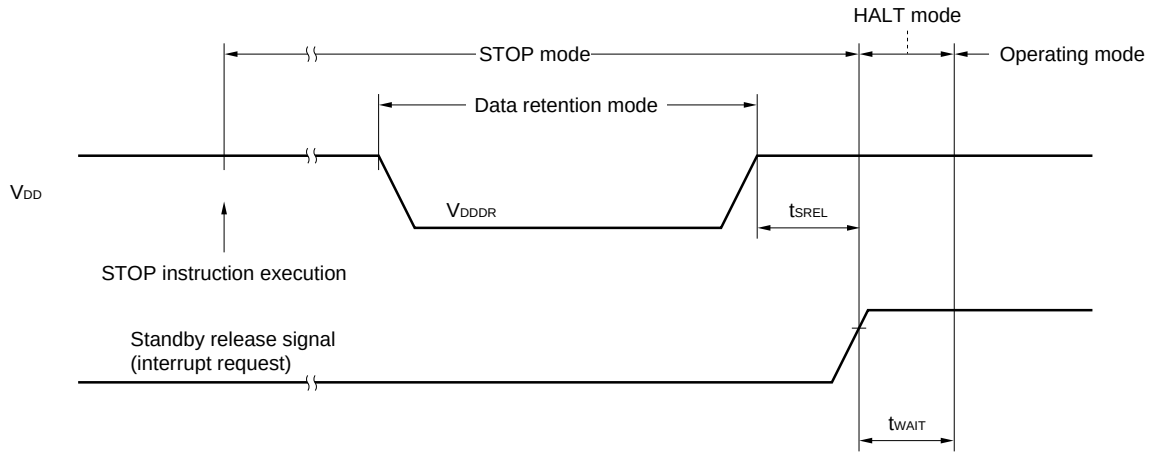
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

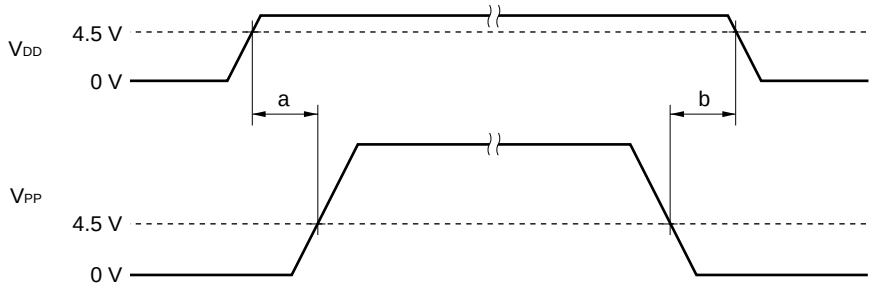


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–4	mA
		Total for all pins		–14	mA
Output current, low	I_{OL}	Per pin		5	mA
		Total for all pins		80	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +105	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

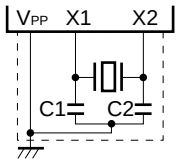
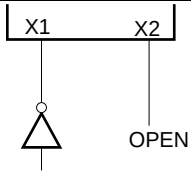
- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (4.5 V) of the operating voltage range (see a in the figure below).
- When supply voltage drops
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (4.5 V) of the operating voltage range of V_{DD} (see b in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use a resonator that stabilizes oscillation during the oscillation wait time.

Cautions 1. When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Use a ceramic resonator that is guaranteed by the resonator manufacturer to operate at T_A = 105°C.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–7	mA
Output current, low	I_{OL}	Per pin				1.6	mA
		Total for all pins				40	mA
Input voltage, high	V_{IH1}	Pins other than described below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	0.7V_{DD}		10	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		0.8V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		0		0.3V_{DD}	V
	V_{IL2}	P50 to P53		0		0.3V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		0		0.2V_{DD}	V
	V_{IL4}	X1, X2		0		0.1	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA		V_{DD} – 2.0			V
	V_{OH2}	I_{OH} = –100 μA		V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA			2.0	V
			I_{OL} = 400 μA			1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA			1.0	V
Input leakage current, high	I_{LIH1}	Pins other than X1, X2, or P50 to P53	V_I = V_{DD}			10	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 10 V			80	μA
Input leakage current, low	I_{LIL1}	Pins other than X1, X2, or P50 to P53	V_I = 0 V			–10	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–10[Note]	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA

Note When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63	50	100	300	kΩ
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF) Note 3		7.5	20.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF) Note 3		3.0	5.5	mA
	I_{DD3} Note 1	STOP mode		1	1000	μA
	I_{DD4} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF) Note 3		8.7	22.3	mA

Notes 1. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

3. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (@ 5.0 MHz operation)			21	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (@ 5.0 MHz operation)			21	mA
Erase current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.2	0.2	0.2	s
Total erase time	t_{era}				20	s
Rewrite count		Erase/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

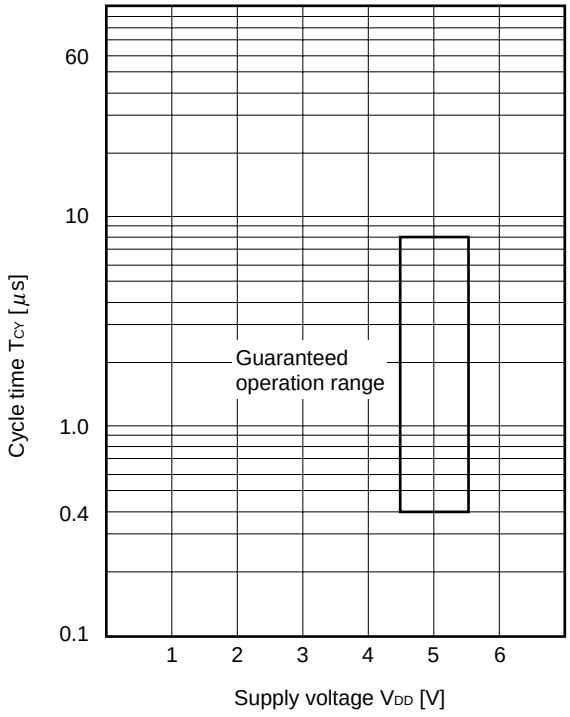
Note The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}		0.4		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
TI80 input frequency	f_{TI}		0		4	MHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}\uparrow$)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}\uparrow$)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}\downarrow$	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}\uparrow$)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}\uparrow$)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}\downarrow$	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (to $\overline{SS20}\downarrow$ when $\overline{SS20}$ is used)	t_{KAS2}				120	ns
SO20 disable time (for $\overline{SS20}\uparrow$ when $\overline{SS20}$ is used)	t_{KDS2}				240	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}		100			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}		400			ns

Note R and C are the load resistance and load capacitance of the SO output line.

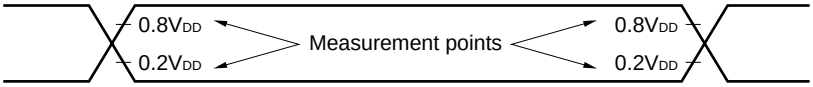
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

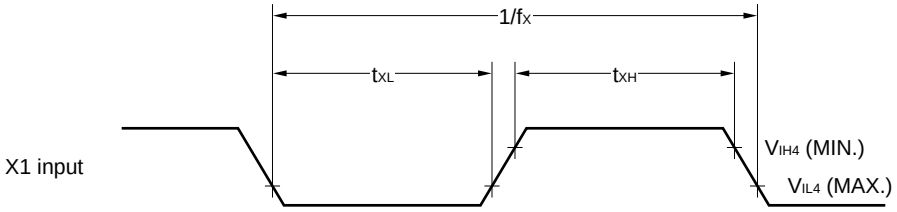
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		800			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

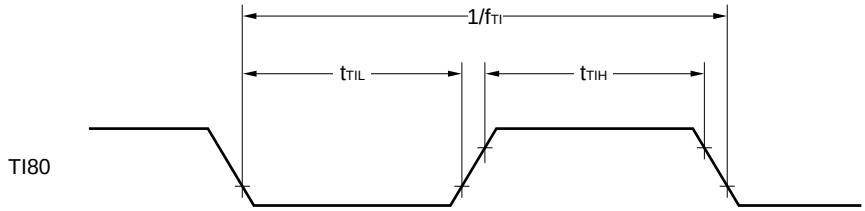
AC Timing Measurement Points (Excluding X1 Input)



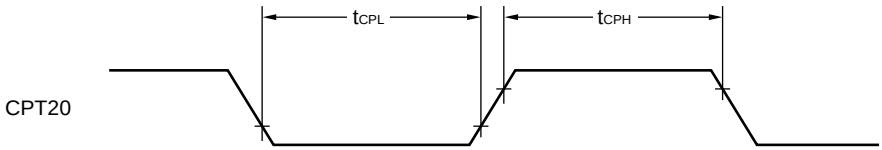
Clock Timing



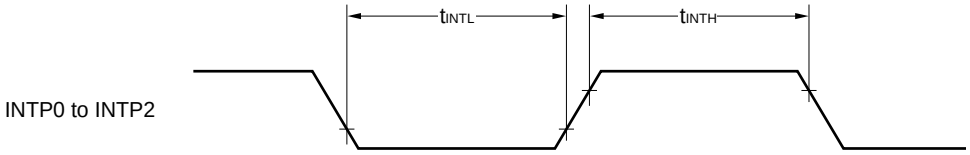
TI Timing



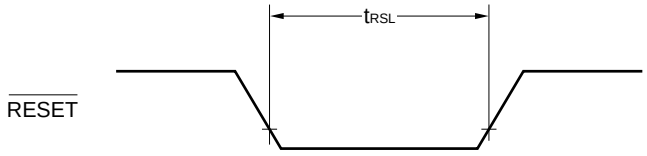
Capture Input Timing



Interrupt Input Timing

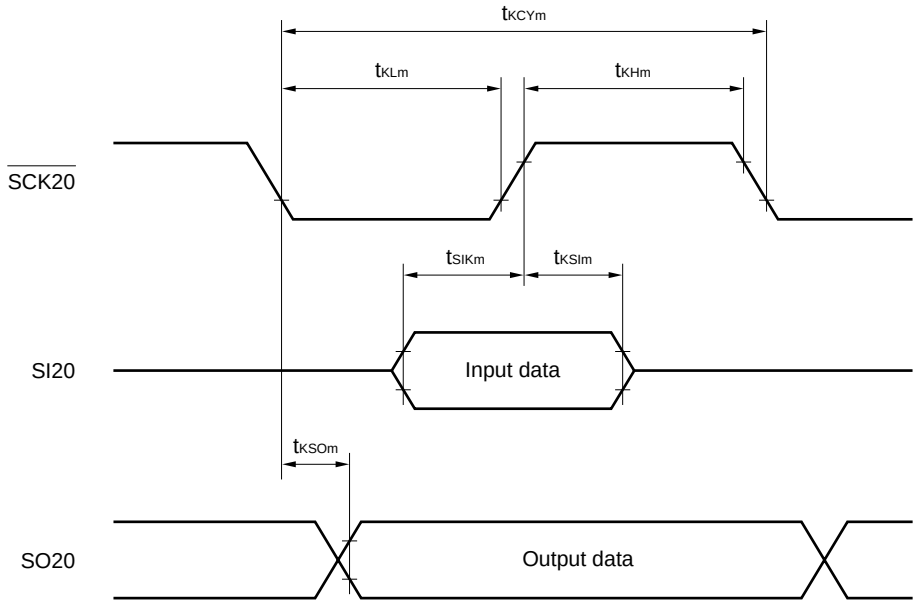


$\overline{\text{RESET}}$ Input Timing



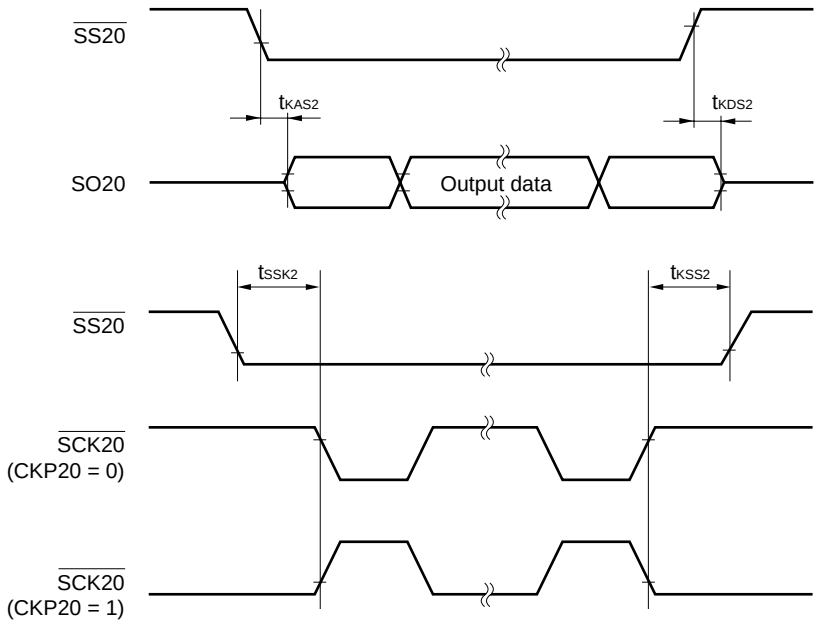
Serial Transfer Timing

3-wire serial I/O mode:

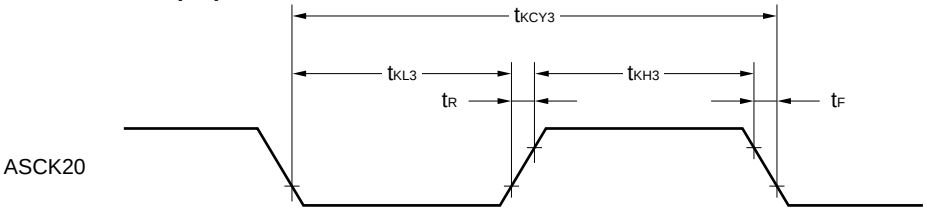


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +105°C, AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1,2]				±0.4	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Notes 1,2]					±0.6	%FSR
Full-scale error[Notes 1,2]					±0.6	%FSR
Integral linearity error[Note 1]	ILE				±4.5	LSB
Differential linearity error[Note 1]	DLE				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +105°C)

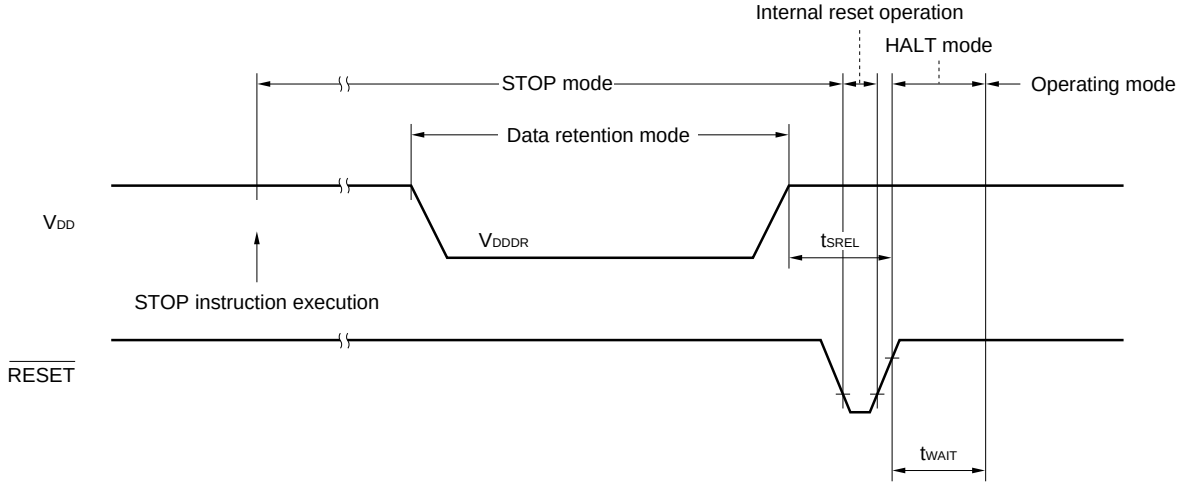
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

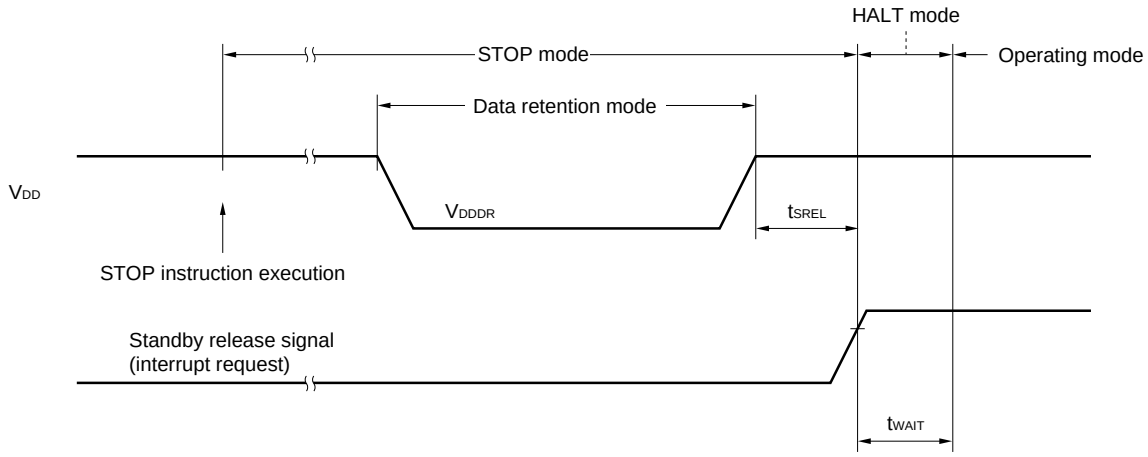
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

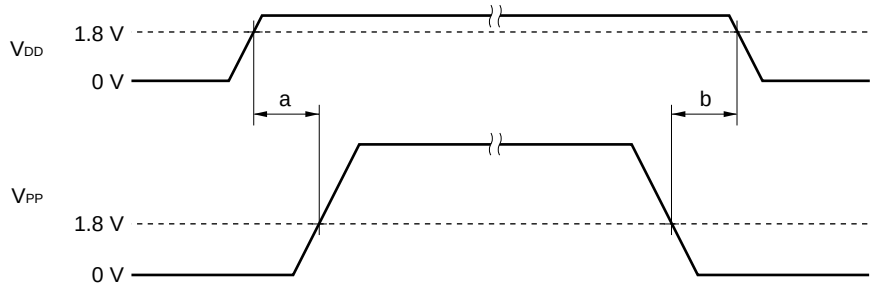


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for all pins		–30	mA
Output current, low	I_{OL}	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

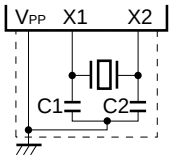
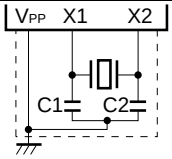
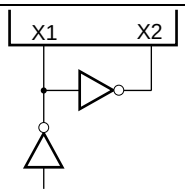
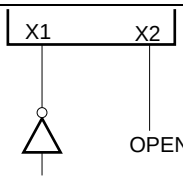
- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see a in the figure below).
- When supply voltage drops
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see b in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use a resonator that stabilizes oscillation during the oscillation wait time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin					–1	mA
		Total for all pins					–15	mA
Output current, low	I_{OL}	Per pin					10	mA
		Total for all pins					80	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V, T_A = 25 to 85°C	0.9V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V, T_A = 25 to 85°C	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than X1, X2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	X1, X2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than X1, X2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63		50	100	200	kΩ
Power supply current	I_{DD1} Note 2	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		5.0	15.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.9	4.9	mA
			V_{DD} = 2.0 V ±10% Note 5		1.5	3.0	mA
	I_{DD2} Note 2	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.5	5.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.0	2.0	mA
			V_{DD} = 2.0 V ±10% Note 5		0.75	1.5	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA
	I_{DD4} Note 3	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		6.2	17.3	mA
			V_{DD} = 3.0 V ±10% Note 5		3.1	7.2	mA
			V_{DD} = 2.0 V ±10% Note 5		2.5	5.0	mA

Notes 1. When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (@ 5.0 MHz operation)			18	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (@ 5.0 MHz operation)			18	mA
Erase current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.5	1	1	s
Total erase time	t_{era}				20	s
Rewrite count		Erase/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

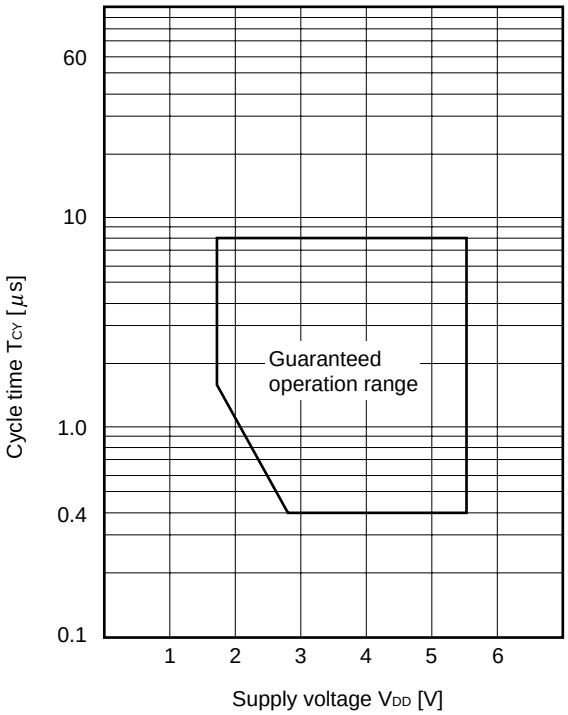
Note The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
		V_{DD} = 1.8 to 5.5 V	1.6		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 – 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 – 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

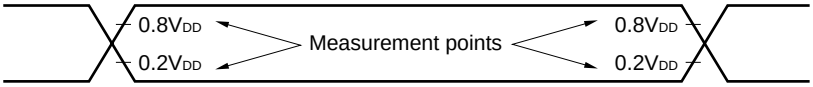
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

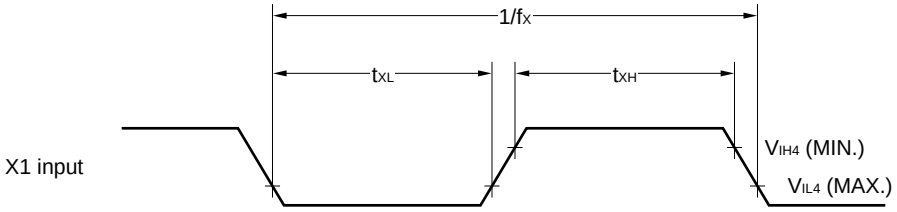
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

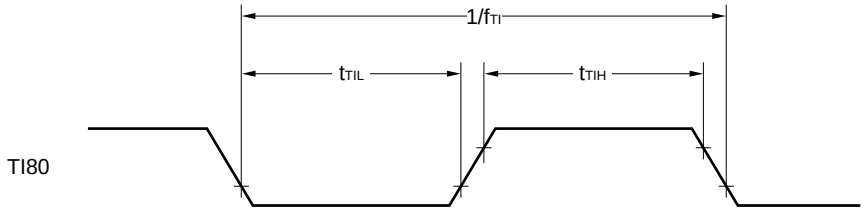
AC Timing Measurement Points (Excluding X1 Input)



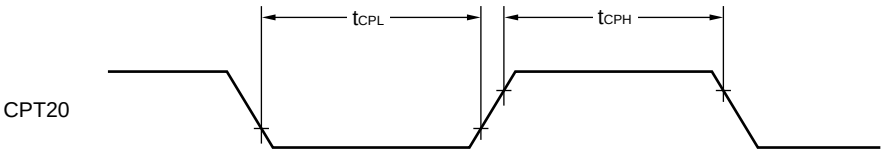
Clock Timing



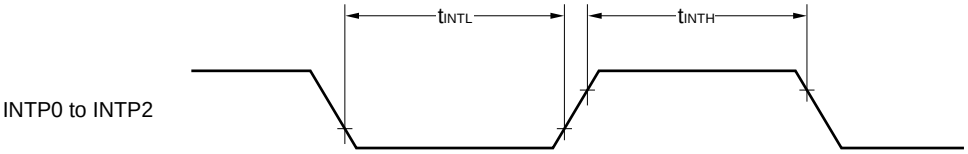
TI Timing



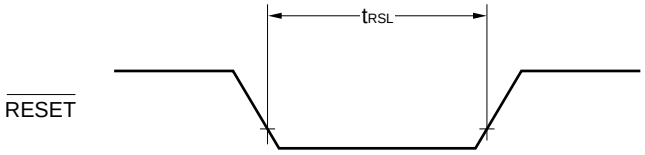
Capture Input Timing



Interrupt Input Timing

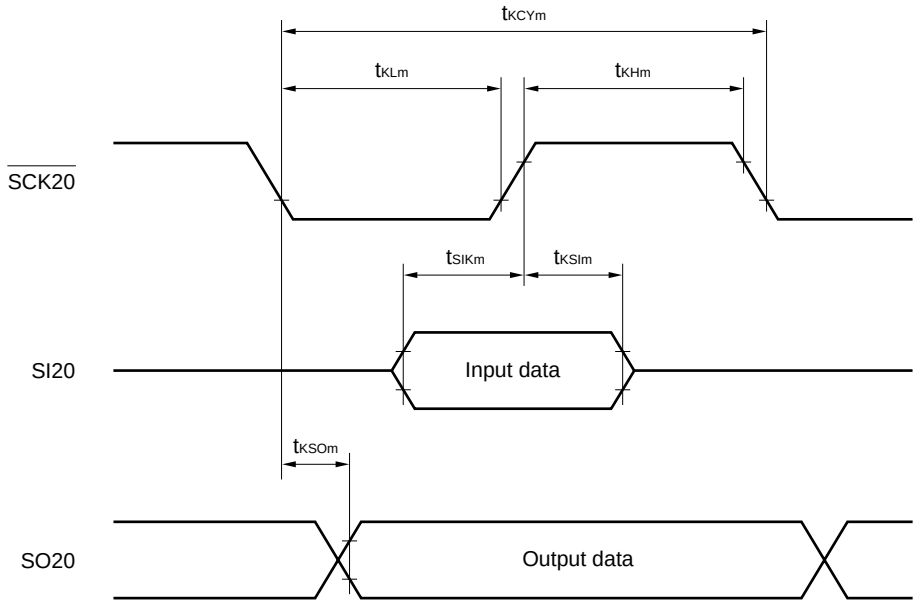


$\overline{\text{RESET}}$ Input Timing



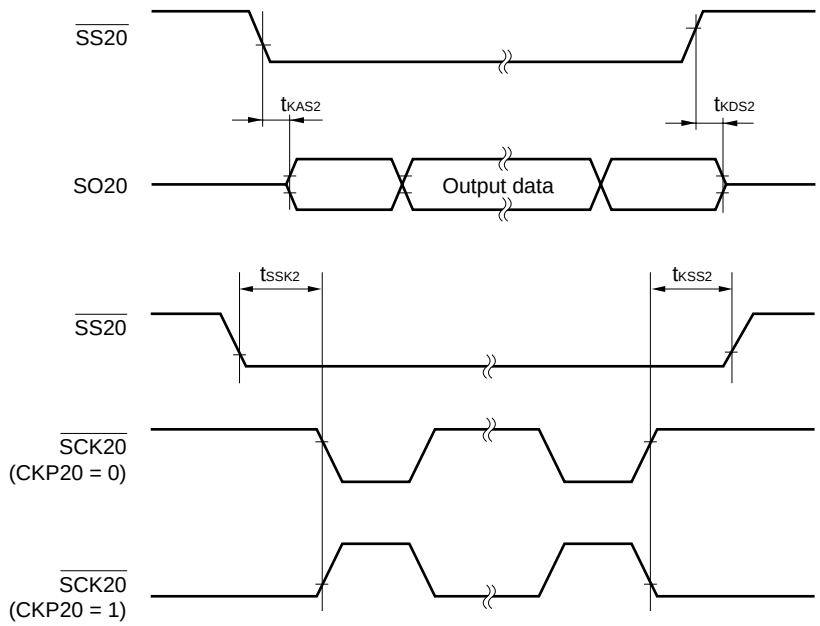
Serial Transfer Timing

3-wire serial I/O mode:

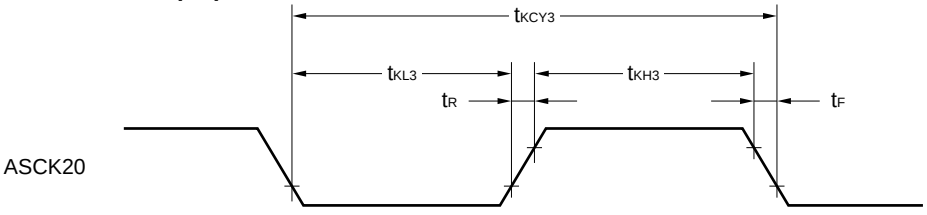


m = 1, 2

3-wire serial I/O mode (when $\overline{\text{SS20}}$ is used):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +85°C, $AV_{DD} = V_{DD}$ = 1.8 to 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	2.7 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

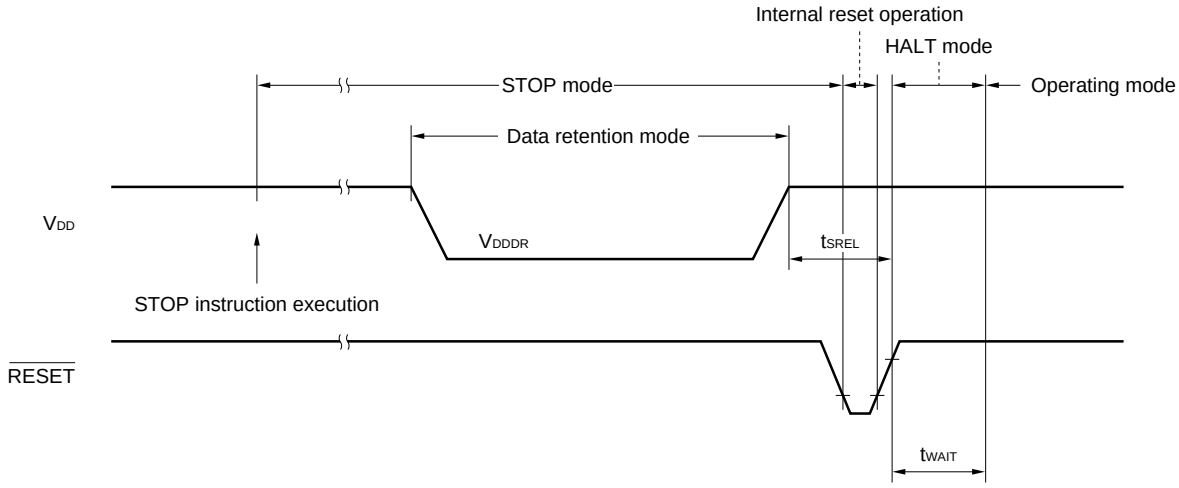
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

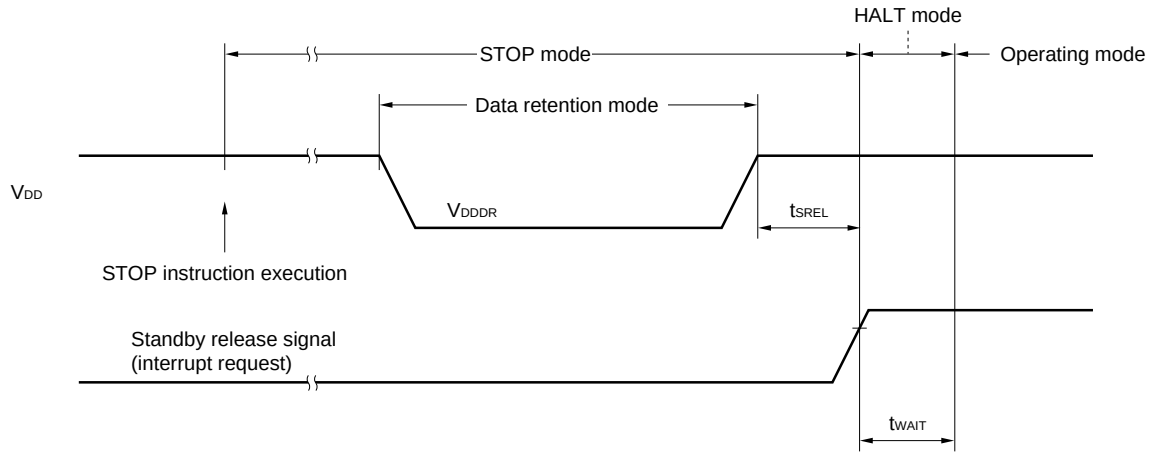
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register.

Remark f_X: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



★ CHAPTER 27 ELECTRICAL SPECIFICATIONS (μPD78912xA, 78913xA, 78912xA(A), 78913xA(A))

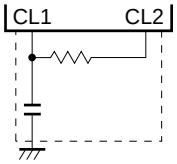
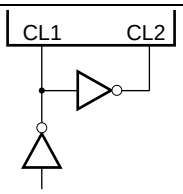
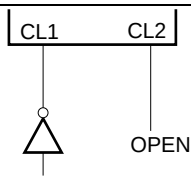
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
			With an on-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78912xA, 78913xA	–10	mA
		Total for all pins		–30	mA
		Per pin	μPD78912xA(A), 78913xA(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	μPD78912xA, 78913xA	30	mA
		Total for all pins		160	mA
		Per pin	μPD78912xA(A), 78913xA(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC})[Note]		2.0		4.0	MHz
External clock		CL1 input frequency (f_{CC})[Note]		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		CL1 input frequency (f_{CC})[Note]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

RC Oscillator Frequency Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{CC1}	R = 11.0 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	1.5	2.0	2.5	MHz
	f_{CC2}	Target: 2 MHz	V_{DD} = 1.8 to 3.6 V	0.5	2.0	2.5	MHz
	f_{CC3}		V_{DD} = 1.8 to 5.5 V	0.5	2.0	2.5	MHz
	f_{CC4}	R = 6.8 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	2.5	3.0	3.5	MHz
	f_{CC5}	Target: 3 MHz	V_{DD} = 1.8 to 3.6 V	0.75	3.0	3.5	MHz
	f_{CC6}		V_{DD} = 1.8 to 5.5 V	0.75	3.0	3.5	MHz
	f_{CC7}	R = 4.7 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	3.5	4.0	4.7	MHz
	f_{CC8}	Target: 4 MHz	V_{DD} = 1.8 to 3.6 V	1.0	4.0	4.7	MHz
	f_{CC9}		V_{DD} = 1.8 to 5.5 V	1.0	4.0	4.7	MHz

Remark So that the TYP. spec. is satisfied between 2.0 to 4.0 MHz, set one of the above nine patterns for R and C.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78912xA, 78913xA				–1	mA
		Total for all pins					–15	mA
		Per pin	μPD78912xA(A), 78913xA(A)				–1	mA
		Total for all pins					–11	mA
Output current, low	I_{OL}	Per pin	μPD78912xA, 78913xA				10	mA
		Total for all pins					80	mA
		Per pin	μPD78912xA(A), 78913xA(A)				3	mA
		Total for all pins					60	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
			With on-chip pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	CL1, CL2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	CL1, CL2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78912xA, 78913xA)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78912xA(A), 78913xA(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78912xA, 78913xA)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78912xA(A), 78913xA(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than CL1, CL2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	CL1, CL2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than CL1, CL2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	CL1, CL2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P50 to P53		50	100	200	kΩ
Mask option pull-up resistor	R_2	V_I = 0 V, P50 to P53		10	30	60	kΩ
Power supply current	I_{DD1} Note 2	4.0 MHz RC oscillation operating mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.8	3.2	mA
			V_{DD} = 3.0 V ±10% Note 5		0.45	0.9	mA
			V_{DD} = 2.0 V ±10% Note 5		0.25	0.45	mA
	I_{DD2} Note 2	4.0 MHz RC oscillation HALT mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		0.8	1.6	mA
			V_{DD} = 3.0 V ±10% Note 5		0.3	0.6	mA
			V_{DD} = 2.0 V ±10% Note 5		0.15	0.3	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			V_{DD} = 2.0 V ±10%		0.05	5.0	μA
	I_{DD4} Note 3	4.0 MHz RC oscillation A/D operating mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	5.5	mA
			V_{DD} = 3.0 V ±10% Note 5		1.65	3.2	mA
			V_{DD} = 2.0 V ±10% Note 5		1.25	2.7	mA

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by the mask option) and when port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

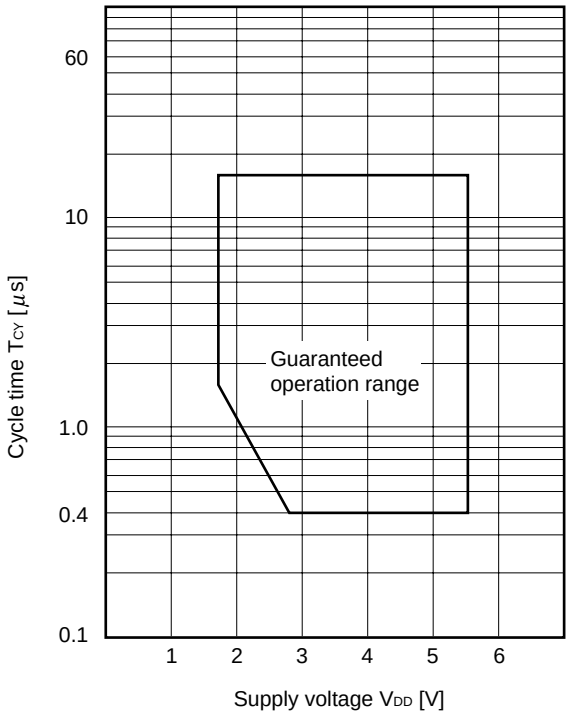
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		16	μs
		V_{DD} = 1.8 to 5.5 V	1.6		16	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 - 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

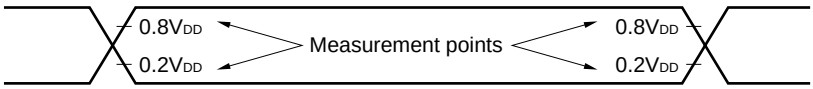
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

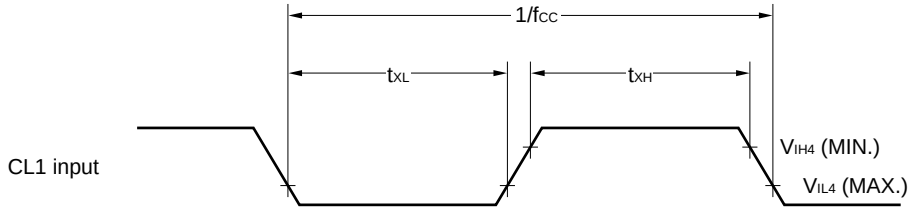
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

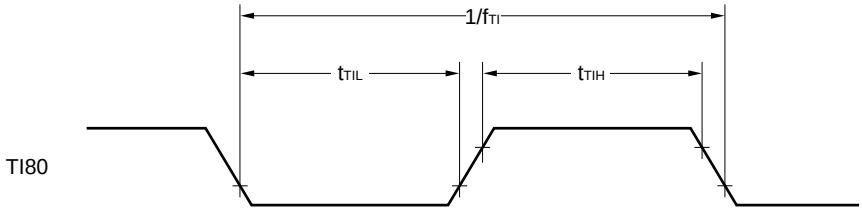
AC Timing Measurement Points (Excluding CL1 Input)



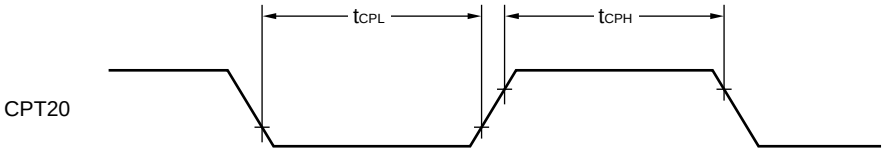
Clock Timing



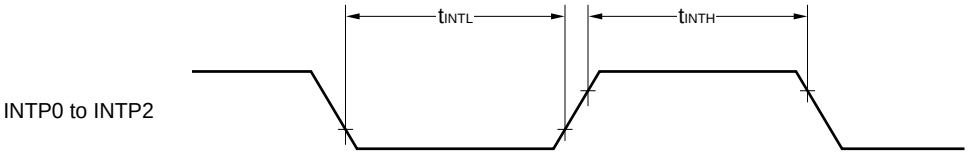
TI Timing



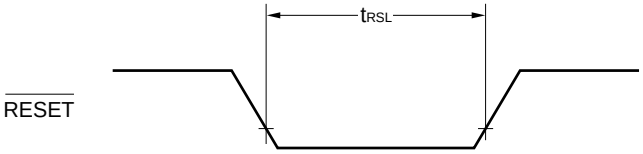
Capture Input Timing



Interrupt Input Timing

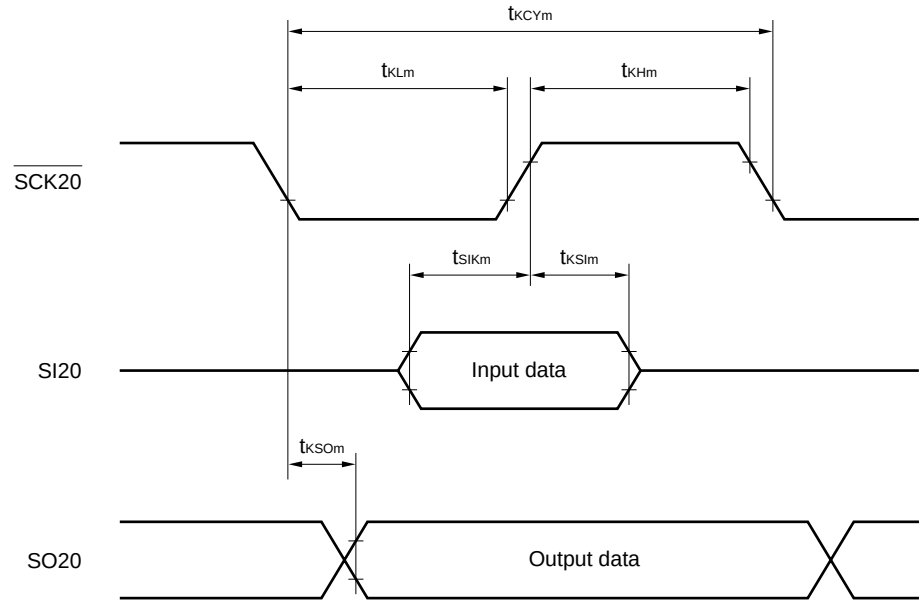


$\overline{\text{RESET}}$ Input Timing



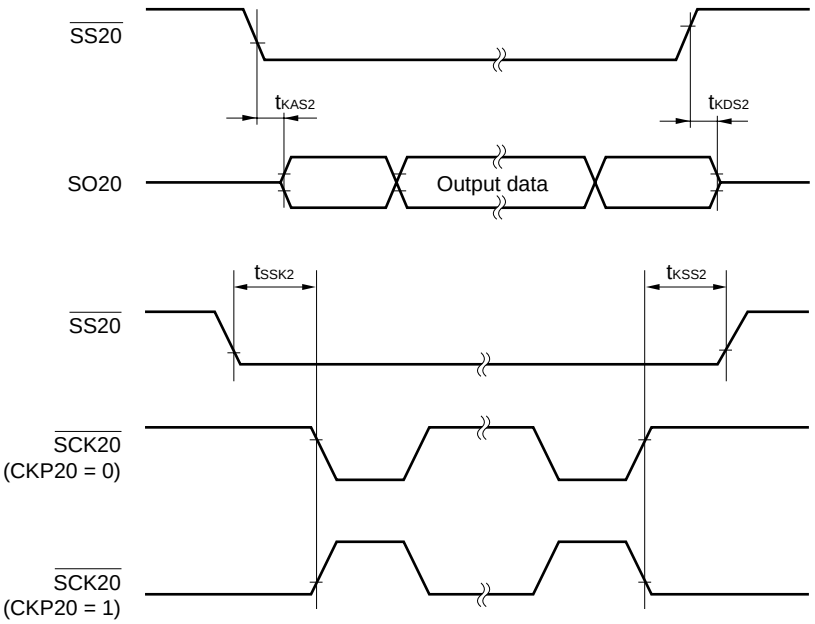
Serial Transfer Timing

3-wire serial I/O mode:

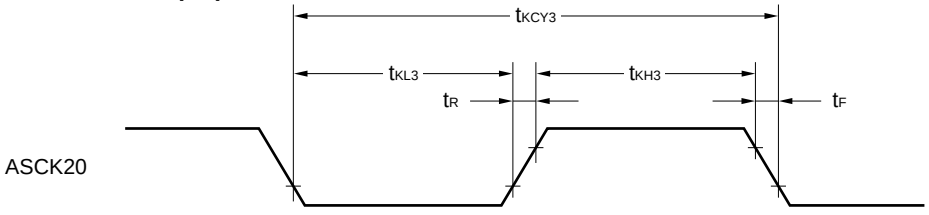


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78912xA, 78912xA(A))

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	Bits
Overall error[Notes 1, 2]		V_{DD} = 2.7 to 5.5 V		±0.4	±0.6	%FSR
		V_{DD} = 1.8 to 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	V_{DD} = 2.7 to 5.5 V	14		100	μs
		V_{DD} = 1.8 to 5.5 V	28		100	μs
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.2%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

10-Bit A/D Converter Characteristics (μPD78913xA, 78913xA(A))

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

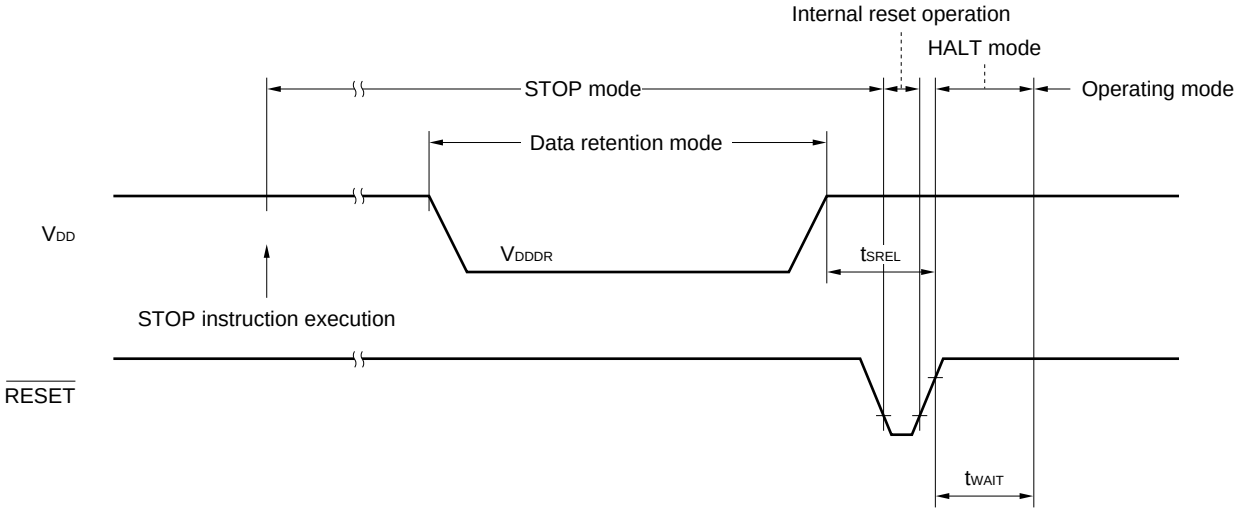
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		s
		Release by interrupt request		$2^7/f_{CC}$		s

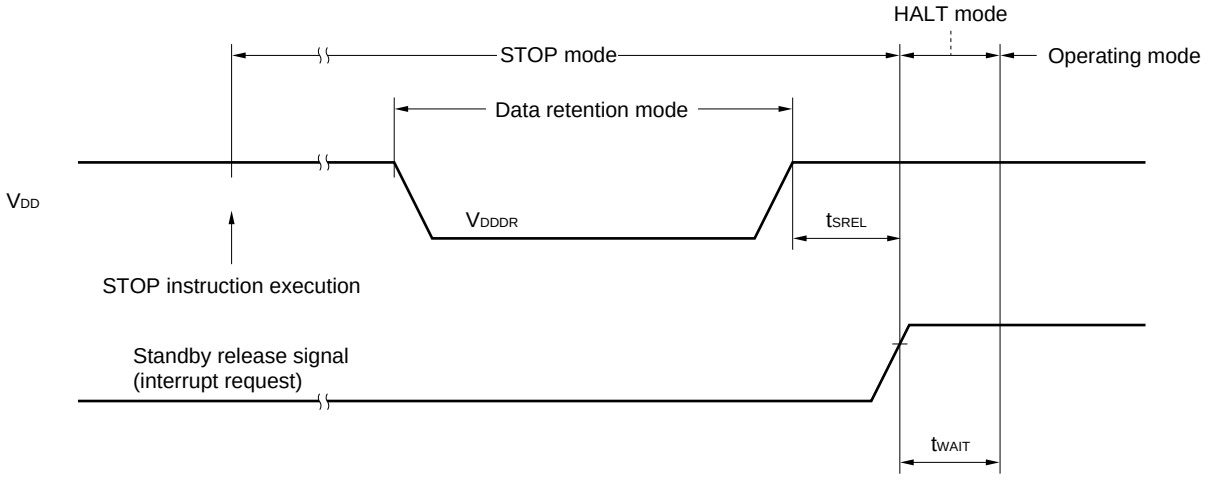
Note The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

Remark f_{CC}: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



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CHAPTER 28 ELECTRICAL SPECIFICATIONS
(μPD78912xA(A1), 78913xA(A1), 78912xA(A2), 78913xA(A2))

Absolute Maximum Ratings (T_A = 25°C)

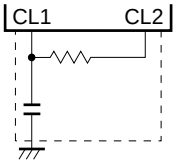
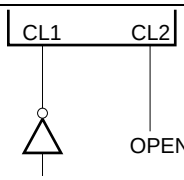
Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
			With an on-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78912xA(A1), 78913xA(A1)	–4	mA
		Total for all pins		–14	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)	–2	mA
		Total for all pins		–6	mA
Output current, low	I_{OL}	Per pin	μPD78912xA(A1), 78913xA(A1)	5	mA
		Total for all pins		80	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)	2	mA
		Total for all pins		40	mA
Operating ambient temperature	T_A	μPD78912xA(A1), 78913xA(A1)		–40 to +110	°C
		μPD78912xA(A2), 78913xA(A2)		–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)),
–40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC})[Note]		2.0		4.0	MHz
External clock		CL1 input frequency (f_{CC})[Note]		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Construct the oscillator with R and C devices that are guaranteed to operate under the following temperature conditions.

μPD78912xA(A1), 78913xA(A1): T_A = 110°C
μPD78912xA(A2), 78913xA(A2): T_A = 125°C

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2))) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78912xA(A1), 78913xA(A1)				–1	mA
		Total for all pins					–7	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)				–1	mA
		Total for all pins					–3	mA
Output current, low	I_{OL}	Per pin	μPD78912xA(A1), 78913xA(A1)				1.6	mA
		Total for all pins					40	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)				1.6	mA
		Total for all pins					20	mA
Input voltage, high	V_{IH1}	Pins other than described below			0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain		0.7V_{DD}		10	V
			With on-chip pull-up resistor		0.7V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25			0.8V_{DD}		V_{DD}	V
	V_{IH4}	CL1, CL2			V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below			0		0.3V_{DD}	V
	V_{IL2}	P50 to P53			0		0.3V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25			0		0.2V_{DD}	V
	V_{IL4}	CL1, CL2			0		0.1	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA			V_{DD} – 2.0			V
	V_{OH2}	I_{OH} = –100 μA			V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA				2.0	V
			I_{OL} = 400 μA				1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA				1.0	V
Input leakage current, high	I_{LIH1}	Pins other than CL1, CL2, or P50 to P53		$V_I = V_{DD}$			10	μA
	I_{LIH2}	CL1, CL2					20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)		V_I = 10 V			80	μA
Input leakage current, low	I_{LIL1}	Pins other than CL1, CL2, or P50 to P53		V_I = 0 V			–10	μA
	I_{LIL2}	CL1, CL2					–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)					–10[Note]	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$					10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V					–10	μA

Note When pull-up resistors are not connected to P50 to P53 (specified by the mask option) and when port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2))) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63	50	100	300	kΩ
Mask option pull-up resistance	R_2	V_I = 0 V, P50 to P53	10	30	100	kΩ
Power supply current	I_{DD1} Note 1	4.0 MHz crystal oscillation operating mode (R = 4.7 kΩ, C = 22 pF) Note 3		1.8	8.0	mA
	I_{DD2} Note 1	4.0 MHz crystal oscillation HALT mode (R = 4.7 kΩ, C = 22 pF) Note 3		0.8	5.0	mA
	I_{DD3} Note 1	STOP mode		0.1	1000	μA
	I_{DD4} Note 2	4.0 MHz crystal oscillation A/D operating mode (R = 4.7 kΩ, C = 22 pF) Note 3		3.0	10	mA

Notes 1. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

3. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

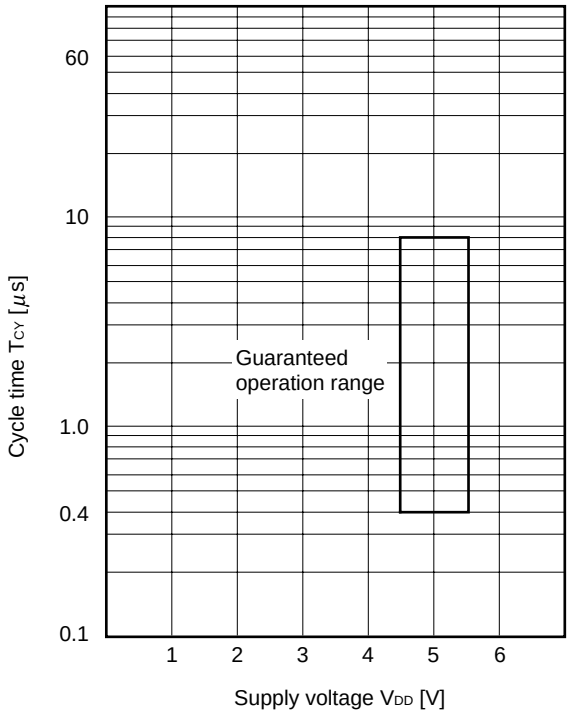
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}		0.4		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
TI80 input frequency	f_{TI}		0		4	MHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}				120	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}				240	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}		100			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}		400			ns

Note R and C are the load resistance and load capacitance of the SO output line.

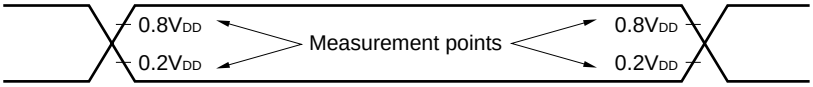
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

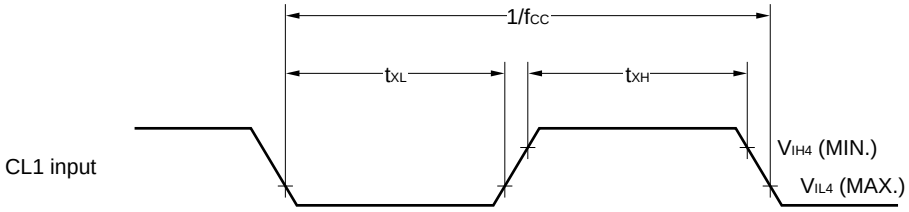
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		800			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

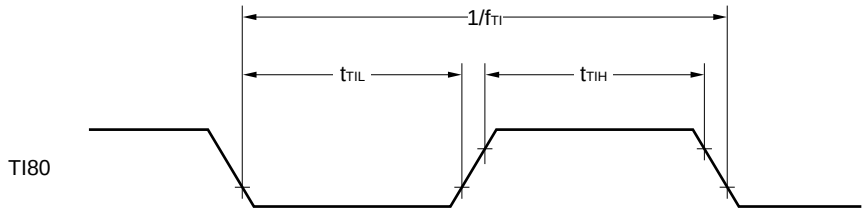
AC Timing Measurement Points (Excluding CL1 Input)



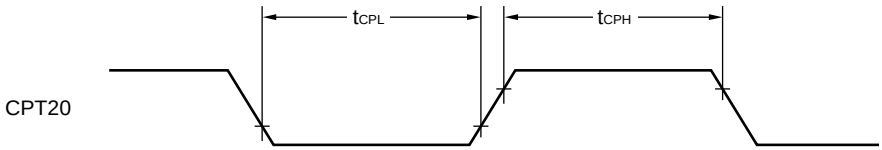
Clock Timing



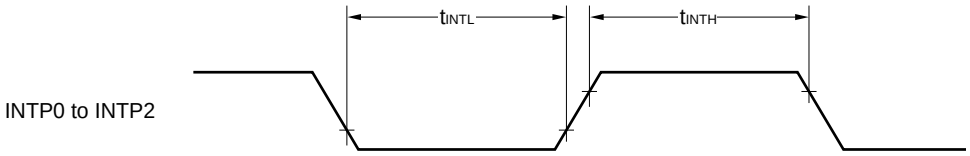
TI Timing



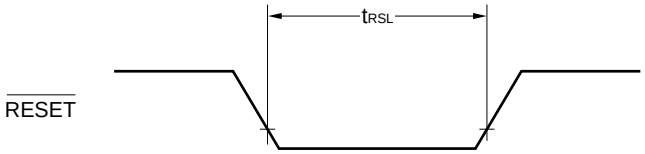
Capture Input Timing



Interrupt Input Timing

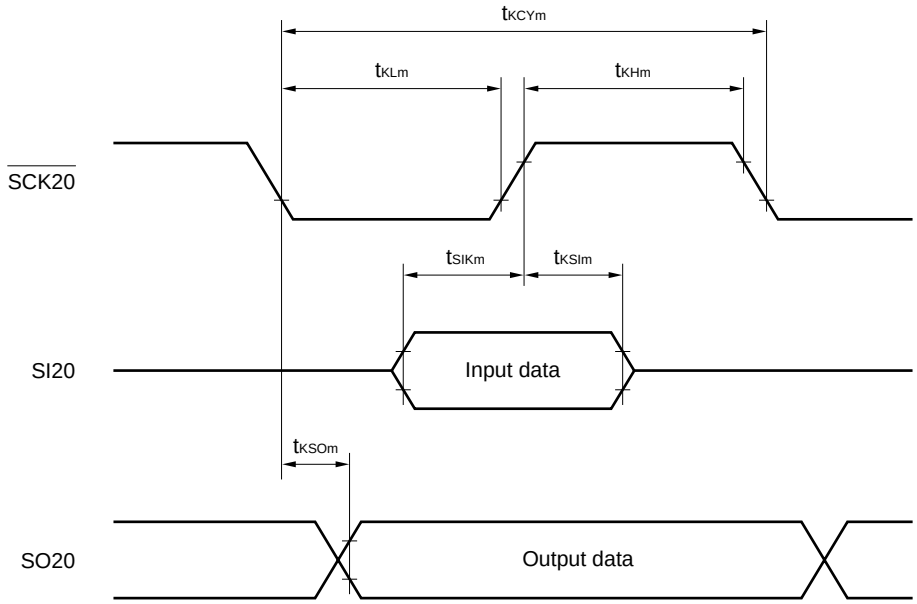


$\overline{\text{RESET}}$ Input Timing



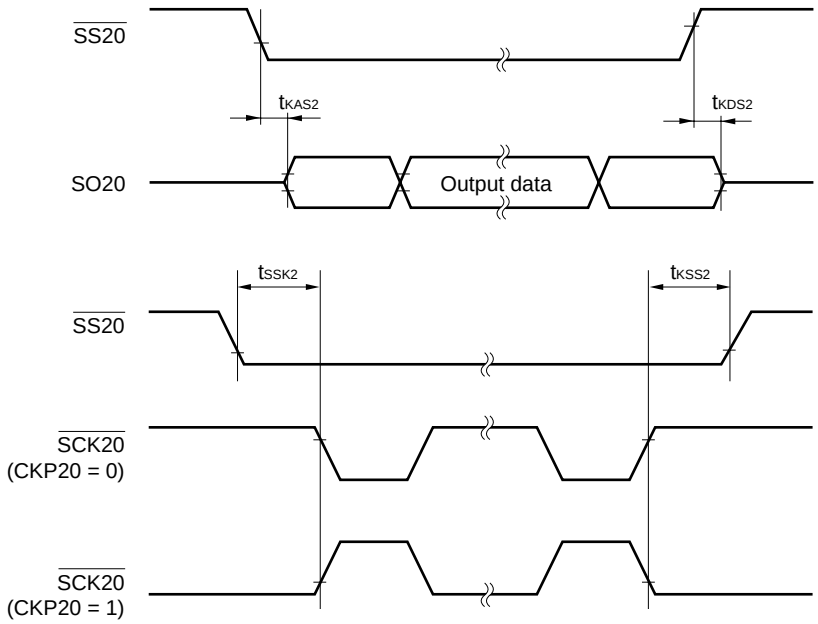
Serial Transfer Timing

3-wire serial I/O mode:

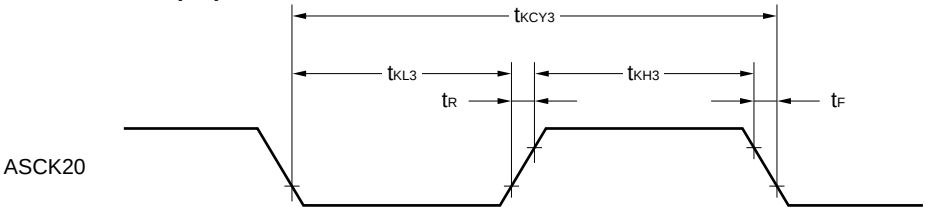


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78912xA(A1), 78912xA(A2) only)

(AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 to +110°C (μPD78912xA(A1)), –40 to +125°C (μPD78912xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	Bits
Overall error[Notes 1, 2]				±0.4	±1.0	%FSR
Conversion time	t_{CONV}		14		28	μs
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.2%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

10-Bit A/D Converter Characteristics (μPD78913xA(A1), 78913xA(A2) only)

(AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 to +110°C (μPD78913xA(A1)), –40 to +125°C (μPD78913xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]				±0.4	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Notes 1, 2]					±0.6	%FSR
Full-scale error[Notes 1, 2]					±0.6	%FSR
Integral linearity error[Note 1]	ILE				±4.5	LSB
Differential linearity error[Note 1]	DLE				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

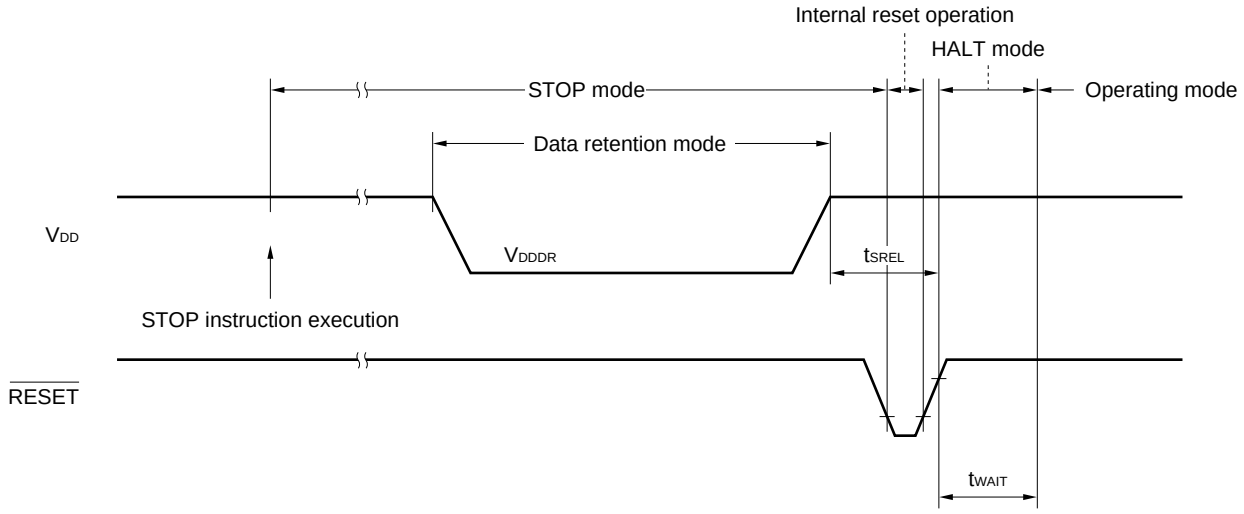
(T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		s
		Release by interrupt request		$2^7/f_{CC}$		s

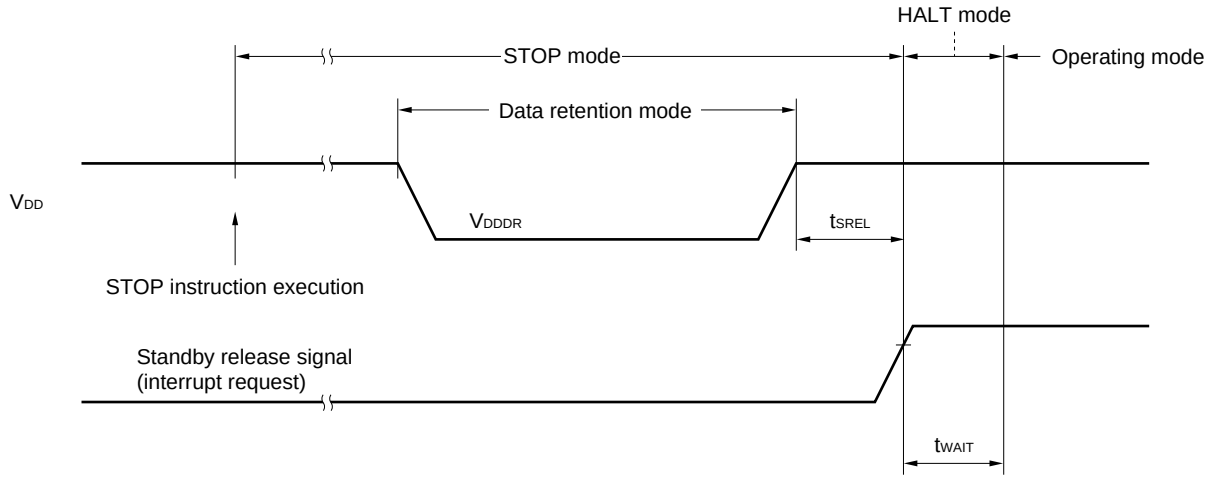
Note The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

Remark f_{CC}: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

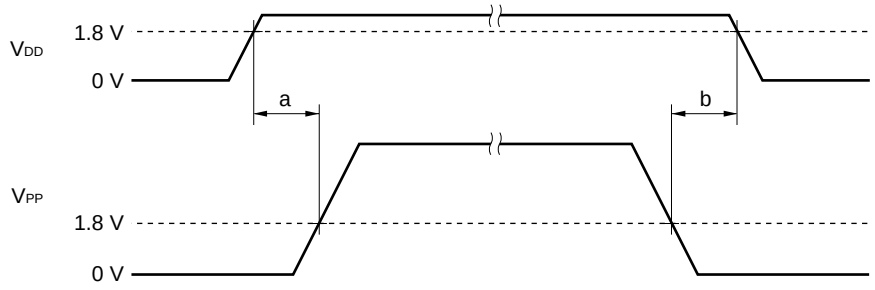


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78F9136B	–10	mA
		Total for all pins		–30	mA
		Per pin	μPD78F9136B(A)	–7	mA
		Total for all pins		–22	mA
Output current, low	I_{OL}	Per pin	μPD78F9136B	30	mA
		Total for all pins		160	mA
		Per pin	μPD78F9136B(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

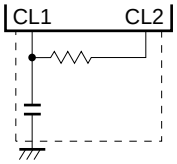
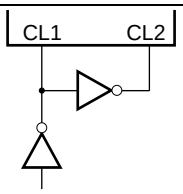
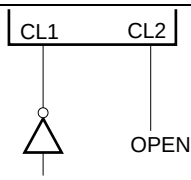
- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see a in the figure below).
- When supply voltage drops
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see b in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC})[Note]		2.0		4.0	MHz
External clock		CL1 input frequency (f_{CC})[Note]		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		CL1 input frequency (f_{CC})[Note]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

RC Oscillator Frequency Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{CC1}	R = 11.0 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	1.5	2.0	2.5	MHz
	f_{CC2}	Target: 2 MHz	V_{DD} = 1.8 to 3.6 V	0.5	2.0	2.5	MHz
	f_{CC3}		V_{DD} = 1.8 to 5.5 V	0.5	2.0	2.5	MHz
	f_{CC4}	R = 6.8 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	2.5	3.0	3.5	MHz
	f_{CC5}	Target: 3 MHz	V_{DD} = 1.8 to 3.6 V	0.75	3.0	3.5	MHz
	f_{CC6}		V_{DD} = 1.8 to 5.5 V	0.75	3.0	3.5	MHz
	f_{CC7}	R = 4.7 kΩ, C = 22 pF	V_{DD} = 2.7 to 5.5 V	3.5	4.0	4.7	MHz
	f_{CC8}	Target: 4 MHz	V_{DD} = 1.8 to 3.6 V	1.0	4.0	4.7	MHz
	f_{CC9}		V_{DD} = 1.8 to 5.5 V	1.0	4.0	4.7	MHz

Remark So that the TYP. spec. is satisfied between 2.0 to 4.0 MHz, set one of the above nine patterns for R and C.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78F9136B				–1	mA
		Total for all pins					–15	mA
		Per pin	μPD78F9136B(A)				–1	mA
		Total for all pins					–11	mA
Output current, low	I_{OL}	Per pin	μPD78F9136B				10	mA
		Total for all pins					80	mA
		Per pin	μPD78F9136B(A)				3	mA
		Total for all pins					60	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	CL1, CL2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	CL1, CL2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78F9136B)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78F9136B(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78F9136B)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78F9136B(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than CL1, CL2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	CL1, CL2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than CL1, CL2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	CL1, CL2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53		50	100	200	kΩ
Power supply current	I_{DD1} Note 2	4.0 MHz RC oscillation operating mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		6.5	18.0	mA
			V_{DD} = 3.0 V ±10% Note 5		3.9	7.9	mA
			V_{DD} = 2.0 V ±10% Note 5		3.0	5.0	mA
	I_{DD2} Note 2	4.0 MHz RC oscillation HALT mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.5	5.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.0	2.0	mA
			V_{DD} = 2.0 V ±10% Note 5		0.75	1.5	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA
	I_{DD4} Note 3	4.0 MHz RC oscillation A/D operating mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		7.7	20.3	mA
			V_{DD} = 3.0 V ±10% Note 5		5.1	10.2	mA
			V_{DD} = 2.0 V ±10% Note 5		4.0	7.0	mA

Notes 1. When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V, RC Oscillation Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1}			21	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1}			21	mA
Erase current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.2	0.2	0.2	s
Total erase time	t_{era}				20	s
Rewrite count		Erase/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

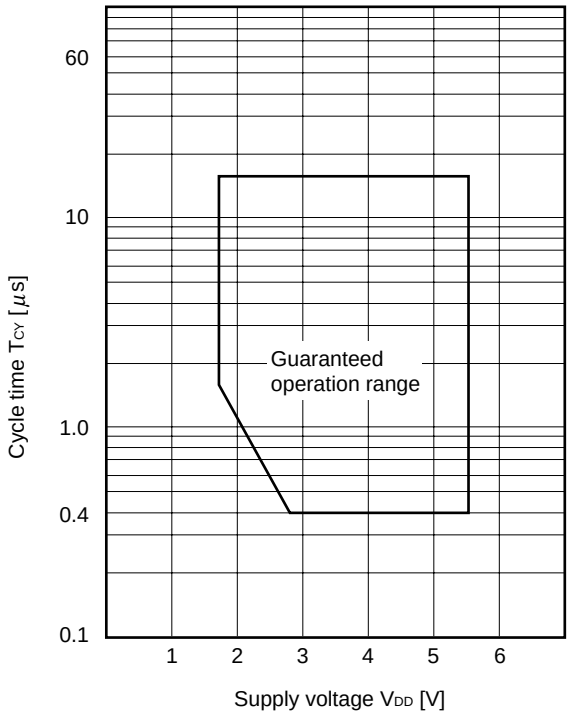
Note The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		16	μs
		V_{DD} = 1.8 to 5.5 V	1.6		16	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 – 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 – 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

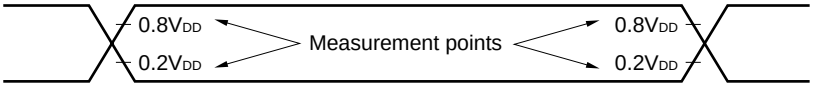
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

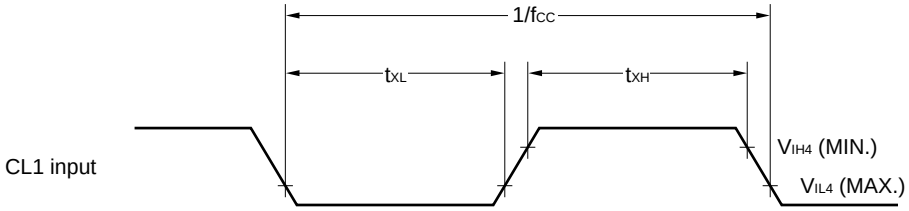
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

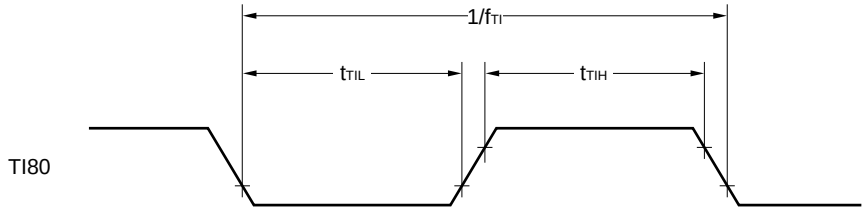
AC Timing Measurement Points (Excluding CL1 Input)



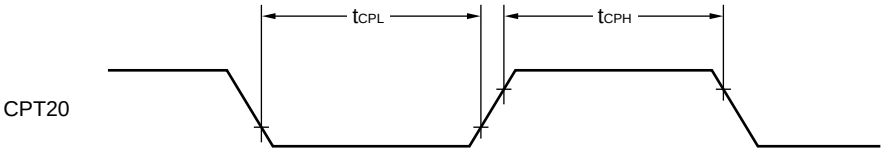
Clock Timing



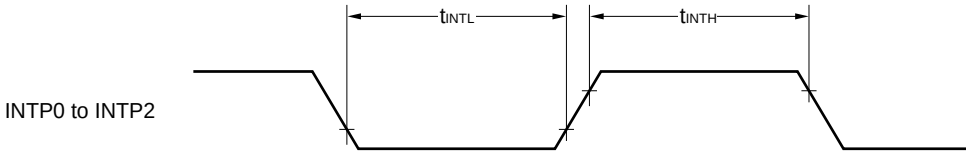
TI Timing



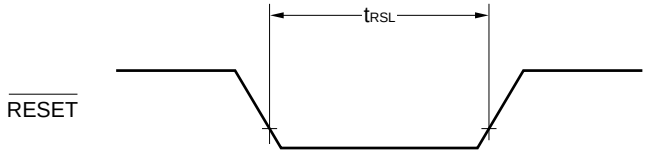
Capture Input Timing



Interrupt Input Timing

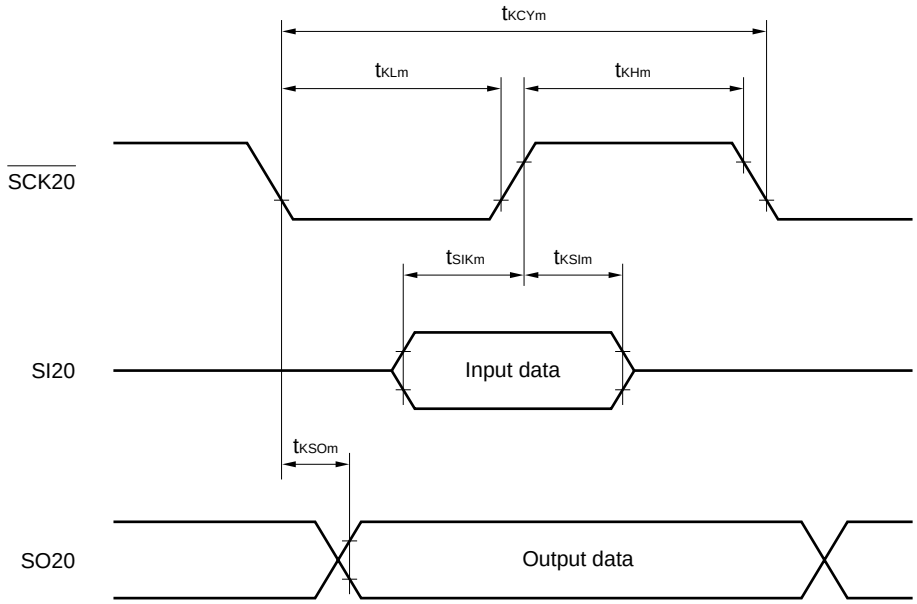


$\overline{\text{RESET}}$ Input Timing



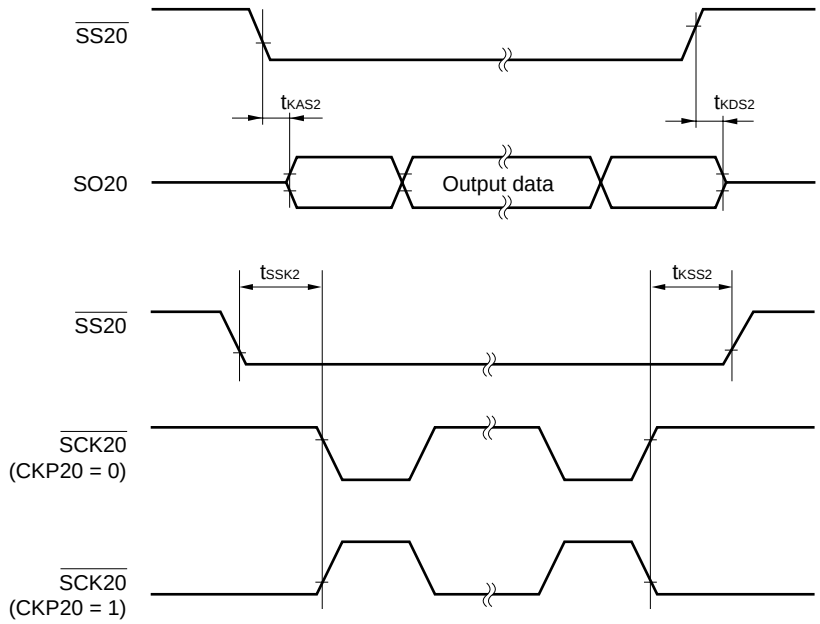
Serial Transfer Timing

3-wire serial I/O mode:

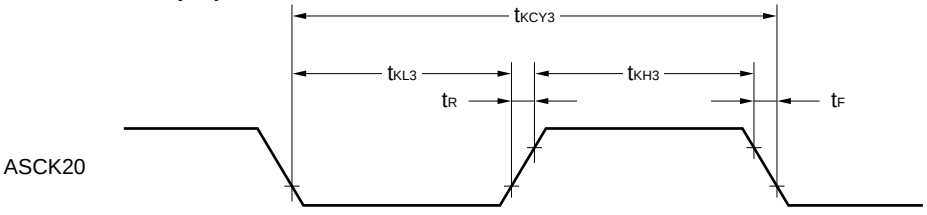


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1, 2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

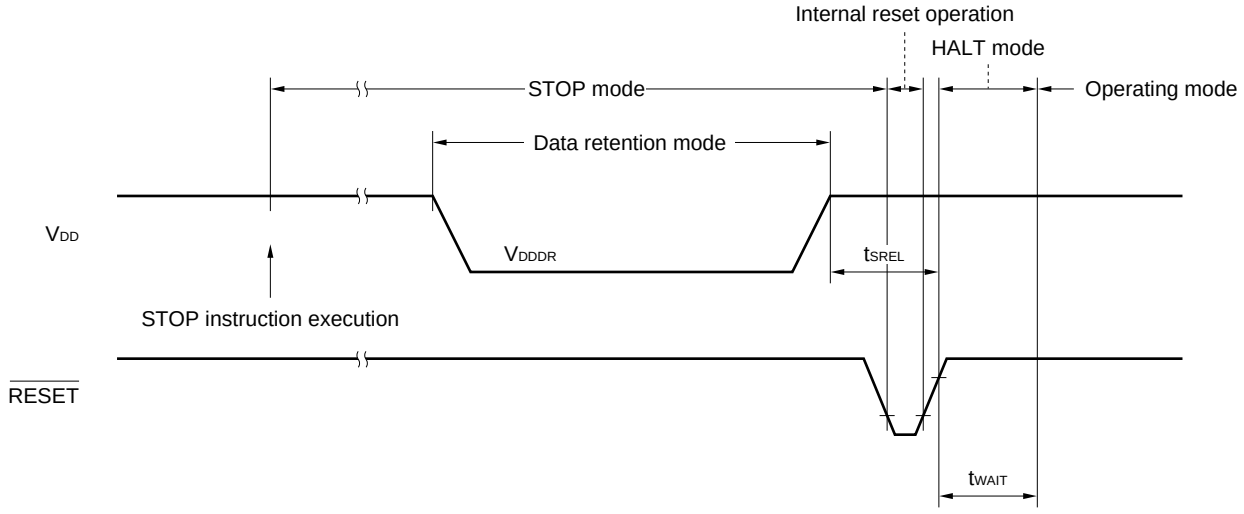
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		s
		Release by interrupt request		$2^7/f_{CC}$		s

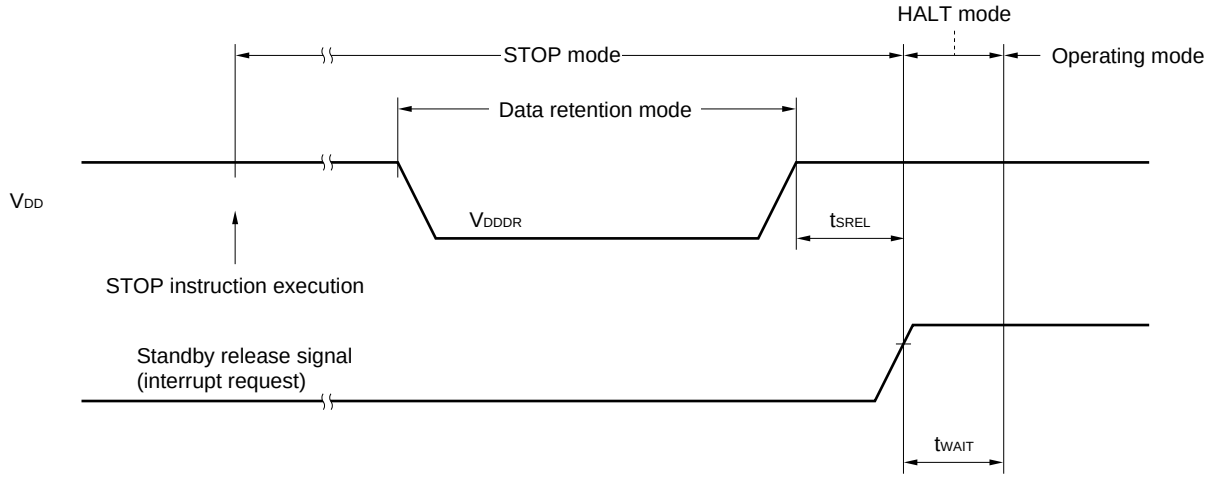
Note The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

Remark f_{CC}: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

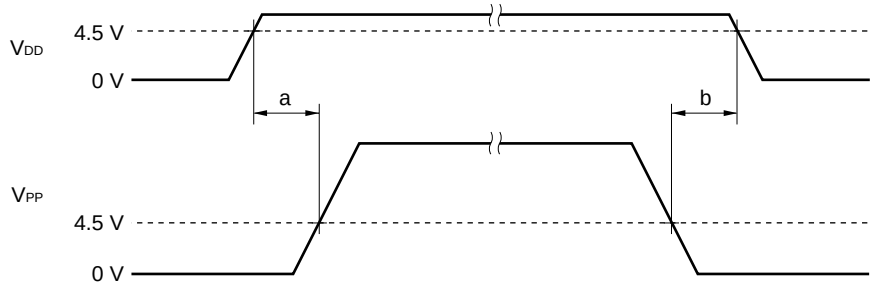


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–4	mA
		Total for all pins		–14	mA
Output current, low	I_{OL}	Per pin		5	mA
		Total for all pins		80	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +105	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

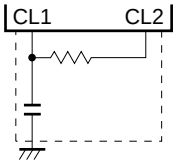
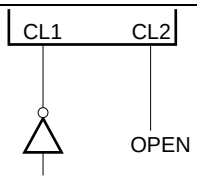
- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (4.5 V) of the operating voltage range (see a in the figure below).
- When supply voltage drops
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (4.5 V) of the operating voltage range of V_{DD} (see b in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC})[Note]		2.0		4.0	MHz
External clock		CL1 input frequency (f_{CC})[Note]		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Construct the oscillator with R and C devices that are guaranteed to operate at T_A = 105°C.

DC Characteristics (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–7	mA
Output current, low	I_{OL}	Per pin				1.6	mA
		Total for all pins				40	mA
Input voltage, high	V_{IH1}	Pins other than described below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	0.7V_{DD}		10	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		0.8V_{DD}		V_{DD}	V
	V_{IH4}	CL1, CL2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		0		0.3V_{DD}	V
	V_{IL2}	P50 to P53		0		0.3V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		0		0.2V_{DD}	V
	V_{IL4}	CL1, CL2		0		0.1	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA		V_{DD} – 2.0			V
	V_{OH2}	I_{OH} = –100 μA		V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA			2.0	V
			I_{OL} = 400 μA			1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA			1.0	V
Input leakage current, high	I_{LIH1}	Pins other than CL1, CL2, or P50 to P53	V_I = V_{DD}			10	μA
	I_{LIH2}	CL1, CL2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 10 V			80	μA
Input leakage current, low	I_{LIL1}	Pins other than CL1, CL2, or P50 to P53	V_I = 0 V			–10	μA
	I_{LIL2}	CL1, CL2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–10[Note]	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA

Note When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53 or P60 to P63	50	100	300	kΩ
Power supply current	I_{DD1} Note 1	4.0 MHz RC oscillation operating mode (R = 4.7 kΩ, C = 22 pF) Note 3		7.5	20.0	mA
	I_{DD2} Note 1	4.0 MHz RC oscillation HALT mode (R = 4.7 kΩ, C = 22 pF) Note 3		3.0	5.5	mA
	I_{DD3} Note 1	STOP mode		1	1000	μA
	I_{DD4} Note 2	4.0 MHz RC oscillation A/D operating mode (R = 4.7 kΩ, C = 22 pF) Note 3		8.7	22.3	mA

Notes 1. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

3. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Erase Characteristics
(T_A = 10 to 40°C, V_{DD} = 4.5 to 5.5 V, RC Oscillation Operating Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1}			21	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1}			21	mA
Erase current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.2	0.2	0.2	s
Total erase time	t_{era}				20	s
Rewrite count		Erase/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

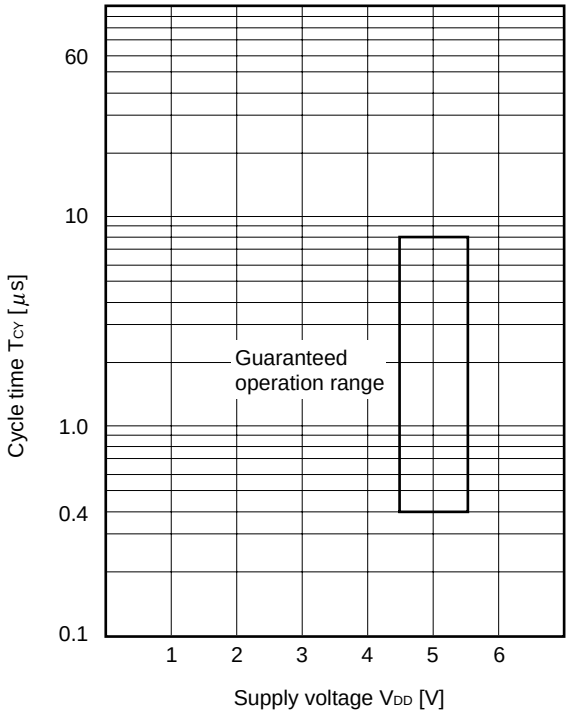
Note The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}		0.4		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
TI80 input frequency	f_{TI}		0		4	MHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +105°C, V_{DD} = 4.5 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}\uparrow$)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}\uparrow$)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}\downarrow$	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}\uparrow$)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}\uparrow$)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}\downarrow$	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (to $\overline{SS20}\downarrow$ when $\overline{SS20}$ is used)	t_{KAS2}				120	ns
SO20 disable time (for $\overline{SS20}\uparrow$ when $\overline{SS20}$ is used)	t_{KDS2}				240	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}		100			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}		400			ns

Note R and C are the load resistance and load capacitance of the SO output line.

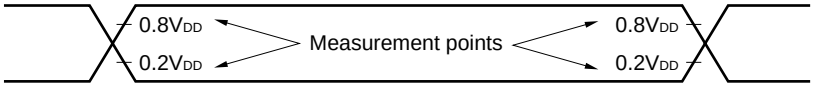
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

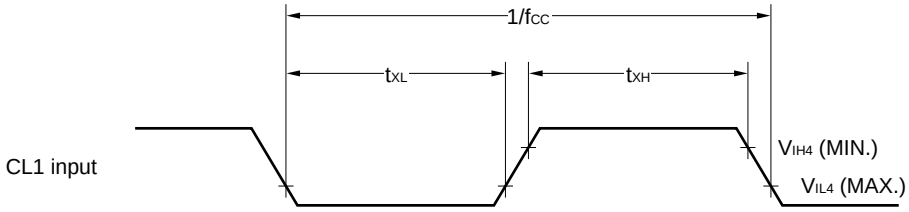
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		800			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

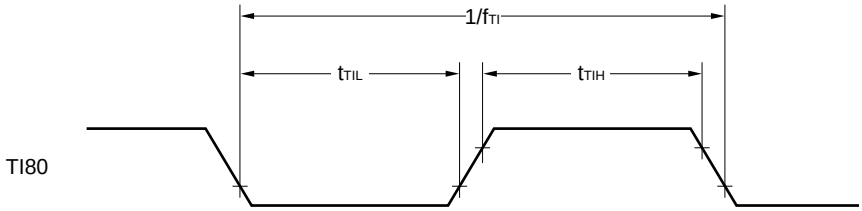
AC Timing Measurement Points (Excluding CL1 Input)



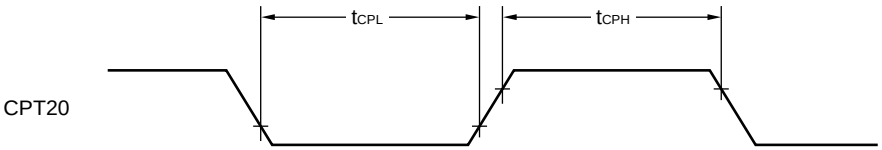
Clock Timing



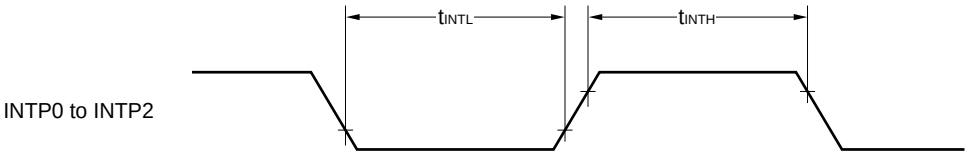
TI Timing



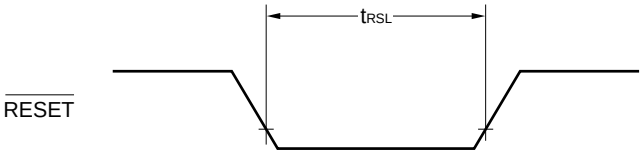
Capture Input Timing



Interrupt Input Timing

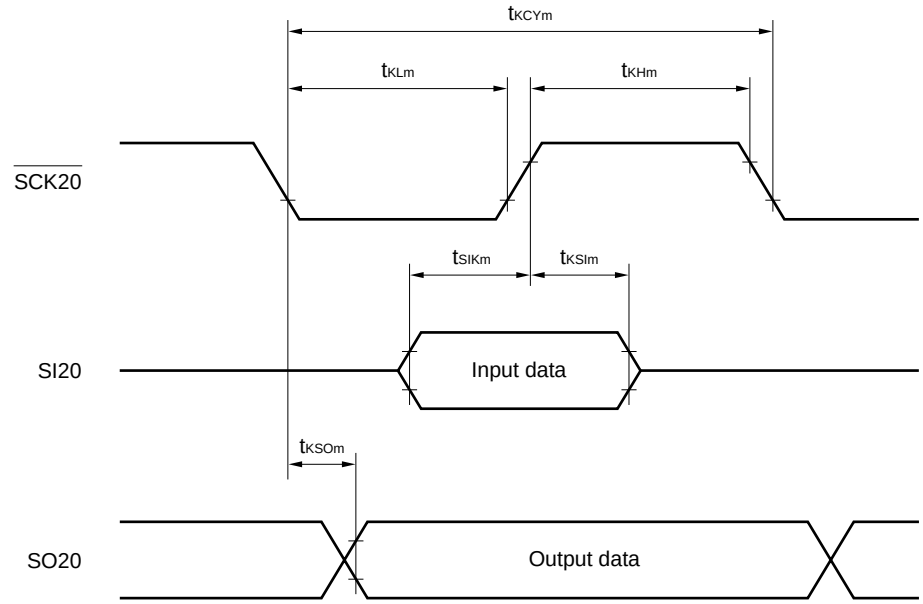


$\overline{\text{RESET}}$ Input Timing



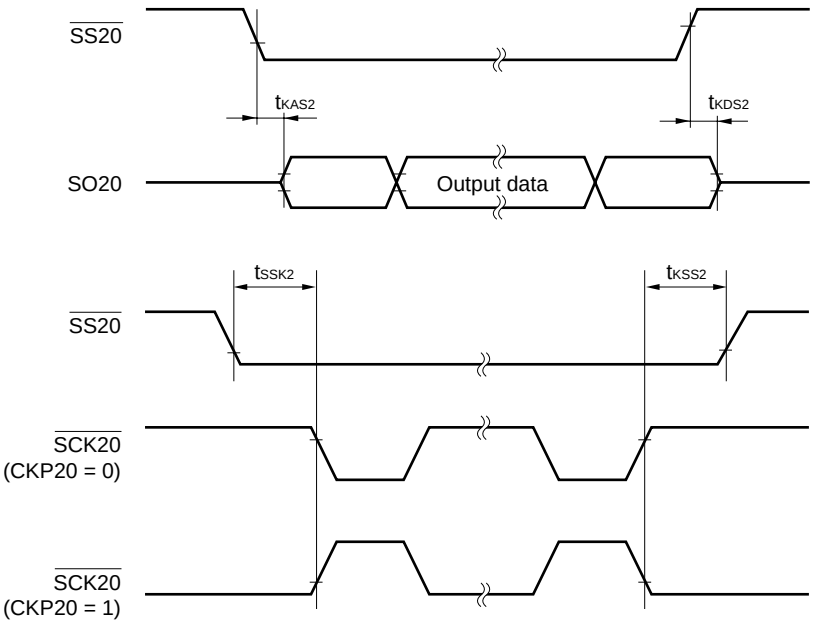
Serial Transfer Timing

3-wire serial I/O mode:

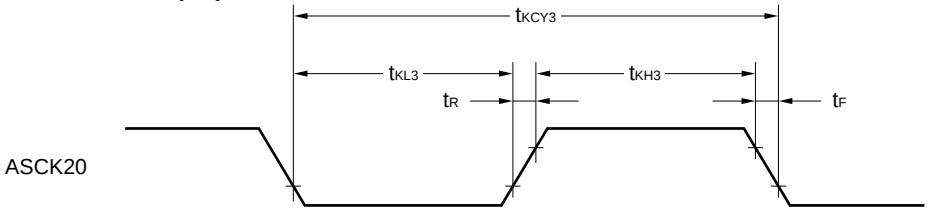


m = 1, 2

3-wire serial I/O mode (when SS20 is used):



UART mode (external clock input):



10-Bit A/D Converter Characteristics (T_A = –40 to +105°C, AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1,2]				±0.4	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Notes 1,2]					±0.6	%FSR
Full-scale error[Notes 1,2]					±0.6	%FSR
Integral linearity error[Note 1]	ILE				±4.5	LSB
Differential linearity error[Note 1]	DLE				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

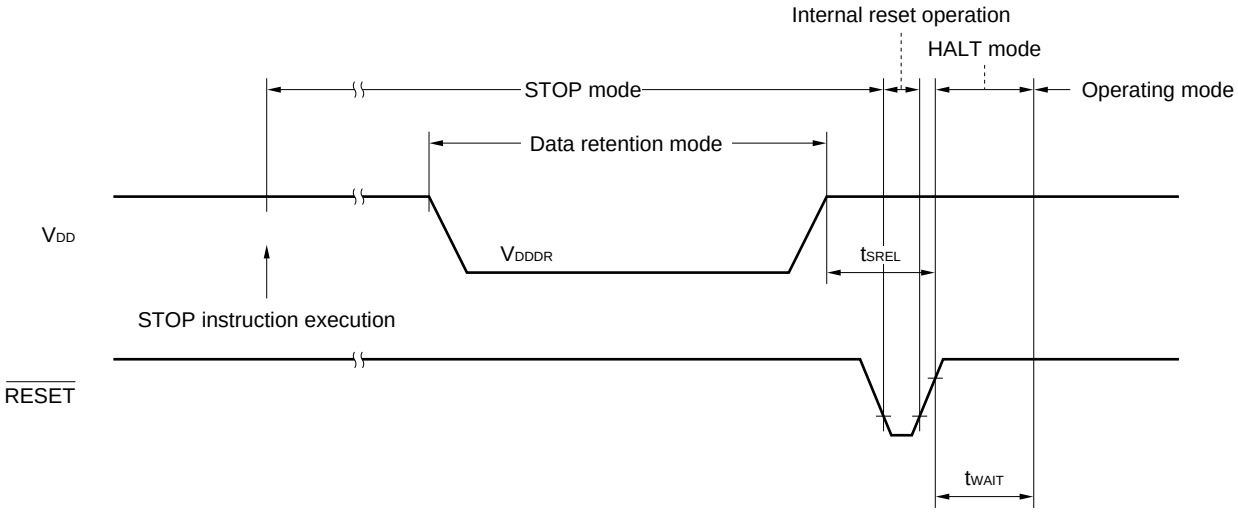
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		s
		Release by interrupt request		$2^7/f_{CC}$		s

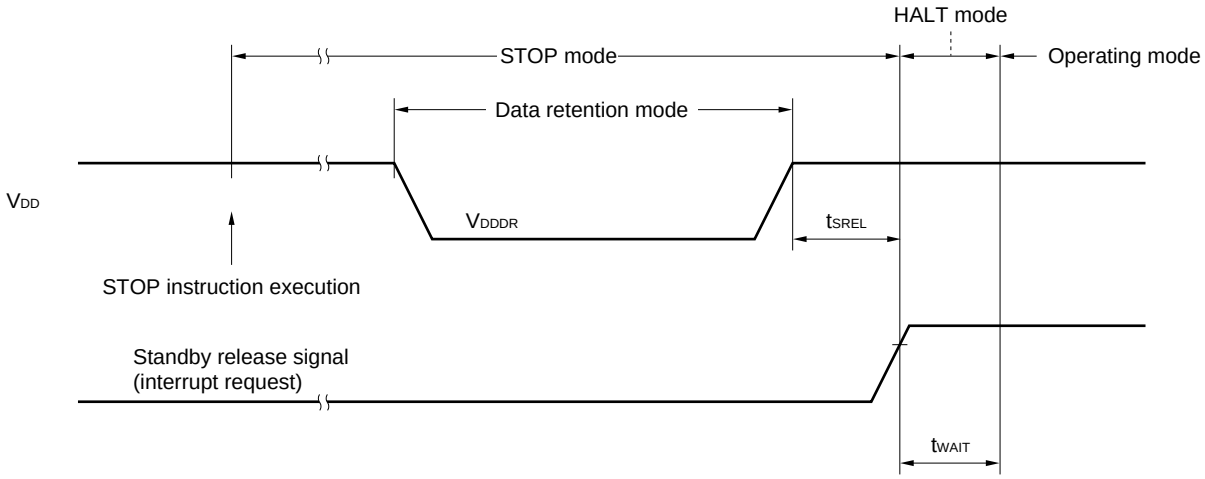
Note The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

Remark f_{CC}: System clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

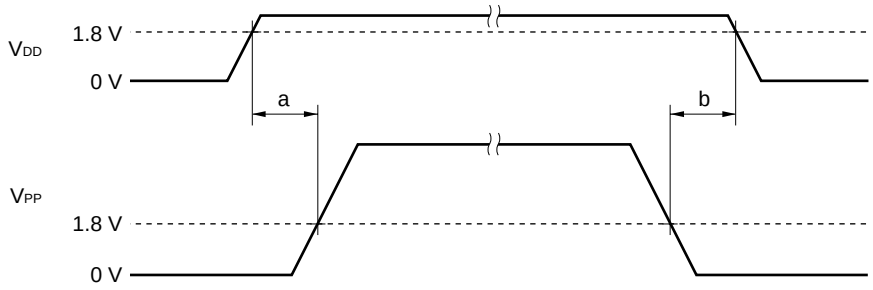


Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}		–0.3 to +6.5	V
	V_{PP}	**Note**		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for all pins		–30	mA
Output current, low	I_{OL}	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

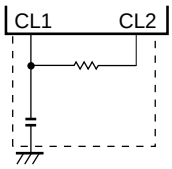
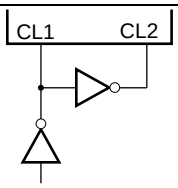
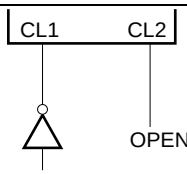
- When supply voltage rises
  V_{PP} must exceed V_{DD} 10 μs or more after V_{DD} has reached the lower-limit value (1.8 V) of the operating voltage range (see a in the figure below).
- When supply voltage drops
  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (1.8 V) of the operating voltage range of V_{DD} (see b in the figure below).



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC})[Note 1]	V_{DD} = oscillation voltage range	2.0		4.0	MHz
External clock		CL1 input frequency (f_{CC})[Note 1]		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		CL1 input frequency (f_{CC})[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

RC Oscillator Frequency Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{CC1}	R = 11.0 kΩ, C = 22 pF Target: 2 MHz	V_{DD} = 2.7 to 5.5 V	1.5	2.0	2.5	MHz
	f_{CC2}		V_{DD} = 1.8 to 3.6 V	0.5	2.0	2.5	MHz
	f_{CC3}		V_{DD} = 1.8 to 5.5 V	0.5	2.0	2.5	MHz
	f_{CC4}	R = 6.8 kΩ, C = 22 pF Target: 3 MHz	V_{DD} = 2.7 to 5.5 V	2.5	3.0	3.5	MHz
	f_{CC5}		V_{DD} = 1.8 to 3.6 V	0.75	3.0	3.5	MHz
	f_{CC6}		V_{DD} = 1.8 to 5.5 V	0.75	3.0	3.5	MHz
	f_{CC7}	R = 4.7 kΩ, C = 22 pF Target: 4 MHz	V_{DD} = 2.7 to 5.5 V	3.5	4.0	4.7	MHz
	f_{CC8}		V_{DD} = 1.8 to 3.6 V	1.0	4.0	4.7	MHz
	f_{CC9}		V_{DD} = 1.8 to 5.5 V	1.0	4.0	4.7	MHz

Remark So that the TYP. Spec is satisfied between 2.0 to 4.0 MHz, set one of the above nine patterns for R and C.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin					–1	mA
		Total for all pins					–15	mA
Output current, low	I_{OL}	Per pin					10	mA
		Total for all pins					80	mA
Input voltage, high	V_{IH1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V, T_A = 25 to 85°C	0.9V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	CL1, CL2		V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25		V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	CL1, CL2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	Pins other than CL1, CL2, or P50 to P53	$V_I = V_{DD}$			3	μA
	I_{LIH2}	CL1, CL2				20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)	V_I = 12 V			20	μA
Input leakage current, low	I_{LIL1}	Pins other than CL1, CL2, or P50 to P53	V_I = 0 V			–3	μA
	I_{LIL2}	CL1, CL2				–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)				–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistance	R_1	V_I = 0 V, for pins other than P50 to P53		50	100	200	kΩ
Power supply current	I_{DD1} Note 2	4.0 MHz RC oscillation operating mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		5.0	15.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.9	4.9	mA
			V_{DD} = 2.0 V ±10% Note 5		1.5	3.0	mA
	I_{DD2} Note 2	4.0 MHz RC oscillation HALT mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.5	5.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.0	2.0	mA
			V_{DD} = 2.0 V ±10% Note 5		0.75	1.5	mA
	I_{DD3} Note 2	STOP mode	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA
	I_{DD4} Note 3	4.0 MHz RC oscillation A/D operating mode (R = 4.7 kΩ, C = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		6.2	17.3	mA
			V_{DD} = 3.0 V ±10% Note 5		3.1	7.2	mA
			V_{DD} = 2.0 V ±10% Note 5		2.5	5.0	mA

Notes 1. When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

2. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

3. The current flowing to the ports (including the current flowing through on-chip pull-up resistors) is not included.

4. High-speed mode operation (when the processor clock control register (PCC) is set to 00H).

5. Low-speed mode operation (when PCC is set to 02H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Erase Characteristics (T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V, RC Oscillation Operating Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1}			18	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1}			18	mA
Erase current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.5	1	1	s
Total erase time	t_{era}				20	s
Rewrite count		Erase/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

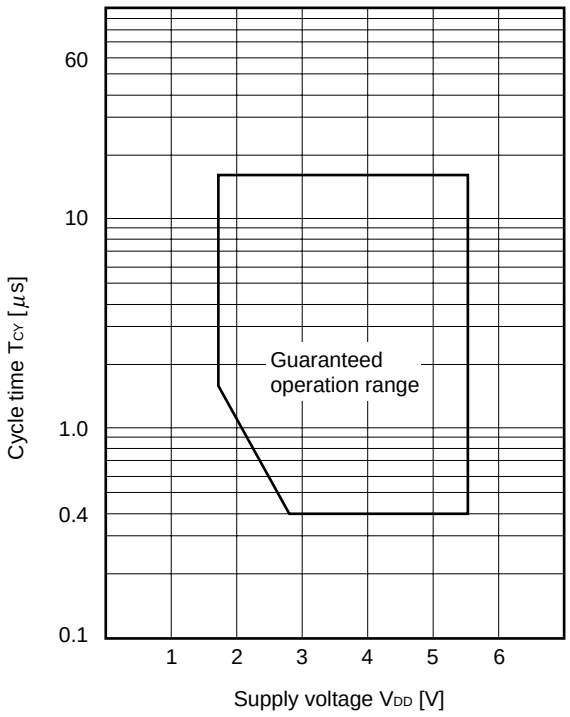
Note The current flowing to the ports (including the current flowing through on-chip pull-up resistors) and AV_{DD} current are not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V	0.4		16	μs
		V_{DD} = 1.8 to 5.5 V	1.6		16	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V	0.1			μs
		V_{DD} = 1.8 to 5.5 V	1.8			μs
TI80 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V	0		4	MHz
		V_{DD} = 1.8 to 5.5 V	0		275	kHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK20}$...internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2 - 150$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (to $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns
SS20 setup time (to $\overline{SCK20}$ first edge)	t_{SSK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SS20 hold time (from $\overline{SCK20}$ last edge)	t_{KSS2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns

Note R and C are the load resistance and load capacitance of the SO output line.

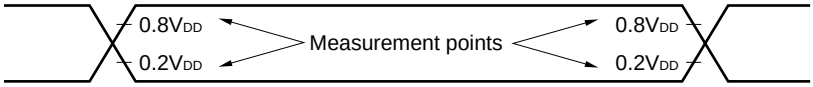
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

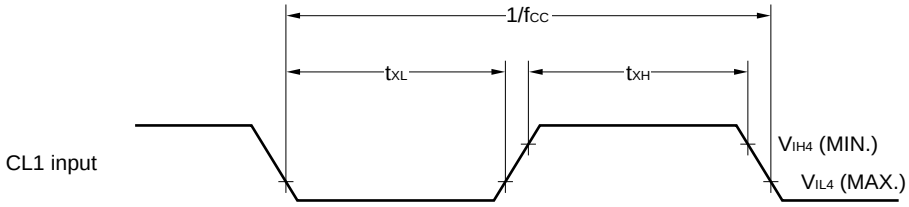
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

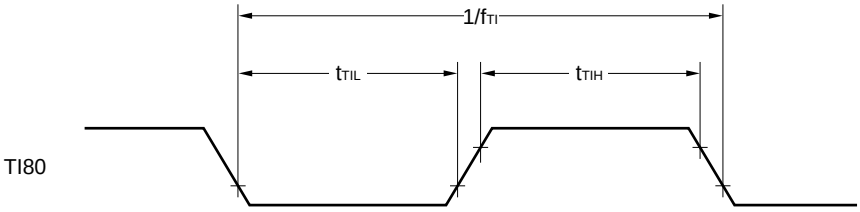
AC Timing Measurement Points (Excluding CL1 Input)



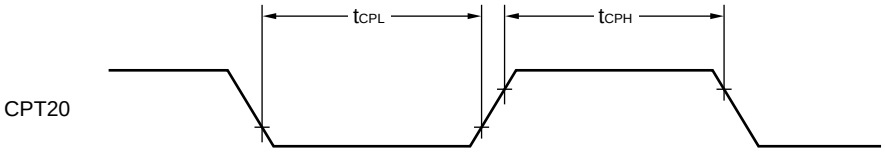
Clock Timing



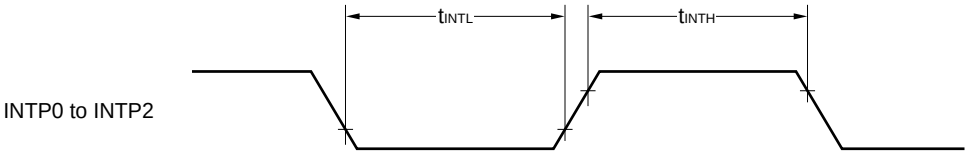
TI Timing



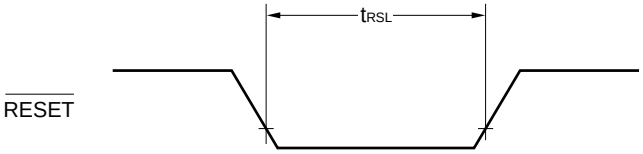
Capture Input Timing



Interrupt Input Timing

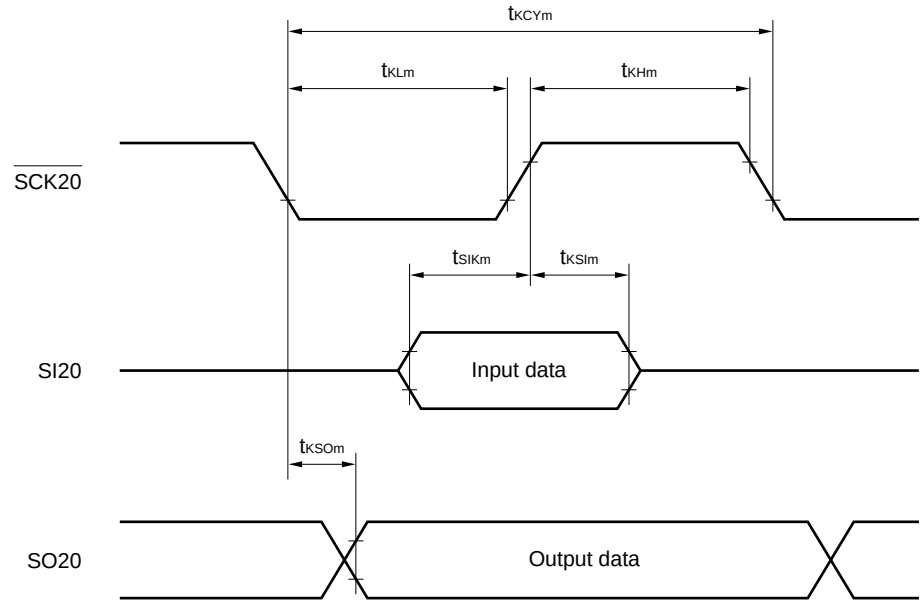


$\overline{\text{RESET}}$ Input Timing



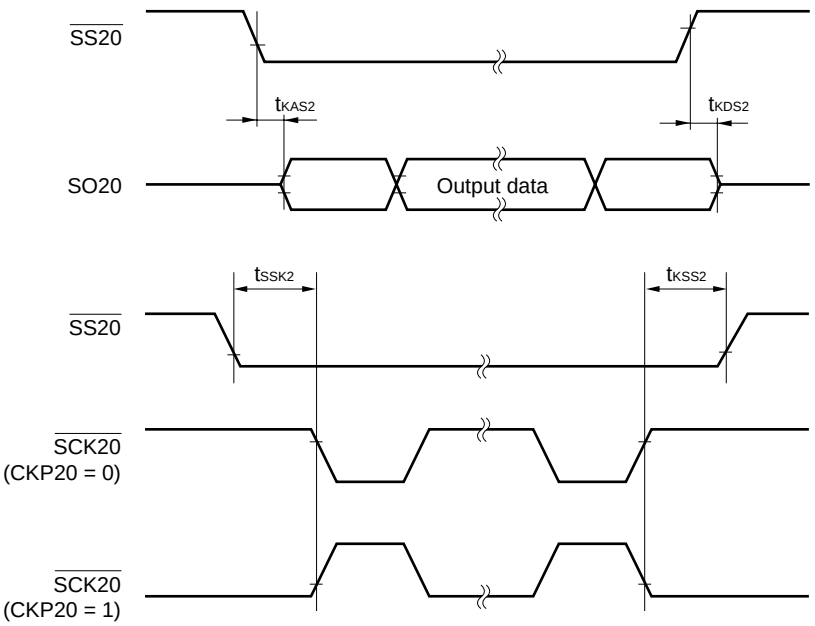
Serial Transfer Timing

3-wire serial I/O mode:

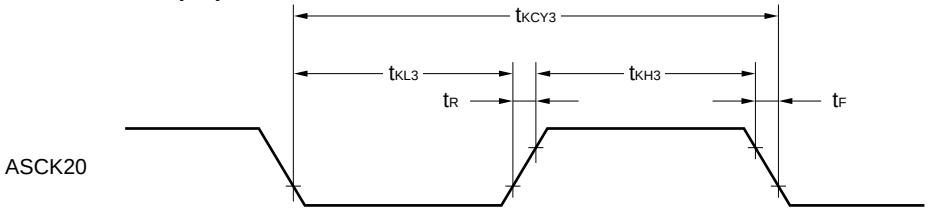


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



10-Bit A/D Converter Characteristics

(T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bits
Overall error[Notes 1,2]		4.5 V ≤ V_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	2.7 V ≤ V_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ V_{DD} < 2.7 V	28		100	μs
Zero-scale error[Notes 1,2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Full-scale error[Notes 1,2]		4.5 V ≤ V_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ V_{DD} < 4.5 V			±0.6	%FSR
		1.8 V ≤ V_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error[Note 1]	ILE	4.5 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±4.5	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±8.5	LSB
Differential linearity error[Note 1]	DLE	4.5 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ V_{DD} < 4.5 V			±2.0	LSB
		1.8 V ≤ V_{DD} < 2.7 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. This value is indicated as a ratio to the full-scale value (%FSR).

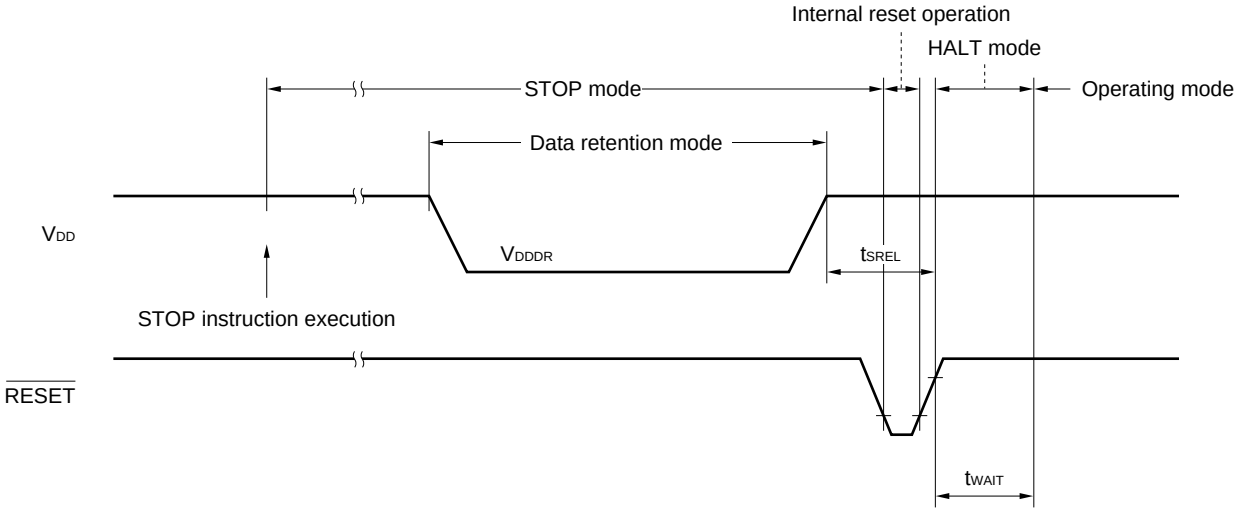
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		s
		Release by interrupt request		$2^7/f_{CC}$		s

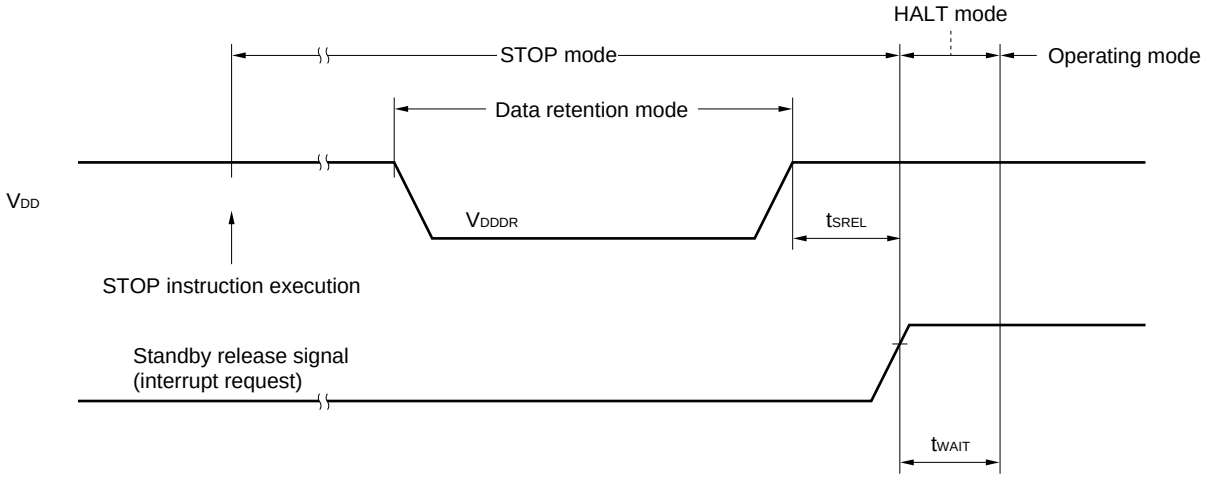
Note The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

Remark f_{CC}: System clock oscillation frequency

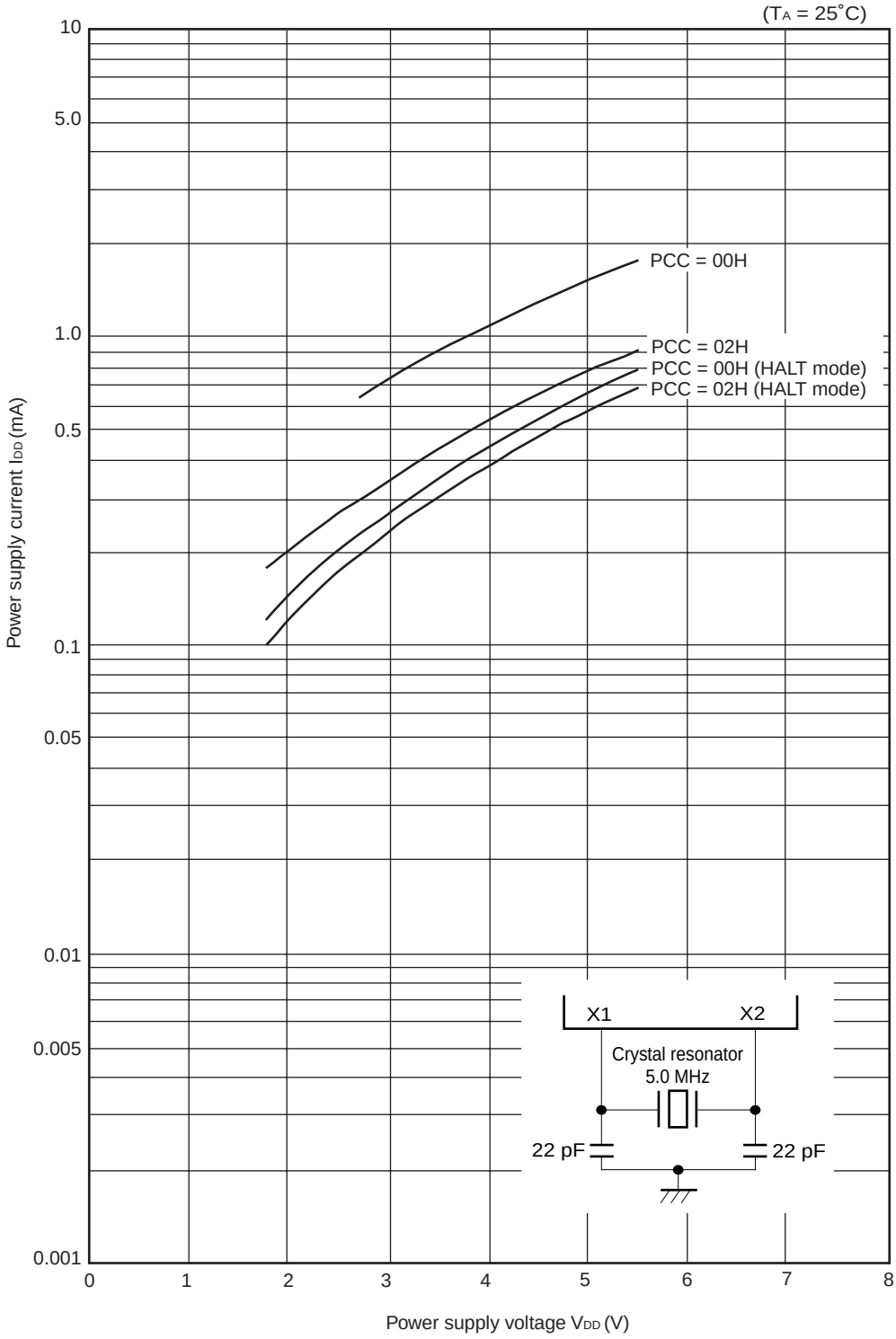
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



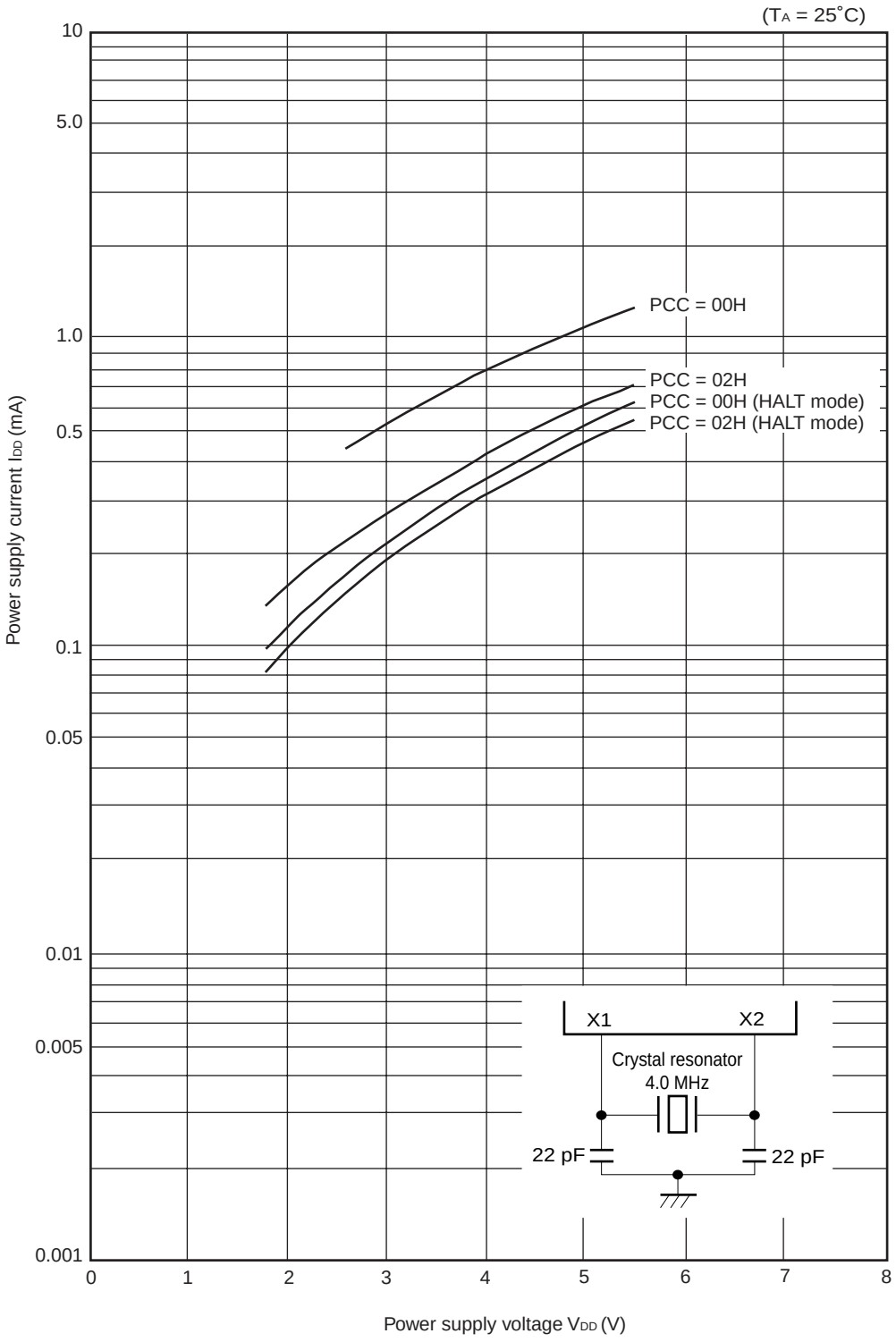
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



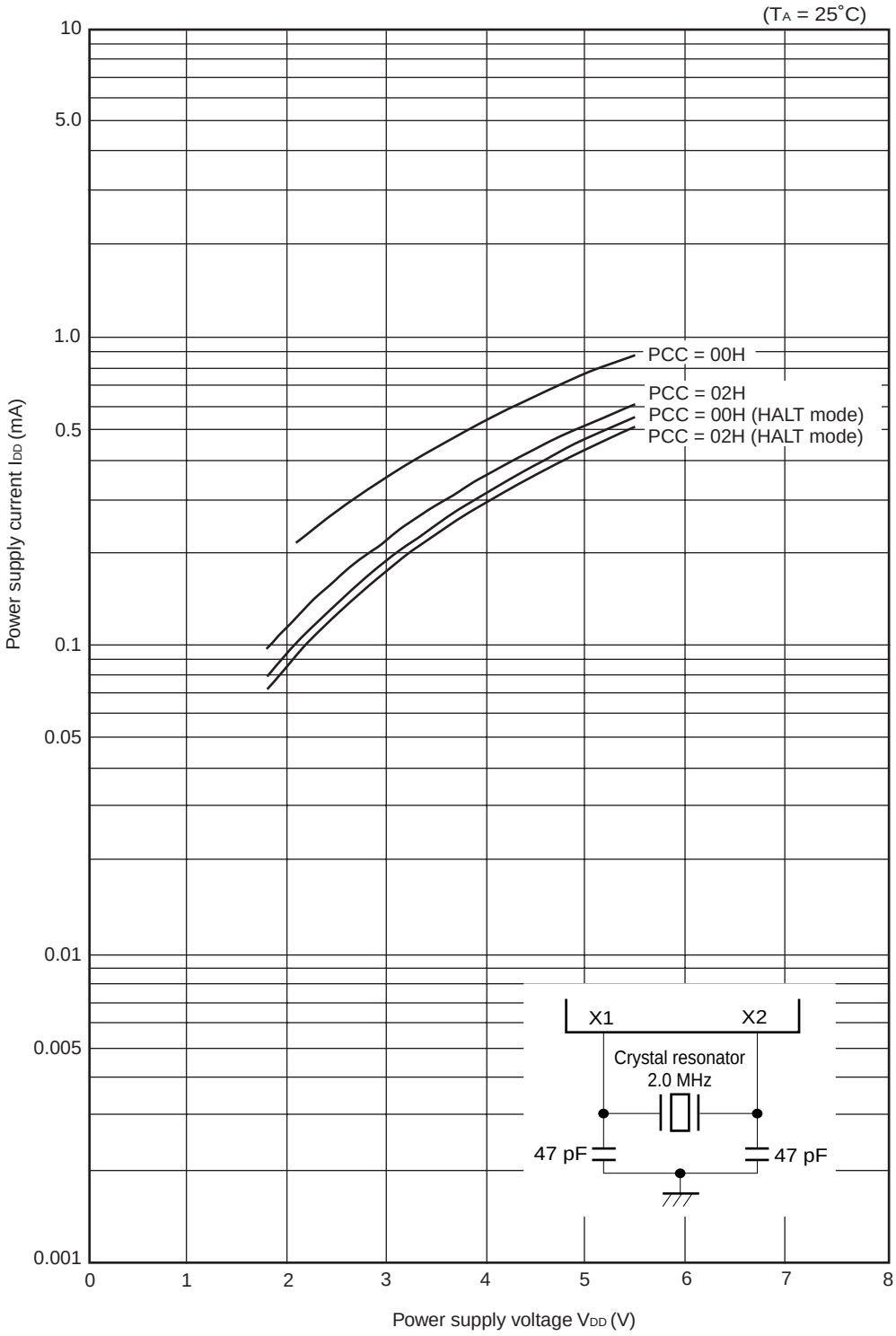
I_{DD} vs V_{DD} (System clock: 5.0 MHz crystal resonator)



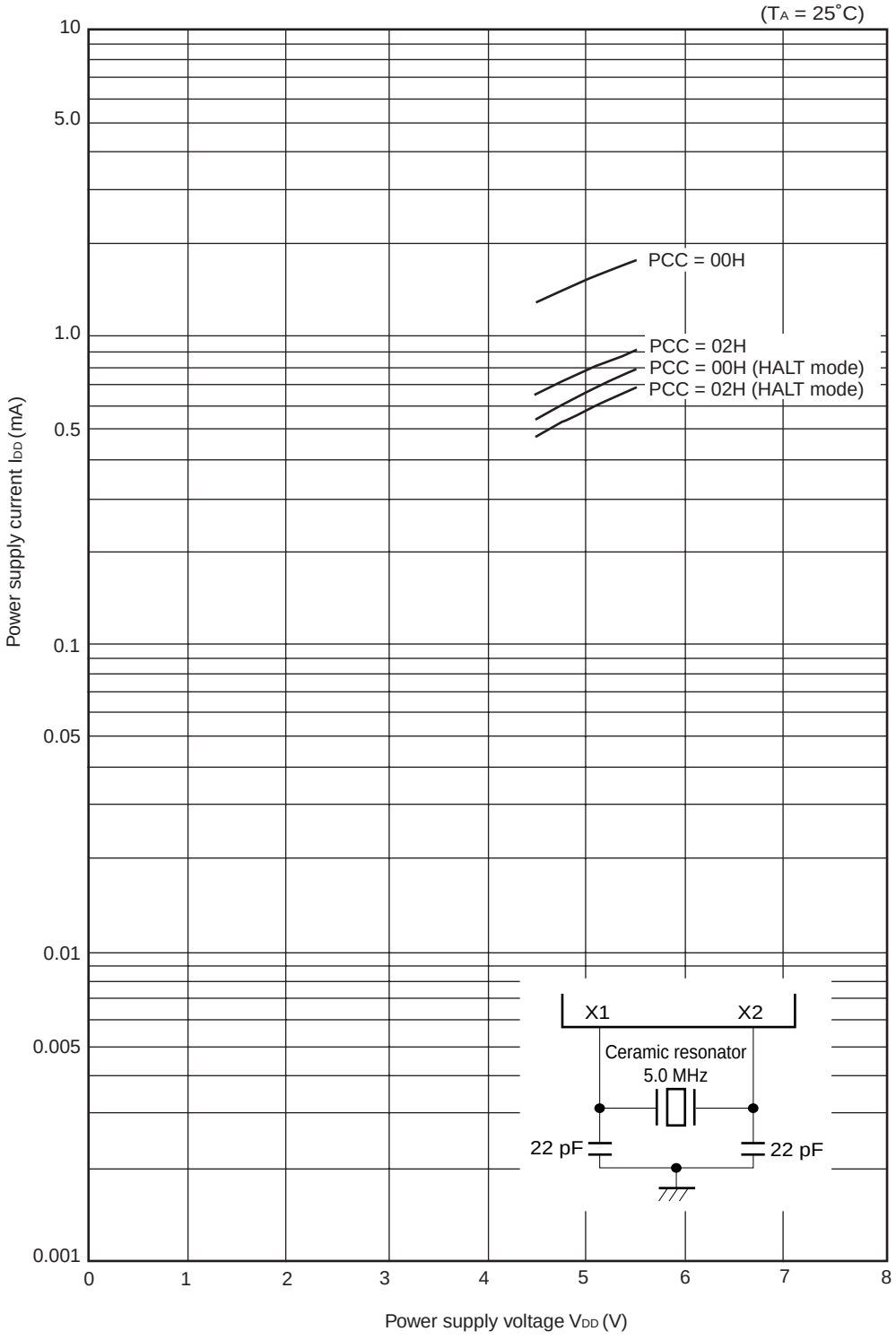
I_{DD} vs V_{DD} (System clock: 4.0 MHz crystal resonator)



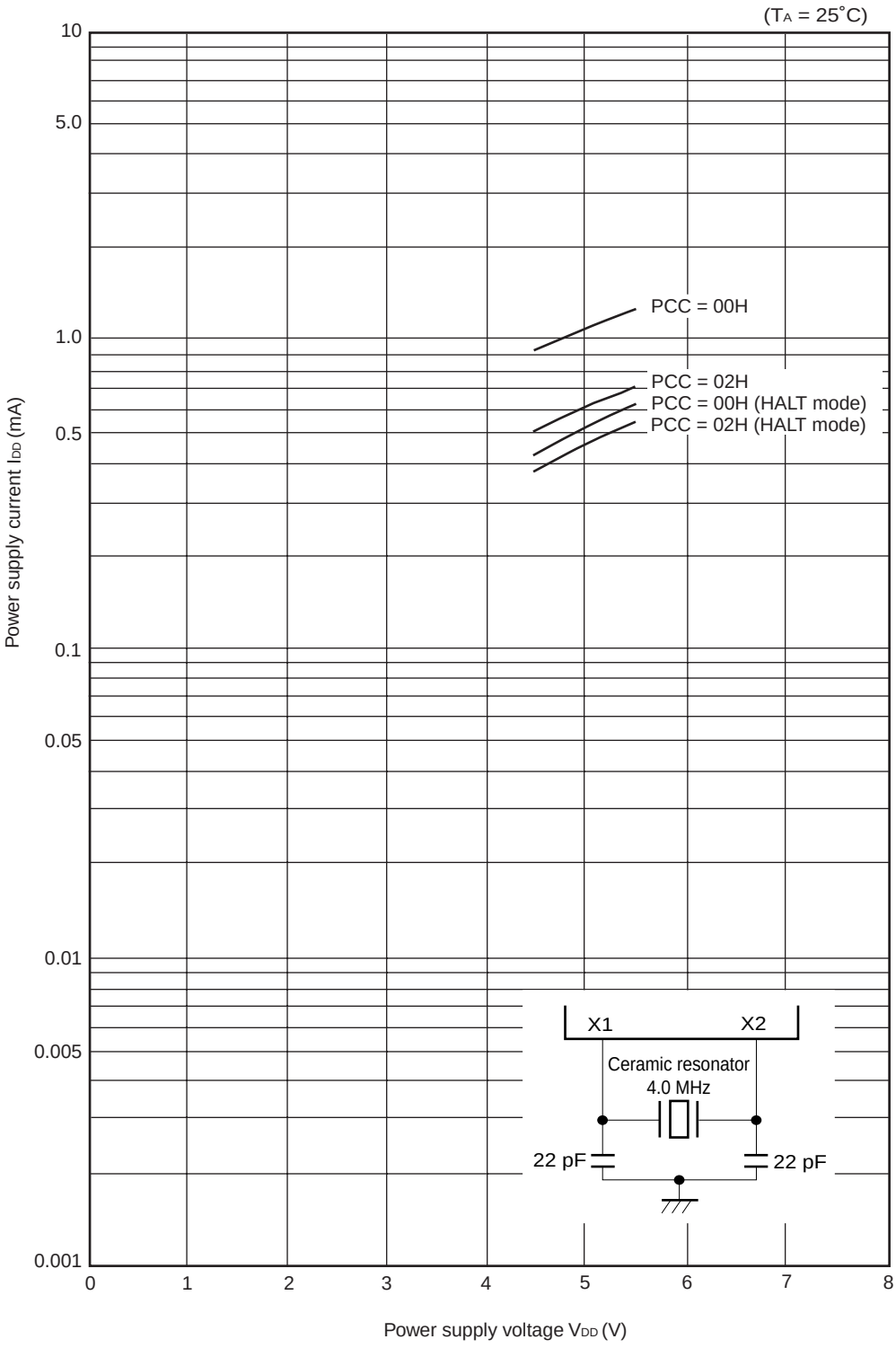
I_{DD} vs V_{DD} (System clock: 2.0 MHz crystal resonator)



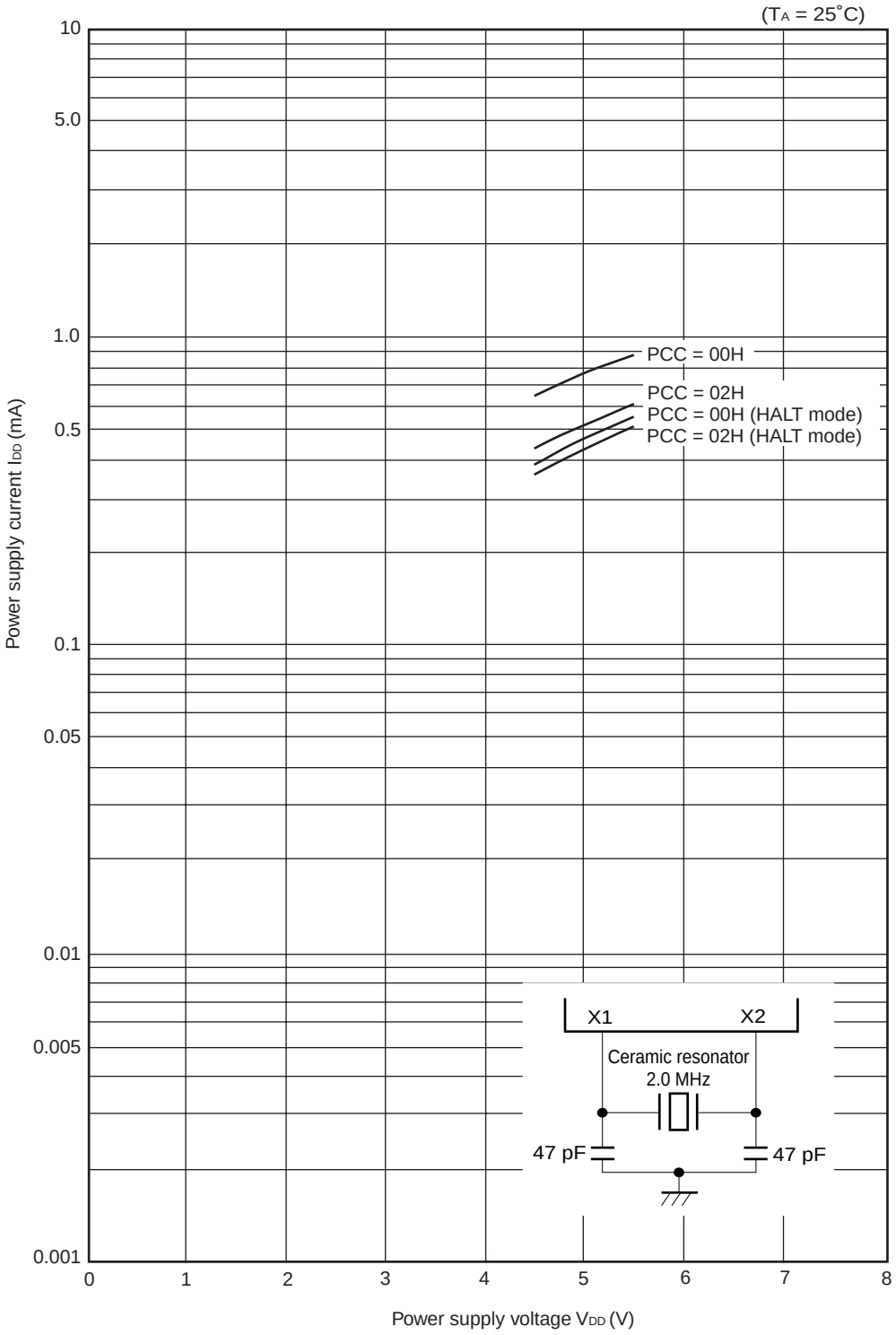
I_{DD} vs V_{DD} (System clock: 5.0 MHz ceramic resonator)



I_{DD} vs V_{DD} (System clock: 4.0 MHz ceramic resonator)



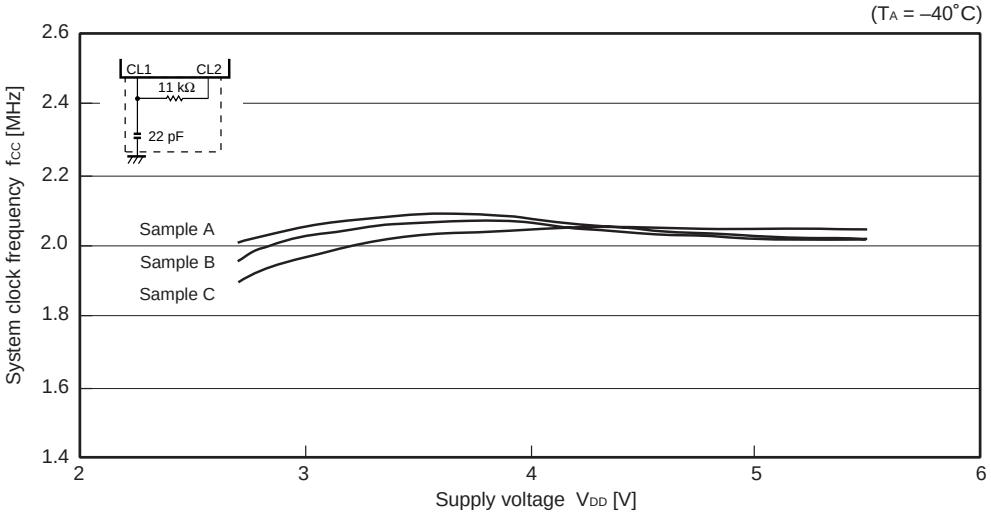
I_{DD} vs V_{DD} (System clock: 2.0 MHz ceramic resonator)



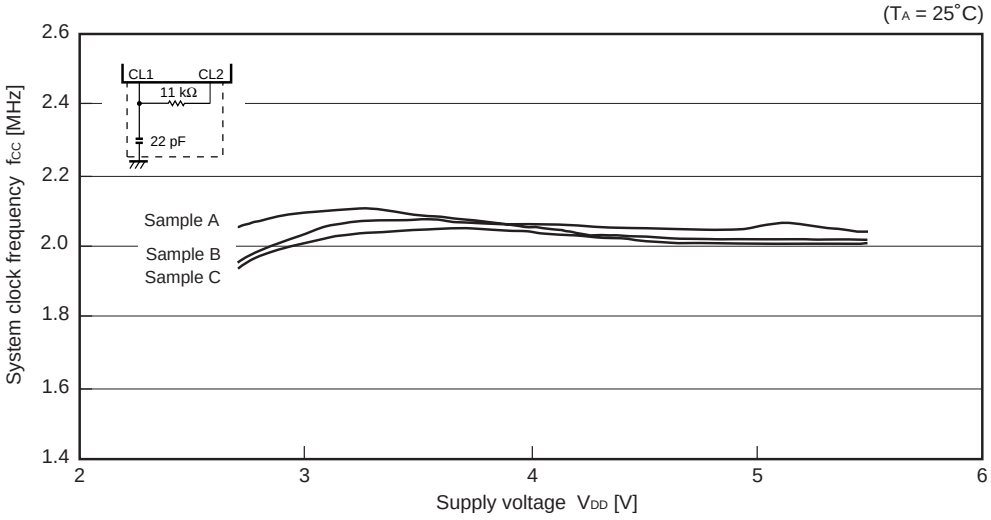
★ **CHAPTER 34 EXAMPLE OF RC OSCILLATOR FREQUENCY CHARACTERISTICS (REFERENCE VALUES) (μPD78912xA, 78913xA, 78912xA(A), 78913xA(A), 78F9136A)**

f_{CC} vs V_{DD} (RC oscillation, R = 11 kΩ, C= 22 pF)

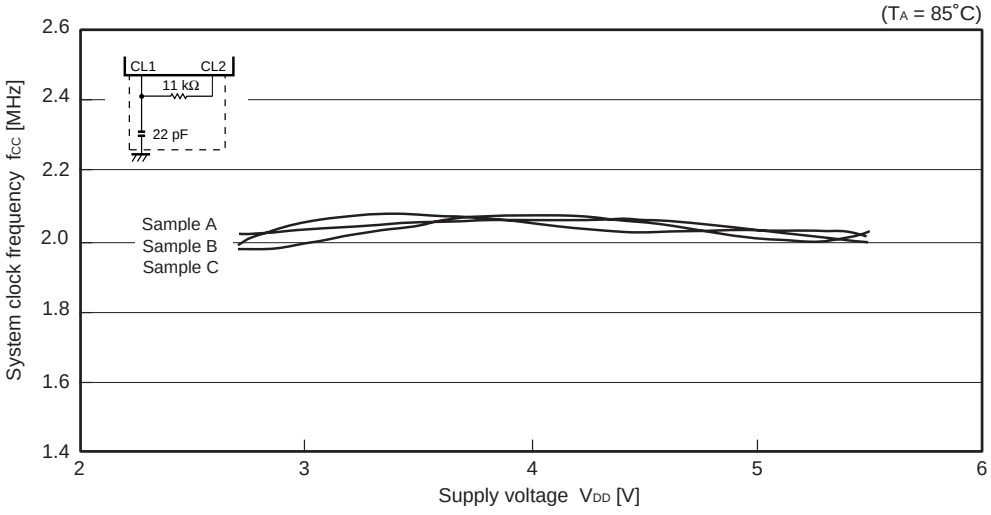
(T_A = –40°C)



(T_A = 25°C)

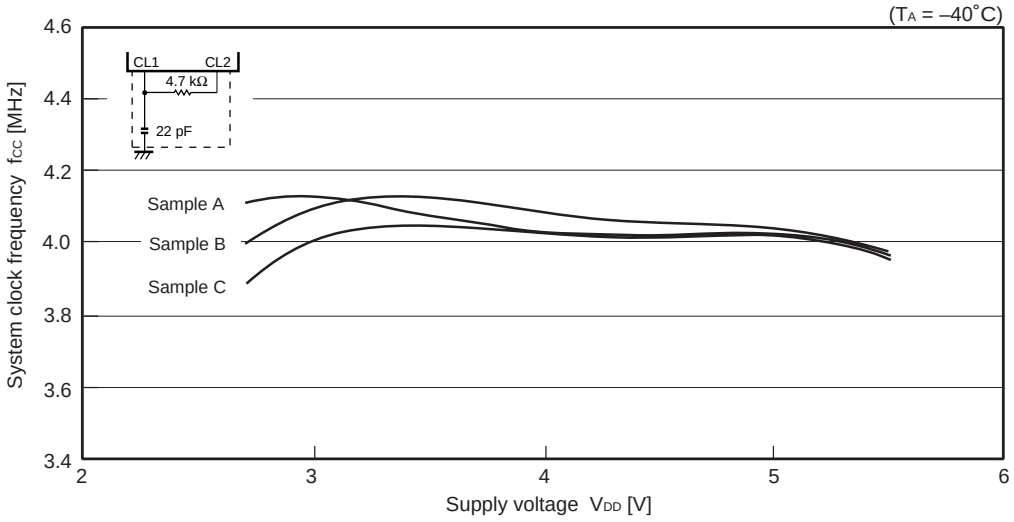


(T_A = 85°C)

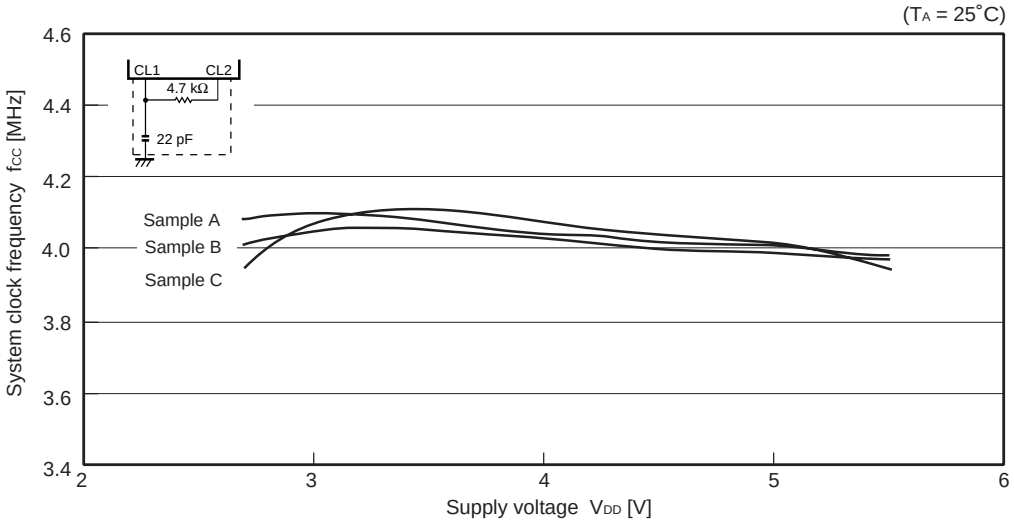


f_{CC} vs V_{DD} (RC oscillation, R = 4.7 kΩ, C= 22 pF)

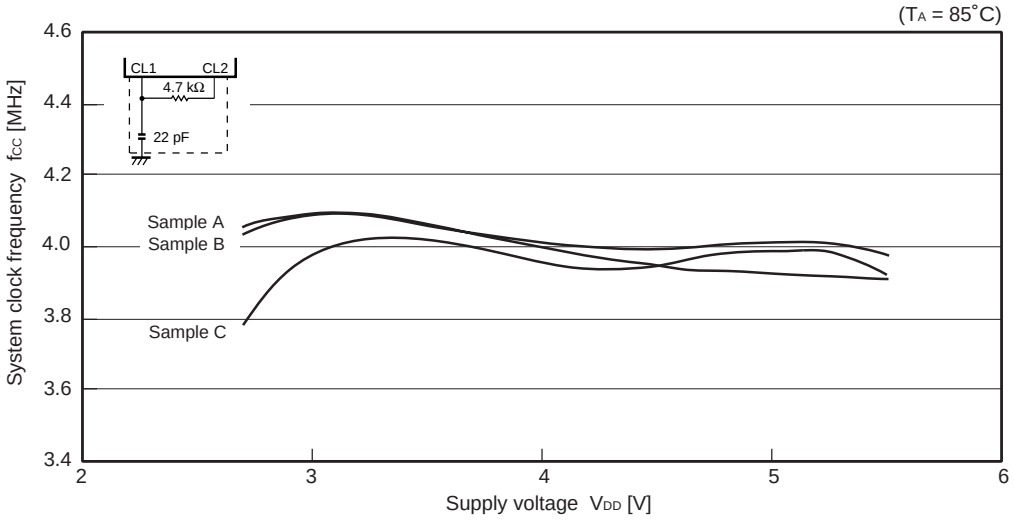
(T_A = –40˚C)



(T_A = 25˚C)



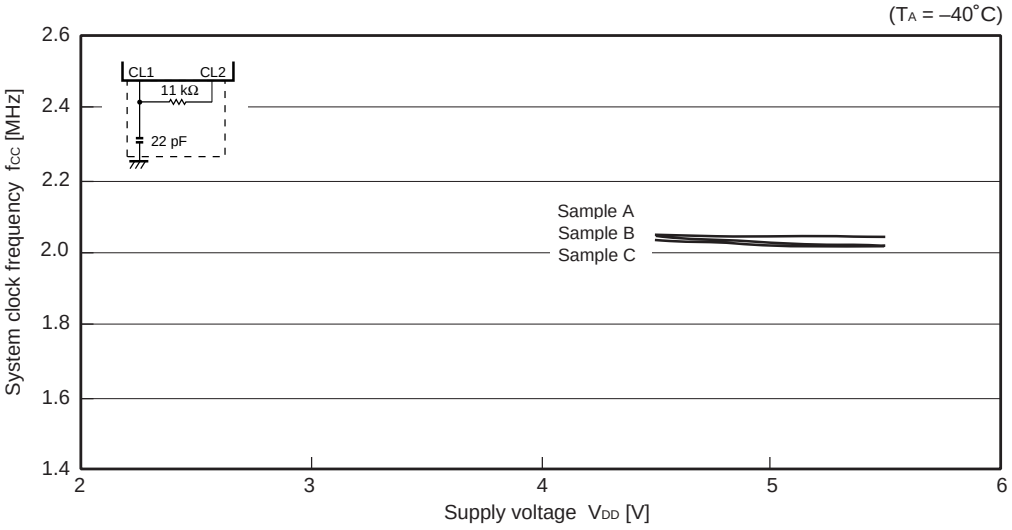
(T_A = 85˚C)



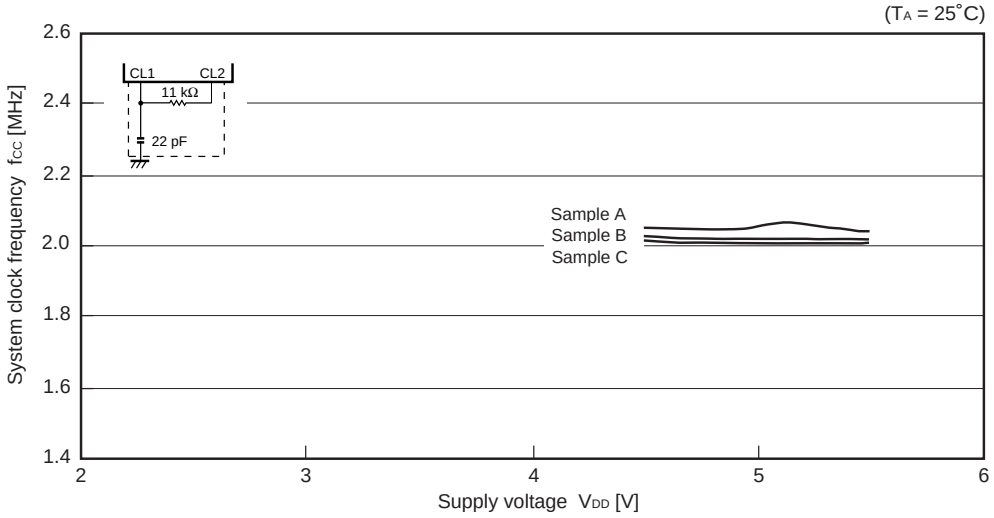
★ **CHAPTER 35 EXAMPLE OF RC OSCILLATOR FREQUENCY CHARACTERISTICS (REFERENCE VALUES) (μPD78912xA(A1), 78913xA(A1), 78912xA(A2), 78913xA(A2))**

f_{CC} vs V_{DD} (RC oscillation, R = 11 kΩ, C= 22 pF)

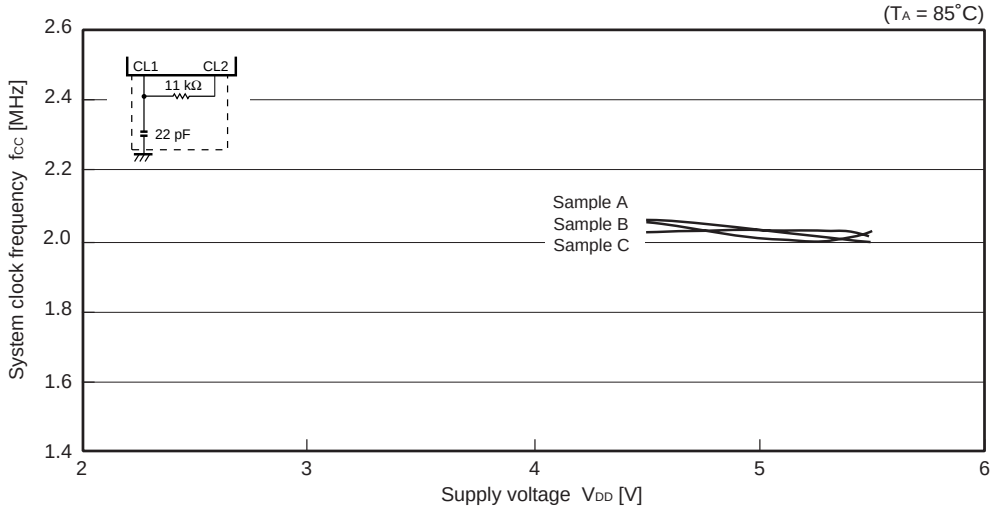
(T_A = –40°C)



(T_A = 25°C)

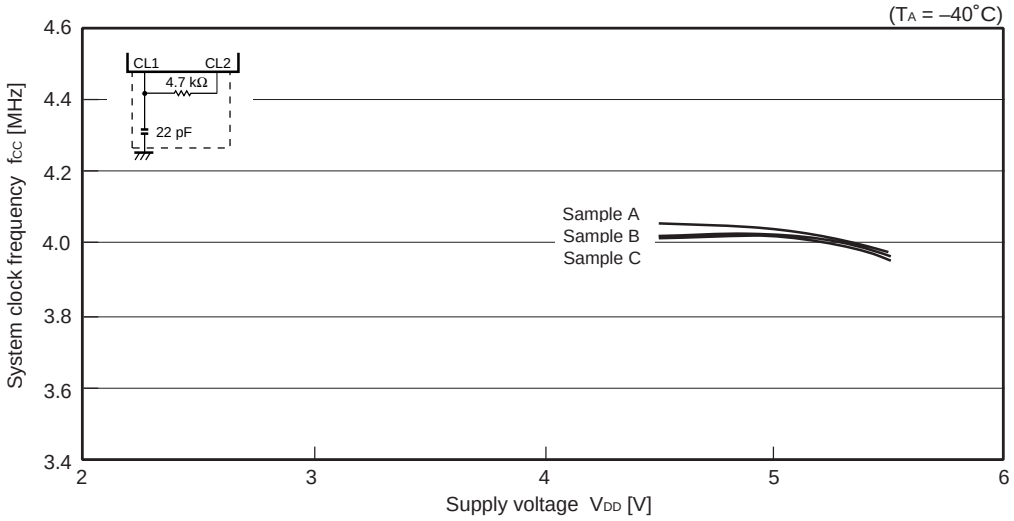


(T_A = 85°C)

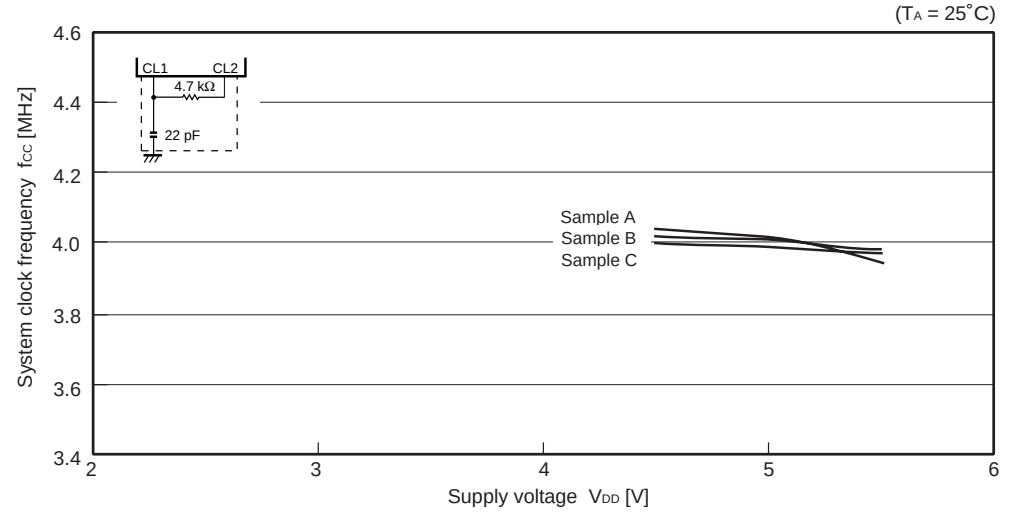


f_{CC} vs V_{DD} (RC oscillation, R = 4.7 kΩ, C= 22 pF)

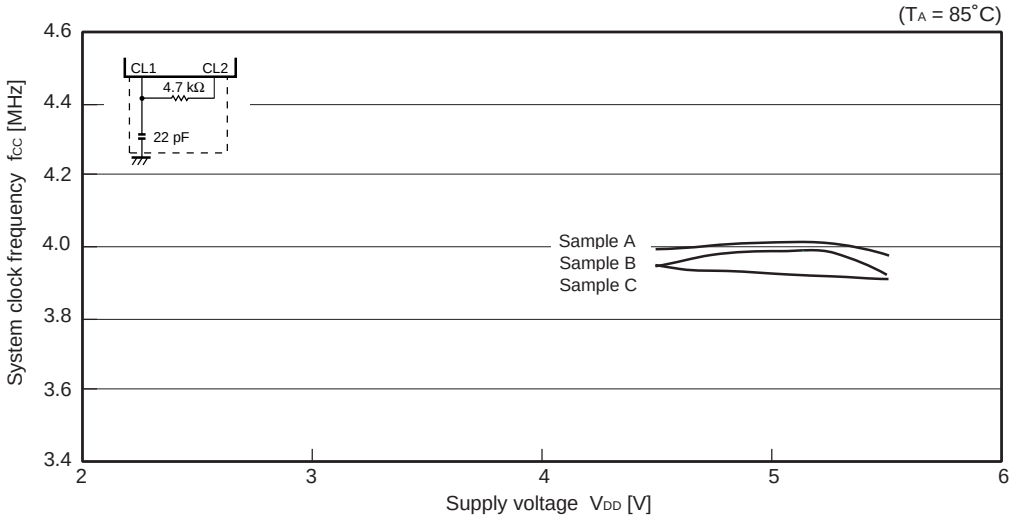
(T_A = –40˚C)



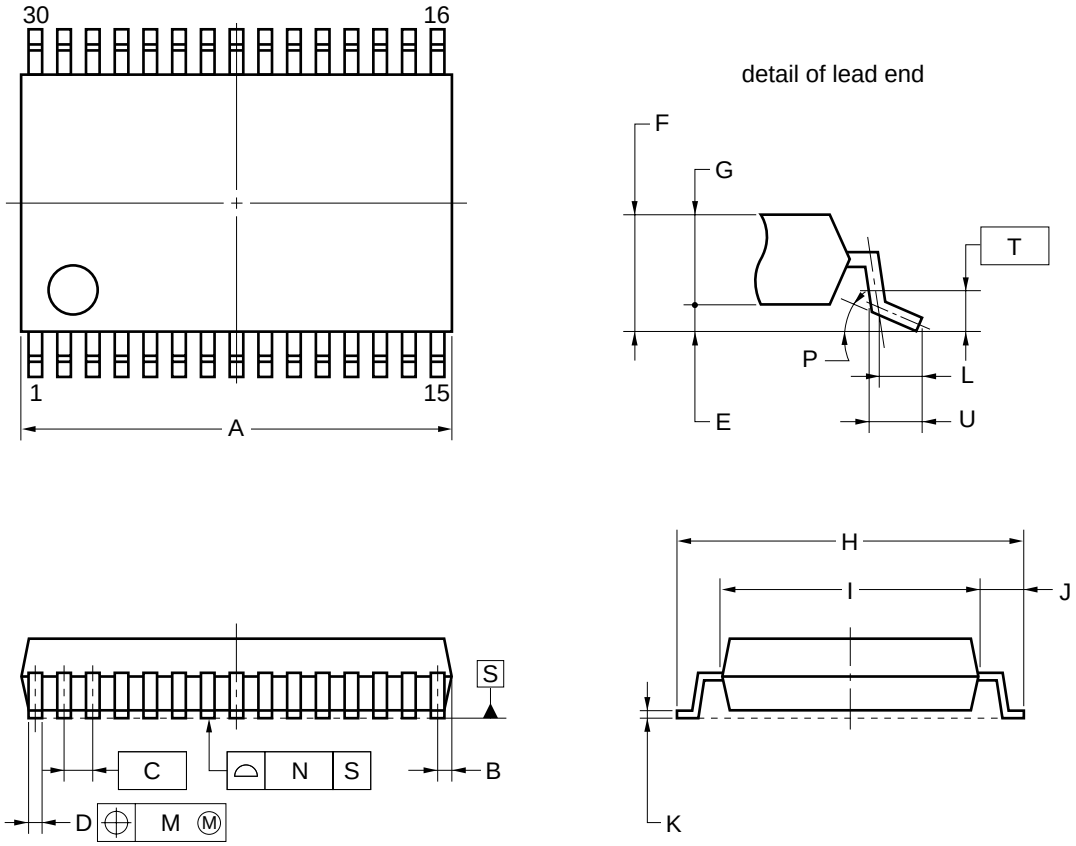
(T_A = 25˚C)



(T_A = 85˚C)



30-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

★ CHAPTER 37 RECOMMENDED SOLDERING CONDITIONS

The μPD789104A, 789114A, 789124A, and 789134A Subseries should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 37-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD789101AMC-×××-5A4, μPD789102AMC-×××-5A4, μPD789104AMC-×××-5A4
μPD789111AMC-×××-5A4, μPD789112AMC-×××-5A4, μPD789114AMC-×××-5A4
μPD789121AMC-×××-5A4, μPD789122AMC-×××-5A4, μPD789124AMC-×××-5A4
μPD789131AMC-×××-5A4, μPD789132AMC-×××-5A4, μPD789134AMC-×××-5A4
μPD789101AMC(A)-×××-5A4, μPD789102AMC(A)-×××-5A4, μPD789104AMC(A)-×××-5A4
μPD789111AMC(A)-×××-5A4, μPD789112AMC(A)-×××-5A4, μPD789114AMC(A)-×××-5A4
μPD789121AMC(A)-×××-5A4, μPD789122AMC(A)-×××-5A4, μPD789124AMC(A)-×××-5A4
μPD789131AMC(A)-×××-5A4, μPD789132AMC(A)-×××-5A4, μPD789134AMC(A)-×××-5A4
μPD789101AMC(A1)-×××-5A4, μPD789102AMC(A1)-×××-5A4, μPD789104AMC(A1)-×××-5A4
μPD789111AMC(A1)-×××-5A4, μPD789112AMC(A1)-×××-5A4, μPD789114AMC(A1)-×××-5A4
μPD789121AMC(A1)-×××-5A4, μPD789122AMC(A1)-×××-5A4, μPD789124AMC(A1)-×××-5A4
μPD789131AMC(A1)-×××-5A4, μPD789132AMC(A1)-×××-5A4, μPD789134AMC(A1)-×××-5A4
μPD789101AMC(A2)-×××-5A4, μPD789102AMC(A2)-×××-5A4, μPD789104AMC(A2)-×××-5A4
μPD789111AMC(A2)-×××-5A4, μPD789112AMC(A2)-×××-5A4, μPD789114AMC(A2)-×××-5A4
μPD789121AMC(A2)-×××-5A4, μPD789122AMC(A2)-×××-5A4, μPD789124AMC(A2)-×××-5A4
μPD789131AMC(A2)-×××-5A4, μPD789132AMC(A2)-×××-5A4, μPD789134AMC(A2)-×××-5A4

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 37-1. Surface Mounting Type Soldering Conditions (2/2)

(2) μPD78F9116BMC-5A4, μPD78F9136BMC-5A4,
μPD78F9116BMC(A)-5A4, μPD78F9136BMC(A)-5A4,
μPD78F9116BMC(A1)-5A4, μPD78F9136BMC(A1)-5A4

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(3) μPD78F9116AMC-5A4, μPD78F9136AMC-5A4

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C max.(package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

★ APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μPD789104A/114A/124A/134A Subseries.

Figure A-1 shows the development tool configuration.

- **Support of the PC98-NX Series**

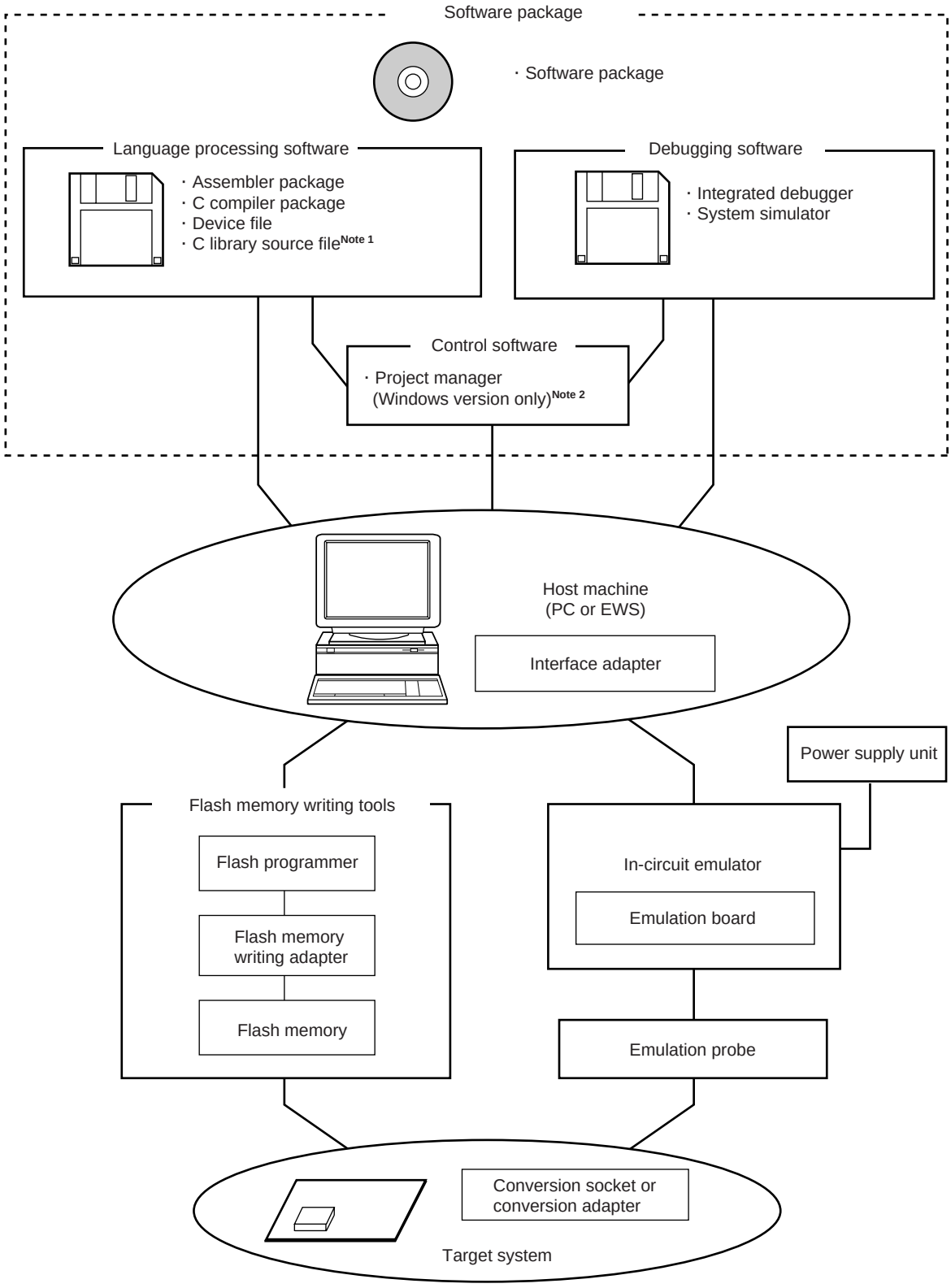
  Unless otherwise specified, the μPD789104A/114A/124A/134A Subseries supported by IBM PC/AT™ and compatibles can be used for the PC98-NX Series. When using the PC98-NX Series, refer to the descriptions of IBM PC/AT and compatibles.

- **Windows**

  Unless otherwise specified, “Windows” indicates the following OSs.

  - Windows 3.1
  - Windows 95
  - Windows 98
  - Windows 2000
  - Windows NT™ Ver. 4.0

Figure A-1. Development Tools



Notes 1. The C library source file is not included in the software package.

2. The project manager is included in the assembler package and is available only for Windows.

A.1 Software Package

SP78K0S Software package	Various software tools for 78K/0S development are integrated in one package. The following tools are included. RA78K0S, CC78K0S, ID78K0S-NS, SM78K0S, various device files
	Part number: μS××××SP78K0S

Remark ×××× in the part number differs depending on the operating system to be used.

μS×××× SP78K0S

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	CD-ROM
BB17		English Windows	

A.2 Language Processing Software

RA78K0S Assembler package	Program that converts program written in mnemonic into object codes that can be executed by a microcontroller. In addition, automatic functions to generate a symbol table and optimize branch instructions are also provided. Used in combination with a device file (DF789136) (sold separately). **<Caution when used in PC environment>** The assembler package is a DOS-based application but may be used in the Windows environment by using the Project Manager of Windows (included in the package).
	Part number: μS××××RA78K0S
CC78K0S C compiler package	Program that converts program written in C language into object codes that can be executed by a microcontroller. Used in combination with an assembler package (RA78K0S) and device file (DF789136) (both sold separately). **<Caution when used in PC environment>** The C compiler package is a DOS-based application but may be used in the Windows environment by using the Project Manager of Windows (included in the assembler package).
	Part number: μS××××CC78K0S
DF789136[Note 1] Device file	File containing the information inherent to the device. Used in combination with other tools (RA78K0S, CC78K0S, ID78K0S-NS, SM78K0S) (all sold separately).
	Part number: μS××××DF789136
CC78K0S-L[Note 2] C library source file	Source file of functions constituting the object library included in the C compiler package. Necessary for changing the object library included in the C compiler package according to the customer's specifications. Since this is the source file, its working environment does not depend on any particular operating system.
	Part number: μS××××CC78K0S-L

Notes 1. DF789136 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S.

2. CC78K0S-L is not included in the software package (SP78K0S).

Remark ××××in the part number differs depending on the host machine and operating system to be used.

μS××××RA78K0S
μS××××CC78K0S

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	
AB17		Japanese Windows	CD-ROM
BB17		English Windows	
3P17	HP9000 series 700™	HP-UX™ (Rel.10.10)	
3K17	SPARCstation™	SunOS™ (Rel.4.1.1), Solaris™ (Rel.2.5.1)	

μS××××DF789136
μS××××CC78K0S-L

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	
3P16	HP9000 series 700	HP-UX (Rel.10.10)	DAT
3K13	SPARCstation	SunOS (Rel.4.1.1), Solaris (Rel.2.5.1)	3.5” 2HD FD
3K15			1/4” CGMT

A.3 Control Software

Project Manager	Control software provided for efficient user program development in the Windows environment. The Project Manager allows a series of tasks required for user program development to be performed, including starting the editor, building, and starting the debugger. **<Caution>** The Project Manager is included in the assembler package (RA78K0S). It cannot be used in an environment other than Windows.

A.4 Flash Memory Writing Tools

Flashpro III (part number: FL-PR3, PG-FP3) Flashpro IV (part number: FL-PR4, PG-FP4) Flash programmer	Flash programmer dedicated to microcontrollers incorporating flash memory.
FA-30MC Flash memory writing adapter	Flash memory writing adapter. Used connected to Flashpro III. 30-pin plastic SSOP (MC-5A4 type)

Remark FL-PR3, FL-PR4, and FA-30MC are products of Naito Densei Machida Mfg. Co., Ltd.
For further information, contact: Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191)

A.5 Debugging Tools (Hardware)

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging the hardware and software of an application system using the 78K/0S Series. Used with an integrated debugger (ID78K0S-NS). Used in combination with an AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-78K0S-NS-A In-circuit emulator	In-circuit emulator with enhanced functions of the IE-78K0S-NS. The debug function is further enhanced by adding a coverage function and enhancing the tracer and timer functions.
IE-70000-MC-PS-B AC adapter	Adapter for supplying power from a 100 to 240 VAC outlet.
IE-70000-98-IF-C Interface adapter	Adapter required when using a PC-9800 series (except notebook type) as the host machine (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable required when using a notebook type PC as the host machine (PCMICA socket supported).
IE-70000-PC-IF-C Interface adapter	Adapter required when using an IBM PC/AT or compatible as the host machine (ISA bus supported).
IE-70000-PCI-IF-A Interface adapter	Adapter required when using a personal computer incorporating a PCI bus as the host machine.
IE-789136-NS-EM1 Emulation board	Emulation board for emulating the peripheral hardware inherent to the device. Used in combination with an in-circuit emulator.
NP-30MC Emulation probe	Probe for connecting the in-circuit emulator and target system. Used in combination with the NSPACK30BK and YSPACK30BK.
NSPACK30BK YSPACK30BK Conversion adapter	Conversion adapter used to connect a target system board designed to allow mounting a 30-pin plastic SSOP (MC-5A4 type) and the NP-30MC.

Remarks 1. The NP-30MC is a product of Naito Densei Machida Mfg. Co., Ltd.
For further information, contact: Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191)

2. The NSPACK30BK and YSPACK30BK are products of TOKYO ELETECH CORPORATION.
For further information, contact: Daimaru Kogyo, Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)

A.6 Debugging Tools (Software)

ID78K0S-NS Integrated debugger	This debugger supports the in-circuit emulators IE-78K0S-NS and IE-78K0S-NS-A for the 78K/0S Series. The ID78K0S-NS is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. Used in combination with a device file (DF789136) (sold separately).
	Part number: μS××××ID78K0S-NS
SM78K0S System simulator	This is a system simulator for the 78K/0S Series. The SM78K0S is Windows-based software. It can be used to debug the target system at C source level or assembler level while simulating the operation of the target system on the host machine. Using SM78K0S, the logic and performance of the application can be verified independently of hardware development. Therefore, the development efficiency can be enhanced and the software quality can be improved. Used in combination with a device file (DF789136) (sold separately).
	Part number: μS××××SM78K0S
DF789136[Note] Device file	File containing the information inherent to the device. Used in combination with other tools (RA78K0S, CC78K0S, ID78K0S-NS, SM78K0S) (all sold separately).
	Part number: μS××××DF789136

Note DF789136 is a common file that can be used with the RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S.

Remark ×××× in the part number differs depending on the operating system to be used and the supply medium.

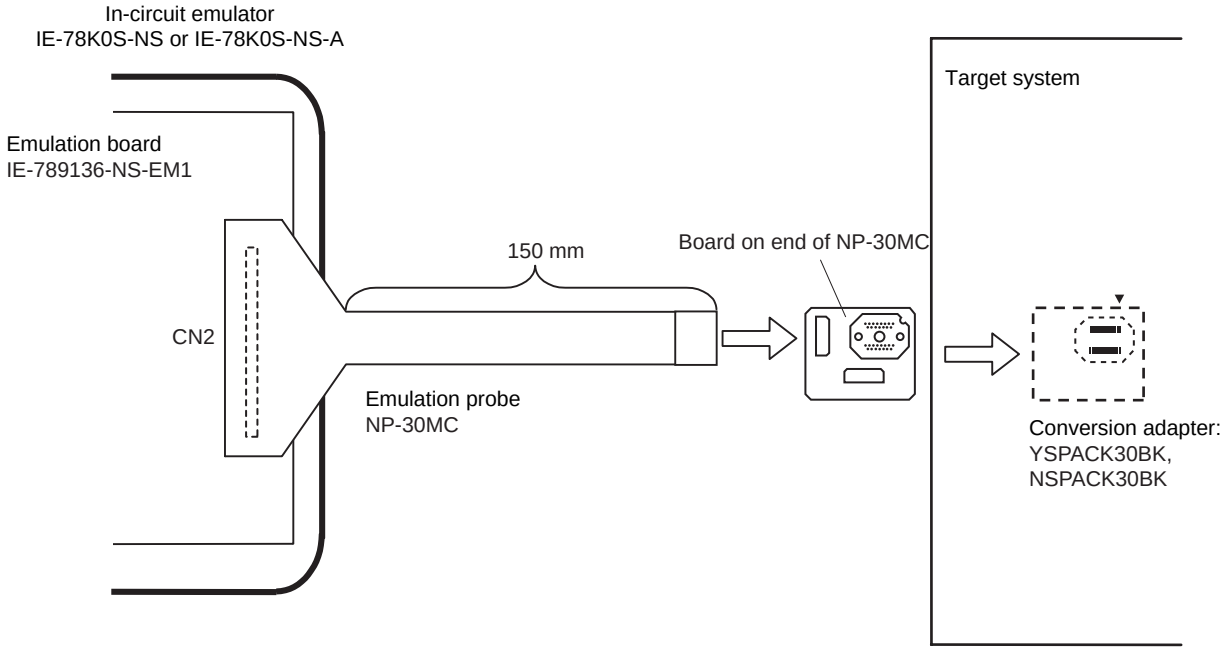
μS××××ID78K0S-NS
μS××××SM78K0S

××××	Host Machine	OS	Supply Medium
AB13	PC-9800 series, IBM PC/AT and compatibles	Japanese Windows	3.5” 2HD FD
BB13		English Windows	
AB17		Japanese Windows	CD-ROM
BB17		English Windows	

★ APPENDIX B NOTES ON TARGET SYSTEM DESIGN

The following show the conditions when connecting the emulation probe to the conversion adapter. Follow the configuration below and consider the shape of parts to be mounted on the target system when designing a system.

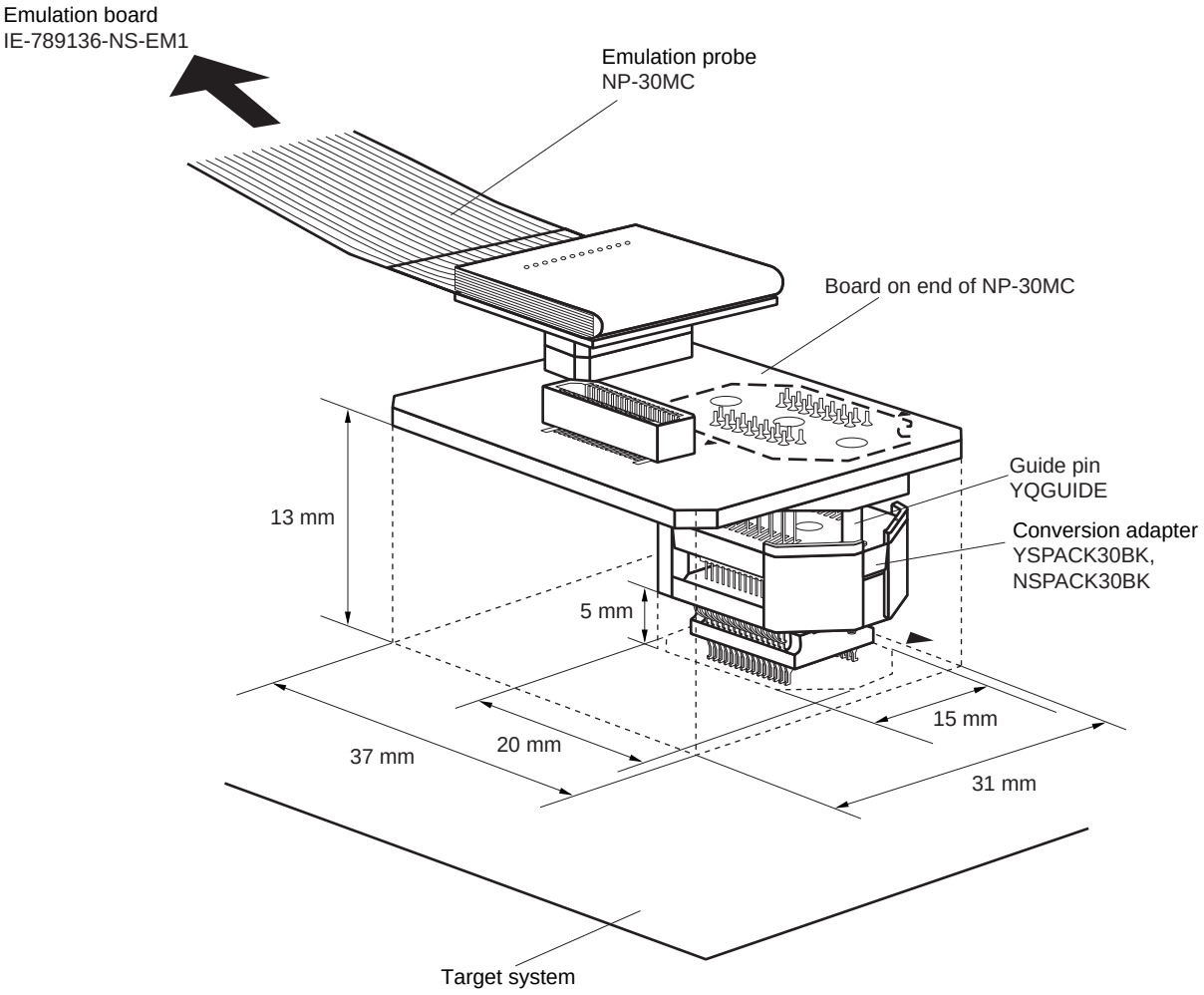
Figure B-1. Distance Between In-Circuit Emulator and Conversion Adapter



Remarks 1. The NP-30MC is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The YSPACK30BK and NSPACK30BK are products of TOKYO ELETECH CORPORATION.

Figure B-2. Connection Condition of Target System



Remarks 1. The NP-30MC is a product of Naito Densei Machida Mfg. Co., Ltd.

2. The YSPACK30BK, NSPACK30BK, and YQGUIDE are products of TOKYO ELETECH CORPORATION.

APPENDIX C REGISTER INDEX

C.1 Register Name Index (Alphabetical Order)

[A]

A/D conversion result register 0 (ADCR0) 143, 155
A/D converter mode register 0 (ADM0) 144, 156
Analog input channel specification register 0 (ADS0) 145, 157
Asynchronous serial interface mode register 20 (ASIM20) 172, 178, 181, 193
Asynchronous serial interface status register 20 (ASIS20) 174, 182

[B]

Baud rate generator control register 20 (BRGC20) 175, 183, 194

[E]

8-bit compare register 80 (CR80) 125
8-bit timer counter 80 (TM80) 125
8-bit timer mode control register 80 (TMC80) 126
External interrupt mode register 0 (INTM0) 212

[I]

Interrupt mask flag register 0 (MK0) 211
Interrupt mask flag register 1 (MK1) 211
Interrupt request flag register 0 (IF0) 210
Interrupt request flag register 1 (IF1) 210

[M]

Multiplication data register A0 (MRA0) 202
Multiplication data register B0 (MRB0) 202
Multiplier control register 0 (MULC0) 204

[O]

Oscillation stabilization time select register (OSTS) 222

[P]

Port 0 (P0) 82
Port 1 (P1) 83
Port 2 (P2) 84
Port 5 (P5) 88
Port 6 (P6) 89
Port mode register 0 (PM0) 90
Port mode register 1 (PM1) 90
Port mode register 2 (PM2) 90, 115, 127
Port mode register 5 (PM5) 90
Processor clock control register (PCC) 96, 103
Pull-up resistor option register 0 (PU0) 91
Pull-up resistor option register B2 (PUB2) 92

[R]

Receive buffer register 20 (RXB20) 169
Receive shift register 20 (RXS20) 169

[S]

Serial operating mode register 20 (CSIM20) 170, 178, 180, 192
16-bit capture register 20 (TCP20) 112
16-bit compare register 20 (CR20) 112
16-bit multiplication result storage register 0 (MUL0) 202
16-bit timer counter 20 (TM20) 112
16-bit timer mode control register 20 (TMC20) 113

[T]

Timer clock select register 2 (TCL2) 138
Transmit shift register 20 (TXS20) 169

[W]

Watchdog timer mode register (WDTM) 139

C.2 Register Symbol Index (Alphabetical Order)

[A]

ADCR0: A/D conversion result register 0 ....143, 155
ADM0: A/D converter mode register 0....144, 156
ADS0: Analog input channel specification register 0 ....145, 157
ASIM20: Asynchronous serial interface mode register 20....172, 178, 181, 193
ASIS20: Asynchronous serial interface status register 20....174, 182

[B]

BRGC20: Baud rate generator control register 20....175, 183, 194

[C]

CR20: 16-bit compare register 20 112
CR80: 8-bit compare register 80 125
CSIM20: Serial operating mode register 20 ....170, 178, 180, 192

[I]

IF0: Interrupt request flag register 0 210
IF1: Interrupt request flag register 1 210
INTM0: External interrupt mode register 0 212

[M]

MK0: Interrupt mask flag register 0....211
MK1: Interrupt mask flag register 1....211
MRA0: Multiplication data register A0 202
MRB0: Multiplication data register B0 202
MUL0: 16-bit multiplication result storage register 0 202
MULC0: Multiplier control register 0 204

[O]

OSTS: Oscillation stabilization time select register 222

[P]

P0: Port 0.... 82
P1: Port 1.... 83
P2: Port 2.... 84
P5: Port 5.... 88
P6: Port 6.... 89
PCC: Processor clock control register 96, 103
PM0: Port mode register 0.... 90
PM1: Port mode register 1.... 90
PM2: Port mode register 2....90, 115, 127
PM5: Port mode register 5.... 90
PU0: Pull-up resistor option register 0.... 91
PUB2: Pull-up resistor option register B2 92

[R]

RXB20: Receive buffer register 20 169
RXS20: Receive shift register 20 169

[T]

TCL2: Timer clock select register 2 138
TCP20: 16-bit capture register 20 112
TM20: 16-bit timer counter 20 112
TM80: 8-bit timer counter 80 125
TMC20: 16-bit timer mode control register 20 113
TMC80: 8-bit timer mode control register 80 126
TXS20: Transmit shift register 20 169

[W]

WDTM: Watchdog timer mode register 139

★ APPENDIX D REVISION HISTORY

The following table shows the revision history up to this edition. The “Applied to:” column indicates the chapters of each edition in which the revision was applied.

(1/2)

Edition	Major Revision from Previous Edition	Applied to:
2nd	• Addition of μPD789101A(A1), 789102A(A1), 789104A(A1), 789111A(A1), 789112A(A1), 789114A(A1), 789121A(A1), 789122A(A1), 789124A(A1), 789131A(A1), 789132A(A1), 789134A(A1), 789101A(A2), 789102A(A2), 789104A(A2), 789111A(A2), 789112A(A2), 789114A(A2), 789121A(A2), 789122A(A2), 789124A(A2), 789131A(A2), 789132A(A2), 789134A(A2), 78F9116B, 78F9136B, 78F9116B(A), 78F9136B(A), 78F9116B(A1), 78F9136B(A1) • Addition of description related to expanded-specification products	Throughout
	• Addition of **1.1 Expanded-Specification Products and Conventional-Specification Products** • Addition of **1.10 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**	**CHAPTER 1 GENERAL (μPD789104A, 789114A SUBSERIES)**
	Addition of **2.9 Differences Between Standard Quality Grade Products and (A), (A1), (A2) Products**	**CHAPTER 2 GENERAL (μPD789124A, 789134A SUBSERIES)**
	• Modification of description in **8.4.1 Operation as timer interrupt** • Modification of **Figure 8-5 Timing of Timer Interrupt Operation** • Modification of description in **8.4.2 Operation as timer output** • Modification of description in **Figure 8-7 Timer Output Timing** • Addition of **8.5 Notes on Using 16-Bit Timer 20**	**CHAPTER 8 16-BIT TIMER 20**
	Addition of description to **9.5 Notes on Using 8-Bit Timer/Event Counter 80**	**CHAPTER 9 8-BIT TIMER/EVENT COUNTER 80**
	Addition of **11.5 (8) Input impedance of ANI0 to ANI3 pins**	**CHAPTER 11 8-BIT A/D CONVERTER (μPD789104A, 789124A SUBSERIES)**
	• Modification of description in **12.2 (2) A/D conversion result register 0 (ADCR0)** • Addition of **12.5 (8) Input impedance of ANI0 to ANI3 pins**	**CHAPTER 12 10-BIT A/D CONVERTER (μPD789114A, 789134A SUBSERIES)**
	• Modification of **Figure 13-1 Block Diagram of Serial Interface 20** • Addition of **13.3 (4) (c) Generation of serial clock from system clock in 3-wire serial I/O mode** • Addition of **13.4.2 (2) (f) Reading receive data**	**CHAPTER 13 SERIAL INTERFACE 20**
	Addition of **Caution 3** in **Figure 15-2 Format of Interrupt Request Flag Register**	**CHAPTER 15 INTERRUPT FUNCTIONS**
	Revision of chapter	**CHAPTER 18 μPD78F9116A, 78F9116B, 78F9136A, 78F9136B**

(2/2)

Edition	Major Revision from Previous Edition	Applied to:
2nd	Addition of chapters	**CHAPTER 21** to **CHAPTER 31 ELECTRICAL SPECIFICATIONS**
		CHAPTER 32, **CHAPTER 33 CHARACTERISTICS CURVES (REFERENCE VALUES)**
		CHAPTER 34, **CHAPTER 35 EXAMPLE OF RC OSCILLATOR FREQUENCY CHARACTERISTICS (REFERENCE VALUES)**
		CHAPTER 36 PACKAGE DRAWING
		CHAPTER 37 RECOMMENDED SOLDERING CONDITIONS
	Revision of appendix	**APPENDIX A DEVELOPMENT TOOLS**
	Addition of appendices	**APPENDIX B NOTES ON TARGET SYSTEM DESIGN**
		APPENDIX D REVISION HISTORY
	Deletion of **APPENDIX B EMBEDDED SOFTWARE**	–