

BIPOLAR ANALOG INTEGRATED CIRCUITS

μ PC2746T, 2747T, 2748T

3V BIAS SILICON MMIC AMPLIFIERS FOR 900 MHz BAND MOBILE TELEPHONE

FEATURES

- Low voltage operation – Single supply voltage 3.0 V TYP. minimum operating voltage 1.8 V
- Wide Band Operation – μ PC2746T: $G_p = 19$ dB TYP., $f_u = 1.5$ GHz/ μ PC2747T: $G_p = 12$ dB TYP., $f_u = 1.8$ GHz
- Low Noise Figure – μ PC2747T: NF = 3.3 dB TYP./ μ PC2748T: NF = 2.8 dB TYP. @900 MHz
- Packaged in 6 pin mini mold suitable for high-density surface mounting.

DESCRIPTION

μ PC2746T to μ PC2748T are silicon monolithic integrated circuits designed as buffer amplifiers for 900 MHz band cellular and cordless telephone applications, etc. These high isolation amplifiers suit to local buffers. These ICs operate on 3 V TYP. (minimum operating voltage 1.8 V) and therefore are suitable for hand-held, battery-operated systems. Due to the line-up with various performance, this series can be selected correspondingly to user's system design.

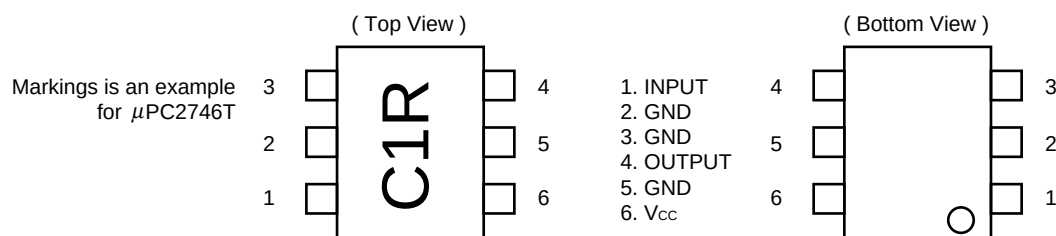
μ PC2746T to μ PC2748T are manufactured using NEC's 20 GHz fr NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold metalization wirings. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, these ICs have excellent performance, uniformity and reliability.

ORDER INFORMATION

PART NUMBER	PACKAGE	MARKING	SUPPLYING FORM	PRODUCT TYPE (TYP.)
μ PC2746T-E3	6 pin mini mold	C1R	Embossed tape 8 mm wide. QTY 3 K/Reel	19 dB gain/wideband
μ PC2747T-E3		C1S	Pin 1, 2, 3 face to perforation side of the tape.	12 dB gain/3.3 dB NF
μ PC2748T-E3		C1T		19 dB gain/2.8 dB NF

Remarks To order evaluation samples, please contact your local NEC office. (Order number: μ PC2746T, μ PC2747T, μ PC2748T)

PIN CONNECTIONS



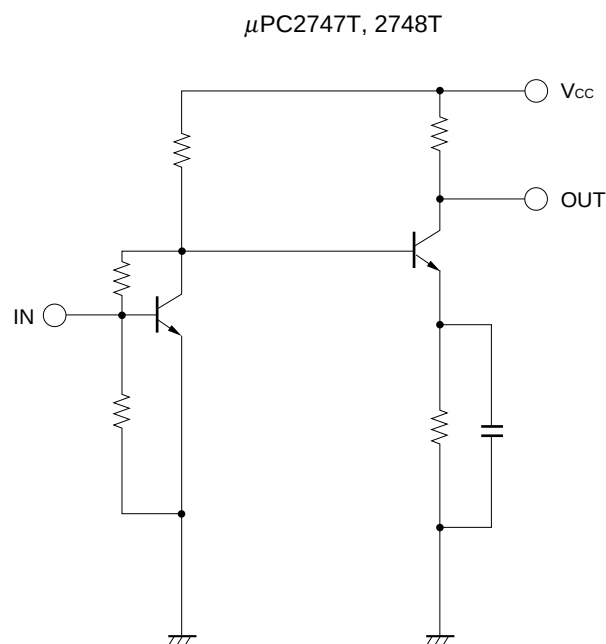
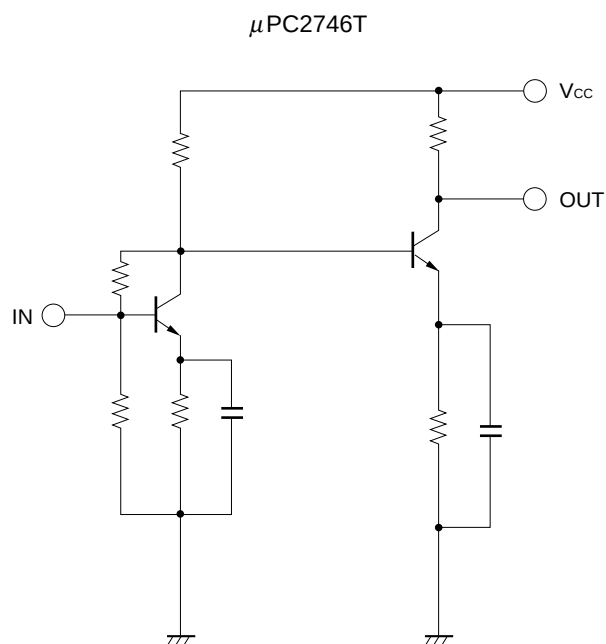
Caution: Electro-static sensitive devices

SELECTOR GUIDE ($T_A = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.0\text{ V}$, $Z_L = Z_S = 50\text{ }\Omega$)

Features	Device number	I_{CC} (mA)	G_P (dB)	NF (dB)	f_u (GHz)	$P_{O(sat)}$ (dBm)
19 dB gain/Wide band	μ PC2746T	7.5	19	4.0	1.5	0
12 dB gain/3.3 dB NF	μ PC2747T	5	12	3.3	1.8	-7
19 dB gain/2.8 dB NF	μ PC2748T	6	19	2.8	0.2-1.5	-3.5

* Typical Performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

EQUIVALENT CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V _{CC}	T _A = +25 °C	4.0	V
Total circuit current	I _{CC}	T _A = +25 °C	15*	mA
Total Power dissipation	P _D	Mounted on 50 × 50 × 1.6 mm epoxy glass PWB (T _A = +85 °C)	280	mW
Operating temperature	T _{opt}	ambient temperature	−40 to +85	°C
Storage temperature	T _{stg}	ambient temperature	−55 to +150	°C
Input power	P _{in}	T _A = +25 °C	0	dBm

* except μ PC2746T: 16 mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Operating temperature	T _{opt}	−40	+25	+85	°C

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = 3.0 V, Z_L = Z_S = 50 Ω)

PARAMETER	SYMBOL	μ PC2746T			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Circuit current	I _{CC}	5.0	7.5	10.0	mA	No input signal
Power Gain	G _P	16	19	21	dB	f = 500 MHz
Noise Figure	NF		4.0	5.5	dB	f = 500 MHz
Upper limit operating frequency	f _u	1.1	1.5		GHz	3 dB down below flat gain at 0.1 GHz
Isolation	ISL	40	45		dB	f = 500 MHz
Input return loss	RL _{in}	10	13		dB	f = 500 MHz
Output return loss	RL _{out}	5.5	8.5		dB	f = 500 MHz
Maximum output level	P _{O(sat)}	−3	0		dBm	f = 500 MHz, P _{in} = −6 dBm

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = 3.0 V, Z_L = Z_S = 50 Ω)

PARAMETER	SYMBOL	μ PC2747T			μ PC2748T			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Circuit current	I _{CC}	3.8	5	7	4.5	6	8	mA	No input signal
Power Gain	G _P	9	12	14	16	19	21	dB	f = 900 MHz
Noise Figure	NF		3.3	4.5		2.8	4.0	dB	f = 900 MHz
Lower limit operating frequency	f _L	—	—	—		0.2	0.4	GHz	3 dB down below flat gain at 0.9 GHz
Upper limit operating frequency	f _u	1.5	1.8		1.2	1.5		GHz	3 dB down below flat gain at 0.9 GHz
Isolation	ISL	35	40		35	40		dB	f = 900 MHz
Input return loss	RL _{in}	11	14		8.5	11.5		dB	f = 900 MHz
Output return loss	RL _{out}	7	10		5.5	8.5		dB	f = 900 MHz
Maximum output level	P _{O(sat)}	−9.5	−7		−6	−3.5		dBm	f = 900 MHz, P _{in} = −8 dBm

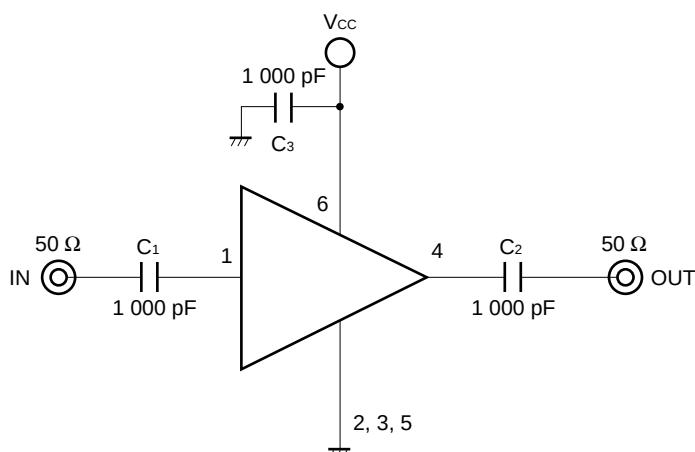
Standard characteristics for reference ($T_A = +25\text{ }^{\circ}\text{C}$, $Z_L = Z_S = 50\text{ }\Omega$)

FEATURES	SYMBOL	Reference value	Unit	TEST CONDITIONS
		μ PC2746T		
Circuit current	I_{CC}	4.5	mA	$V_{CC} = 1.8\text{ V}$, No input signal
Power Gain	G_P	18.5 14	dB	$V_{CC} = 3.0\text{ V}$, $f = 1\text{ GHz}$ $V_{CC} = 1.8\text{ V}$, $f = 500\text{ MHz}$
Noise Figure	NF	4.2 5.0	dB	$V_{CC} = 3.0\text{ V}$, $f = 1\text{ GHz}$ $V_{CC} = 1.8\text{ V}$, $f = 500\text{ MHz}$
Upper limit operating frequency	f_u	1.1	GHz	3 dB down below flat gain at 0.1 GHz, $V_{CC} = 1.8\text{ V}$
Isolation	ISL	38 37	dB	$V_{CC} = 3.0\text{ V}$, $f = 1\text{ GHz}$ $V_{CC} = 1.8\text{ V}$, $f = 500\text{ MHz}$
Input return loss	RL_{in}	10 10	dB	$V_{CC} = 3.0\text{ V}$, $f = 1\text{ GHz}$ $V_{CC} = 1.8\text{ V}$, $f = 500\text{ MHz}$
Output return loss	RL_{out}	8.5 9.5	dB	$V_{CC} = 3.0\text{ V}$, $f = 1\text{ GHz}$ $V_{CC} = 1.8\text{ V}$, $f = 500\text{ MHz}$
Maximum output level	$PO_{(sat)}$	-1 -8	dBm	$V_{CC} = 3.0\text{ V}$, $f = 1\text{ GHz}$, $P_{in} = -6\text{ dBm}$ $V_{CC} = 1.8\text{ V}$, $f = 500\text{ MHz}$, $P_{in} = -10\text{ dBm}$
3rd order intermodulation distortion	IM_3	51 37	dBc	$V_{CC} = 3.0\text{ V}$, $P_{out} = -20\text{ dBm}$, $f_1 = 500\text{ MHz}$, $f_2 = 502\text{ MHz}$ $V_{CC} = 1.8\text{ V}$, $P_{out} = -20\text{ dBm}$, $f_1 = 500\text{ MHz}$, $f_2 = 502\text{ MHz}$

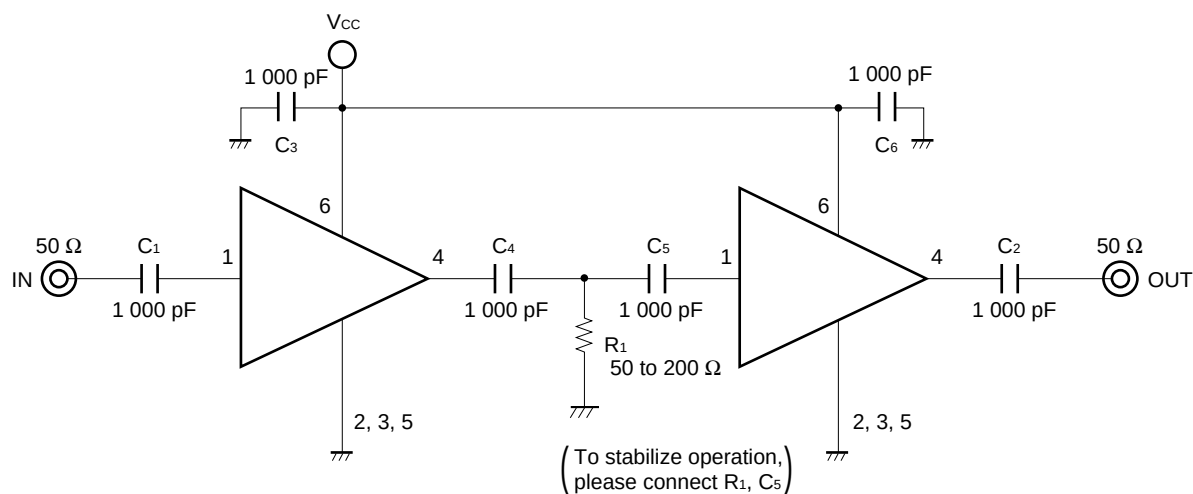
Standard characteristics for reference ($T_A = +25\text{ }^{\circ}\text{C}$, $Z_L = Z_S = 50\text{ }\Omega$)

FEATURES	SYMBOL	Reference value		Unit	TEST CONDITIONS
		μ PC2747T	μ PC2748T		
Circuit current	I_{CC}	3.0	3.5	mA	$V_{CC} = 1.8\text{ V}$, No input signal
Power Gain	G_P	5.5	11.5	dB	$V_{CC} = 1.8\text{ V}$, $f = 900\text{ MHz}$
Noise Figure	NF	5.2	4.5	dB	$V_{CC} = 1.8\text{ V}$, $f = 900\text{ MHz}$
Lower limit operating frequency	f_L	-	0.2	GHz	3 dB down below flat gain at 0.9 GHz, $V_{CC} = 1.8\text{ V}$
Upper limit operating frequency	f_u	1.8	1.5	GHz	3 dB down below flat gain at 0.9 GHz, $V_{CC} = 1.8\text{ V}$
Isolation	ISL	34	34	dB	$V_{CC} = 1.8\text{ V}$, $f = 900\text{ MHz}$
Input return loss	RL_{in}	11	10	dB	$V_{CC} = 1.8\text{ V}$, $f = 900\text{ MHz}$
Output return loss	RL_{out}	13	12	dB	$V_{CC} = 1.8\text{ V}$, $f = 900\text{ MHz}$
Maximum output level	$PO_{(sat)}$	-13.7	-10	dBm	$V_{CC} = 1.8\text{ V}$, $f = 900\text{ MHz}$, $P_{in} = -8\text{ dBm}$
3rd order intermodulation distortion	IM_3	34 20	38 28	dBc	$V_{CC} = 3.0\text{ V}$, $P_{out} = -20\text{ dBm}$, $f_1 = 900\text{ MHz}$, $f_2 = 902\text{ MHz}$ $V_{CC} = 1.8\text{ V}$, $P_{out} = -20\text{ dBm}$, $f_1 = 900\text{ MHz}$, $f_2 = 902\text{ MHz}$

TEST CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

Capacitors for Vcc, input and output pins

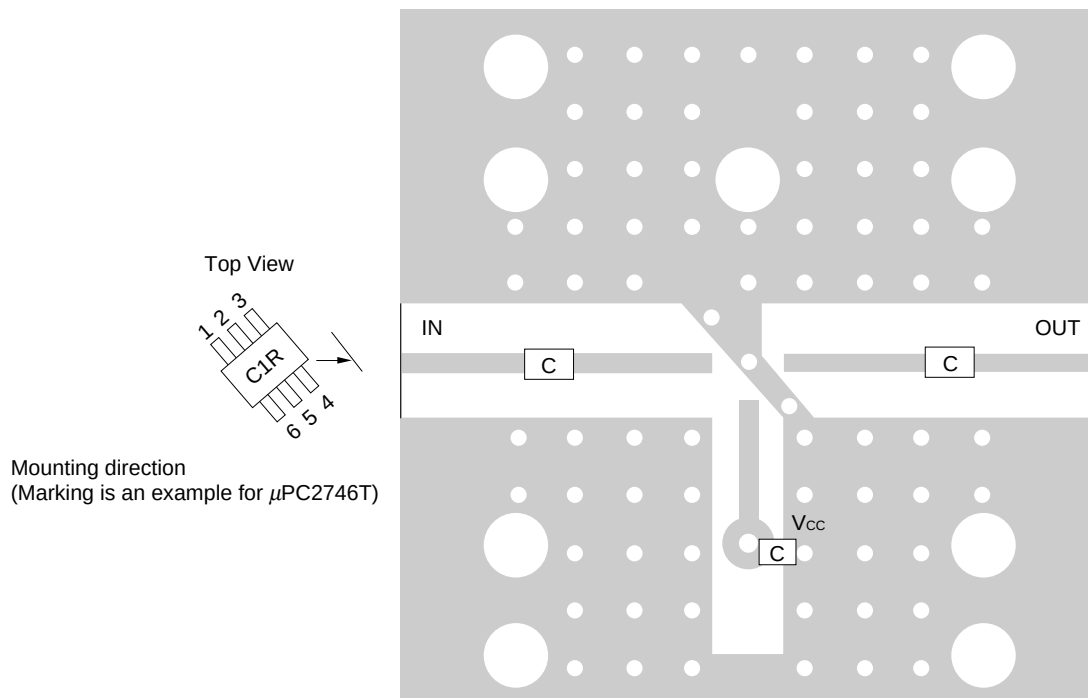
1000 pF capacitors are recommendable as bypass capacitor for Vcc pin and coupling capacitors for input/output pins.

Bypass capacitor for Vcc pin is intended to minimize Vcc pin's ground impedance. Therefore, stable bias can be supplied against Vcc fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

To get flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of $C=1/(2 \pi fZ_s)$.]

Illustration of the test circuit assembled on evaluation board



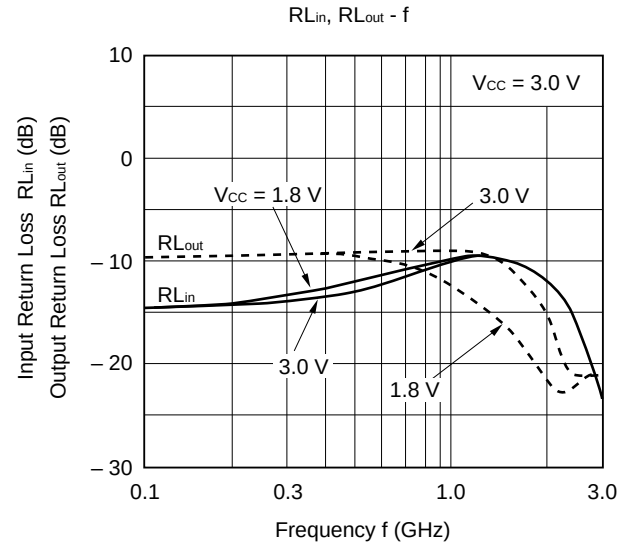
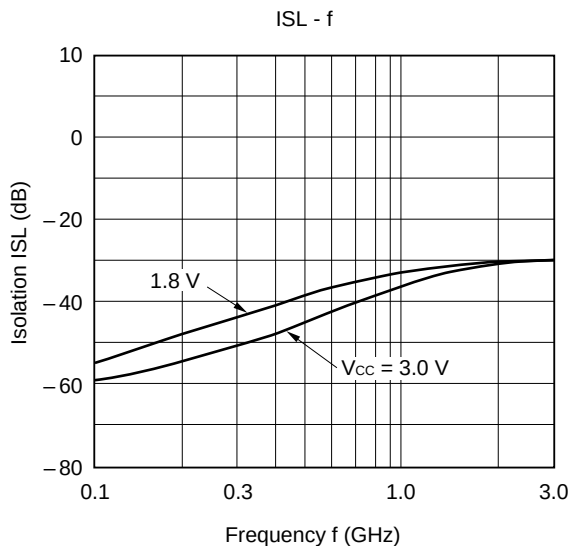
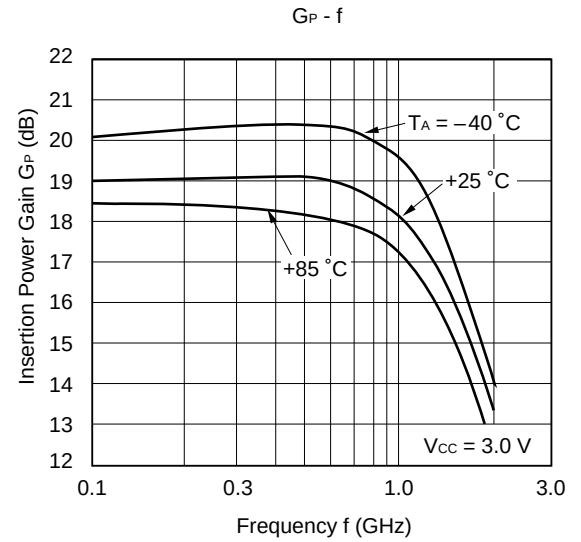
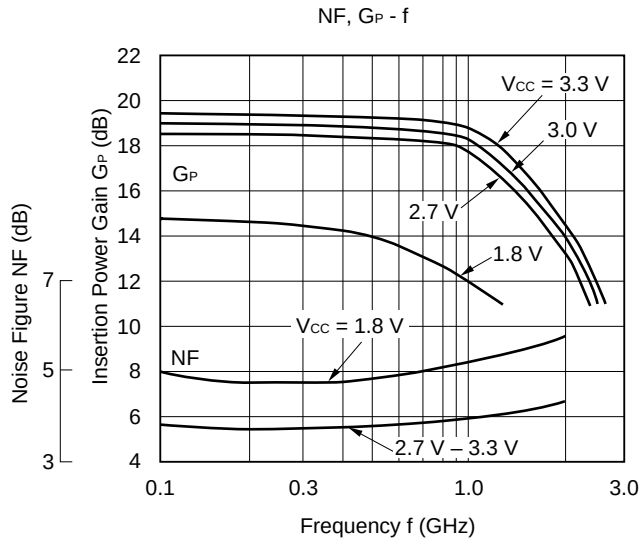
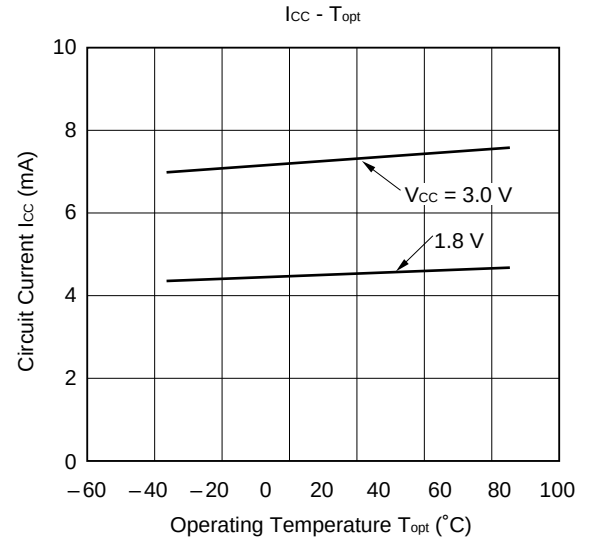
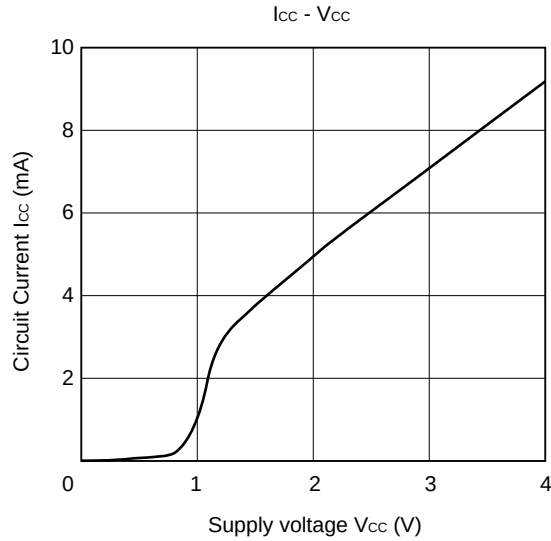
Component List

	Value
C	1 000 pF

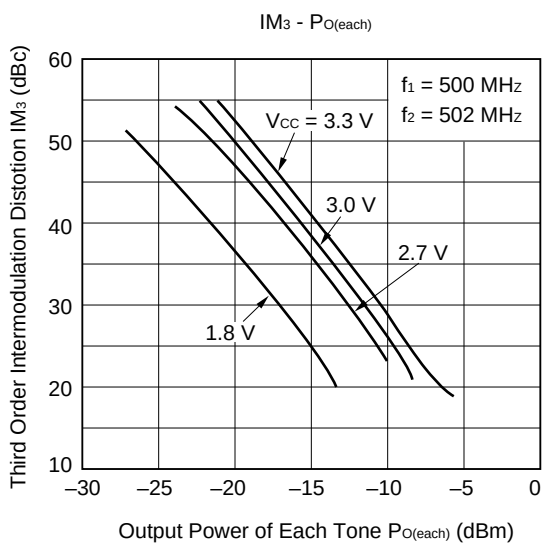
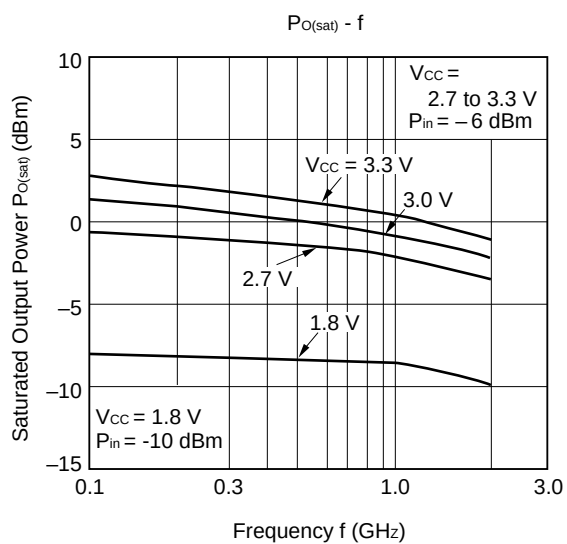
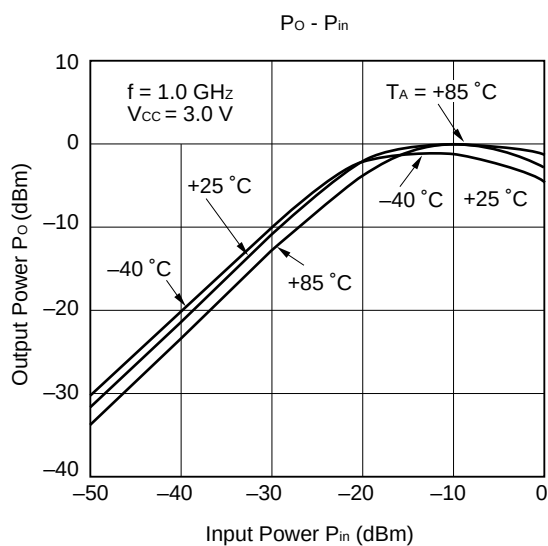
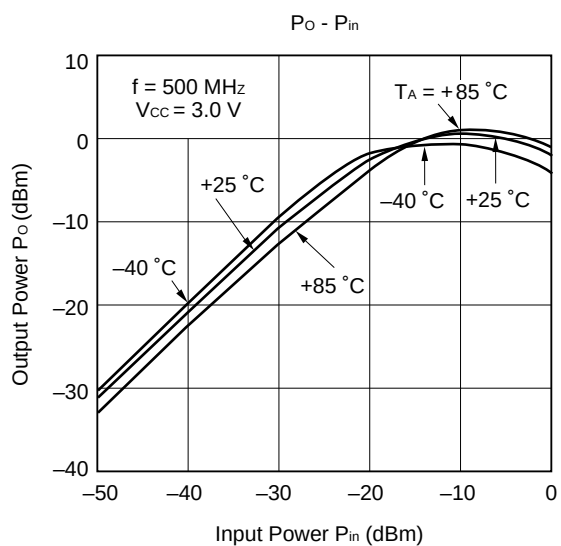
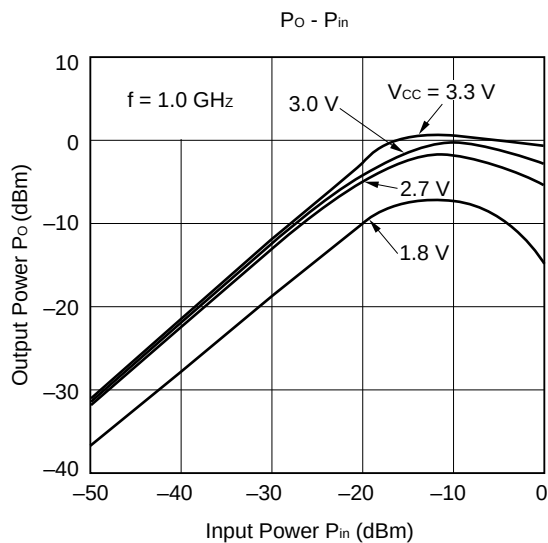
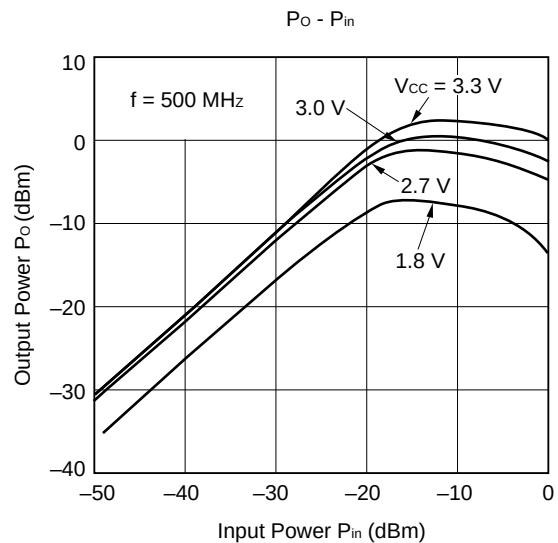
Note

1. $30 \times 30 \times 0.4$ mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. $\oplus \oplus \oplus$: Through holes

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$) – μ PC2746T –

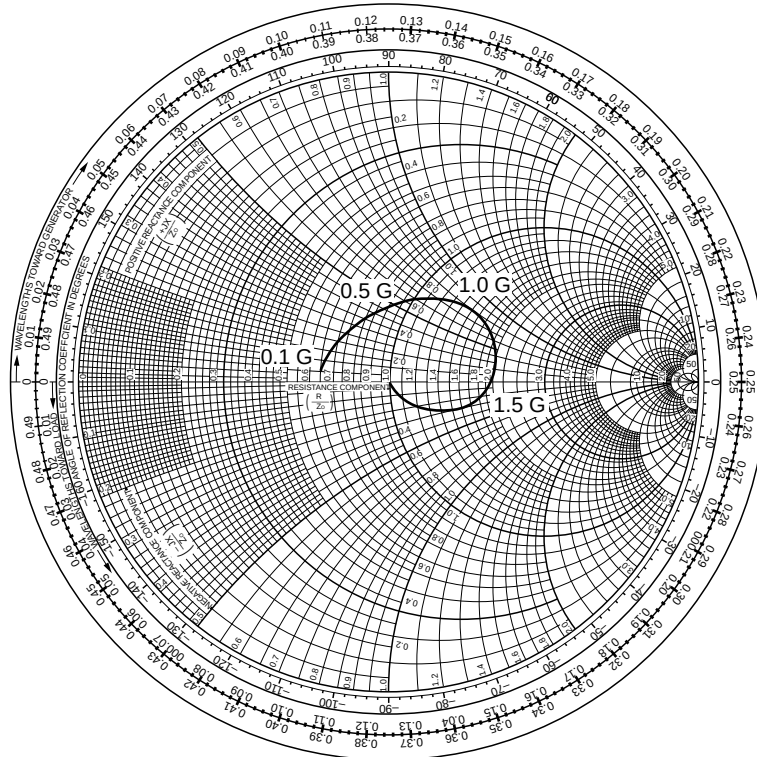


- μ PC2746T -

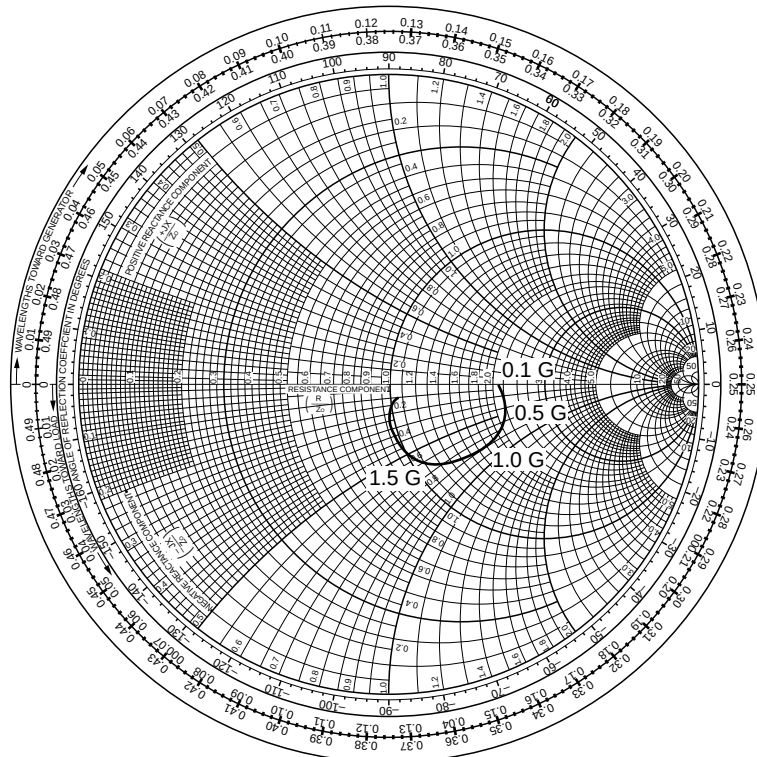


S Parameter – μ PC2746T –

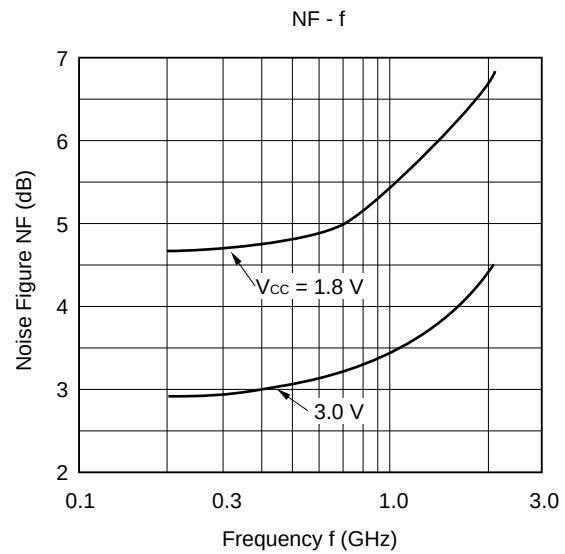
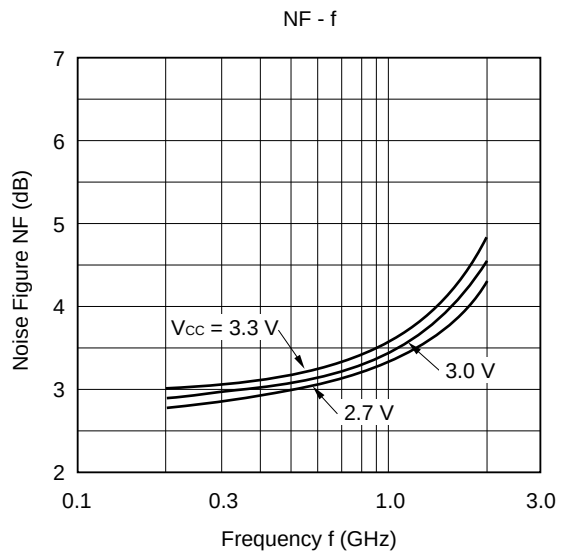
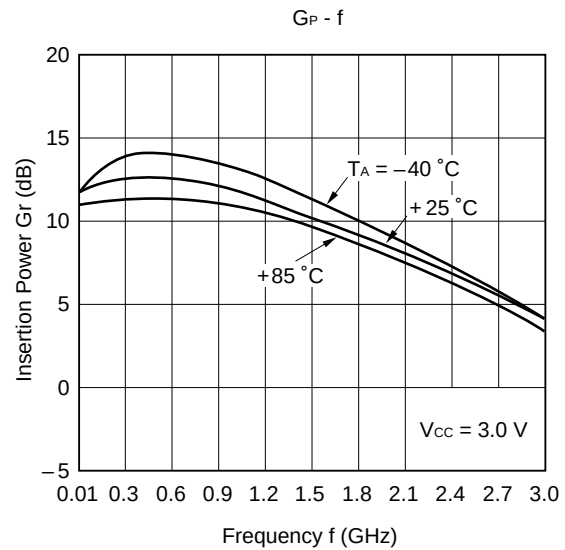
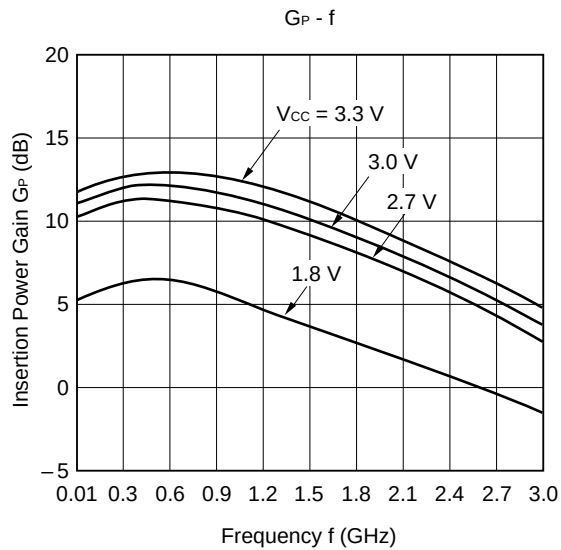
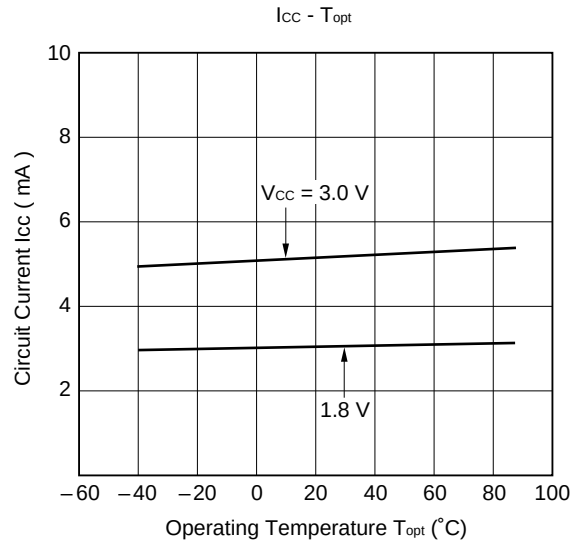
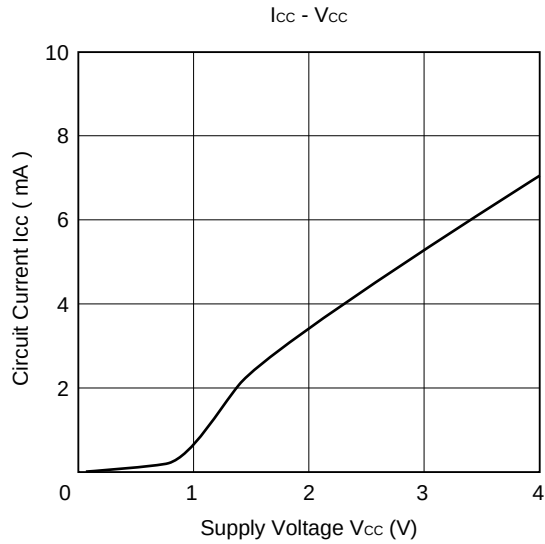
S₁₁-FREQUENCY (V_{CC} = 3.0 V)



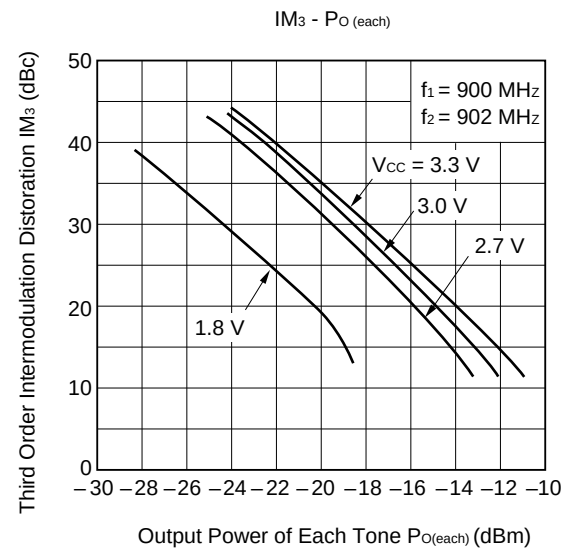
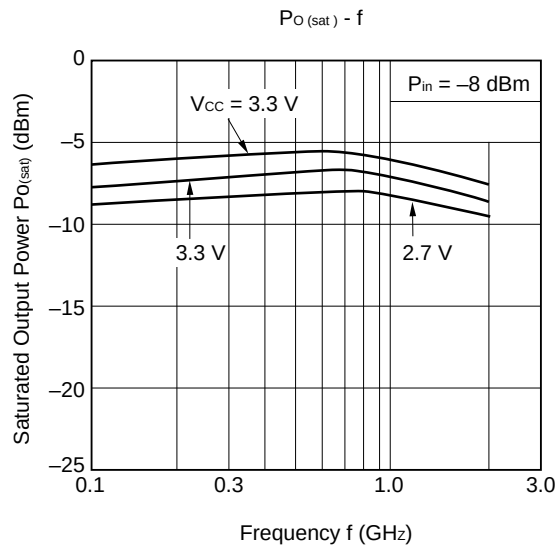
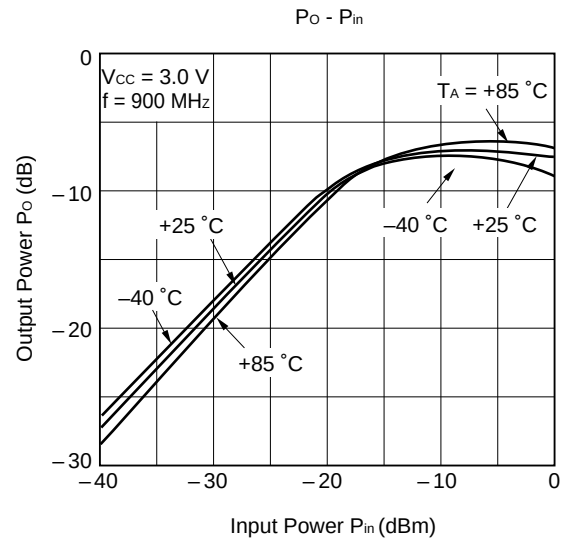
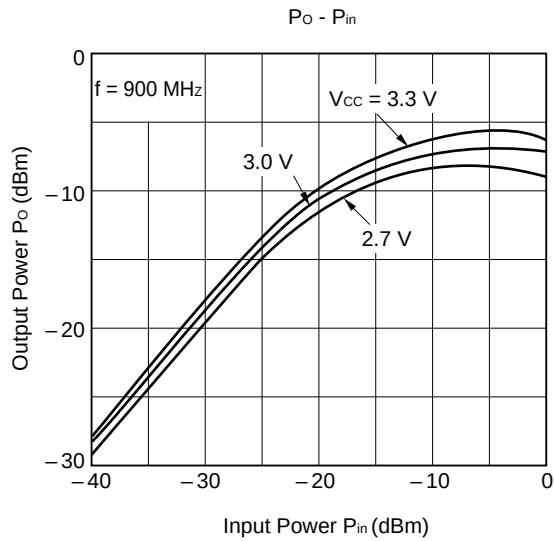
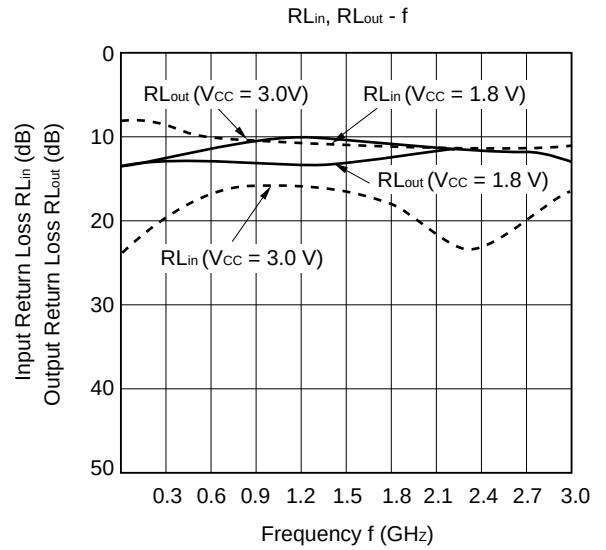
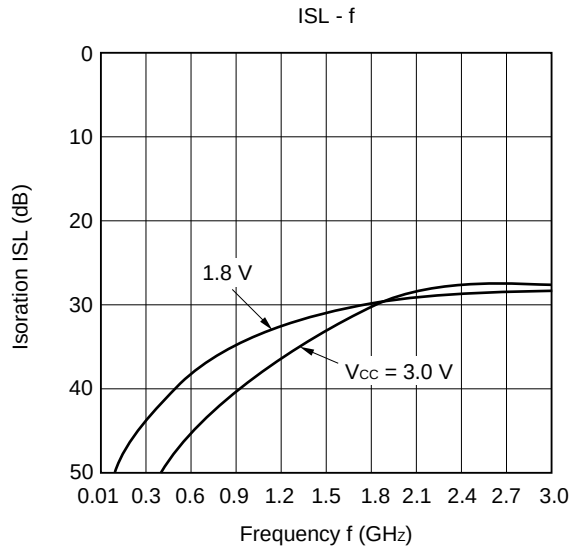
S₂₂-FREQUENCY (V_{CC} = 3.0 V)



TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$) – μ PC2747T –

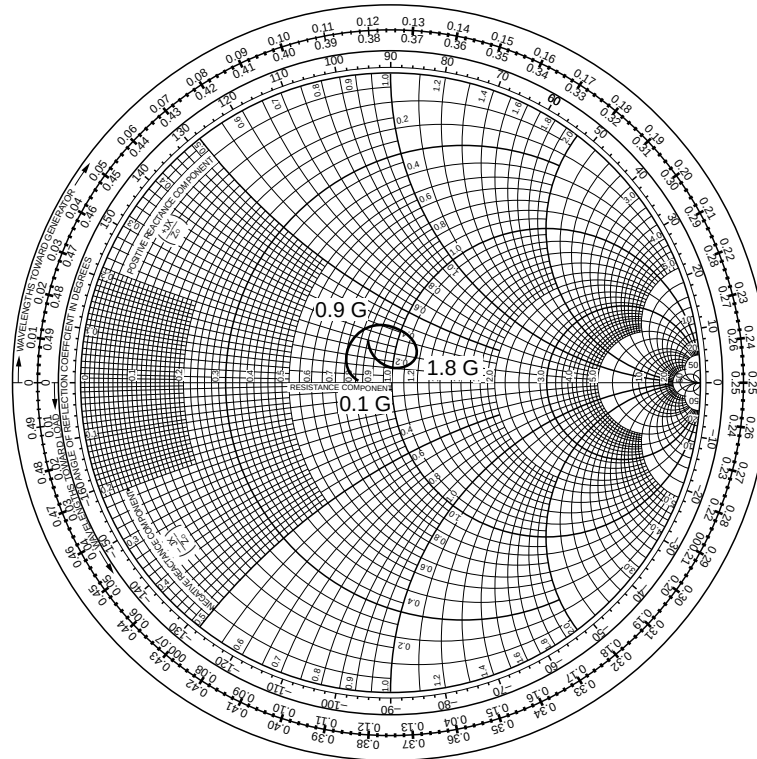


- μ PC2747T -

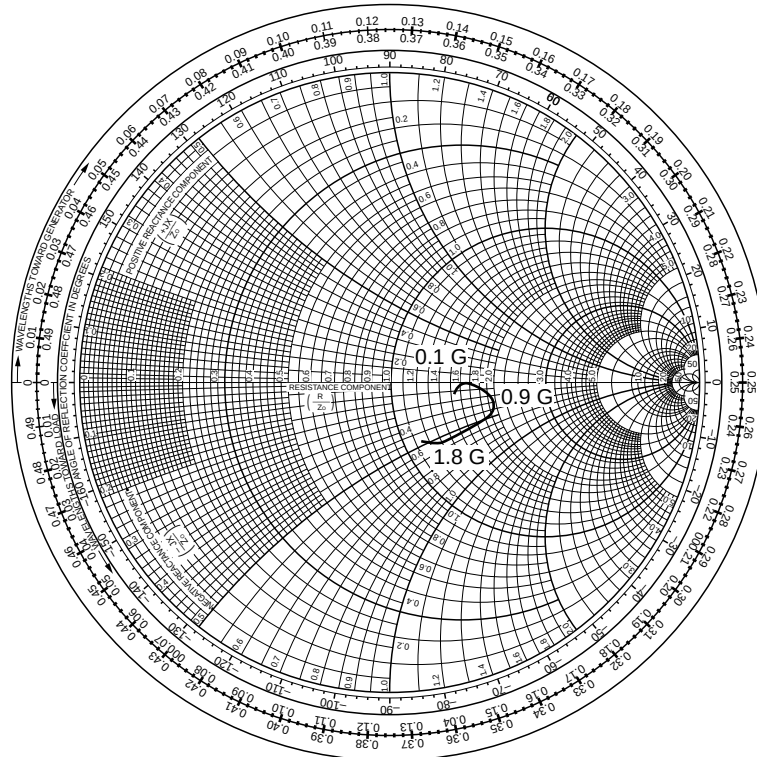


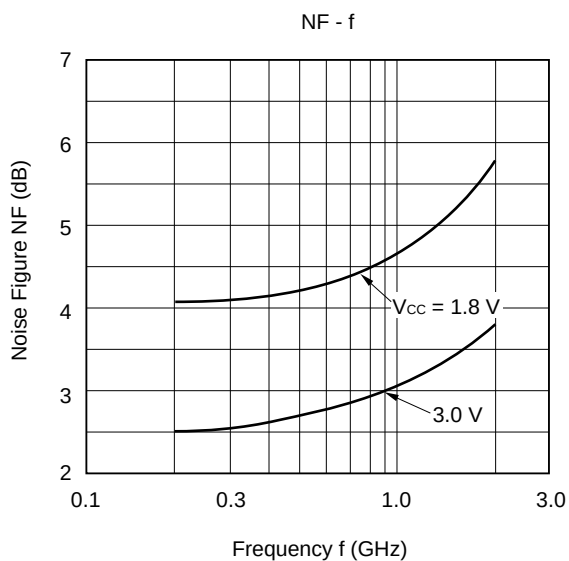
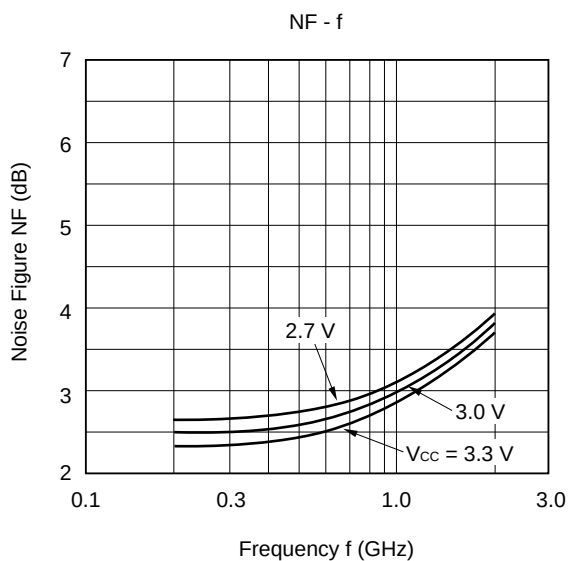
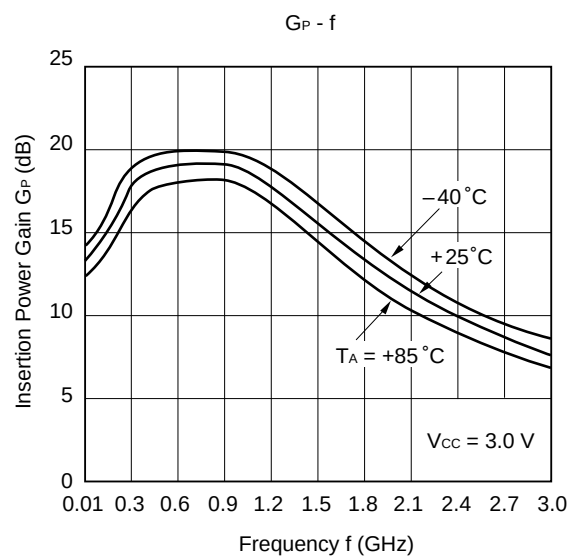
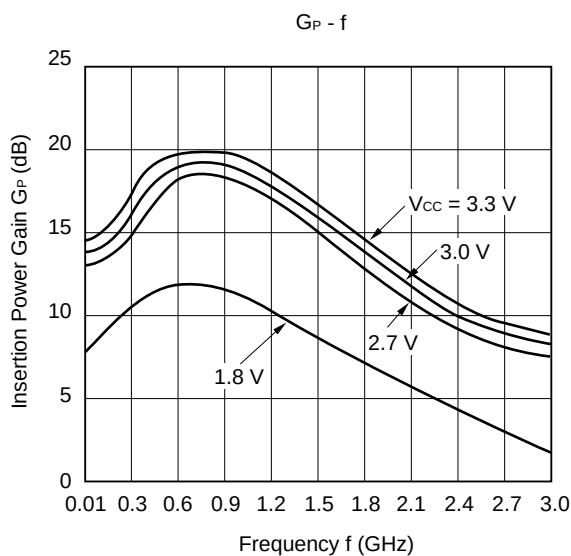
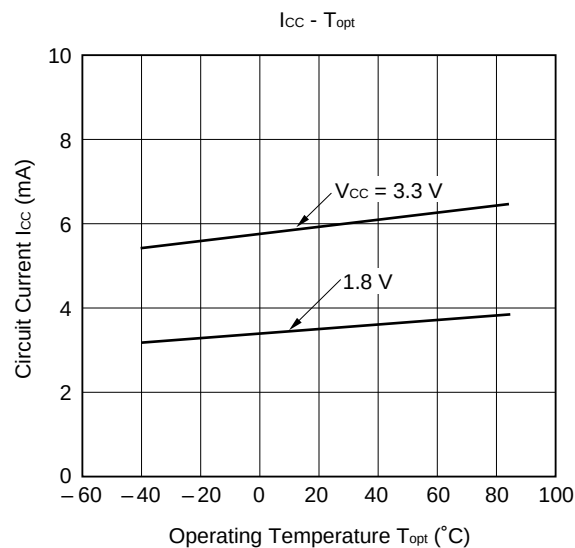
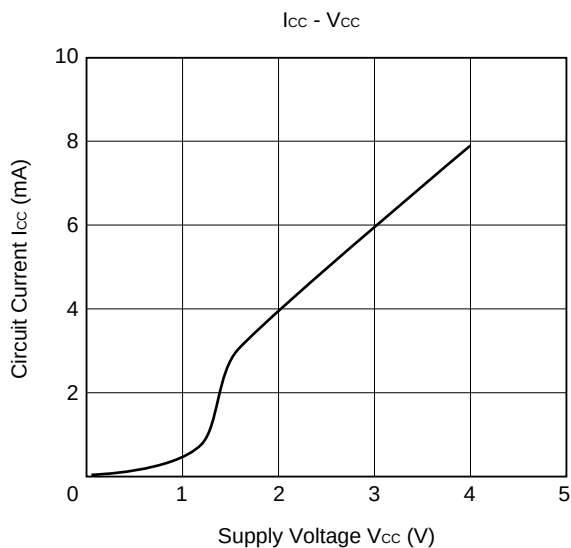
S Parameter ($T_A = +25\text{ }^\circ\text{C}$) – μ PC2747T –

S₁₁-FREQUENCY ($V_{CC} = 3.0\text{ V}$)



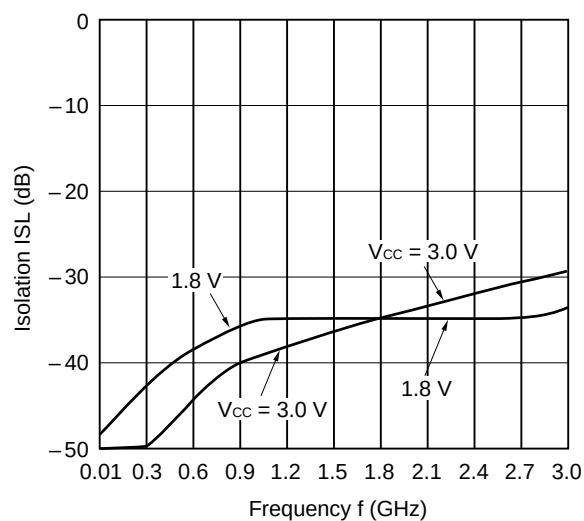
S₂₂-FREQUENCY ($V_{CC} = 3.0\text{ V}$)



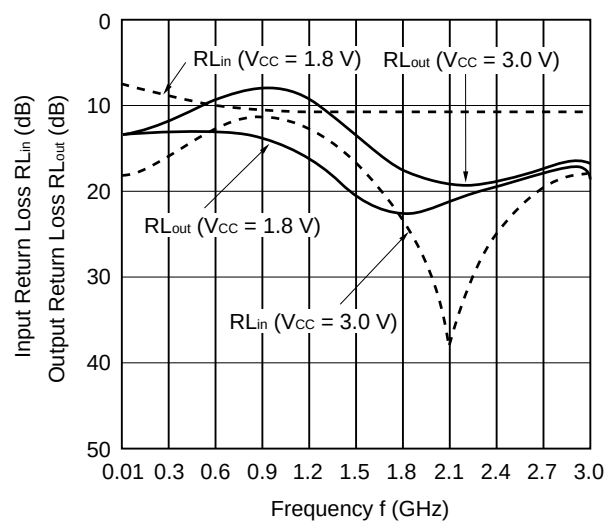
TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$) – μ PC2748T –

– μ PC2748T –

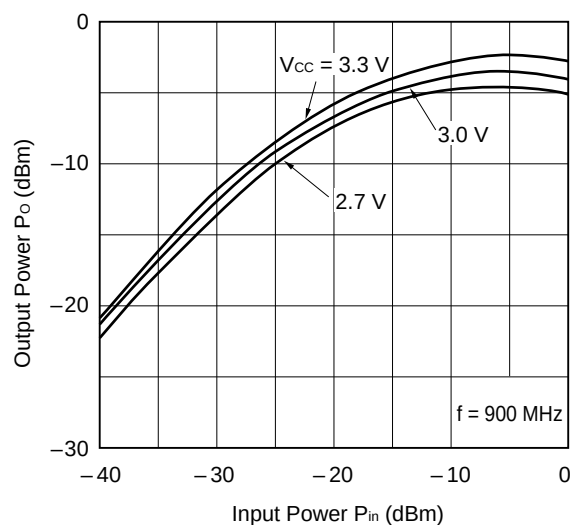
ISL - f



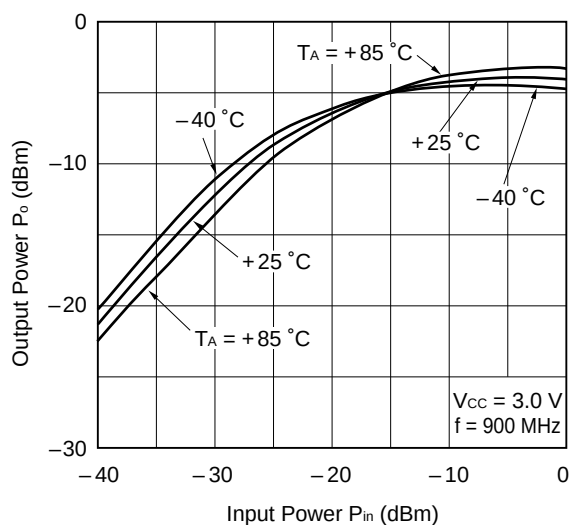
$RL_{in}, RL_{out} - f$



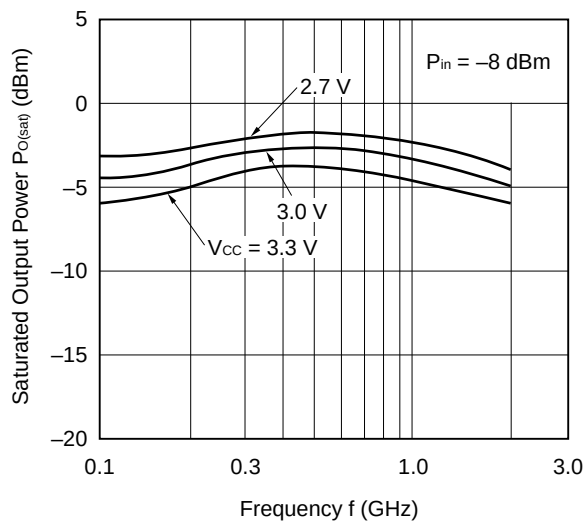
$P_O - P_{in}$



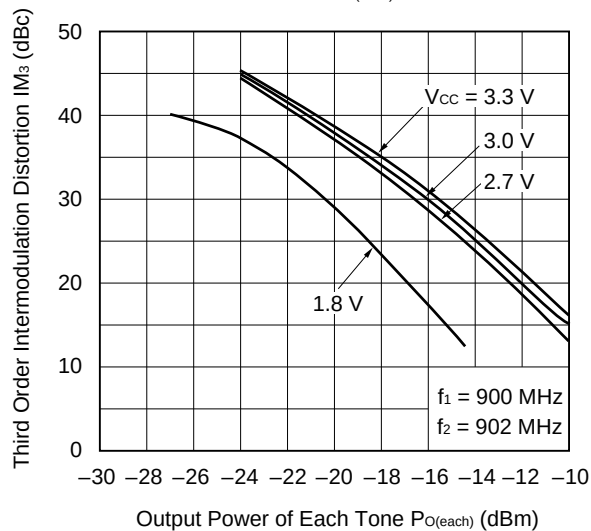
$P_O - P_{in}$



$P_{O(sat)} - f$

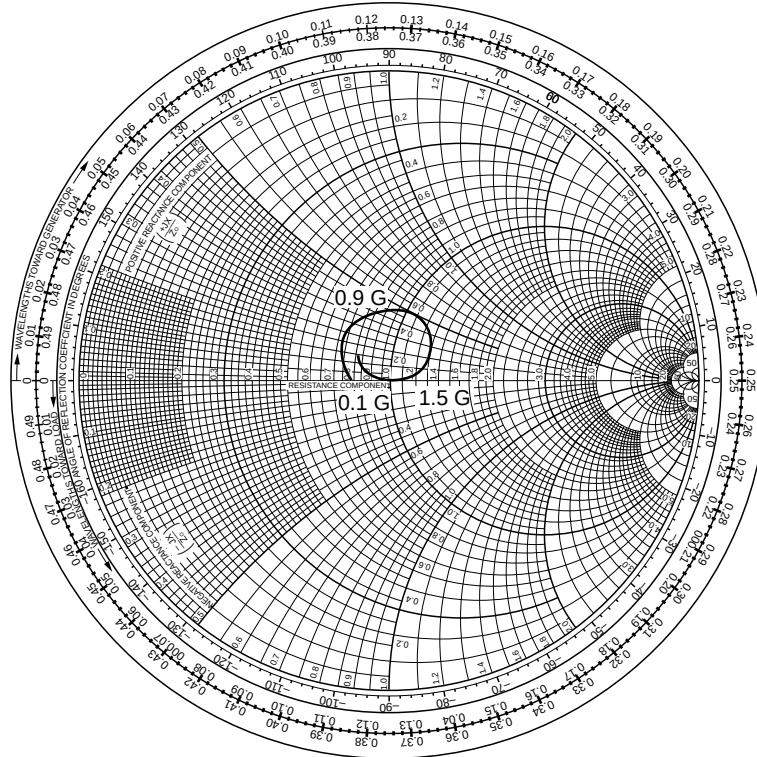


$IM_3 - P_{O(each)}$

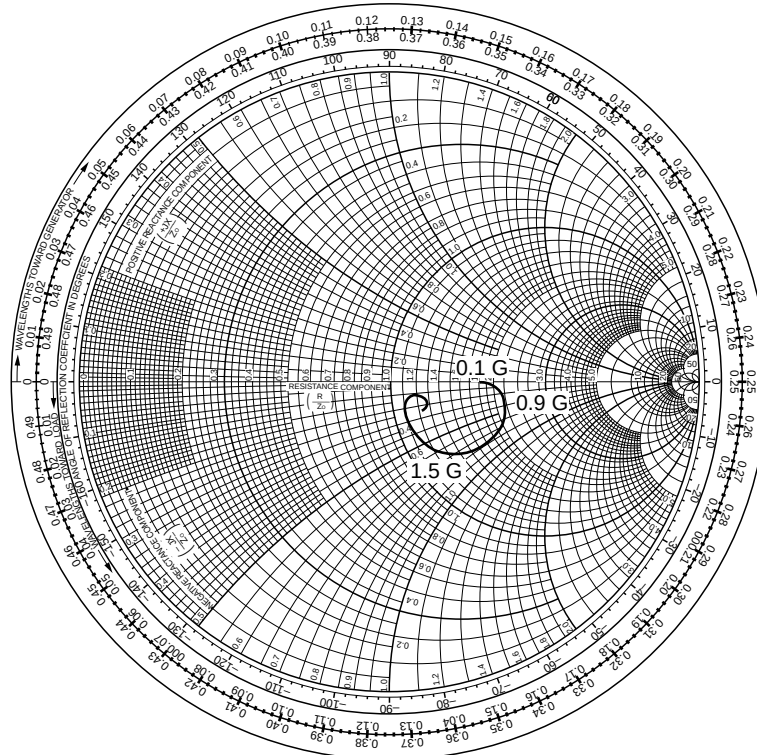


S Parameter – μ PC2748T –

S₁₁-FREQUENCY (V_{CC} = 3.0 V)

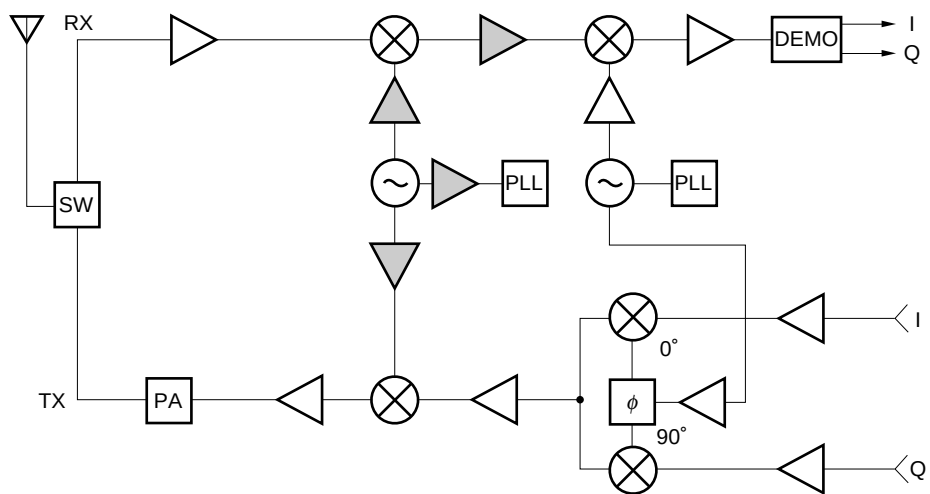


S₂₂-FREQUENCY (V_{CC} = 3.0 V)



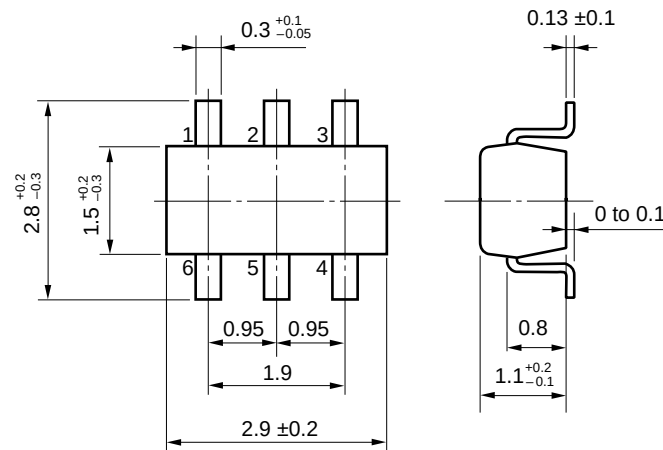
Typical System Application

Digital Cellular System Block Diagram



▶ : μ PC2746T, 2747T, 2748T applicable

6 PIN MINI MOLD PACKAGE DIMENSIONS (Unit: mm)



NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- (3) Keep the wiring length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{cc} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC2746T, 2747T, 2748T

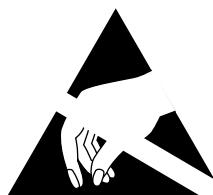
Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210° C) Time: 3 times, Limited days: no.*	IR35-00-3
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C) Time: 3 times, Limited days: no.*	VP15-00-3
Wave soldering	Soldering tub temperature: less than 260° C, Hour: within 10 s. Time: 1 times, Limited days: no.*	WS60-00-1
Pin part heating	Pin area temperature: 300 °C, Hour: within 3 s/pin. Limited days: no.*	

*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10537EJ7V0IF00).

[MEMO]



ATTENTION

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Anti-radioactive design is not implemented in this product.

M4 94.11

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