

HIGH FREQUENCY NPN TRANSISTOR ARRAY

FEATURES

• FIVE MONOLITHIC 9 GHz fr TRANSISTORS:

Two of these use a common emitter pin and can be used as differential amplifiers

• OUTSTANDING h_{FE} LINEARITY

• TWO PACKAGE OPTIONS:

μ PA103B: Superior thermal dissipation due to studded ceramic package

μ PA103G: Reduced circuit size due to 14-pin plastic SOP package for surface mounting

DESCRIPTION AND APPLICATIONS

The μ PA103 is a user configurable Silicon bipolar transistor array consisting of a common emitter pair and three individual bipolar transistors. It is available in a surface mount 14-pin plastic SOP package and a 14-pin ceramic package. Typical applications include: differential amplifiers and oscillators, high speed comparators, advanced cellular phone systems, electro-optic and other signal processing up to 1.5 gigabits/second.

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA103B-E1	14-pin ceramic package
μ PA103G-E1	14-pin plastic SOP (225 mil)

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CBO}^*	Collector to Base Voltage	V	15
V_{CEO}^*	Collector to Emitter Voltage	V	6
V_{EBO}^*	Emitter to Base Voltage	V	2.5
I_C^*	Collector Current	mA	40
P_T	Power Dissipation		
	μ PA103B	mW	650
	μ PA103G	mW	350
T_J	Junction Temperature		
	μ PA103B	$^\circ\text{C}$	200
	μ PA103G	$^\circ\text{C}$	125
T_{STG}	Storage Temperature		
	μ PA103B	$^\circ\text{C}$	-55 to +200
	μ PA103G	$^\circ\text{C}$	-55 to +125

* Absolute maximum ratings for each transistor.

Caution electro-static sensitive devices

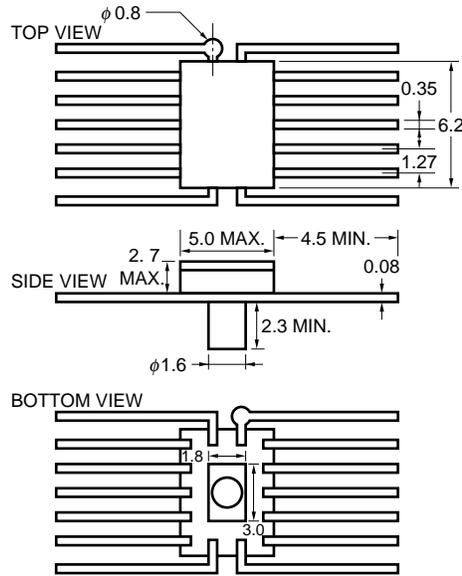
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PACKAGE DIMENSIONS (UNIT: mm)

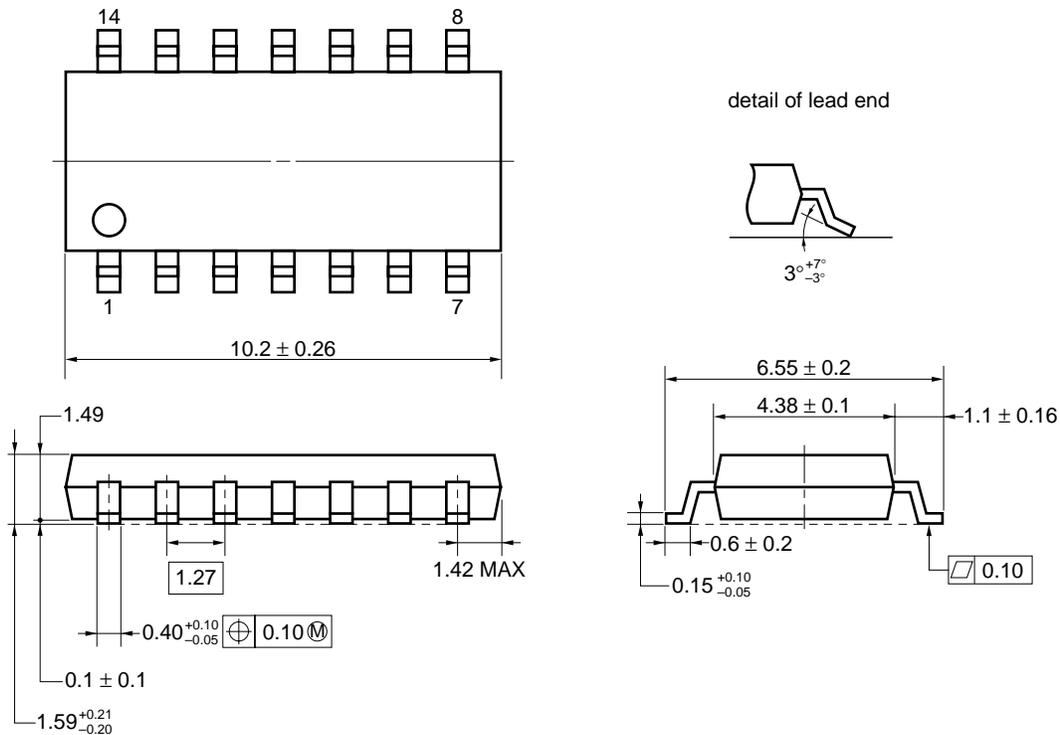
μPA103B

14 PIN CERAMIC PACKAGE



μPA103G

★ 14 PIN PLASTIC SOP (225 mil)



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

See connection diagram for description of leads.

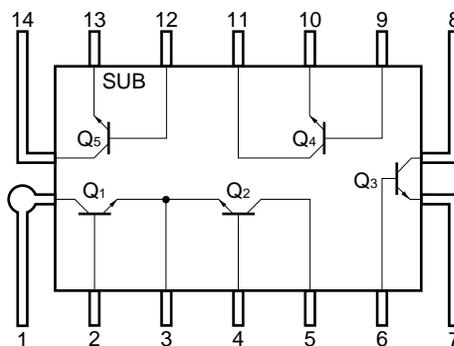
ELECTRICAL CHARACTERISTICS (Unless otherwise specified $T_A = +25\text{ }^\circ\text{C}$ μPA103B, μPA103G common)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN.	TYP.	MAX.
I_{CBO}	Collector Cutoff Current at $V_{CB} = 5\text{ V}$, $I_E = 0$ (Q1 to Q5)	μA			1.0
I_{EBO}	Emitter Cutoff Current at $V_{EB} = 1\text{ V}$, $I_C = 0$ (Q1 to Q5)	μA			1.0
h_{FE}	Direct Current Amplification at $V_{CE} = 3\text{ V}$, $I_C = 5\text{ mA}$ (Q1 to Q5)		40	100	250
h_{FE1}/h_{FE2}	Direct Current Amplification Ratio at $V_{CE} = 3\text{ V}$, $I_C = 5\text{ mA}$, (Q1, Q2)		0.9	1.0	1.1
V_{BE}	Emitter to Base Voltage at $V_{CE} = 3\text{ V}$, $I_C = 5\text{ mA}$ (Q1, Q2)	V		0.8	1.0
ΔV_{BE}	Emitter to Base Voltage Difference, $V_{CE} = 3\text{ V}$, $I_C = 5\text{ mA}$ [Q1 - Q2]	mV		8.0	20
C_{CB}	Collector to Base Capacitance at $V_{CB} = 3\text{ V}$, $f = 1\text{ MHz}$ (Q1 to Q5)	pF		0.9	1.8
C_{EB}	Emitter to Base Capacitance at $V_{EB} = 0$, $f = 1\text{ MHz}$ (Q1 to Q4)	pF		1.4	2.8
C_{CS}	Collector/Substrate Capacitance at $V_{CS} = 3\text{ V}$, $f = 1\text{ MHz}$ (Q1 to Q4)	pF		1.4	2.8
f_T	Gain Bandwidth Product* at $V_{CE} = 3\text{ V}$, $I_C = 10\text{ mA}$	GHz		9.0	

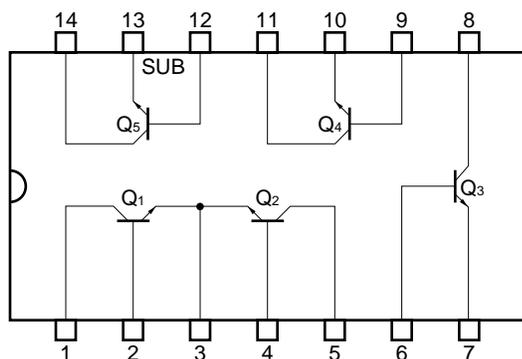
* Measured by installing a single transistor in a Micro-X package: the value shown is a reference value.

CONNECTION DIAGRAM (Top View)

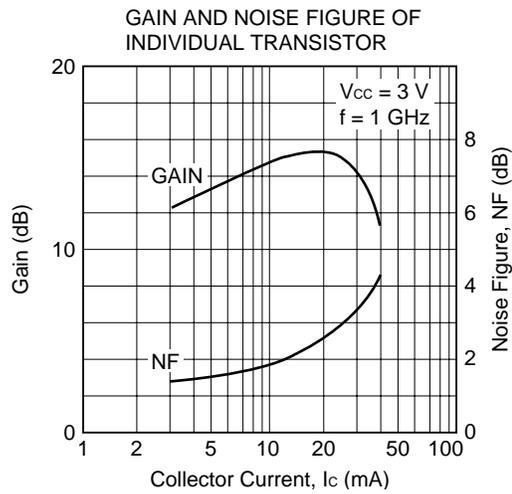
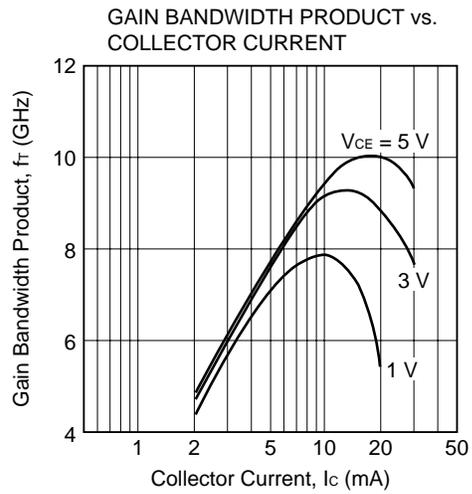
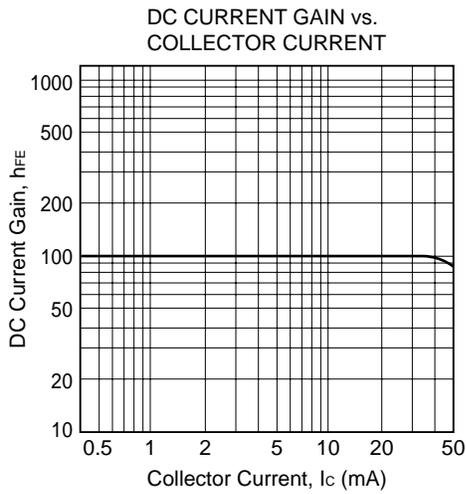
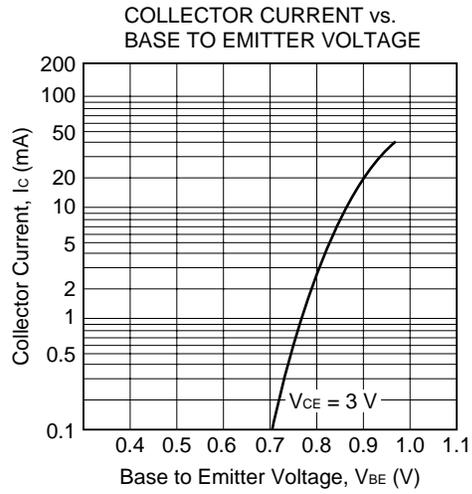
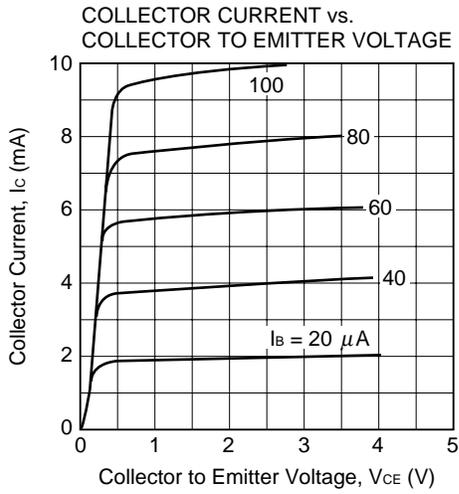
μPA103B



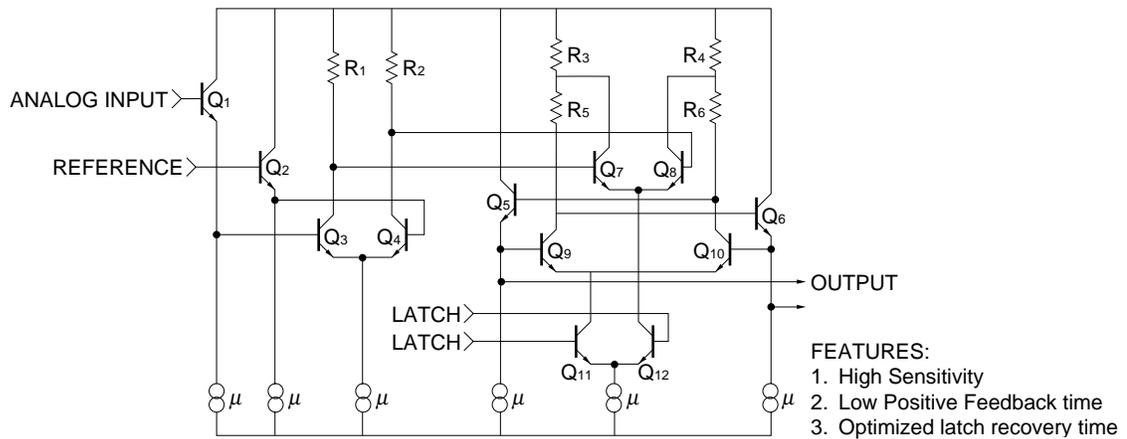
μPA103G



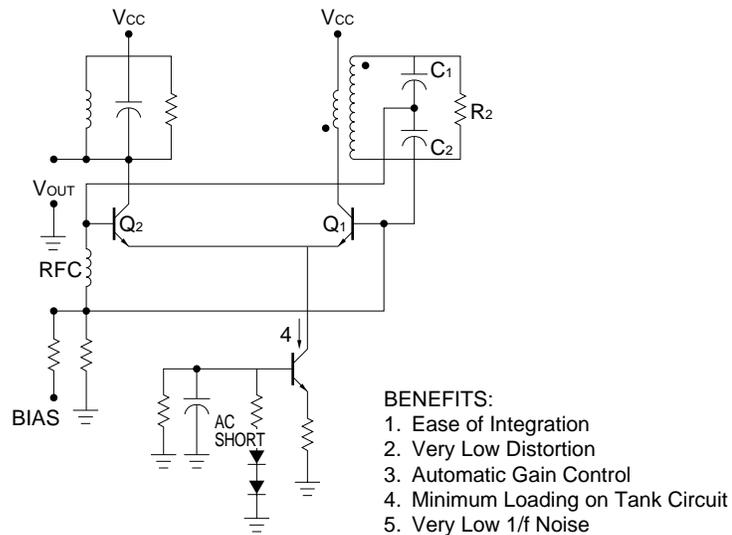
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = +25^\circ\text{C}$)



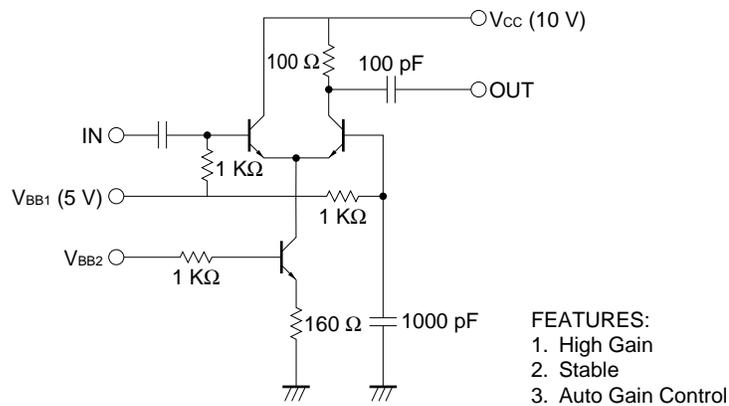
TYPICAL HIGH SPEED COMPARATOR



TYPICAL DIFFERENTIAL OSCILLATOR



TYPICAL COMMON MODE DIFFERENTIAL AMP



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- (3) Design circuits connected Sub pin to the lowest voltage to prevent latch-up.
- (4) Design circuits as each pin voltage difference within 15 V maximum.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPA103G

Soldering process	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 2 times, Limited days: no. ^{Note}	IR35-00-2
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 2 times, Limited days: no. ^{Note}	VP15-00-2
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no. ^{Note}	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s./pin Limited days: no. ^{Note}	

μPA103B

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 10 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	
Partial heating method	Terminal temperature: 260 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

Note It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Caution The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

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