

2M-BIT CMOS STATIC RAM  
128K-WORD BY 16-BIT  
EXTENDED TEMPERATURE OPERATION**Description**

The  $\mu$ PD442012L-X is a high speed, low power, 2,097,152 bits (131,072 words by 16 bits) CMOS static RAM.

The  $\mu$ PD442012L-X has two chip enable pins (/CE1, CE2) to extend the capacity.

★ The  $\mu$ PD442012L-X is packed in 48-pin plastic TSOP (I) (Normal bent).

**Features**

- 131,072 words by 16 bits organization
- Fast access time: 70, 85, 100, 120, 150, 200 ns (MAX.)
- Byte data control: /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation  
(B version:  $V_{CC} = 2.7$  to  $3.6$  V, C version:  $V_{CC} = 2.2$  to  $3.6$  V, D version:  $V_{CC} = 1.8$  to  $3.6$  V)
- Low  $V_{CC}$  data retention  
(B version: 2.0 V (MIN.), C version: 1.5 V (MIN.), D version: 1.5 V (MIN.))
- Operating ambient temperature:  $T_A = -25$  to  $+85$  °C
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

| Part number                          | Access time<br>ns (MAX.) | Operating supply<br>voltage<br>V | Operating ambient<br>temperature<br>°C | Supply current            |                              |                                     |
|--------------------------------------|--------------------------|----------------------------------|--|---------------------------|------------------------------|-------------------------------------|
|                                      |                          |                                  |  | At operating<br>mA (MAX.) | At standby<br>$\mu$ A (MAX.) | At data retention<br>$\mu$ A (MAX.) |
| $\mu$ PD442012L-BxxX                 | 70, 85                   | 2.7 to 3.6                       | -25 to +85                             | 35                        | 4                            | 4                                   |
| $\mu$ PD442012L-CxxX                 | 100, 120                 | 2.2 to 3.6                       |  |                           |                              |                                     |
| $\mu$ PD442012L-DxxX <sup>Note</sup> | 150, 200                 | 1.8 to 3.6                       |  |                           |                              |                                     |

**Note** Under development

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ Ordering Information

| Part number                               | Package  | Access time<br>ns (MAX.) | Operating<br>supply voltage<br>V | Operating<br>temperature<br>°C | Remark    |
|---|--|--------------------------|----------------------------------|--------------------------------|-----------|
| μPD442012LGY-B70X-MJH                     | 48-PIN PLASTIC TSOP (I)<br><br>(12×18) (Normal bent) | 70                       | 2.7 to 3.6                       | −25 to +85                     | B version |
| μPD442012LGY-B85X-MJH                     |  | 85                       | 2.2 to 3.6                       |                                |           |
| μPD442012LGY-C10X-MJH                     |  | 100                      |                                  |                                | C version |
| μPD442012LGY-C12X-MJH                     |  | 120                      | 1.8 to 3.6                       |                                |           |
| μPD442012LGY-D15X-MJH <small>Note</small> |  | 150                      |                                  |                                | D version |
| μPD442012LGY-D20X-MJH <small>Note</small> |  | 200                      |                                  |                                |           |

**Note** Under development

★ Pin Configuration (Marking Side)

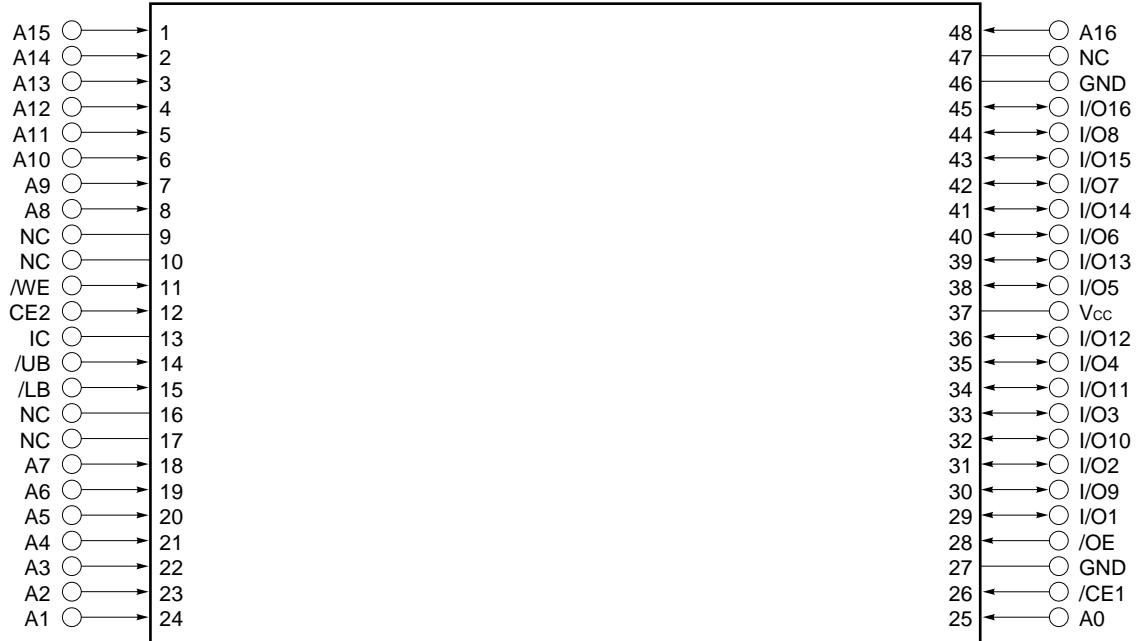
/xxx indicates active low signal.

48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

[ μPD442012LGY-BxxX-MJH ]

[ μPD442012LGY-CxxX-MJH ]

[ μPD442012LGY-DxxX-MJH ]

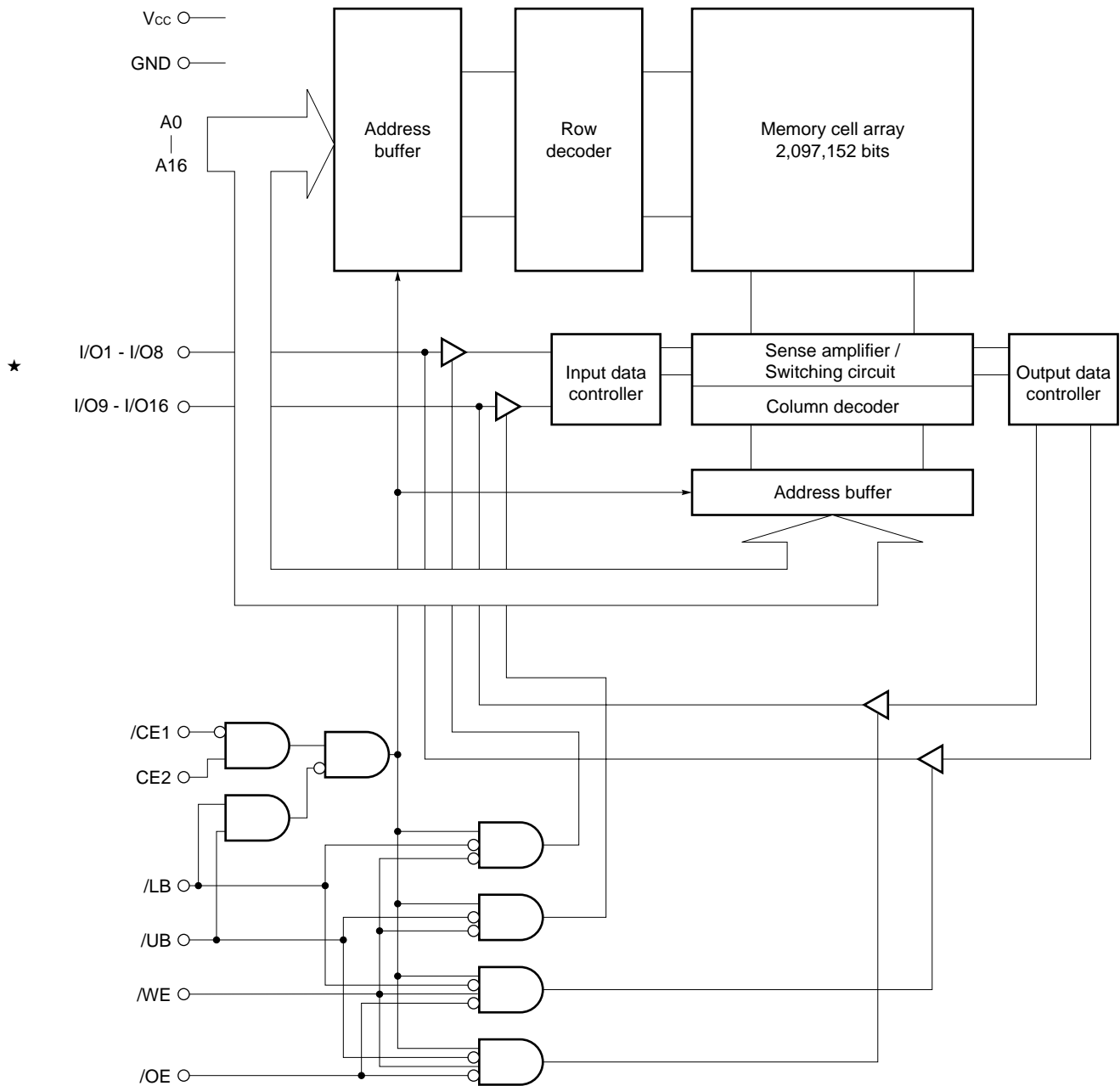


- A0 - A16 : Address inputs
- I/O1 - I/O16 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- V<sub>cc</sub> : Power supply
- GND : Ground
- NC : No Connection
- IC <sup>Note</sup> : Internal Connection

**Note** Leave this pin unconnected or connect to GND.

**Remark** Refer to **Package Drawing** for the 1-pin index mark.

# Block Diagram



Truth Table

| /CE1 | CE2 | /OE | /WE | /LB | /UB | Mode             | I/O              |                  | Supply current   |
|------|-----|-----|-----|-----|-----|------------------|------------------|------------------|------------------|
|      |     |     |     |     |     |                  | I/O1 - I/O8      | I/O9 - I/O16     |                  |
| H    | ×   | ×   | ×   | ×   | ×   | Not selected     | High impedance   | High impedance   | I <sub>SB</sub>  |
| ×    | L   | ×   | ×   | ×   | ×   |                  |                  |                  |                  |
| L    | H   | H   | H   | ×   | ×   | Output disable   | High impedance   | High impedance   | I <sub>CCA</sub> |
|      |     | L   | H   | L   | L   | Word read        | D <sub>OUT</sub> | D <sub>OUT</sub> |                  |
|      |     |     |     | L   | H   | Lower byte read  | D <sub>OUT</sub> | High impedance   |                  |
|      |     |     |     | H   | L   | Upper byte read  | High impedance   | D <sub>OUT</sub> |                  |
|      |     | ×   | L   | L   | L   | Word write       | D <sub>IN</sub>  | D <sub>IN</sub>  |                  |
|      |     |     |     | L   | H   | Lower byte write | D <sub>IN</sub>  | High impedance   |                  |
|      |     |     |     | H   | L   | Upper byte write | High impedance   | D <sub>IN</sub>  |                  |
| ×    | ×   | ×   | ×   | H   | H   | Not selected     | High impedance   | High impedance   | I <sub>SB</sub>  |

★

Remark × : V<sub>IH</sub> or V<sub>IL</sub>

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter                     | Symbol           | Condition | Rating  | Unit |
|-------------------------------|------------------|-----------|---|------|
| Supply voltage                | V <sub>CC</sub>  |           | -0.5 <sup>Note</sup> to +4.0                              | V    |
| Input / Output voltage        | V <sub>I</sub>   |           | -0.5 <sup>Note</sup> to V <sub>CC</sub> +0.4 (4.0 V MAX.) | V    |
| Operating ambient temperature | T <sub>A</sub>   |           | -25 to +85  | °C   |
| Storage temperature           | T <sub>stg</sub> |           | -55 to +125   | °C   |

**Note** -3.0 V (MIN.) (Pulse width : 30 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

| Parameter                     | Symbol          | Condition                       | μPD442012L-BxxX      |                      | μPD442012L-CxxX      |                      | μPD442012L-DxxX      |                      | Unit |
|-------------------------------|-----------------|---------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|------|
|                               |                 |                                 | MIN.                 | MAX.                 | MIN.                 | MAX.                 | MIN.                 | MAX.                 |      |
| Supply voltage                | V <sub>CC</sub> |                                 | 2.7                  | 3.6                  | 2.2                  | 3.6                  | 1.8                  | 3.6                  | V    |
| High level input voltage      | V <sub>IH</sub> | 2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V | 2.4                  | V <sub>CC</sub> +0.4 | 2.4                  | V <sub>CC</sub> +0.4 | 2.4                  | V <sub>CC</sub> +0.4 | V    |
|                               |                 | 2.2 V ≤ V <sub>CC</sub> < 2.7 V | —                    | —                    | 2.0                  | V <sub>CC</sub> +0.3 | 2.0                  | V <sub>CC</sub> +0.3 |      |
|                               |                 | 1.8 V ≤ V <sub>CC</sub> < 2.2 V | —                    | —                    | —                    | —                    | 1.6                  | V <sub>CC</sub> +0.2 |      |
| Low level input voltage       | V <sub>IL</sub> |                                 | -0.3 <sup>Note</sup> | +0.5                 | -0.3 <sup>Note</sup> | +0.3                 | -0.3 <sup>Note</sup> | +0.2                 | V    |
| Operating ambient temperature | T <sub>A</sub>  |                                 | -25                  | +85                  | -25                  | +85                  | -25                  | +85                  | °C   |

**Note** -1.5 V (MIN.) (Pulse width: 30 ns)

### Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)

| Parameter                  | Symbol           | Test condition         | MIN. | TYP. | MAX. | Unit |
|----------------------------|------------------|------------------------|------|------|------|------|
| Input capacitance          | C <sub>IN</sub>  | V <sub>IN</sub> = 0 V  |      |      | 8    | pF   |
| Input / Output capacitance | C <sub>I/O</sub> | V <sub>I/O</sub> = 0 V |      |      | 10   | pF   |

**Remarks 1.** V<sub>IN</sub> : Input voltage

V<sub>I/O</sub> : Input / Output voltage

**2.** These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

| Parameter                 | Symbol                 | Test condition   | V <sub>CC</sub> ≥ 2.7 V   |      |      | V <sub>CC</sub> ≥ 2.2 V |      |      | V <sub>CC</sub> ≥ 1.8 V |      |      | Unit |     |
|---------------------------|------------------------|--|---|------|------|-------------------------|------|------|-------------------------|------|------|------|-----|
|                           |                        |  | μPD442012L-BxxX   |      |      | μPD442012L-CxxX         |      |      | μPD442012L-DxxX         |      |      |      |     |
|                           |                        |  | MIN.  | TYP. | MAX. | MIN.                    | TYP. | MAX. | MIN.                    | TYP. | MAX. |      |     |
| Input leakage current     | I <sub>LI</sub>        | V <sub>IN</sub> = 0 V to V <sub>CC</sub>   | −1.0  |      | +1.0 | −1.0                    |      | +1.0 | −1.0                    |      | +1.0 | μA   |     |
| I/O leakage current       | I <sub>LO</sub>        | V <sub>I/O</sub> = 0 V to V <sub>CC</sub> , /CE1 = V <sub>IH</sub> or<br>CE2 = V <sub>IL</sub> or /WE = V <sub>IL</sub> or /OE = V <sub>IH</sub>                 | −1.0  |      | +1.0 | −1.0                    |      | +1.0 | −1.0                    |      | +1.0 | μA   |     |
| Operating supply current  | I <sub>CCA1</sub>      | /CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> ,   |   | −    | 35   |                         | −    | 35   |                         | −    | 35   | mA   |     |
|                           |                        | Minimum cycle time,<br>I <sub>I/O</sub> = 0 mA   | V <sub>CC</sub> ≤ 2.7 V   |      | −    | −                       |      | −    | 20                      |      | −    |      | 20  |
|                           |                        |  | V <sub>CC</sub> ≤ 2.2 V   |      | −    | −                       |      | −    | −                       |      | −    |      | 15  |
|                           | I <sub>CCA2</sub>      | /CE1 = V <sub>IL</sub> , CE2 = V <sub>IH</sub> ,   |   | −    | 10   |                         | −    | 10   |                         | −    | 10   |      |     |
|                           |                        | I <sub>I/O</sub> = 0 mA  | V <sub>CC</sub> ≤ 2.7 V   |      | −    | −                       |      | −    | 8                       |      | −    |      | 8   |
|                           |                        |  | V <sub>CC</sub> ≤ 2.2 V   |      | −    | −                       |      | −    | −                       |      | −    |      | 6   |
|                           | I <sub>CCA3</sub>      | /CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> − 0.2 V,<br>Cycle = 1 MHz, I <sub>I/O</sub> = 0 mA,<br>V <sub>IL</sub> ≤ 0.2 V,<br>V <sub>IH</sub> ≥ V <sub>CC</sub> − 0.2 V |   | −    | 8    |                         | −    | 8    |                         | −    | 8    |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.7 V  |   | −    | −    |                         | −    | 6    |                         | −    | 6    |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.2 V  |   | −    | −    |                         | −    | −    |                         | −    | 5    |      |     |
|                           | Standby supply current | I <sub>SB</sub>  | /CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or<br>/LB = /UB = V <sub>IH</sub> , |      | −    | 0.6                     |      | −    | 0.6                     |      | −    |      | 0.6 |
| V <sub>CC</sub> ≤ 2.7 V   |                        |  |   | −    | −    |                         | −    | 0.6  |                         | −    | 0.6  |      |     |
| V <sub>CC</sub> ≤ 2.2 V   |                        |  |   | −    | −    |                         | −    | −    |                         | −    | 0.6  |      |     |
| I <sub>SB1</sub>          |                        | /CE1 ≥ V <sub>CC</sub> − 0.2 V,<br>CE2 ≥ V <sub>CC</sub> − 0.2 V   |   | 0.3  | 4    |                         | 0.3  | 4    |                         | 0.3  | 4    | μA   |     |
|                           |                        | V <sub>CC</sub> ≤ 2.7 V  |   | −    | −    |                         | 0.25 | 3.5  |                         | 0.25 | 3.5  |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.2 V  |   | −    | −    |                         | −    | −    |                         | 0.2  | 3    |      |     |
| I <sub>SB2</sub>          |                        | CE2 ≤ 0.2 V  |   | 0.3  | 4    |                         | 0.3  | 4    |                         | 0.3  | 4    |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.7 V  |   | −    | −    |                         | 0.25 | 3.5  |                         | 0.25 | 3.5  |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.2 V  |   | −    | −    |                         | −    | −    |                         | 0.2  | 3    |      |     |
| I <sub>SB3</sub>          |                        | /LB = /UB ≥ V <sub>CC</sub> − 0.2 V,<br>/CE1 ≤ 0.2 V,<br>CE2 ≥ V <sub>CC</sub> − 0.2 V   |   | 0.3  | 4    |                         | 0.3  | 4    |                         | 0.3  | 4    |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.7 V  |   | −    | −    |                         | 0.25 | 3.5  |                         | 0.25 | 3.5  |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.2 V  |   | −    | −    |                         | −    | −    |                         | 0.2  | 3    |      |     |
| High level output voltage | V <sub>OH</sub>        | I <sub>OH</sub> = −0.5 mA  | 2.4   |      |      | 2.4                     |      |      | 2.4                     |      |      | V    |     |
|                           |                        | V <sub>CC</sub> ≤ 2.7 V  | −   |      |      | 1.8                     |      |      | 1.8                     |      |      |      |     |
|                           |                        | V <sub>CC</sub> ≤ 2.2 V  | −   |      |      | −                       |      |      | 1.5                     |      |      |      |     |
| Low level output voltage  | V <sub>OL</sub>        | I <sub>OL</sub> = 1.0 mA   |   |      | 0.4  |                         |      | 0.4  |                         |      | 0.4  | V    |     |

Remarks 1. V<sub>IN</sub> : Input voltage

V<sub>I/O</sub> : Input / Output voltage

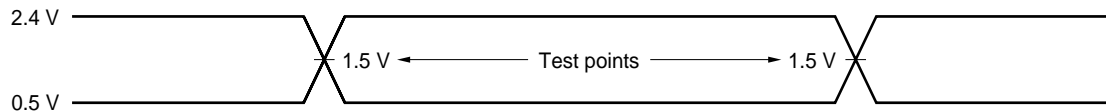
2. These DC characteristics are in common regardless of access time.

# AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

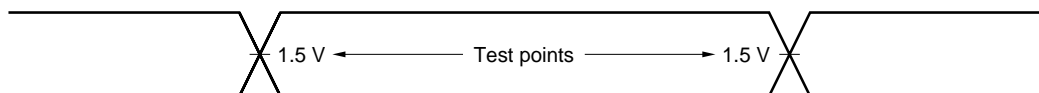
## AC Test Conditions

[ μPD442012L-B70X, μPD442012L-B85X ]

### Input Waveform (Rise and Fall Time ≤ 5 ns)



### Output Waveform

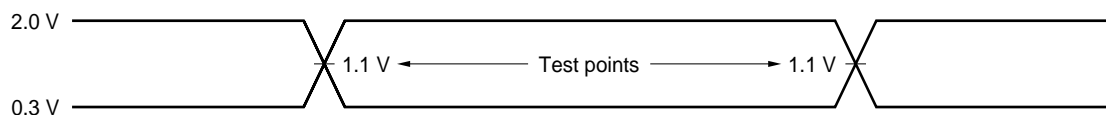


### Output Load

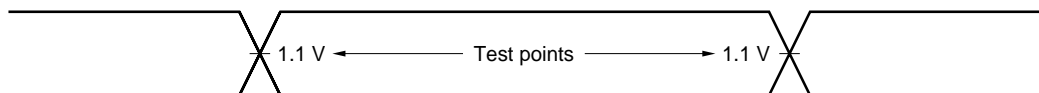
1TTL + 50 pF

[ μPD442012L-C10X, μPD442012L-C12X ]

### Input Waveform (Rise and Fall Time ≤ 5 ns)



### Output Waveform

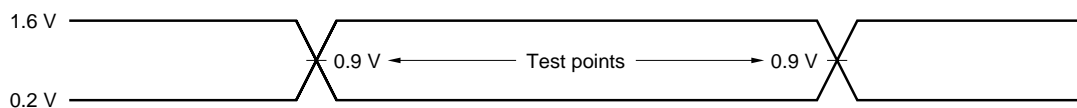


### Output Load

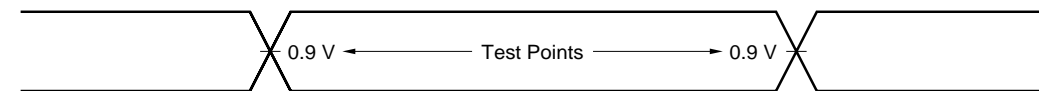
1TTL + 30 pF

[ μPD442012L-D15X, μPD442012L-D20X ]

### Input Waveform (Rise and Fall Time ≤ 5 ns)



### Output Waveform



### Output Load

1TTL + 30 pF

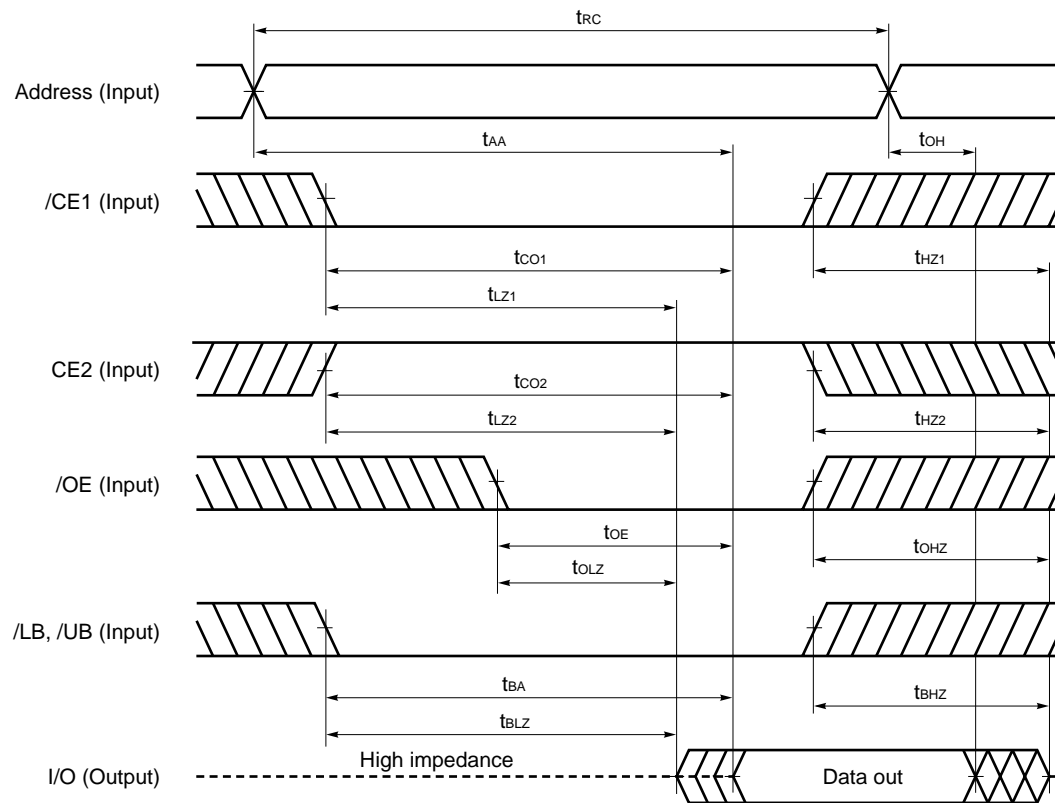


Read Cycle

| Parameter                            | Symbol           | V <sub>CC</sub> ≥ 2.7 V |      |                     |      | V <sub>CC</sub> ≥ 2.2 V |      |                     |      | V <sub>CC</sub> ≥ 1.8 V |      |                     |      | Unit | Condition |
|--------------------------------------|------------------|-------------------------|------|---------------------|------|-------------------------|------|---------------------|------|-------------------------|------|---------------------|------|------|-----------|
|                                      |                  | μPD442012L<br>-B70X     |      | μPD442012L<br>-B85X |      | μPD442012L<br>-C10X     |      | μPD442012L<br>-C12X |      | μPD442012L<br>-D15X     |      | μPD442012L<br>-D20X |      |      |           |
|                                      |                  | MIN.                    | MAX. | MIN.                | MAX. | MIN.                    | MAX. | MIN.                | MAX. | MIN.                    | MAX. | MIN.                | MAX. |      |           |
| Read cycle time                      | t <sub>RC</sub>  | 70                      |      | 85                  |      | 100                     |      | 120                 |      | 150                     |      | 200                 |      | ns   | Note 1    |
| Address access time                  | t <sub>AA</sub>  |                         | 70   |                     | 85   |                         | 100  |                     | 120  |                         | 150  |                     | 200  | ns   |           |
| /CE1 access time                     | t <sub>CO1</sub> |                         | 70   |                     | 85   |                         | 100  |                     | 120  |                         | 150  |                     | 200  | ns   |           |
| CE2 access time                      | t <sub>CO2</sub> |                         | 70   |                     | 85   |                         | 100  |                     | 120  |                         | 150  |                     | 200  | ns   |           |
| /OE to output valid                  | t <sub>OE</sub>  |                         | 35   |                     | 40   |                         | 50   |                     | 60   |                         | 70   |                     | 100  | ns   |           |
| /LB, /UB to output valid             | t <sub>BA</sub>  |                         | 70   |                     | 85   |                         | 100  |                     | 120  |                         | 150  |                     | 200  | ns   |           |
| Output hold from address change      | t <sub>OH</sub>  | 10                      |      | 10                  |      | 10                      |      | 10                  |      | 10                      |      | 10                  |      | ns   | Note 2    |
| /CE1 to output in low impedance      | t <sub>LZ1</sub> | 10                      |      | 10                  |      | 10                      |      | 10                  |      | 10                      |      | 10                  |      | ns   |           |
| CE2 to output in low impedance       | t <sub>LZ2</sub> | 10                      |      | 10                  |      | 10                      |      | 10                  |      | 10                      |      | 10                  |      | ns   |           |
| /OE to output in low impedance       | t <sub>OLZ</sub> | 5                       |      | 5                   |      | 5                       |      | 5                   |      | 5                       |      | 5                   |      | ns   |           |
| /LB, /UB to output in low impedance  | t <sub>BLZ</sub> | 10                      |      | 10                  |      | 10                      |      | 10                  |      | 10                      |      | 10                  |      | ns   |           |
| /CE1 to output in high impedance     | t <sub>HZ1</sub> |                         | 25   |                     | 30   |                         | 35   |                     | 40   |                         | 50   |                     | 70   | ns   |           |
| CE2 to output in high impedance      | t <sub>HZ2</sub> |                         | 25   |                     | 30   |                         | 35   |                     | 40   |                         | 50   |                     | 70   | ns   |           |
| /OE to output in high impedance      | t <sub>OHZ</sub> |                         | 25   |                     | 30   |                         | 35   |                     | 40   |                         | 50   |                     | 70   | ns   |           |
| /LB, /UB to output in high impedance | t <sub>BHZ</sub> |                         | 25   |                     | 30   |                         | 35   |                     | 40   |                         | 50   |                     | 70   | ns   |           |

- Notes** 1. The output load is 1TTL + 50 pF (μPD442012L-BxxX) or 1TTL + 30 pF (μPD442012L-CxxX, -DxxX).  
2. The output load is 1TTL + 5 pF.

# Read Cycle Timing Chart



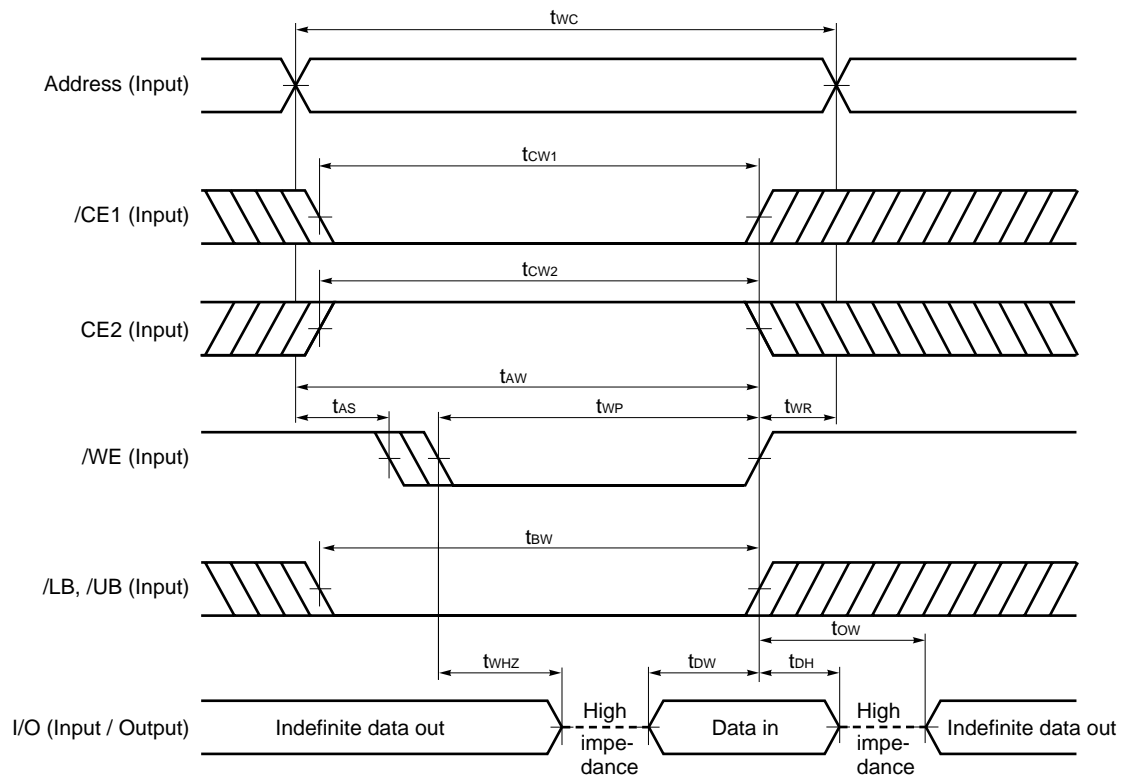
**Remark** In read cycle, /WE should be fixed to high level.

Write Cycle

| Parameter                          | Symbol           | V <sub>CC</sub> ≥ 2.7 V |      |                     |      | V <sub>CC</sub> ≥ 2.2 V |      |                     |      | V <sub>CC</sub> ≥ 1.8 V |      |                     |      | Unit | Condition |
|------------------------------------|------------------|-------------------------|------|---------------------|------|-------------------------|------|---------------------|------|-------------------------|------|---------------------|------|------|-----------|
|                                    |                  | μPD442012L<br>-B70X     |      | μPD442012L<br>-B85X |      | μPD442012L<br>-C10X     |      | μPD442012L<br>-C12X |      | μPD442012L<br>-D15X     |      | μPD442012L<br>-D20X |      |      |           |
|                                    |                  | MIN.                    | MAX. | MIN.                | MAX. | MIN.                    | MAX. | MIN.                | MAX. | MIN.                    | MAX. | MIN.                | MAX. |      |           |
| Write cycle time                   | t <sub>wc</sub>  | 70                      |      | 85                  |      | 100                     |      | 120                 |      | 150                     |      | 200                 |      | ns   |           |
| /CE1 to end of write               | t <sub>cw1</sub> | 55                      |      | 70                  |      | 80                      |      | 100                 |      | 120                     |      | 160                 |      | ns   |           |
| CE2 to end of write                | t <sub>cw2</sub> | 55                      |      | 70                  |      | 80                      |      | 100                 |      | 120                     |      | 160                 |      | ns   |           |
| /LB, /UB to end of write           | t <sub>bw</sub>  | 55                      |      | 70                  |      | 80                      |      | 100                 |      | 120                     |      | 160                 |      | ns   |           |
| Address valid to end of write      | t <sub>aw</sub>  | 55                      |      | 70                  |      | 80                      |      | 100                 |      | 120                     |      | 160                 |      | ns   |           |
| Address setup time                 | t <sub>as</sub>  | 0                       |      | 0                   |      | 0                       |      | 0                   |      | 0                       |      | 0                   |      | ns   |           |
| Write pulse width                  | t <sub>wP</sub>  | 50                      |      | 55                  |      | 60                      |      | 85                  |      | 100                     |      | 140                 |      | ns   |           |
| Write recovery time                | t <sub>wR</sub>  | 0                       |      | 0                   |      | 0                       |      | 0                   |      | 0                       |      | 0                   |      | ns   |           |
| Data valid to end of write         | t <sub>dW</sub>  | 30                      |      | 35                  |      | 40                      |      | 60                  |      | 80                      |      | 100                 |      | ns   |           |
| Data hold time                     | t <sub>dH</sub>  | 0                       |      | 0                   |      | 0                       |      | 0                   |      | 0                       |      | 0                   |      | ns   |           |
| /WE to output<br>in high impedance | t <sub>whZ</sub> |                         | 25   |                     | 30   |                         | 35   |                     | 40   |                         | 50   |                     | 70   | ns   | Note      |
| Output active<br>from end of write | t <sub>ow</sub>  | 5                       |      | 5                   |      | 5                       |      | 5                   |      | 5                       |      | 5                   |      | ns   |           |

**Note** The output load is 1TTL + 5 pF.

Write Cycle Timing Chart 1 (/WE Controlled)



**Cautions** 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

★

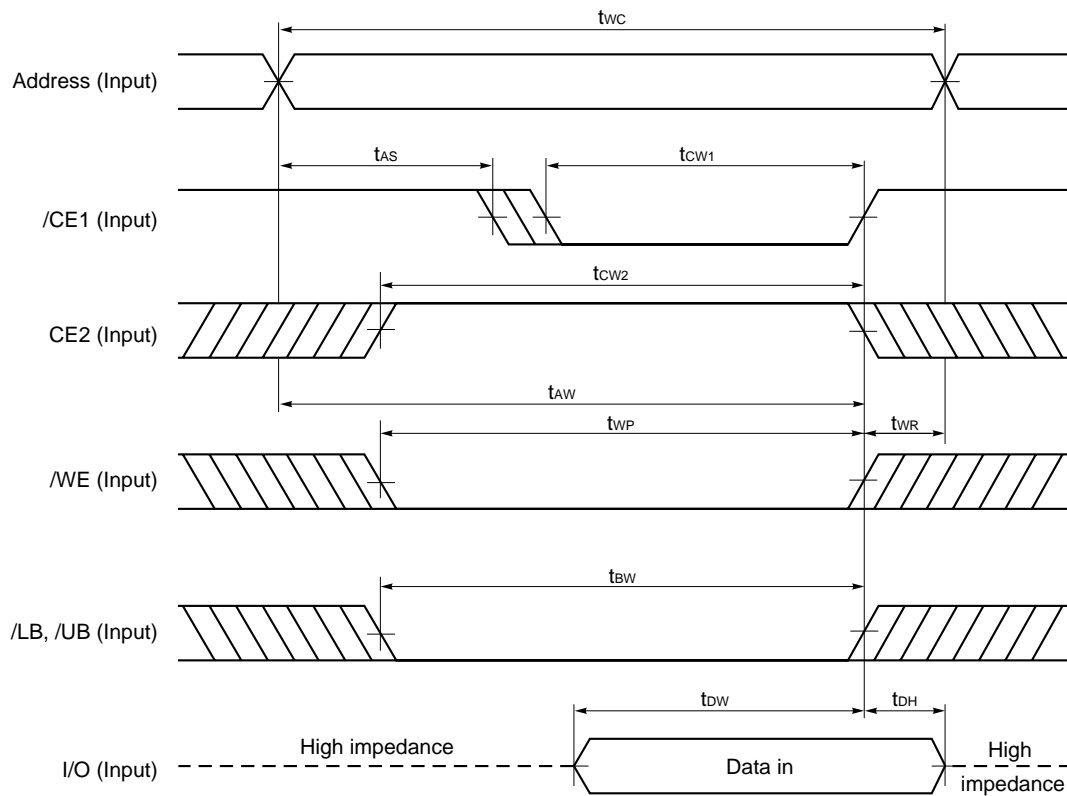
2. Do not input data to the I/O pins while they are in the output state.

**Remarks** 1. Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)



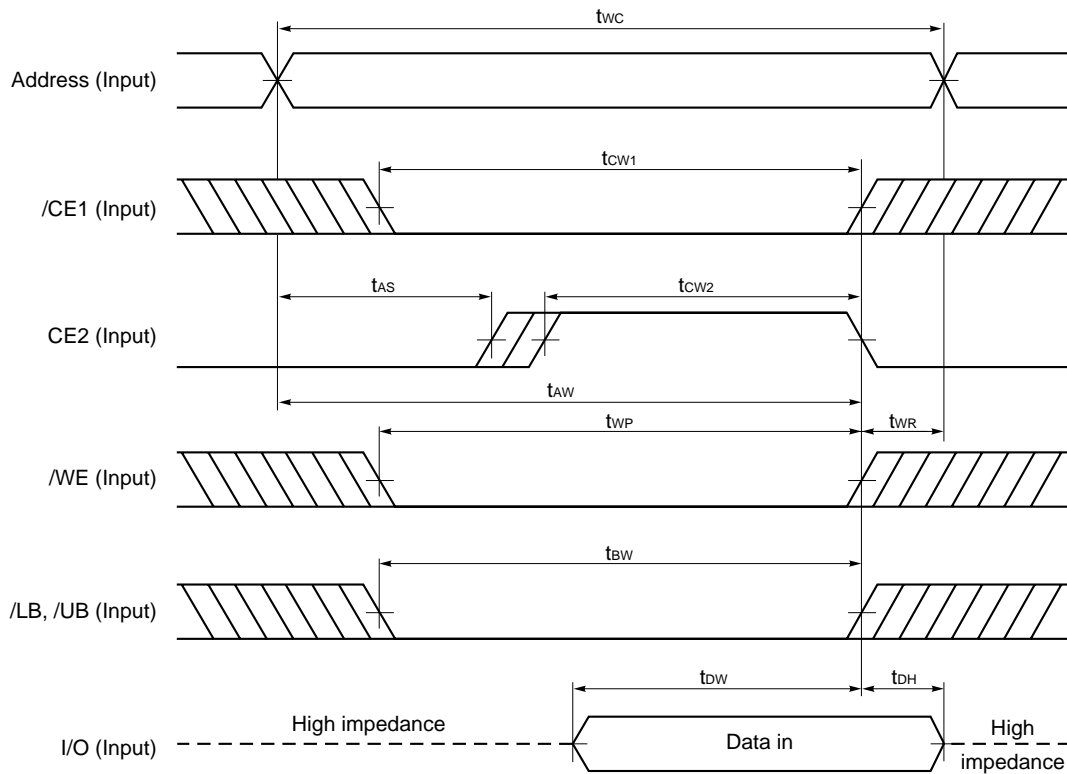
**Cautions** 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

★

2. Do not input data to the I/O pins while they are in the output state.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



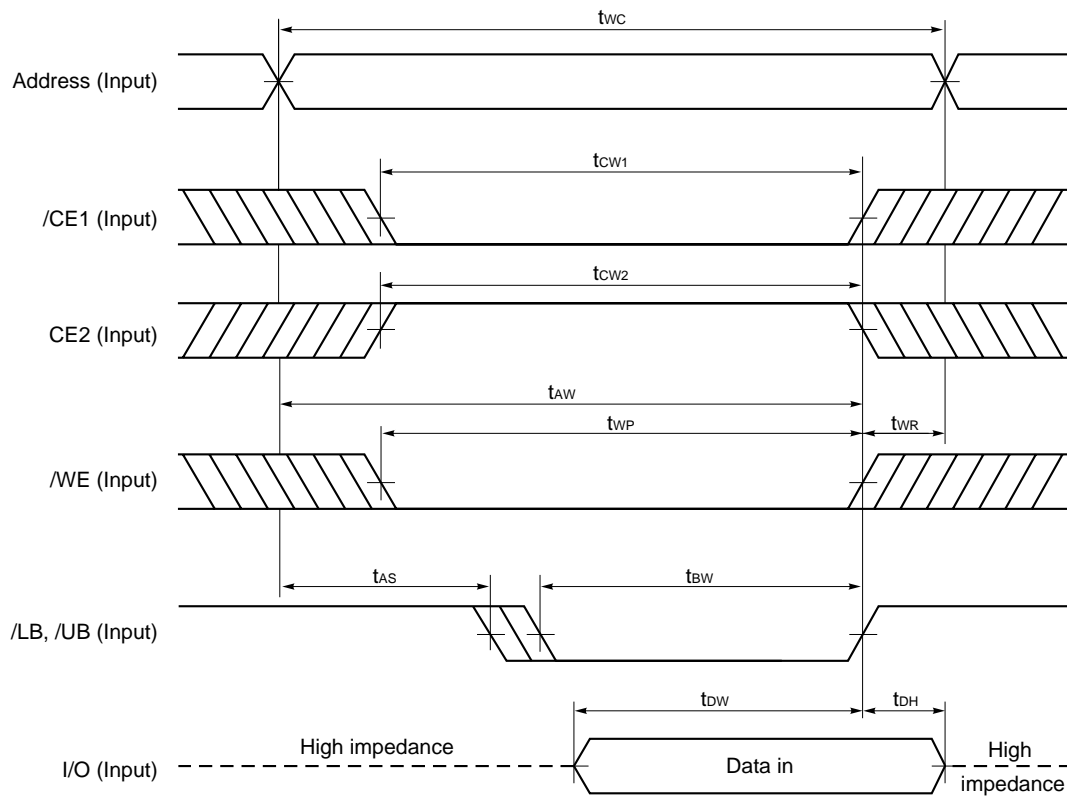
**Cautions** 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

★

2. Do not input data to the I/O pins while they are in the output state.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 4 (/LB, /UB Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
  2. Do not input data to the I/O pins while they are in the output state.

**Remark** Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Low V<sub>CC</sub> Data Retention Characteristics (T<sub>A</sub> = -25 to +85 °C)

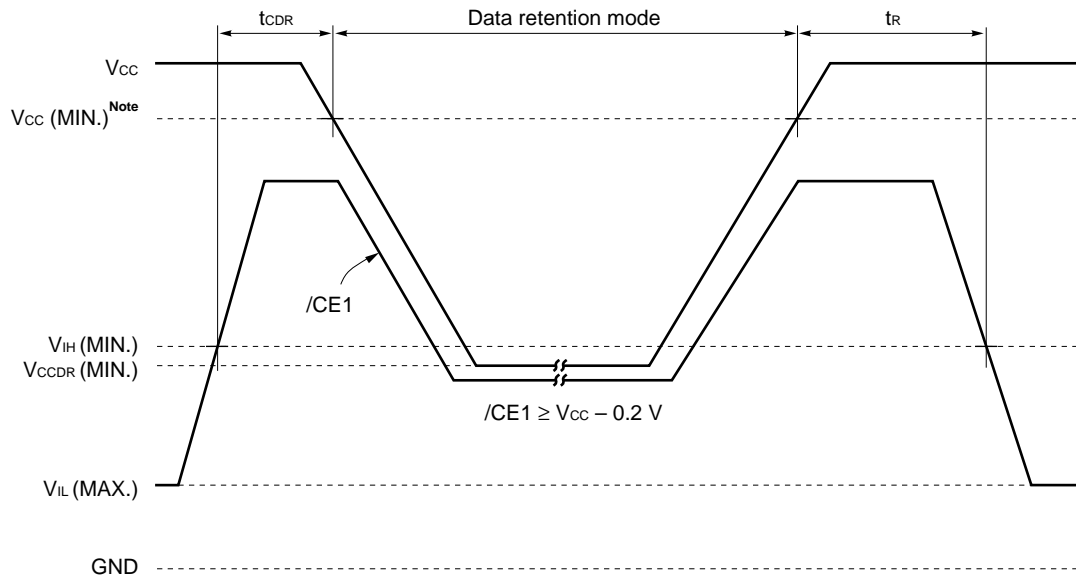
| Parameter                                     | Symbol             | Test Condition   | V <sub>CC</sub> ≥ 2.7 V         |      |      | V <sub>CC</sub> ≥ 2.2 V         |      |      | V <sub>CC</sub> ≥ 1.8 V         |      |      | Unit |
|---|--------------------|--|---------------------------------|------|------|---------------------------------|------|------|---------------------------------|------|------|------|
|   |                    |  | μPD442012L<br>-BxxX             |      |      | μPD442012L<br>-CxxX             |      |      | μPD442012L<br>-DxxX             |      |      |      |
|   |                    |  | MIN.                            | TYP. | MAX. | MIN.                            | TYP. | MAX. | MIN.                            | TYP. | MAX. |      |
| Data retention<br>supply voltage              | V <sub>CCDR1</sub> | /CE1 ≥ V <sub>CC</sub> – 0.2 V,<br>CE2 ≥ V <sub>CC</sub> – 0.2 V   | 2.0                             |      | 3.6  | 1.5                             |      | 3.6  | 1.5                             |      | 3.6  | V    |
|   | V <sub>CCDR2</sub> | CE2 ≤ 0.2 V  | 2.0                             |      | 3.6  | 1.5                             |      | 3.6  | 1.5                             |      | 3.6  |      |
|   | V <sub>CCDR3</sub> | /LB = /UB ≥ V <sub>CC</sub> – 0.2 V,<br>/CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> – 0.2 V                          | 2.0                             |      | 3.6  | 1.5                             |      | 3.6  | 1.5                             |      | 3.6  |      |
| Data retention<br>supply current              | I <sub>CCDR1</sub> | V <sub>CC</sub> = 3.0 V, /CE1 ≥ V <sub>CC</sub> – 0.2 V,<br>CE2 ≥ V <sub>CC</sub> – 0.2 V or CE2 ≤ 0.2 V     |                                 | 0.3  | 4    |                                 | 0.3  | 4    |                                 | 0.3  | 4    | μA   |
|   | I <sub>CCDR2</sub> | V <sub>CC</sub> = 3.0 V, CE2 ≤ 0.2 V   |                                 | 0.3  | 4    |                                 | 0.3  | 4    |                                 | 0.3  | 4    |      |
|   | I <sub>CCDR3</sub> | V <sub>CC</sub> = 3.0 V, /LB = /UB ≥ V <sub>CC</sub> – 0.2 V,<br>/CE1 ≤ 0.2 V, CE2 ≥ V <sub>CC</sub> – 0.2 V |                                 | 0.3  | 4    |                                 | 0.3  | 4    |                                 | 0.3  | 4    |      |
| Chip deselection<br>to data retention<br>mode | t <sub>CDR</sub>   |  | 0                               |      |      | 0                               |      |      | 0                               |      |      | ns   |
| Operation<br>recovery time                    | t <sub>R</sub>     |  | t <sub>RC</sub> <sup>Note</sup> |      |      | t <sub>RC</sub> <sup>Note</sup> |      |      | t <sub>RC</sub> <sup>Note</sup> |      |      | ns   |

**Note** t<sub>RC</sub> : Read cycle time



## Data Retention Timing Chart

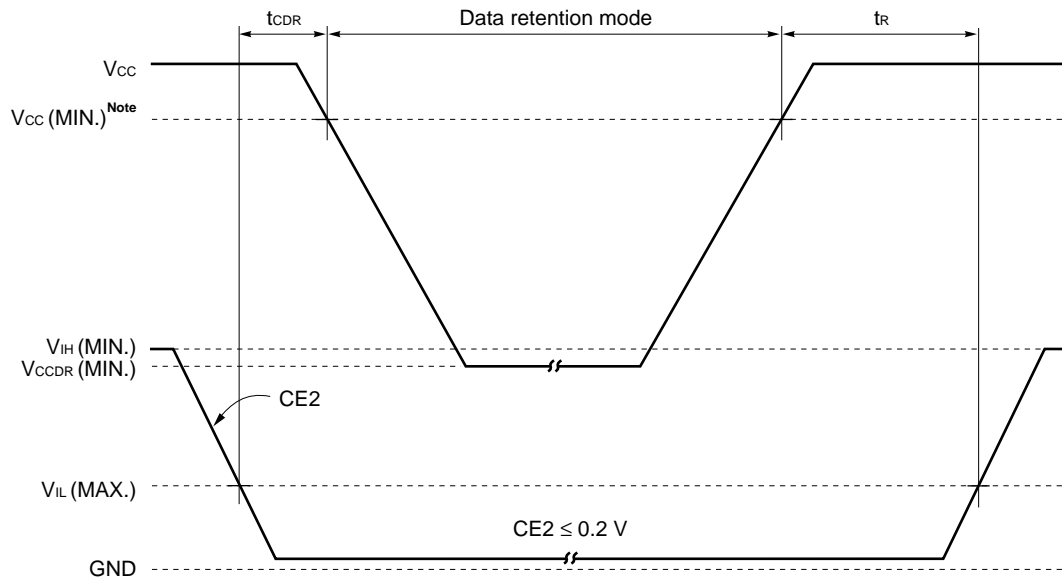
### (1) /CE1 Controlled



**Note** B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

**Remark** On the data retention mode by controlling  $\overline{\text{CE1}}$ , the input level of CE2 must be  $\geq V_{\text{CC}} - 0.2 \text{ V}$  or  $\leq 0.2 \text{ V}$ .  
The other pins (Address, I/O,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ ) can be in high impedance state.

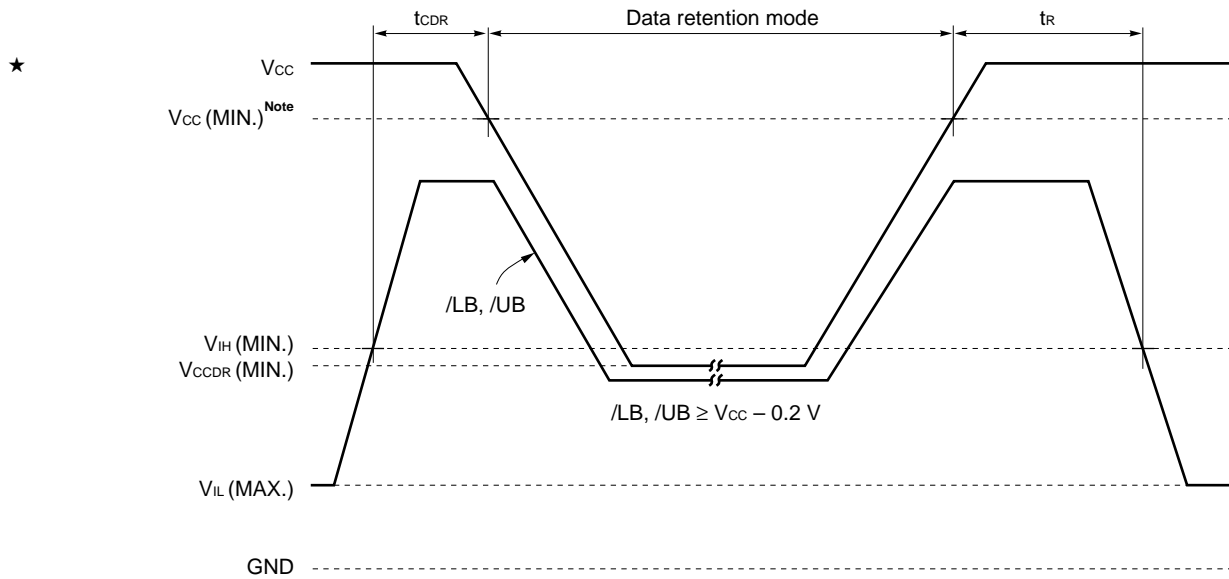
### (2) CE2 Controlled



**Note** B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

**Remark** On the data retention mode by controlling CE2, the other pins ( $\overline{\text{CE1}}$ , Address, I/O,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ ) can be in high impedance state.

(3) /LB, /UB Controlled

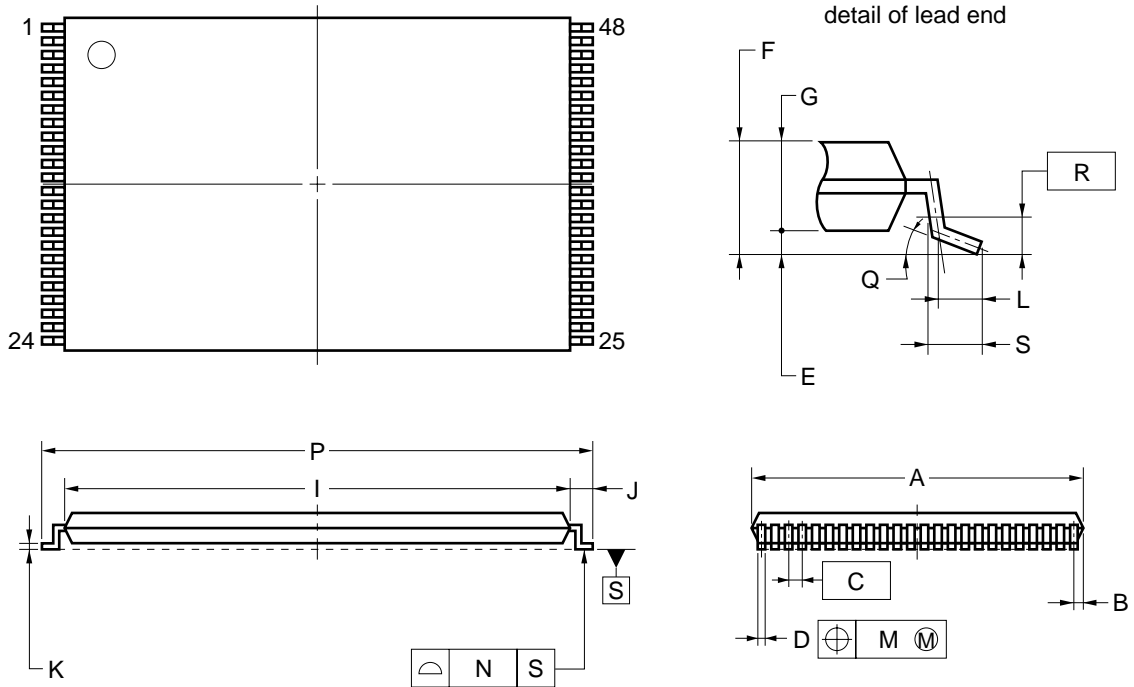


**Note** B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

**Remark** On the data retention mode by controlling /LB and /UB, the input level of /CE1 and CE2 must be  $\geq V_{cc} - 0.2 \text{ V}$  or  $\leq 0.2 \text{ V}$ . The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

★ Package Drawing

48-PIN PLASTIC TSOP(I) (12x18)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

| ITEM | MILLIMETERS  |
|------|--------------|
| A    | 12.0±0.1     |
| B    | 0.45 MAX.    |
| C    | 0.5 (T.P.)   |
| D    | 0.22±0.05    |
| E    | 0.1±0.05     |
| F    | 1.2 MAX.     |
| G    | 1.0±0.05     |
| I    | 16.4±0.1     |
| J    | 0.8±0.2      |
| K    | 0.145±0.05   |
| L    | 0.5          |
| M    | 0.10         |
| N    | 0.10         |
| P    | 18.0±0.2     |
| Q    | 3°+5°<br>-3° |
| R    | 0.25         |
| S    | 0.60±0.15    |

S48GY-50-MJH1-1

## Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD442012L-X.

### ★ Types of Surface Mount Device

$\mu$ PD442012LGY-BxxX-MJH: 48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

$\mu$ PD442012LGY-CxxX-MJH: 48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

$\mu$ PD442012LGY-DxxX-MJH: 48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

[ MEMO ]

[ MEMO ]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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