

4M-BIT CMOS FAST SRAM 1M-WORD BY 4-BIT

Description

The μPD434004A is a high speed, low power, 4,194,304 bits (1,048,576 words by 4 bits) CMOS static RAM.

Operating supply voltage is 5.0 V ± 0.5 V.

The μPD434004A is packaged in a 32-pin plastic SOJ.

Features

- 1,048,576 words by 4 bits organization
- Fast access time : 15, 17, 20 ns (MAX.)
- Output Enable input for easy application
- Single +5.0 V power supply

Ordering Information

Part number	Package	Access time ns (MAX.)	Supply current mA (MAX.)	
			At operating	At standby
μPD434004ALE-15	32-pin plastic SOJ (10.16 mm (400))	15	140	10
μPD434004ALE-17		17	130	
μPD434004ALE-20		20	120	

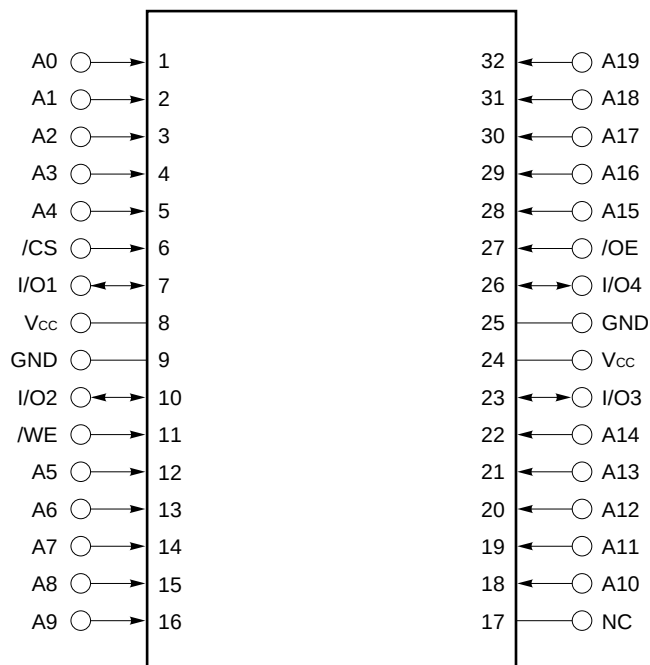
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ Pin Configuration (Marking Side)

/xxx indicates active low signal.

32-pin plastic SOJ (10.16 mm (400))

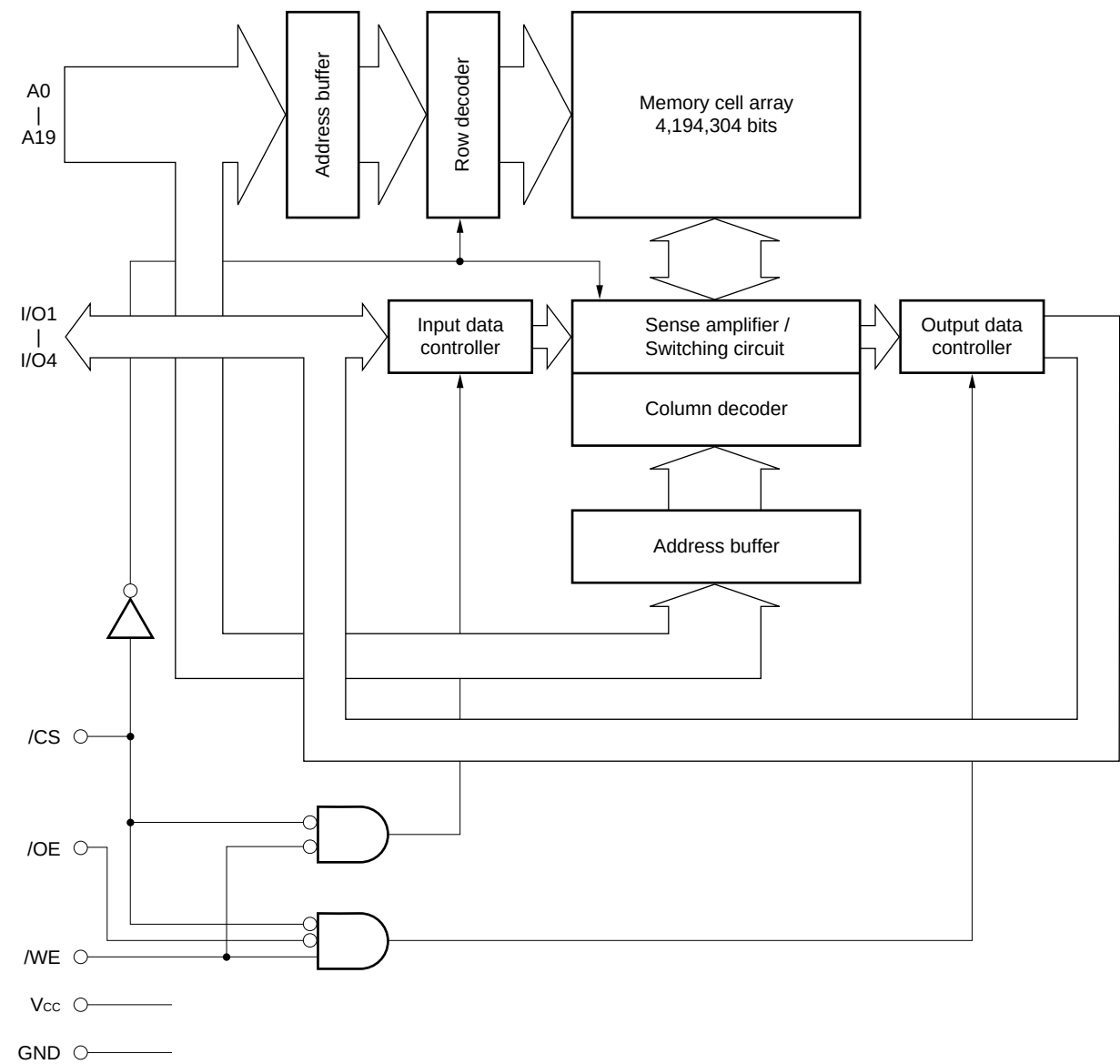
[μPD434004ALE]



- A0 - A19 : Address Inputs
- I/O1 - I/O4 : Data Inputs / Outputs
- /CS : Chip Select
- /WE : Write Enable
- /OE : Output Enable
- Vcc : Power supply
- GND : Ground
- NC : No connection

Remark Refer to **Package Drawing** for the 1-pin index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I _{SB}
L	L	H	Read	D _{OUT}	I _{CC}
L	×	L	Write	D _{IN}	
L	H	H	Output disable	High impedance	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V _{CC}		−0.5 ^{Note} to +7.0	V
Input / Output voltage	V _I		−0.5 ^{Note} to V _{CC} +0.5	V
Operating ambient temperature	T _A		0 to 70	°C
Storage temperature	T _{stg}		−55 to +125	°C

Note −2.0 V (MIN.) (pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		4.5	5.0	5.5	V
High level input voltage	V _{IH}		2.2		V _{CC} +0.5	V
Low level input voltage	V _{IL}		−0.5 ^{Note}		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Note −2.0 V (MIN.) (pulse width : 2 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	$V_{IN} = 0\text{ V to }V_{CC}$	-2		+2	μA
Output leakage current	I_{LO}	$V_{I/O} = 0\text{ V to }V_{CC}$, $/CS = V_{IH}$ or $/OE = V_{IH}$ or $/WE = V_{IL}$	-2		+2	μA
Operating supply current	I_{CC}	$/CS = V_{IL}$, $I_{I/O} = 0\text{ mA}$, Minimum cycle time	Cycle time : 15 ns		140	mA
			Cycle time : 17 ns		130	
			Cycle time : 20 ns		120	
Standby supply current	I_{SB}	$/CS = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}			50	mA
	I_{SB1}	$/CS \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			10	
High level output voltage	V_{OH}	$I_{OH} = -4.0\text{ mA}$	2.4			V
Low level output voltage	V_{OL}	$I_{OL} = +8.0\text{ mA}$			0.4	V

Remark V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

Capacitance ($T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

Remarks 1. V_{IN} : Input voltage

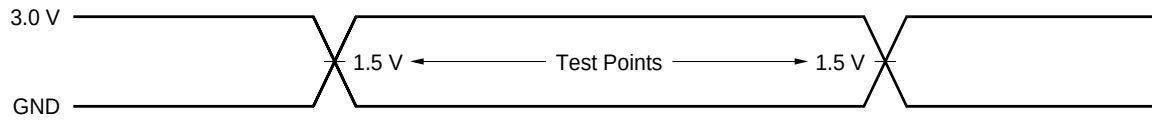
$V_{I/O}$: Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

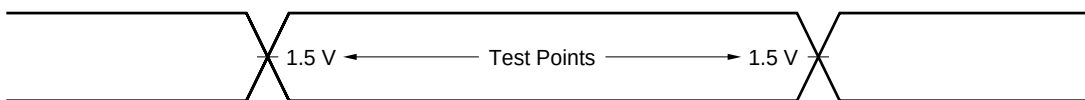
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)



Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.

Figure 1

(for t_{AA} , t_{ACS} , t_{OE} , t_{OH})

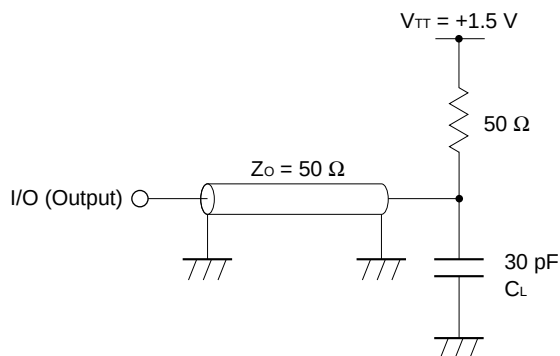
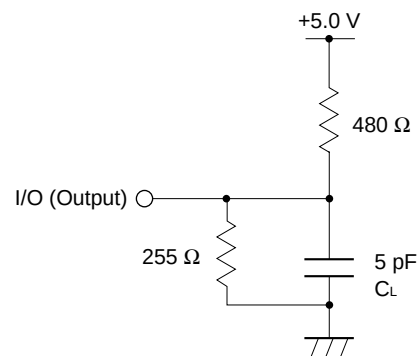


Figure 2

(for t_{CLZ} , t_{OLZ} , t_{CHZ} , t_{OHZ} , t_{WHZ} , t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

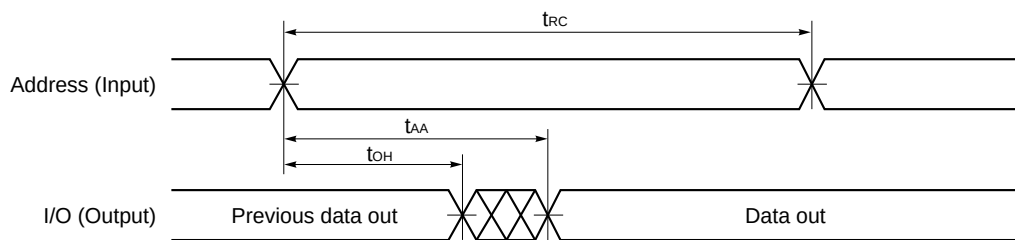
Parameter	Symbol	μ PD434004A-15		μ PD434004A-17		μ PD434004A-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	15		17		20		ns	
Address access time	t_{AA}		15		17		20	ns	1
/CS access time	t_{ACS}		15		17		20	ns	
/OE access time	t_{OE}		7		8		10	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
/CS to output in low impedance	t_{CLZ}	3		3		3		ns	2, 3
/OE to output in low impedance	t_{OLZ}	0		0		0		ns	
/CS to output in high impedance	t_{CHZ}		7		8		8	ns	
/OE to output hold in high impedance	t_{OHZ}		7		8		8	ns	

Notes 1. See the output load shown in **Figure 1**.

2. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

3. These parameters are periodically sampled and not 100% tested.

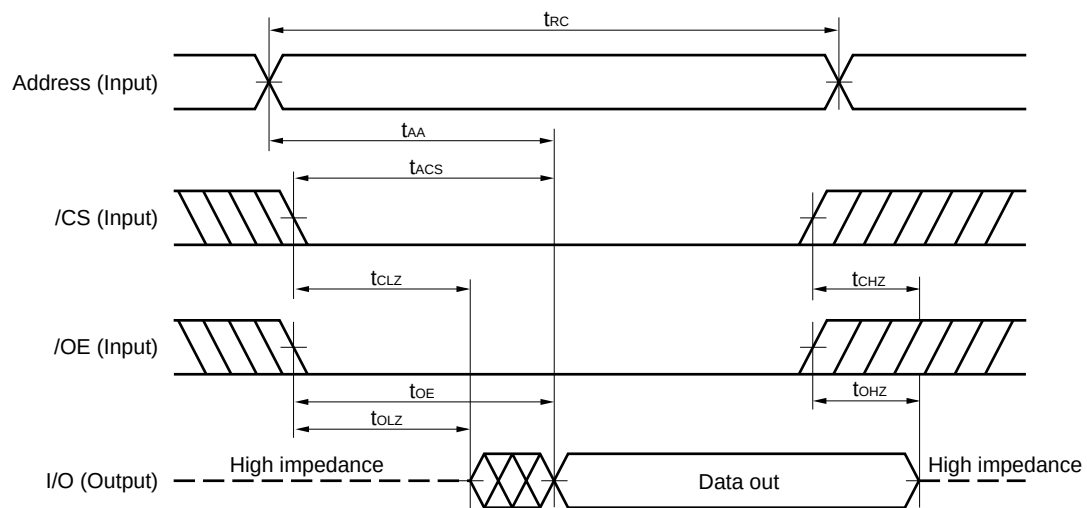
Read Cycle Timing Chart 1 (Address Access)



Remarks 1. In read cycle, /WE should be fixed to high level.

2. /CS = /OE = V_{IL}

Read Cycle Timing Chart 2 (/CS Access)



Caution Address valid prior to or coincident with /CS low level input.

Remark In read cycle, /WE should be fixed to high level.

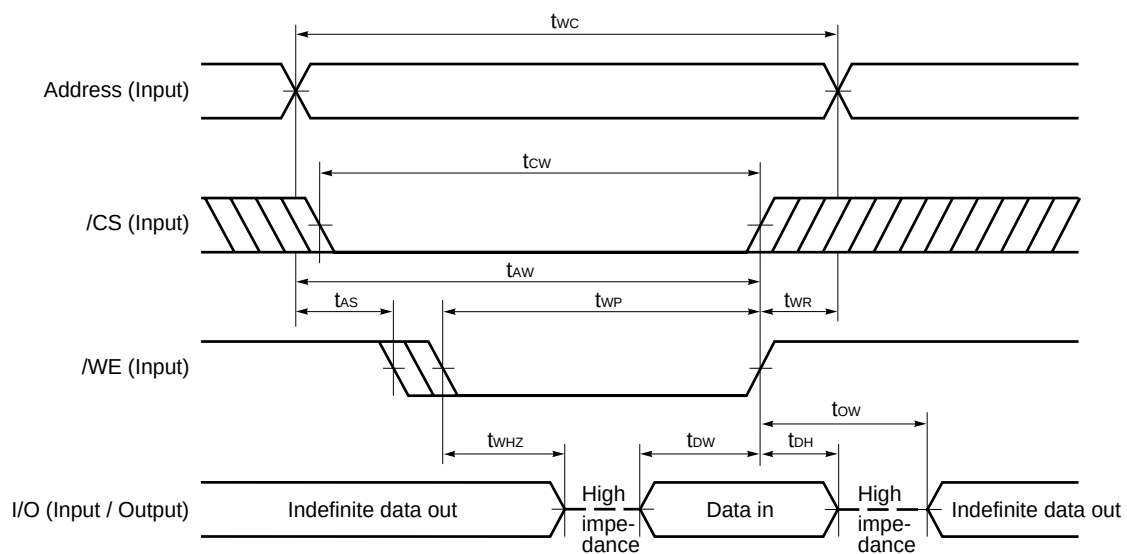
Write Cycle

Parameter	Symbol	μPD434004A-15		μPD434004A-17		μPD434004A-20		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{wc}	15		17		20		ns	
/CS to end of write	t_{cw}	10		11		12		ns	
Address valid to end of write	t_{aw}	10		11		12		ns	
Write pulse width	t_{wp}	10		11		12		ns	
Data valid to end of write	t_{dw}	7		8		9		ns	
Data hold time	t_{dh}	0		0		0		ns	
Address setup time	t_{as}	0		0		0		ns	
Write recovery time	t_{wr}	1		1		1		ns	
/WE to output in high impedance	t_{whz}		7		8		8	ns	1, 2
Output active from end of write	t_{ow}	3		3		3		ns	

Notes 1. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

2. These parameters are periodically sampled and not 100% tested.

Write Cycle Timing Chart 1 (/WE Controlled)

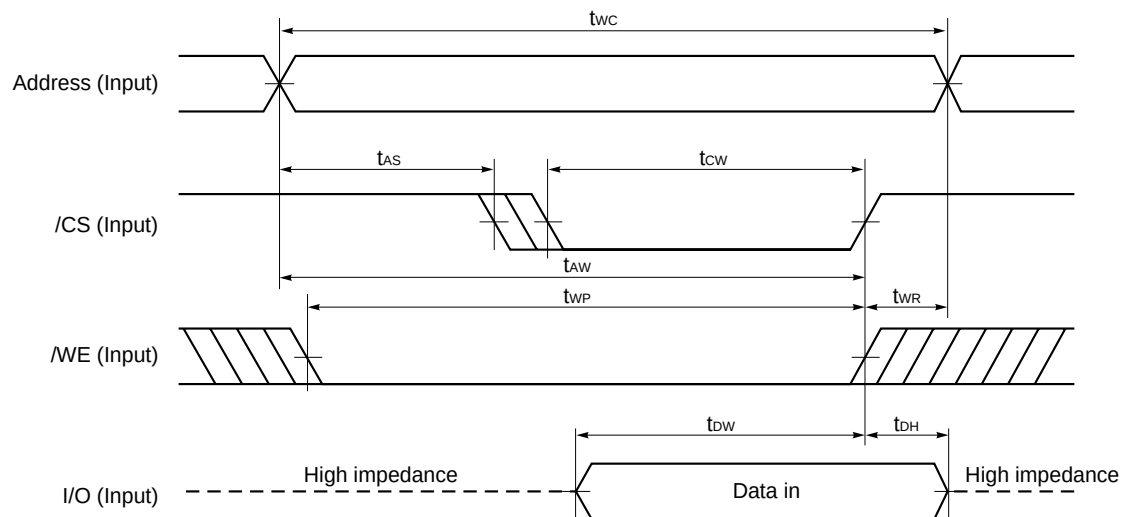


Caution /CS or /WE should be fixed to high level during address transition.

Remarks 1. Write operation is done during the overlap time of a low level /CS and a low level /WE.

- During t_{whz} , I/O pins are in the output state, therefore the input signals must not be applied to the output.
- When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CS Controlled)

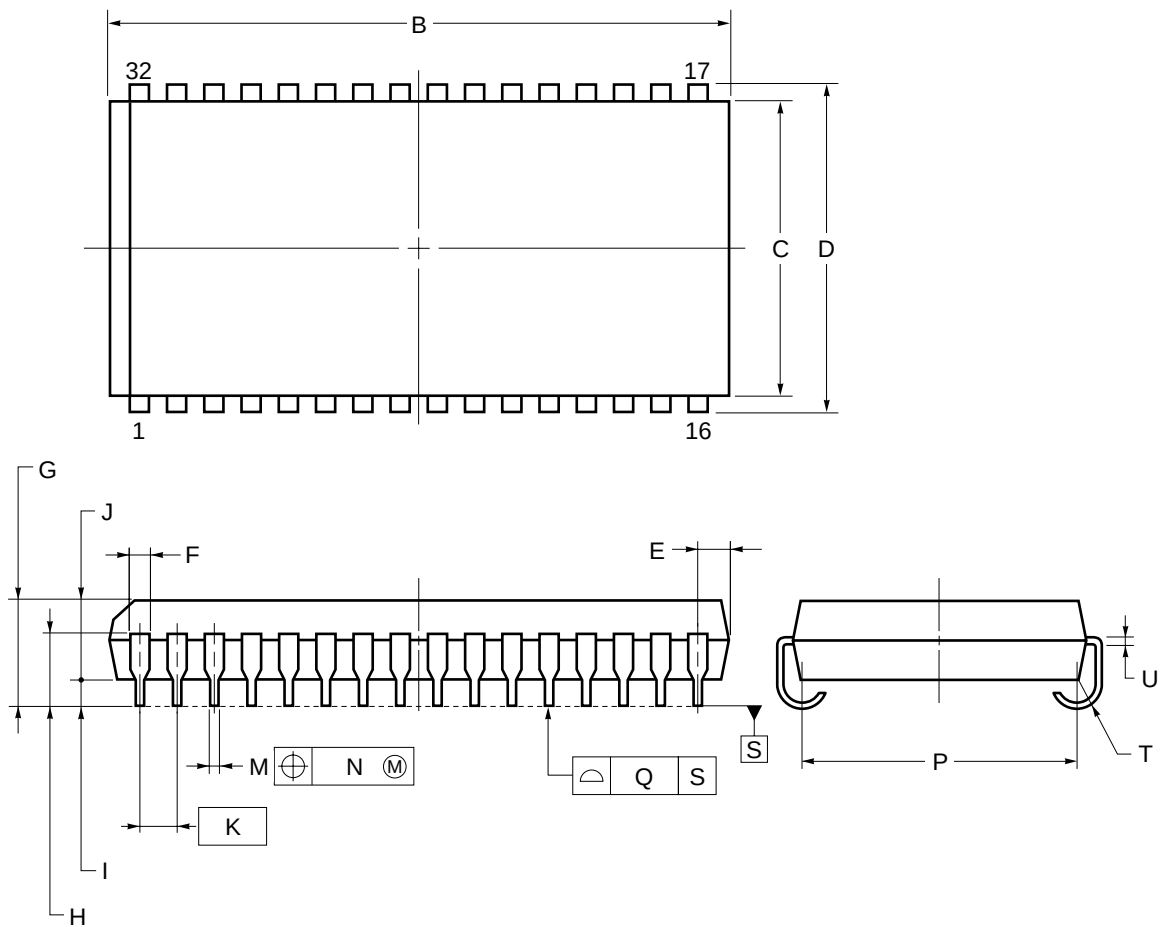


Caution /CS or /WE should be fixed to high level during address transition.

Remark Write operation is done during the overlap time of a low level /CS and a low level /WE.

★ Package Drawing

32-PIN PLASTIC SOJ (10.16mm (400))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
B	21.26±0.2
C	10.16
D	11.18±0.2
E	1.005±0.1
F	0.74
G	3.5±0.2
H	2.545±0.2
I	0.8 MIN.
J	2.6
K	1.27(T.P.)
M	0.40±0.10
N	0.12
P	9.4±0.20
Q	0.1
T	R0.85
U	0.20 ^{+0.10} _{-0.05}
P32LE-400A-1	

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD434004A.

Type of Surface Mount Device

μ PD434004ALE : 32-pin plastic SOJ (10.16 mm (400))

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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