NEC

MOS INTEGRATED CIRCUIT
μPD43257B

256K-BIT CMOS STATIC RAM
32K-WORD BY 8-BIT

Description

The μPD43257B is a high speed, low power, and 262,144 bits (32,768 words by 8 bits) CMOS static RAM. Battery backup is available. And the μPD43257B has two chip enable pins (/CE1, CE2) to extend the capacity. The μPD43257B is packed in 28-pin plastic DIP and 28-pin plastic SOP.

Features

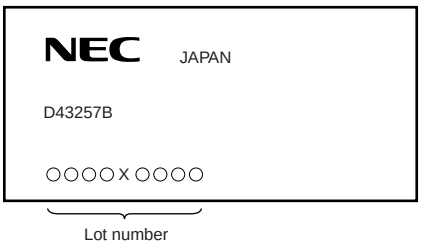
- 32,768 words by 8 bits organization
- Fast access time: 70, 85 ns (MAX.)
- Low V_{CC} data retention: 2.0 V (MIN.)
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.) Note
μPD43257B-xxL	70, 85	4.5 to 5.5	0 to 70	45	50	3
μPD43257B-xxLL				45	15	2

Note $T_A \leq 40$ °C, $V_{CC} = 3.0$ V

Version X

This Data sheet can be applied to the version X. This version is identified with its lot number. Letter X in the fifth character position in a lot number signifies version X.



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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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Printed in Japan

The mark ★ shows major revised points.

Ordering Information

Part number	Package	Access time	Supply current μA (MAX.)		Remark
		ns (MAX.)	At standby	At data retention [Note]	
μPD43257BCZ-70L	28-PIN PLASTIC DIP	70	50	3	L version
μPD43257BCZ-85L	(15.24 mm (600))	85			
μPD43257BCZ-70LL		70	15	2	LL version
μPD43257BCZ-85LL		85			
μPD43257BGU-70L	28-PIN PLASTIC SOP	70	50	3	L version
μPD43257BGU-85L	(11.43 mm (450))	85			
μPD43257BGU-70LL		70	15	2	LL version
μPD43257BGU-85LL		85			

Note $T_A \leq 40$ °C, $V_{CC} = 3.0$ V

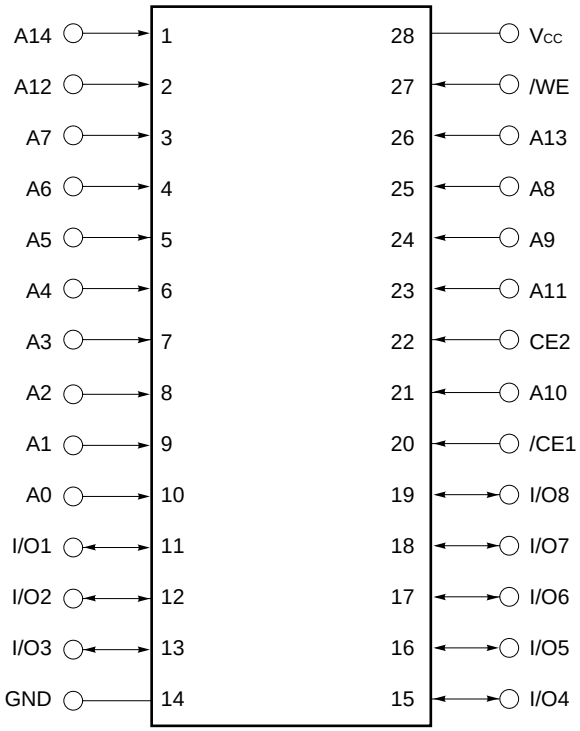
Pin Configurations (Marking Side)

/xxx indicates active low signal.

28-PIN PLASTIC DIP (15.24 mm (600))

[μPD43257BCZ-xxL]

[μPD43257BCZ-xxLL]



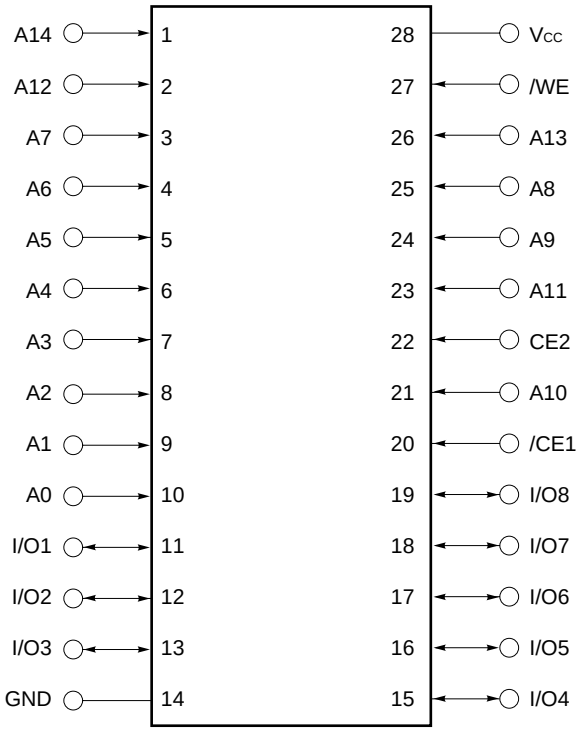
A0 - A14	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1	:	Chip Enable 1
CE2	:	Chip Enable 2
/WE	:	Write Enable
V_{CC}	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin marking.

28-PIN PLASTIC SOP (11.43 mm (450))

[μPD43257BGU-xxL]

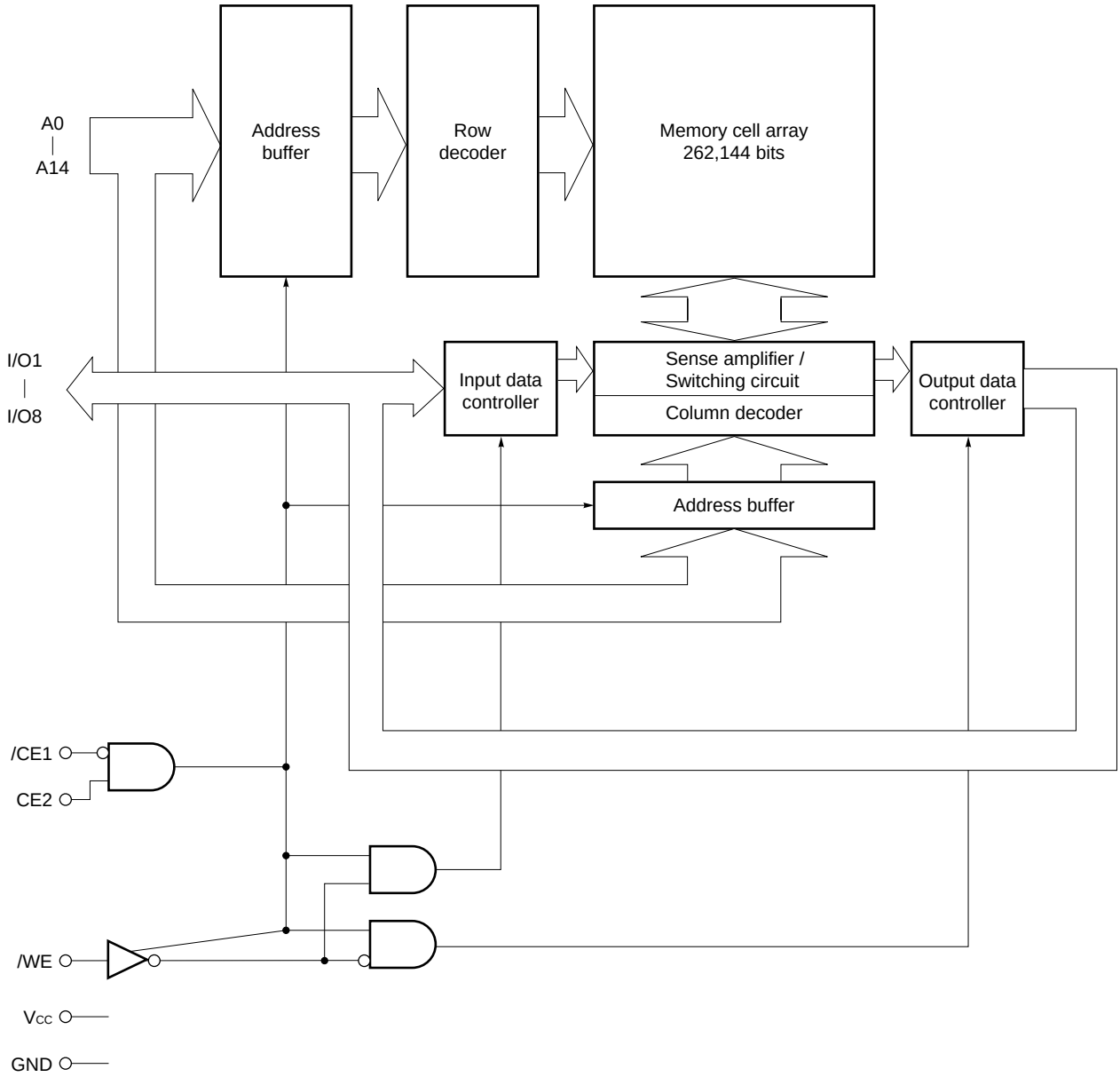
[μPD43257BGU-xxLL]



A0 - A14	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1	:	Chip Enable 1
CE2	:	Chip Enable 2
/WE	:	Write Enable
V_{CC}	:	Power supply
GND	:	Ground

Remark Refer to **Package Drawings** for the 1-pin marking.

Block Diagram



Truth Table

/CE1	CE2	/WE	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
×	L	×			
L	H	H	Read	D_{OUT}	I_{CCA}
L	H	L	Write	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 [Note] to +7.0	V
Input / Output voltage	V_T		–0.5 [Note] to V_{CC} + 0.5	V
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 50 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.2		V_{CC}+0.5	V
Low level input voltage	V_{IL}		–0.3 [Note]		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Note –3.0 V (MIN.) (Pulse width: 50 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			5	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		μPD43257B-xxL			μPD43257B-xxLL			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL}		–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH}, Minimum cycle time, $I_{I/O}$ = 0 mA	μPD43257B-70			45			45	mA
			μPD43257B-85			45			45	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA				10			10	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V				10			10	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL},				3			3	mA
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V			1.0	50		0.5	15	μA
	I_{SB2}	CE2 ≤ 0.2 V			1.0	50		0.5	15	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA		2.4			2.4			V
	V_{OH2}	I_{OH} = –0.1 mA		V_{CC}–0.5			V_{CC}–0.5			
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA				0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

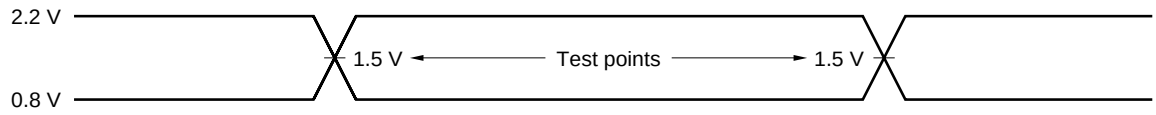
2. These DC characteristics are in common regardless of package types and access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

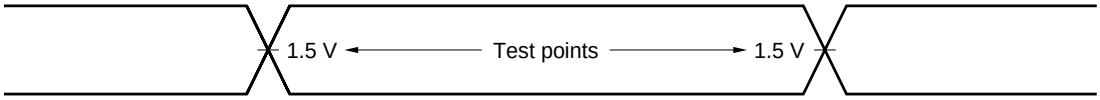
AC Test Conditions

[μPD43257B-70L, μPD43257B-85L, μPD43257B-70LL, μPD43257B-85LL]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics with notes should be measured with the output load shown in **Figure 1** and **Figure 2**.

Figure 1

(t_{AA}, t_{CO1}, t_{CO2}, t_{OH})

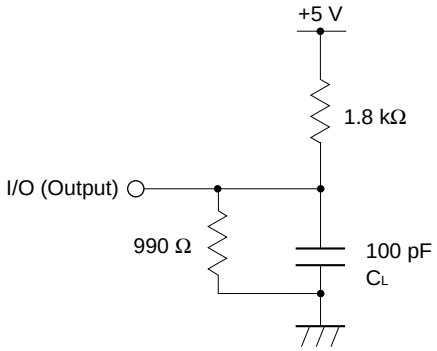
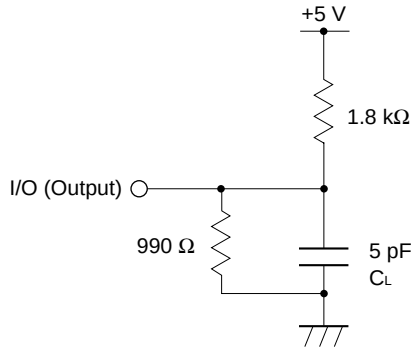


Figure 2

(t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{WHZ}, t_{OW})



Remark C_L includes capacitance of the probe and jig, and stray capacitance.

Read Cycle

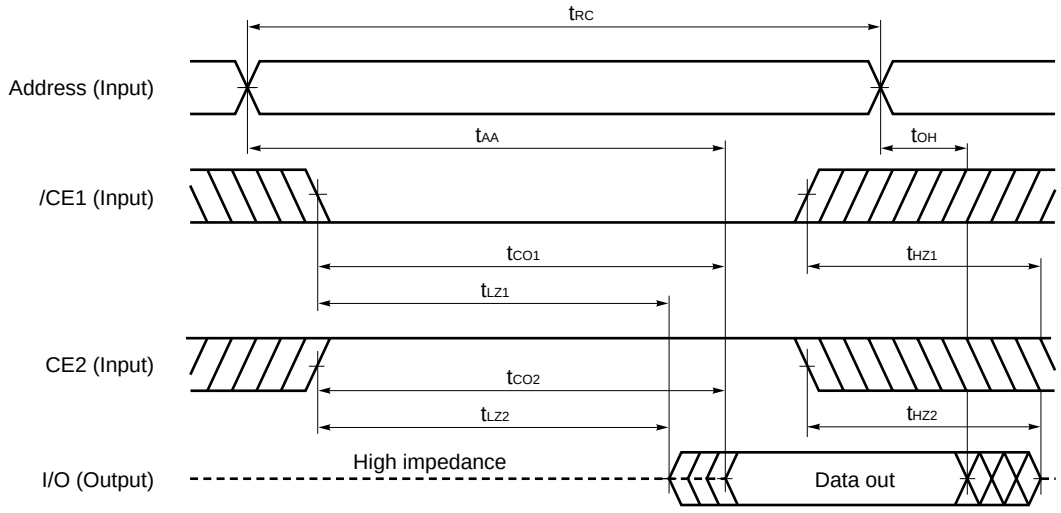
Parameter	Symbol	μPD43257B-70		μPD43257B-85		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		ns	
Address access time	t_{AA}		70		85	ns	**Note 1**
/CE1 access time	t_{CO1}		70		85	ns	
CE2 access time	t_{CO2}		70		85	ns	
Output hold from address change	t_{OH}	10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		ns	**Note 2**
CE2 to output in low impedance	t_{LZ2}	10		10		ns	
/CE1 to output in high impedance	t_{HZ1}		30		30	ns	
CE2 to output in high impedance	t_{HZ2}		30		30	ns	

Notes 1. See the output load shown in **Figure 1**.

2. See the output load shown in **Figure 2**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

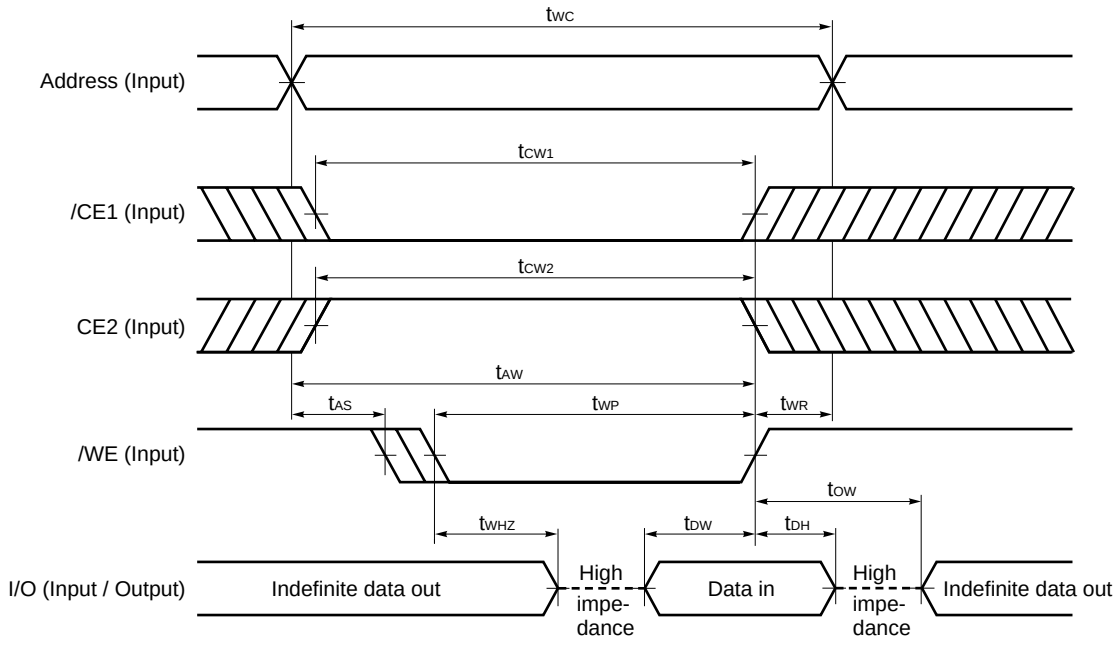
Write Cycle

Parameter	Symbol	μPD43257B-70		μPD43257B-85		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		ns	
/CE1 to end of write	t_{CW1}	50		70		ns	
CE2 to end of write	t_{CW2}	50		70		ns	
Address valid to end of write	t_{AW}	50		70		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	55		65		ns	
Write recovery time	t_{WR}	0		0		ns	
Data valid to end of write	t_{DW}	30		35		ns	
Data hold time	t_{DH}	0		0		ns	
/WE to output in high impedance	t_{WHZ}		30		30	ns	**Note**
Output active from end of write	t_{OW}	10		10		ns	

Note See the output load shown in **Figure 2**.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

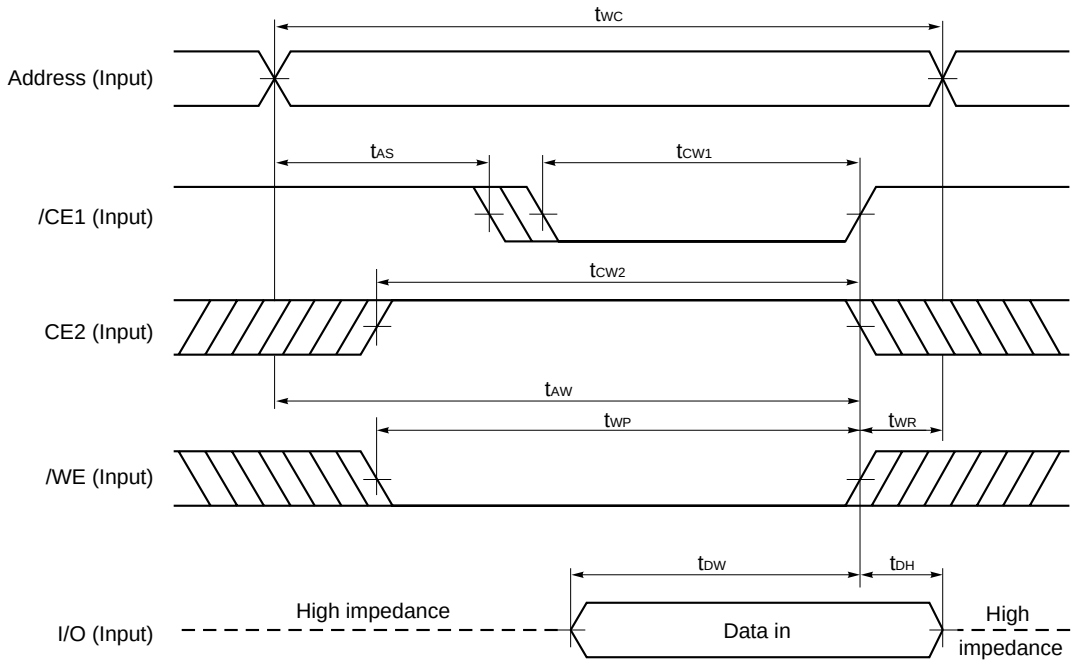
★ **2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.**

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

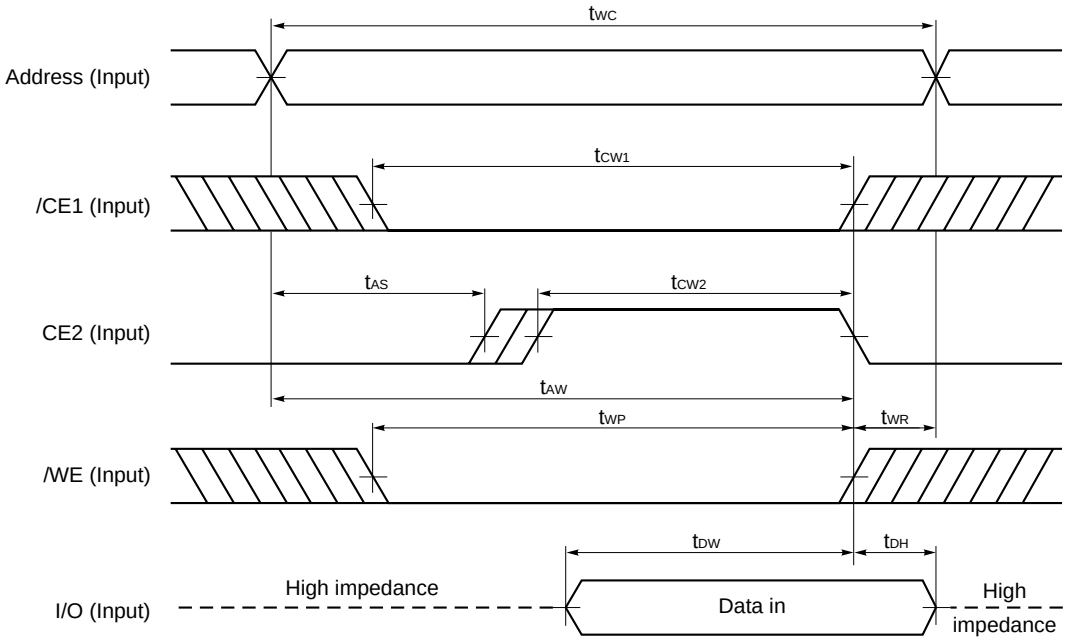


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

★ **2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.**

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

★ **2. When I/O pins are in the output state, therefore the input signals must not be applied to the output.**

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Low V_{CC} Data Retention Characteristics (T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	μPD43257B-xxL			μPD43257B-xxLL			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	2.0		5.5	2.0		5.5	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		5.5	2.0		5.5	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V		0.5	20 Note1		0.5	7 Note2	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.5	20 Note1		0.5	7 Note2	
Chip deselection to data retention mode	t_{CDR}		0			0			ns
Operation recovery time	t_R		5			5			ms

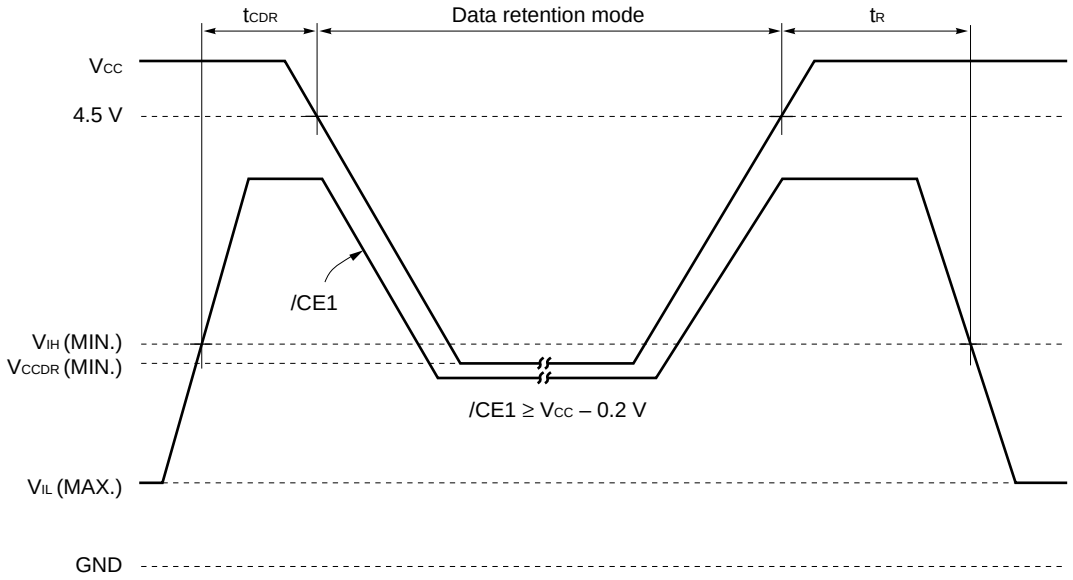
Notes 1. 3 μA (T_A ≤ 40 °C)

2. 2 μA (T_A ≤ 40 °C), 1 μA (T_A ≤ 25 °C)

Data Retention Timing Chart

(1) /CE1 Controlled

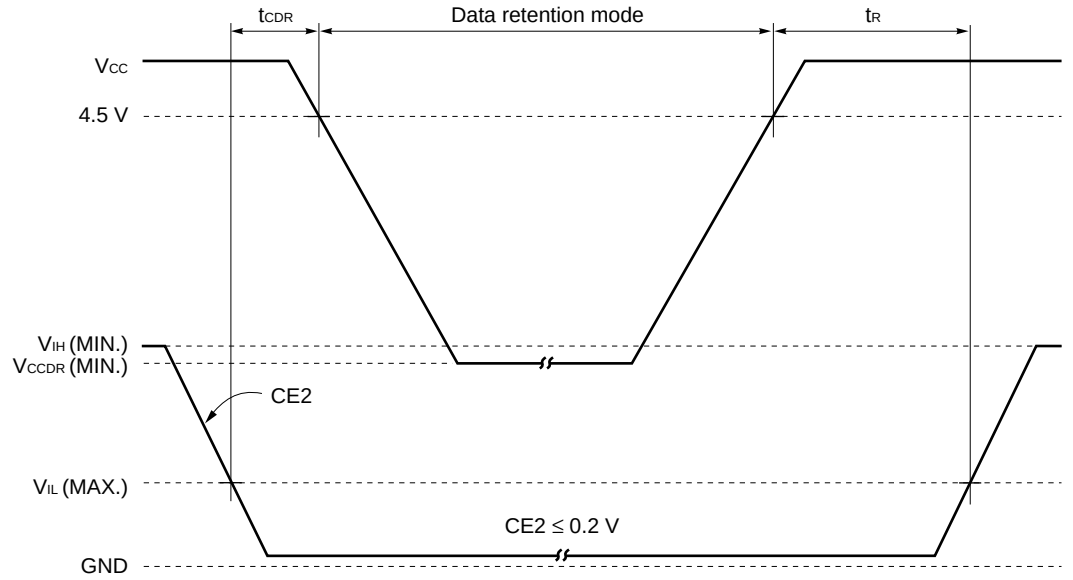
★



Remark On the data retention mode by controlling /CE1, the input level of CE2 must be CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V. The other pins (Address, I/O, /WE) can be in high impedance state.

(2) CE2 Controlled

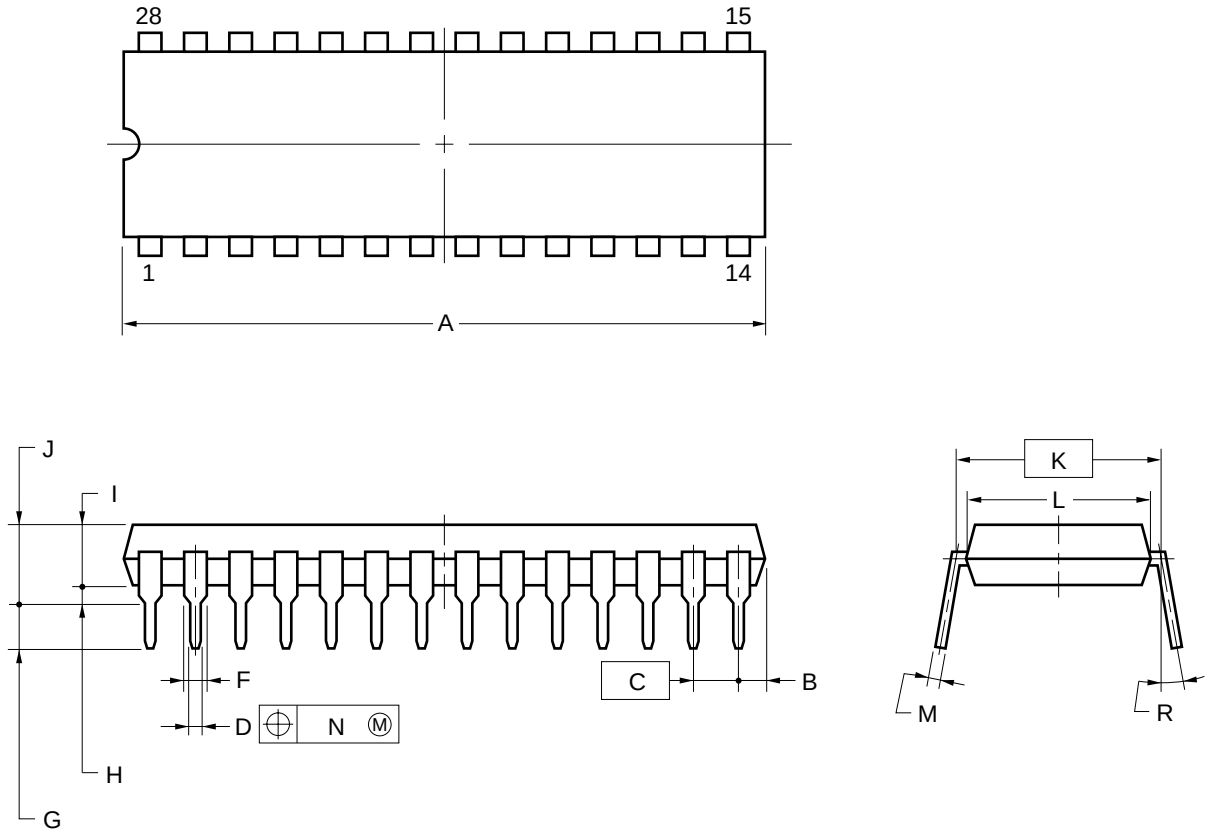
★



Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE) can be in high impedance state.

★ **Package Drawings**

28-PIN PLASTIC DIP (15.24 mm (600))



NOTES

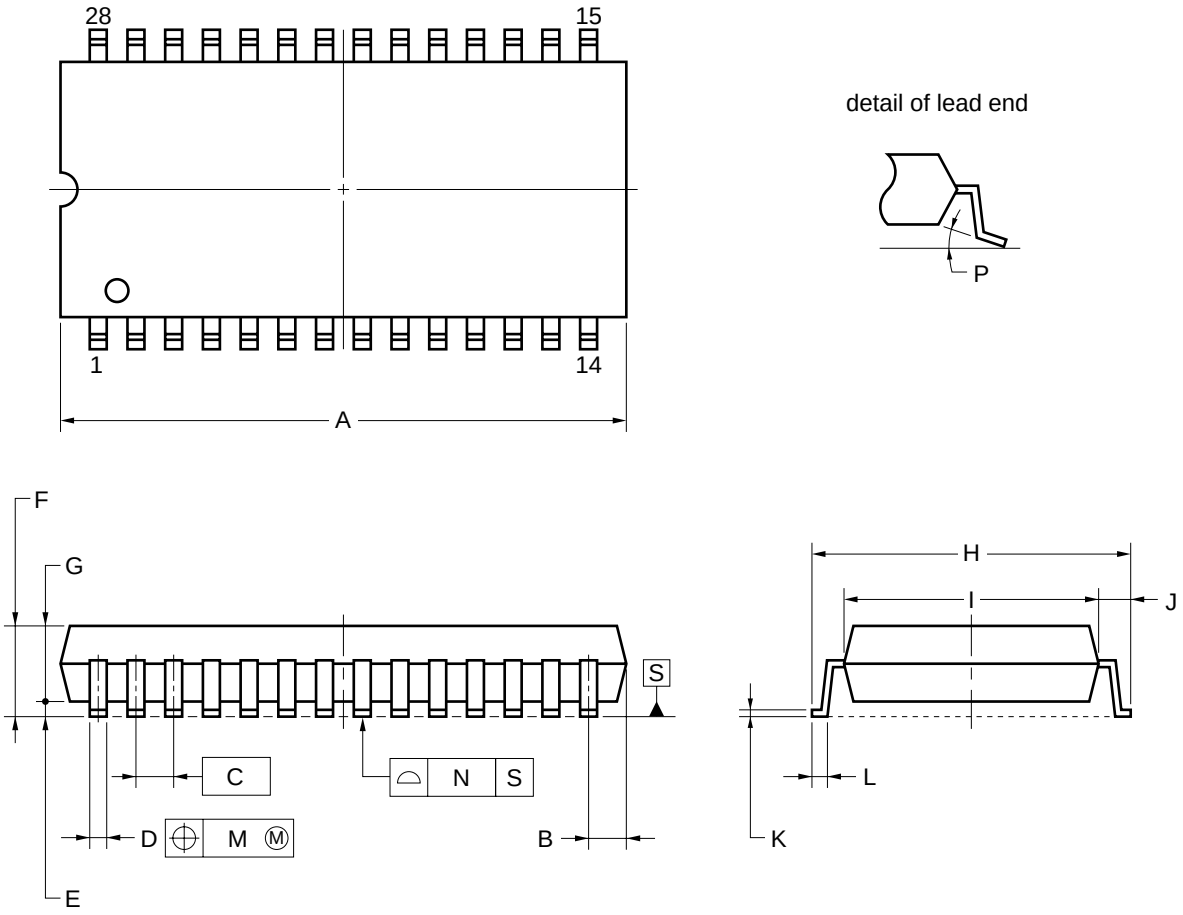
1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.

2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	38.10 MAX.
B	2.54 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.2 MIN.
G	3.6±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.72 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25
R	0~15°

P28C-100-600A1-2

28-PIN PLASTIC SOP (11.43 mm (450))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$18.0^{+0.6}_{-0.05}$
B	1.27 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.2±0.1
F	2.95 MAX.
G	2.55±0.1
H	11.8±0.3
I	8.4±0.1
J	1.7±0.2
K	0.22±0.05
L	0.7±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P28GU-50-450A-4

Recommended Soldering Conditions

The following conditions must be met when soldering μPD43257B. For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD43257BGU-xxL : 28-PIN PLASTIC SOP (11.43 mm (450))

μPD43257BGU-xxLL : 28-PIN PLASTIC SOP (11.43 mm (450))

Please consult with our sales offices.

Types of Through Hole Mount Device

μPD43257BCZ-xxL : 28-PIN PLASTIC DIP (15.24 mm (600))

μPD43257BCZ-xxLL : 28-PIN PLASTIC DIP (15.24 mm (600))

Soldering process	Soldering conditions
Wave soldering (only to leads)	Solder temperature : 260 °C or below, Flow time : 10 seconds or below
Partial heating method	Terminal temperature : 300 °C or below, Time : 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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