NEC

MOS INTEGRATED CIRCUIT
μPD16837

MONOLITHIC QUAD H-BRIDGE DRIVER

DESCRIPTION

The μPD16837 is a monolithic quad H-bridge driver employing power MOS FETs in the output stage. The MOS FETs in the output stage lower the saturation voltage and power consumption as compared with conventional drivers using bipolar transistors.

In addition, a low-voltage malfunction prevention circuit is also provided that prevents the IC from malfunctioning when the supply voltage drops. A 30-pin plastic shrink SOP package is adopted to help create compact and slim application sets.

In the output stage H-bridge circuits, two low-ON resistance H-bridge circuits for driving actuators, and another two channels for driving sled motors and loading motors are provided, making the product ideal for applications in CD-ROM and DVD.

FEATURES

- Four H-bridge circuits employing power MOS FETs
- High-speed PWM drive: Operating frequency: 120 kHz MAX.
- Low-voltage malfunction prevention circuit: Operating voltage: 2.5 V (TYP.)
- 30-pin plastic SSOP (7.62 mm (300))

ORDERING INFORMATION

Part Number	Package
μPD16837GS	30-pin plastic SSOP (7.62 mm (300))

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Control block supply voltage	V_{DD}		–0.5 to +7.0	V
Output block supply voltage	V_M		–0.5 to +15	V
Input voltage	V_{IN}		–0.5 to V_{DD} + 0.5	V
H-bridge drive current[Note 1]	$I_{DR\ (pulse)}$	PW ≤ 5 ms, Duty Cycle ≤ 30 %	±1.0	A/phase
Power dissipation[Note 2]	P_T		1.25	W
Operating temperature range	T_A		0 to 75	°C
Peak junction temperature	$T_{j\ (MAX)}$		150	°C
Storage temperature range	T_{stg}		–55 to +150	°C

Notes 1. When only one channel operates.

2. When mounted on a glass epoxy board (100 mm × 100 mm × 1 mm)

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The mark ★ shows major revised points.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Control block supply voltage	V_{DD} **Note 1**	4.0	5.0	6.0	V
Output block supply voltage	V_M	10.8	12.0	13.2	V
H-bridge drive current	$I_{DR\ (pulse)}$ **Note 2**	–600		600	mA
Operating frequency	f_O			120	kHz
Operating temperature range	T_A	0		75	°C
Peak junction temperature	$T_{j\ (MAX)}$			125	°C

Notes 1. The low-voltage malfunction prevention circuit operates when V_{DD} is 1.5 V or higher but less than 4 V (2.5 V TYP.).

2. PW ≤ 5 ms, Duty Cycle ≤ 10%

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_A = 25 °C)

The low-voltage malfunction prevention circuit operates when V_{DD} is 1.5 V to 4 V.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_M pin current (leakage current)	I_M	V_M = 13.2 V			50	μA
V_{DD} pin current	I_{DD}	V_{DD} = 6 V			200	μA
High-level input current	I_{IH}	V_{IN} = V_{DD}			0.25	mA
Low-level input current	I_{IL}	V_{IN} = 0	–2.0			μA
High-level input voltage **Note 1**	V_{IH}	V_{DD} = 5 V, V_M = 12 V	3.0		V_{DD} + 0.3	V
Low-level input voltage **Note 1**	V_{IL}	V_{DD} = 5 V, V_M = 12 V	–0.3		0.8	V
H-bridge ON resistance (ch2, ch3)	R_{ona}	V_{DD} = 5 V, V_M = 12 V		3.0	4.0	Ω
H-bridge ON resistance (ch1, ch4)	R_{onb}	V_{DD} = 5 V, V_M = 12 V		1.5	2.0	Ω
H-bridge switching current without load (ch2, ch3) **Note 2**	$I_{sa\ (AVE)}$	V_{DD} = 5 V V_M = 12 V			3.0	mA
H-bridge switching current without load (ch1, ch4) **Note 2**	$I_{sb\ (AVE)}$	at 100 kHz			4.5	mA

ch2, ch3 2A, 3A, 2B, 3B Output

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rise time	t_{TLHa}	V_{DD} = 5 V			200	ns
Rising delay time	t_{PLHa}	V_M = 12 V			350	ns
Change in rising delay time	Δt_{PLHa}	20 Ω			110	ns
Fall time	t_{THLa}	at 100 kHz			200	ns
Falling delay time	t_{PHLa}				350	ns
Change in falling delay time	Δt_{PHLa}				130	ns

ch2, ch3 2A-2B, 3A-3B

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rising delay time differential	$t_{PLHa\ (A-B)}$	V_{DD} = 5 V, V_M = 12 V			50	ns
Falling delay time differential	$t_{PHLa\ (A-B)}$	20 Ω at 100kHz			50	ns

Notes 1. The input pins are the IN and SEL pins.

2. Average value of the current consumed internally by an H-bridge circuit when the circuit is switched without load.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, T_A = 25 °C)

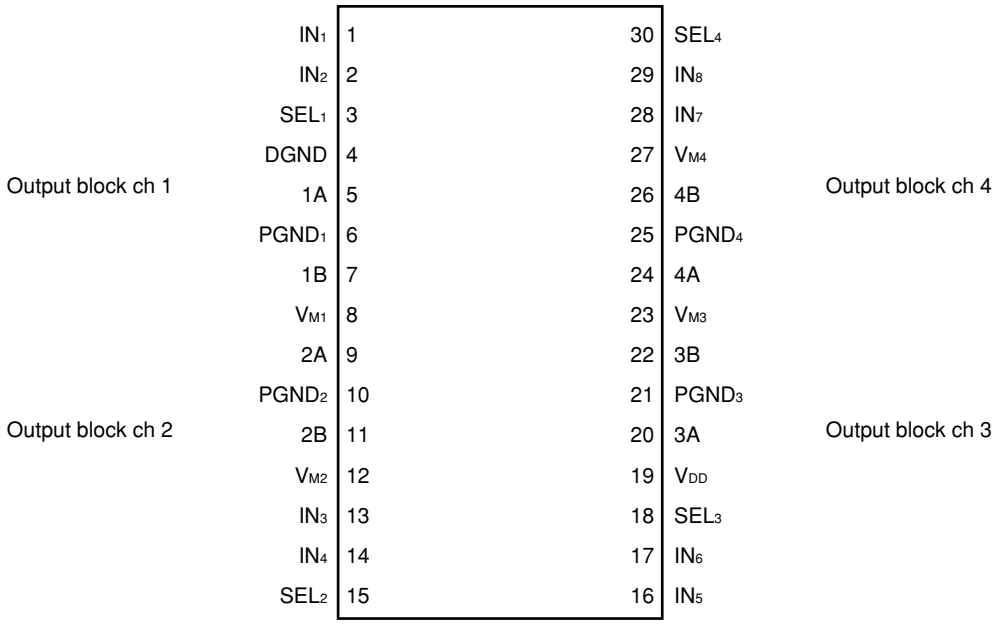
ch1, ch4 1A, 4A, 1B, 4B Output

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rise time	t_{TLHb}	V_{DD} = 5 V			200	ns
Rising delay time	t_{PLHb}	V_M = 12 V			350	ns
Change in rising delay time	Δt_{PLHb}	10 Ω			110	ns
Fall time	t_{THLb}	at 100 kHz			200	ns
Falling delay time	t_{PHLb}				350	ns
Change in falling delay time	Δt_{PHLb}				130	ns

ch1, ch4 1A-1B, 4A-4B

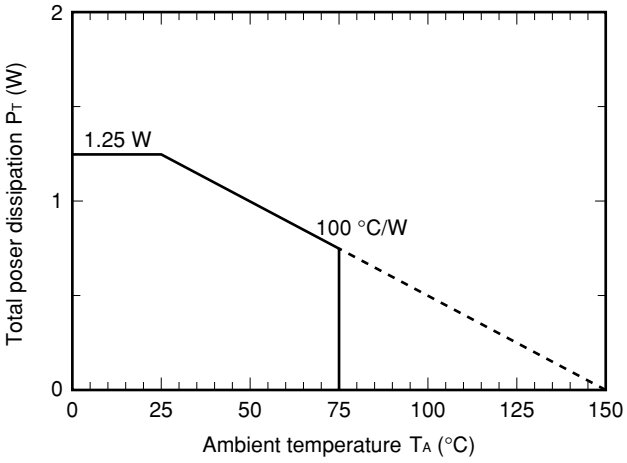
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rising delay time differential	$t_{PLHa\ (A-B)}$	V_{DD} = 5 V, V_M = 12 V			50	ns
Falling delay time differential	$t_{PHLa\ (A-B)}$	10 Ω at 100 kHz			50	ns

PIN CONFIGURATION

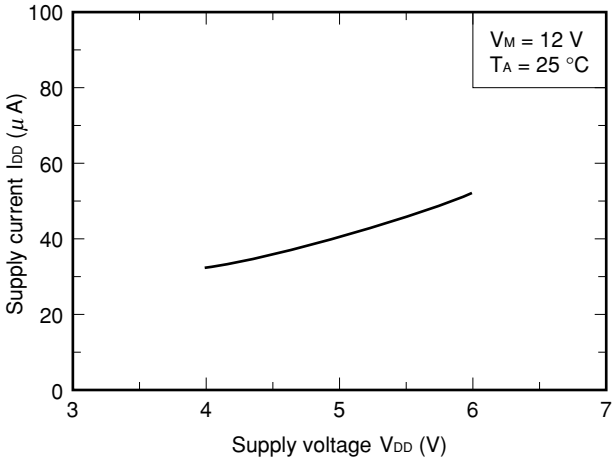


TYPICAL CHARACTERISTICS

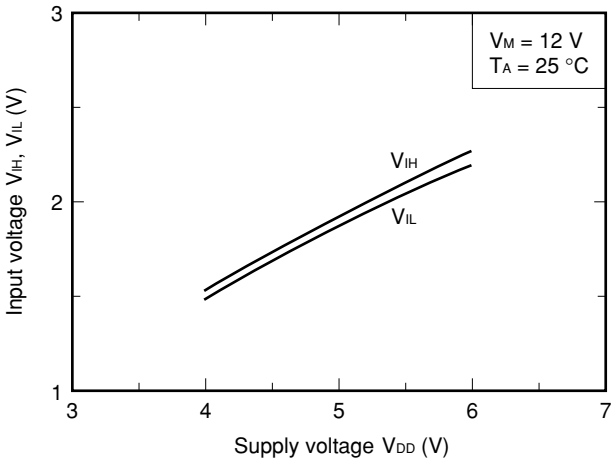
P_T vs. T_A Characteristics



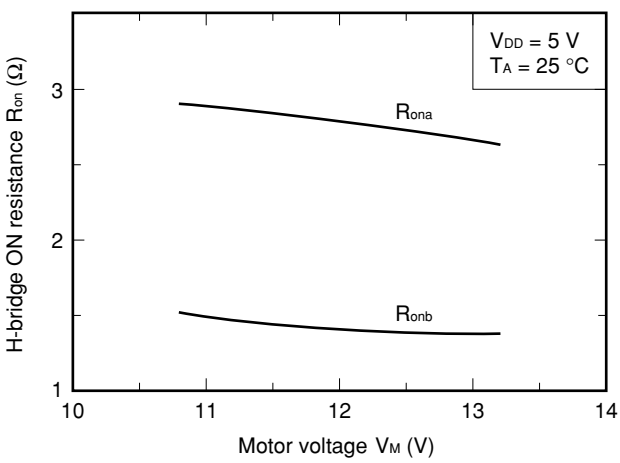
I_{DD} vs. V_{DD} Characteristics



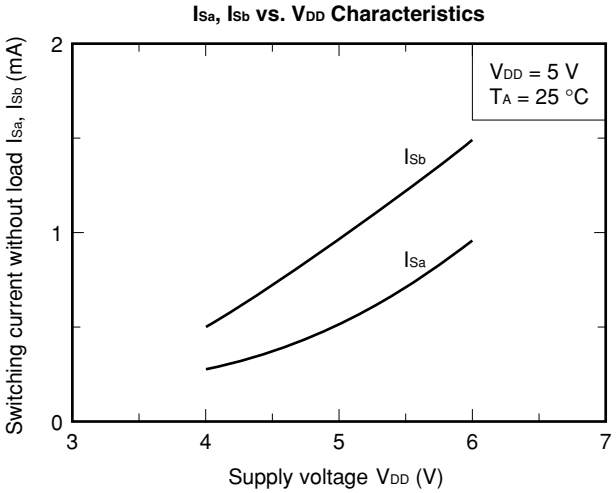
V_{IH}, V_{IL}, vs. V_{DD} Characteristics



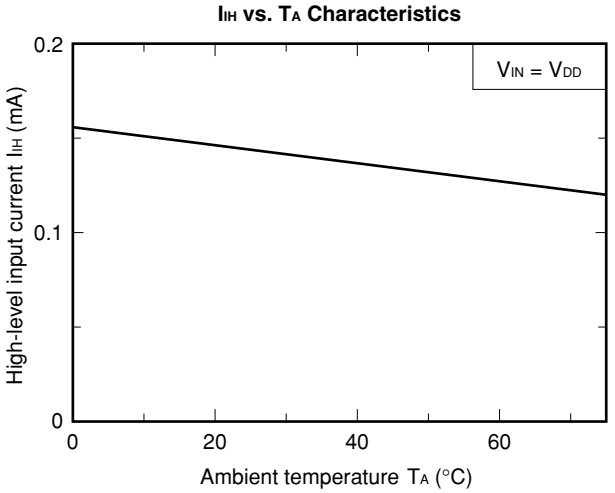
R_{on} vs. V_M Characteristics



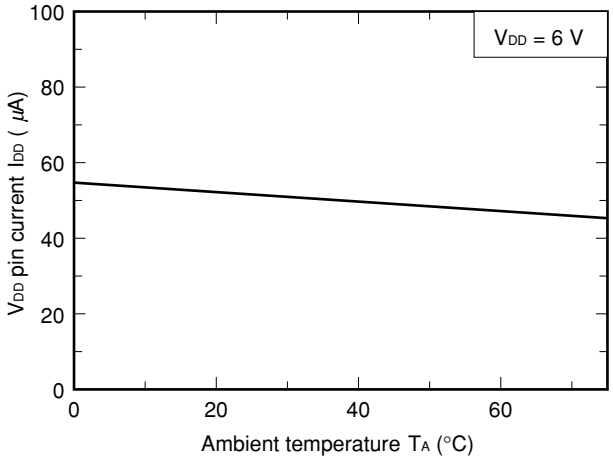
I_{Sa}, I_{Sb} vs. V_{DD} Characteristics



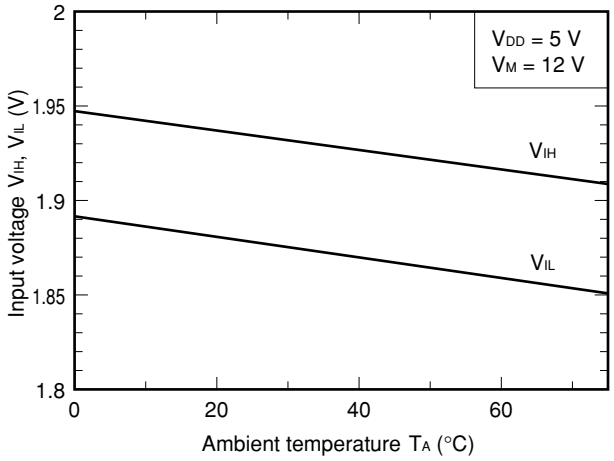
I_{IH} vs. T_A Characteristics



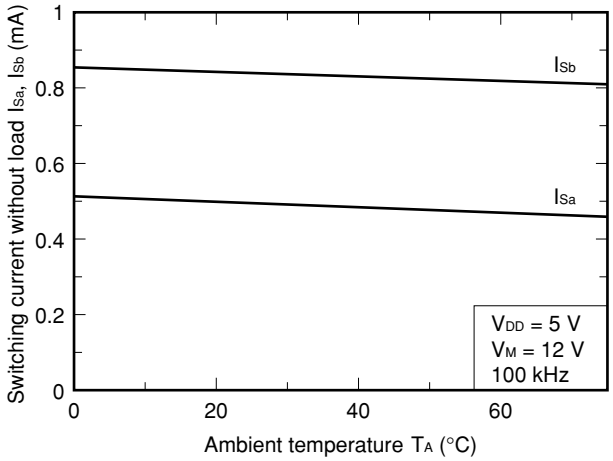
I_{DD} vs. T_A Characteristics



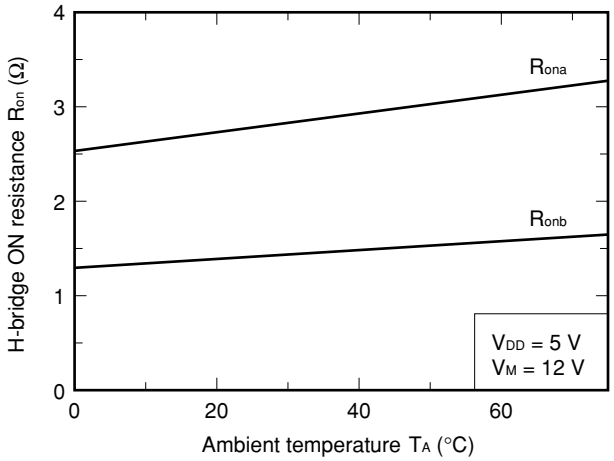
V_{IH}, V_{IL} vs. T_A Characteristics



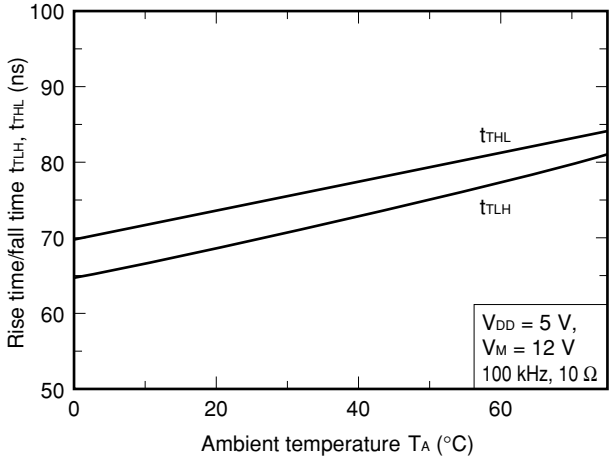
I_{Sa}, I_{Sb} vs. T_A Characteristics



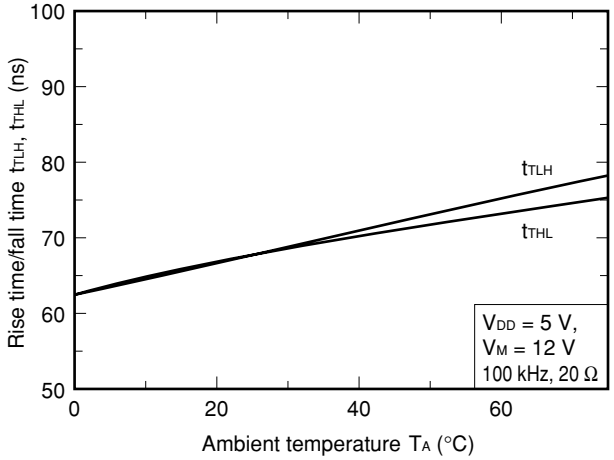
R_{on} vs. T_A Characteristics



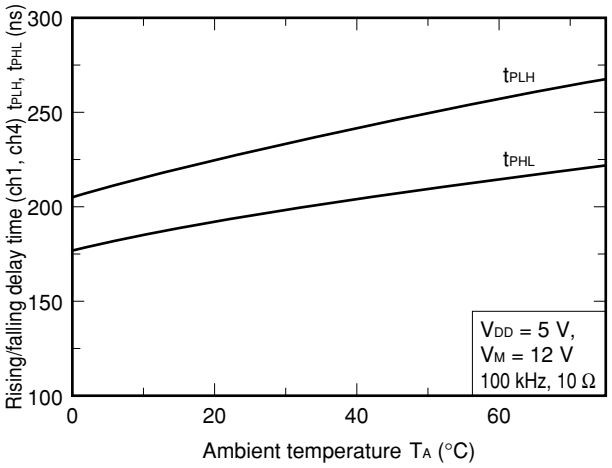
t_{TLH}, t_{THL} vs. T_A Characteristics (ch1, ch4)



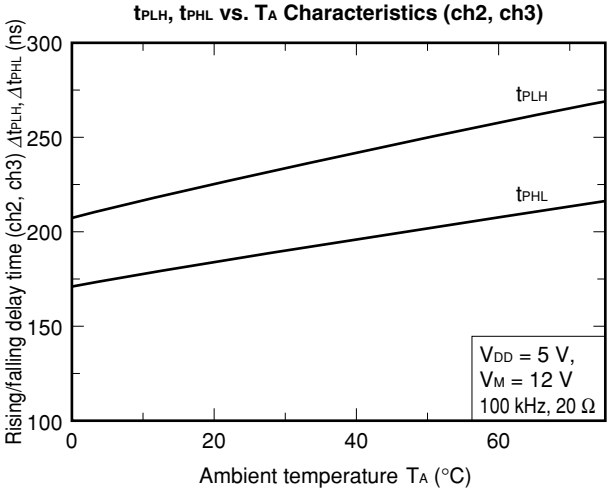
t_{TLH}, t_{THL} vs. T_A Characteristics (ch2, ch3)



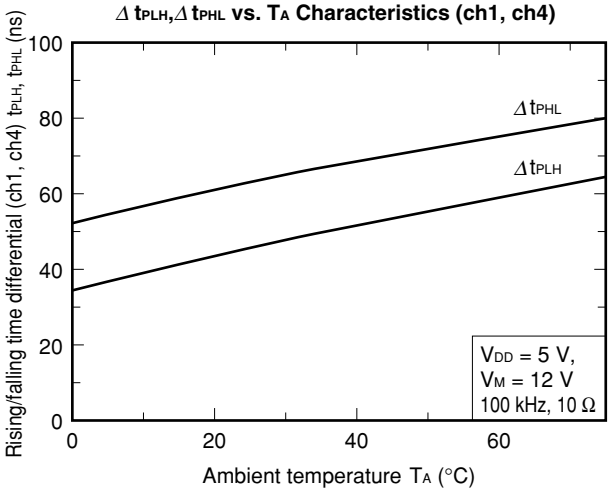
t_{PLH}, t_{PHL} vs. T_A Characteristics (ch1, ch4)



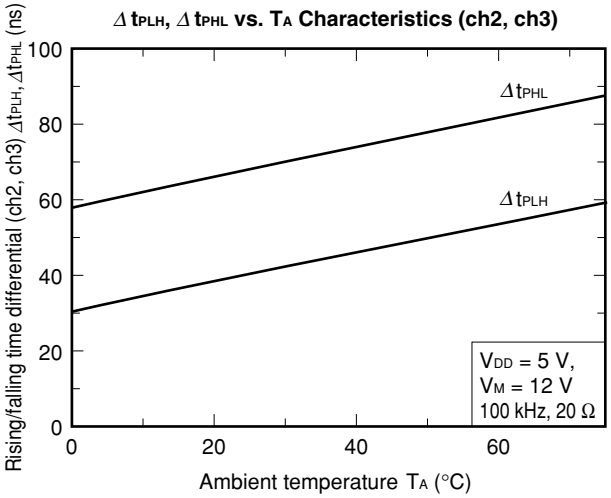
t_{PLH}, t_{PHL} vs. T_A Characteristics (ch2, ch3)



Δt_{PLH},Δt_{PHL} vs. T_A Characteristics (ch1, ch4)

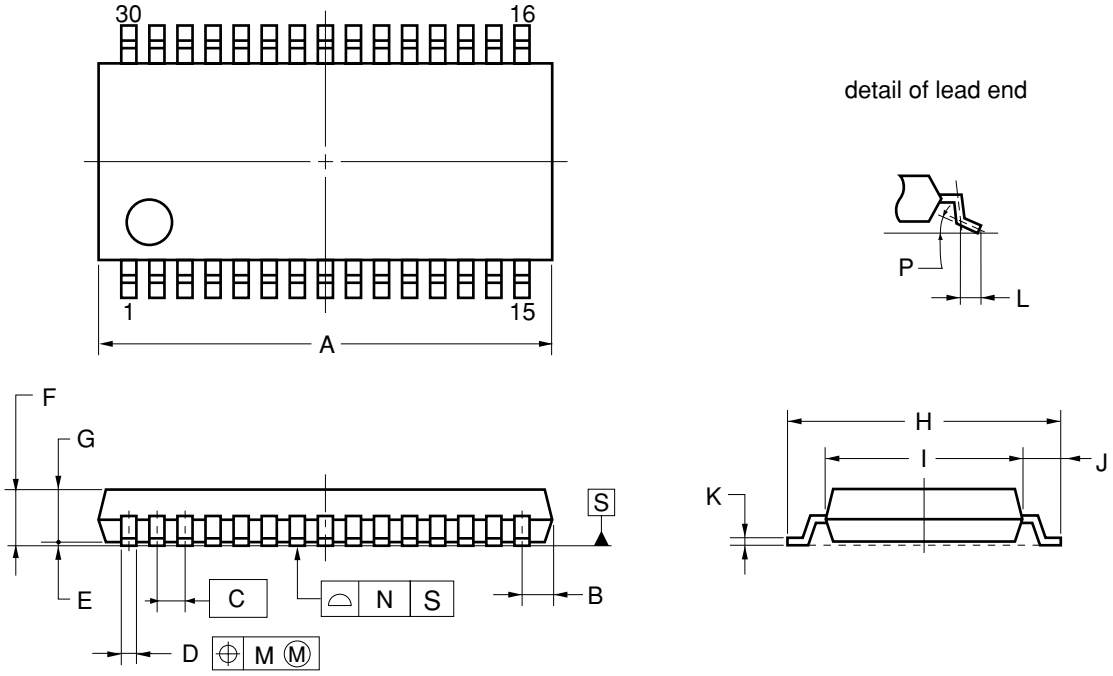


Δt_{PLH}, Δt_{PHL} vs. T_A Characteristics (ch2, ch3)



★ **PACKAGE DRAWING**

30-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

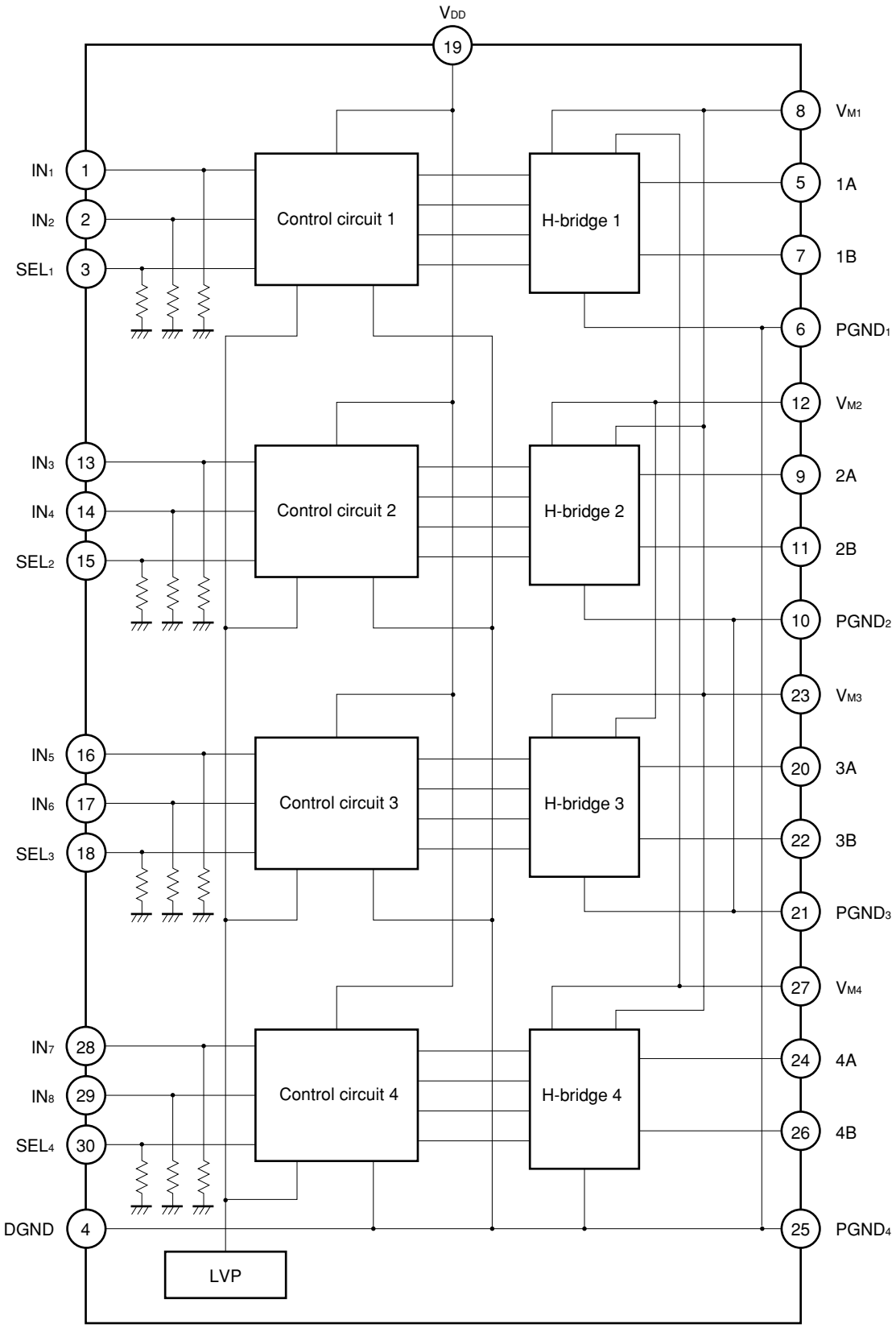
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

(UNIT:mm)

ITEM	DIMENSIONS
A	13.0 MAX.
B	0.9 MAX.
C	0.8 (T.P.)
D	$0.35^{+0.10}_{-0.05}$
E	0.1±0.1
F	1.8 MAX.
G	1.55±0.1
H	7.7±0.2
I	5.6±0.2
J	1.05±0.2
K	$0.20^{+0.10}_{-0.05}$
L	0.6±0.2
M	0.10
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S30GS-80-300C-1

★ BLOCK DIAGRAM

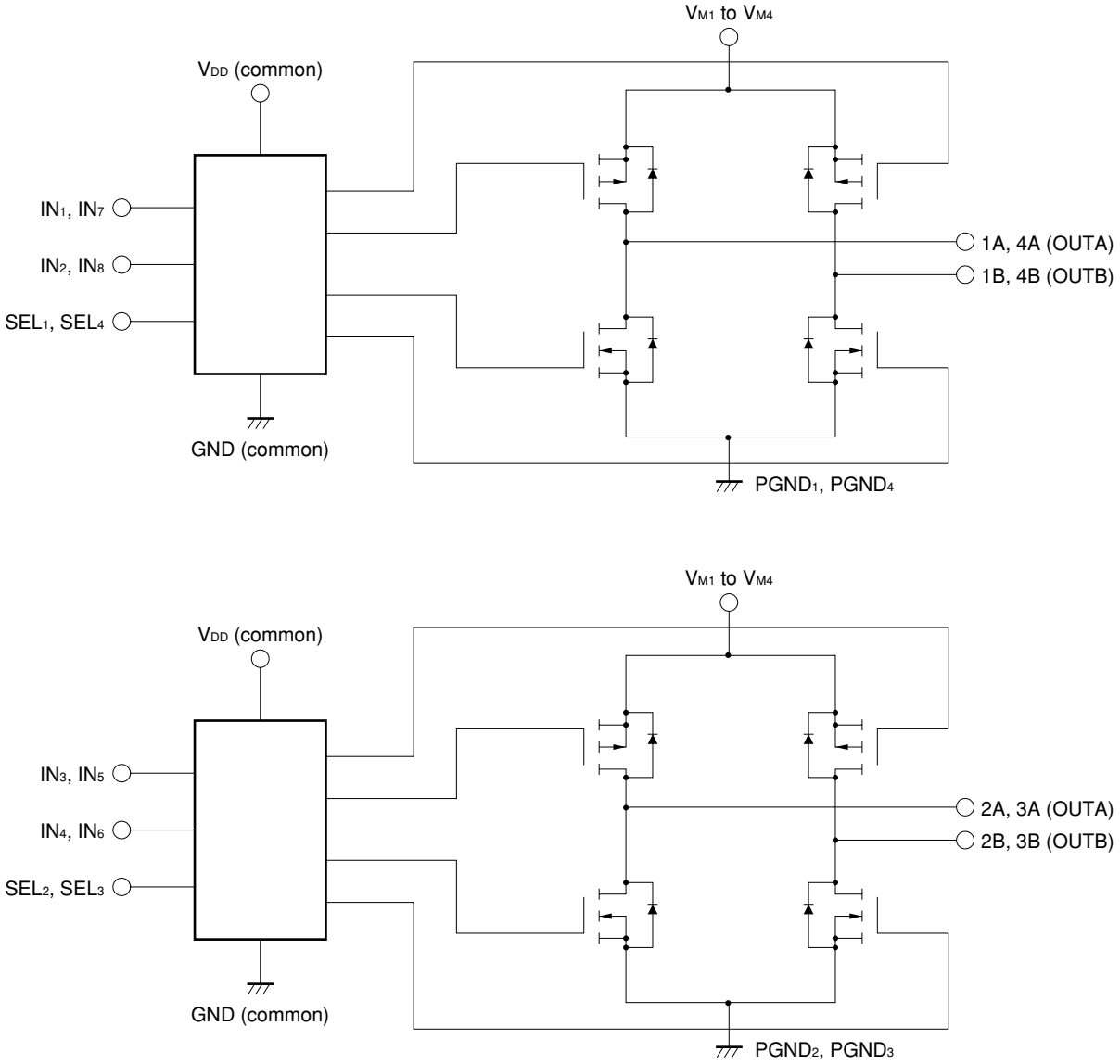


Cautions1. Connect all V_M and GND pins.

2. Internally pulled down to GND via 50 kΩ.

3. LVP (Low-voltage prevention circuit) operates by V_{DD} = 2.5 V (TYP.).

FUNCTION TABLE



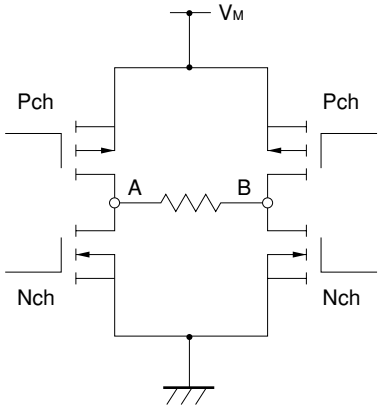
Function Table (common to all chs)				
Input			Output	
IN_1	IN_2	SEL	OUTA	OUTB
H	L	H	H	L
L	L	H	L	L
L	H	H	L	H
H	H	H	H	H
×	×	L	Z	Z

Remark ×: Don't care
Z: High inpedance

ABOUT SWITCHING

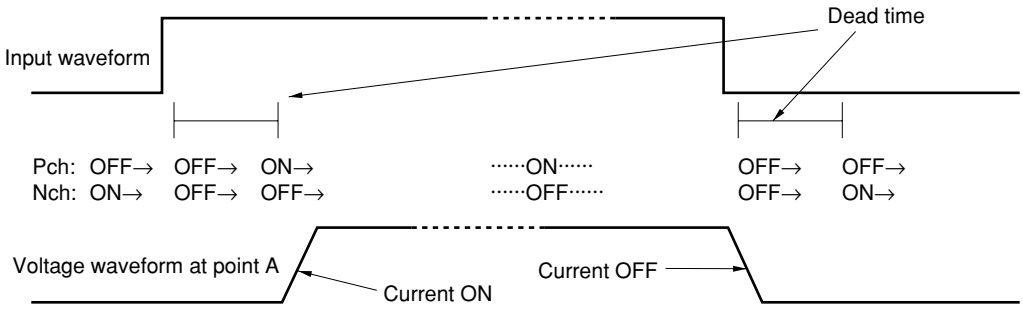
When output A is switched as shown in the figure on the right, a dead time (time during which both P ch and N ch are OFF) elapses to prevent through current. Therefore, the waveform of output A (rise time, fall time, and delay time) changes depending on whether output B is fixed to the high or low level.

The output voltage waveforms of A in response to an input waveform where output B is fixed to the low level (1) or high level (2) are shown below.



(1) Output B: Fixed to low level

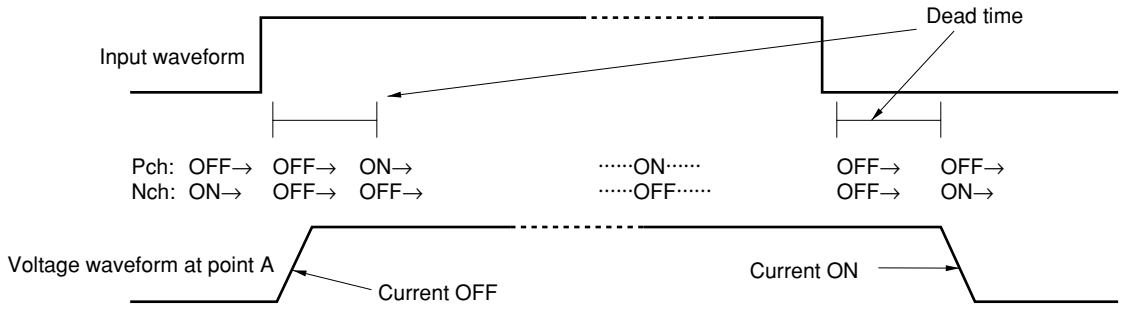
Output A: Switching operation (Operations of P ch and N ch are shown.)



Output A goes into a high-impedance state and is in an undefined status during the dead time period. Because output B is pulled down by the load, a low level is output to A.

(2) Output B: Fixed to high level

Output A: Switching operation (Operations of P ch and N ch are shown.)



Output A goes into a high-impedance state and is in an undefined status during the dead time period. Because output B is pulled up by the load, a high level is output to A.

The switching characteristics shown on the preceding pages are specified as follows ("output at one side" means output B for H bridge output A, or output A for output B).

[Rise time]

Rise time when the output at one side is fixed to the low level (specified on current ON).

[Fall time]

Fall time when the output at one side is fixed to the high level (specified on current ON).

[Rising delay time]

Rising delay time when the output at one side is fixed to the low level (specified on current ON).

[Falling delay time]

Falling delay time when the output at one side is fixed to the high level (specified on current ON).

[Change in rising delay time]

Change (difference) in the rising delay time between when the output at one side is fixed to the low level and when the output at the other side is fixed to the high level.

[Change in falling delay time]

Change (difference) in falling delay time between when the output at one side is fixed to the low level and when the output at the other side is fixed to the high level.

[Rising delay time differential]

Difference in rising delay time between output A and output B.

[Falling delay time differential]

Difference in falling delay time between output A and output B.

Caution Because this IC switches a high current at high speeds, surge may occur due to the V_M and GND wiring and inductance and degrade the performance of the IC.
On the PWB, keep the pattern width of the V_M and GND lines as wide and short as possible, and insert the bypass capacitors between V_M and GND at a location as close to the IC as possible.
Connect a low-inductance magnetic capacitor (4700 pF or more) and an electrolytic capacitor of 10 μF or so, depending on the load current, in parallel.

RECOMMENDED SOLDERING CONDITIONS

The μ PD16837 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

30-PIN PLASTIC SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C; Time: 30 secs. MAX. (210 °C MIN.); Number of times: 3 times MAX.; Number of days: none[Note]; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% MAX.) is recommended.	IR35-00-3
VPS	Package peak temperature: 215 °C; Time: 40 secs. MAX. (200 °C MIN.); Number of times: 3 times MAX.; Number of days: none[Note]; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% MAX.) is recommended.	VP-15-00-3
Wave soldering	Package peak temperature: 260 °C; Time: 10 secs. MAX.; Number of times: once; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt% MAX.) is recommended.	WS60-00-1

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65% RH MAX.

Caution Do not use two or more soldering methods in combination.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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