

SWITCHING DUAL N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

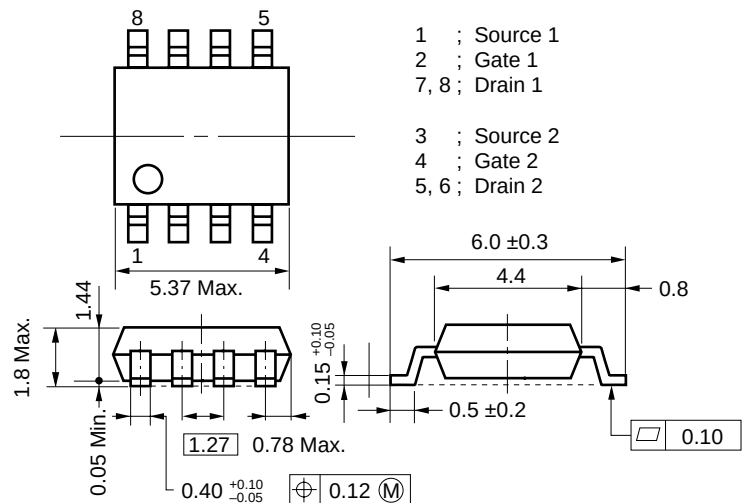
This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

FEATURES

- Dual MOSFET chips in small package
- 4 V Gate Drive Type and Low On-Resistance
 $R_{DS(on)1} = 37 \text{ m}\Omega \text{ Max. (} V_{GS} = 10 \text{ V, } I_D = 2.5 \text{ A)}$
 $R_{DS(on)2} = 64 \text{ m}\Omega \text{ Max. (} V_{GS} = 4 \text{ V, } I_D = 2.5 \text{ A)}$
- Low C_{iss} $C_{iss} = 510 \text{ pF Typ.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS

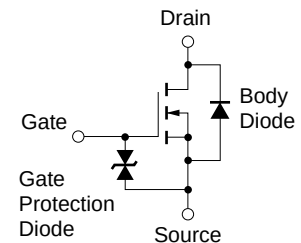
(in: millimeter)

**ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, all terminals are connected)**

Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 5.0	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 20	A
Total Power Dissipation (1 unit)**	P_T	1.7	W
Total Power Dissipation (2 unit)**	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 1.1 \text{ mm}$



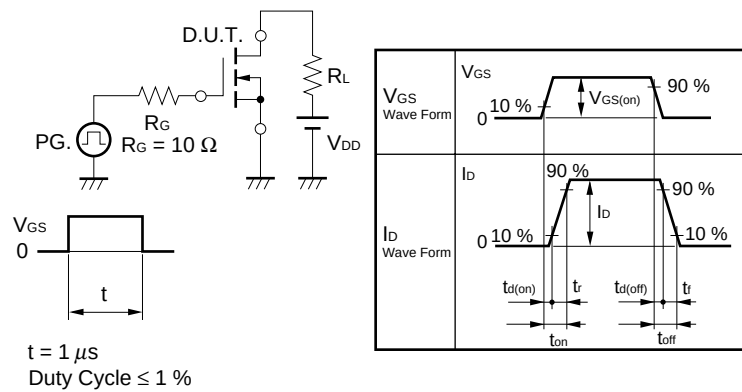
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

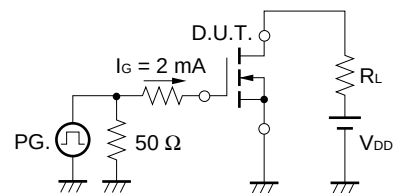
ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, all terminal are connected)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		27	37	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = 4\text{ V}$, $I_D = 2.5\text{ A}$		44	64	$\text{m}\Omega$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$	1.0	1.5	2.0	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 10\text{ V}$, $I_D = 2.5\text{ A}$	3.0	6.0		S
Drain Leakage Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0$			10	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$			± 10	μA
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$		510		pF
Output Capacitance	C_{oss}			350		pF
Reverse Transfer Capacitance	C_{rss}			150		pF
Turn-On Delay Time	$t_{d(on)}$	$I_D = 2.5\text{ A}$ $V_{GS(on)} = 10\text{ V}$ $V_{DD} = 15\text{ V}$ $R_G = 10\text{ }\Omega$		10		ns
Rise Time	t_r			95		ns
Turn-off Delay Time	$t_{d(off)}$			120		ns
Fall Time	t_f			100		ns
Total Gate Charge	Q_G	$I_D = 5.0\text{ A}$ $V_{DD} = 24\text{ V}$ $V_{GS} = 10\text{ V}$		19		nC
Gate to Source Charge	Q_{GS}			1.5		nC
Gate to Drain Charge	Q_{GD}			6.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 5.0\text{ A}$, $V_{GS} = 0$		0.8		V
Reverse Recovery Time	t_{rr}	$I_F = 5.0\text{ A}$, $V_{GS} = 0$ $di/dt = 100\text{ A}/\mu\text{s}$		85		ns
Reverse Recovery Charge	Q_{rr}			90		nC

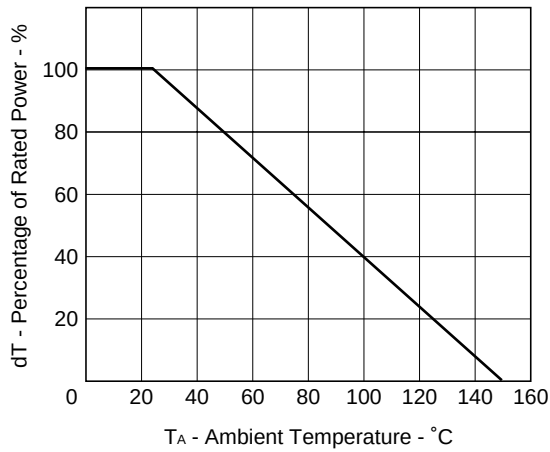
Test Circuit 1 Switching Time



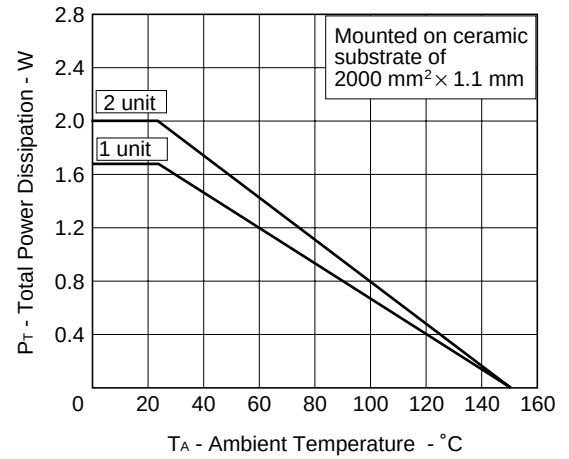
Test Circuit 2 Gate Charge



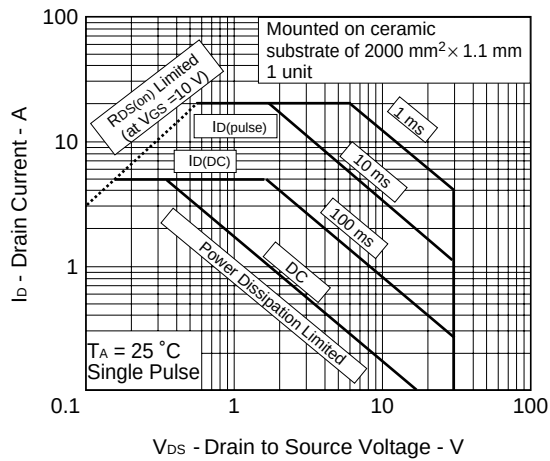
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



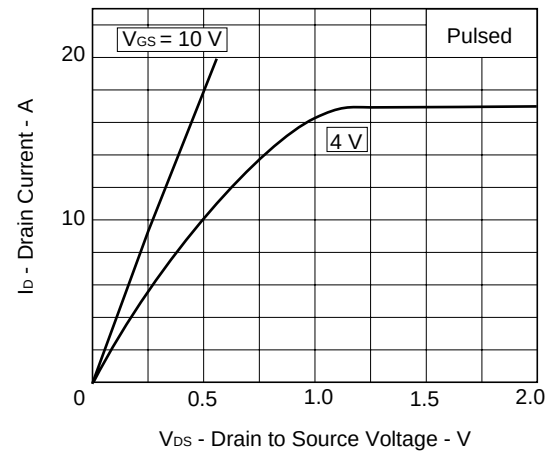
TOTAL POWER DISSIPATION vs.
AMBIENT TEMPERATURE



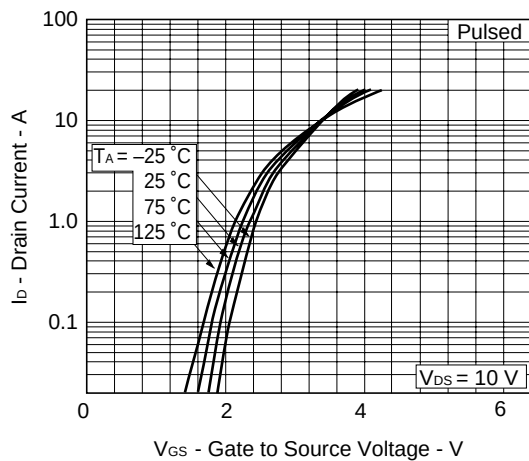
FORWARD BIAS SAFE OPERATING AREA



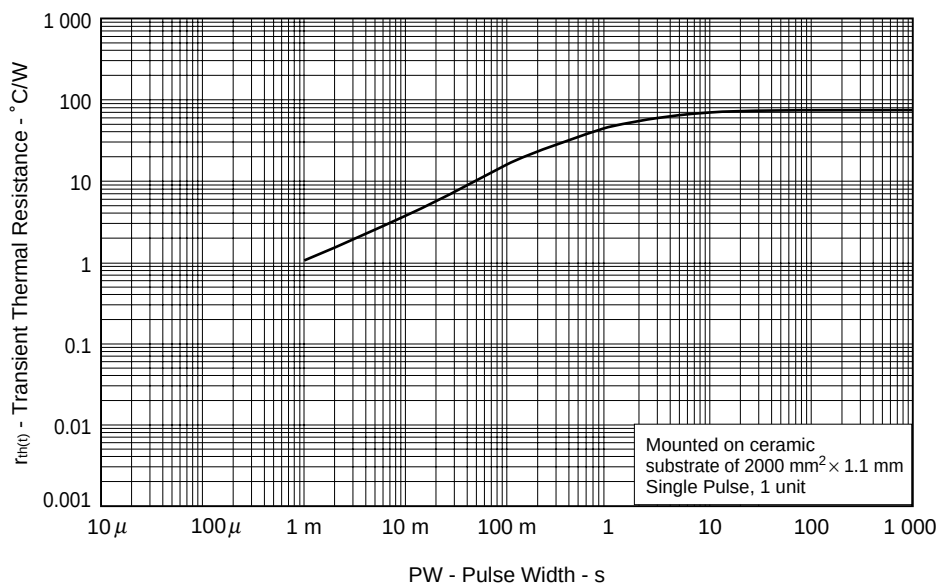
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



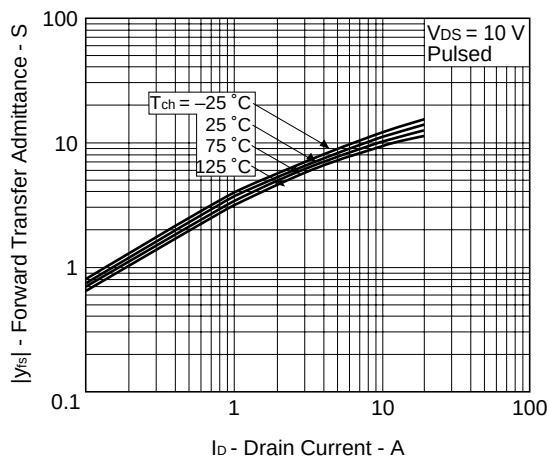
FORWARD TRANSFER CHARACTERISTICS



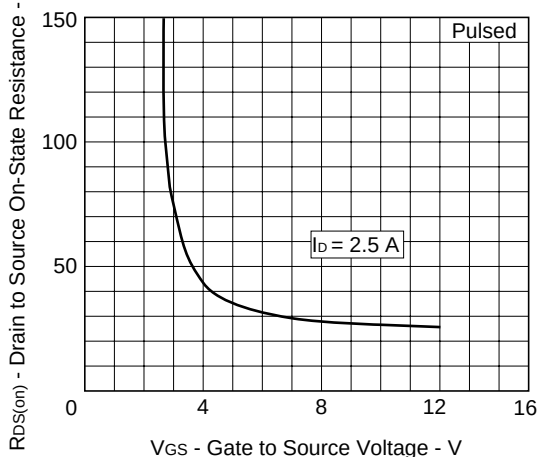
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



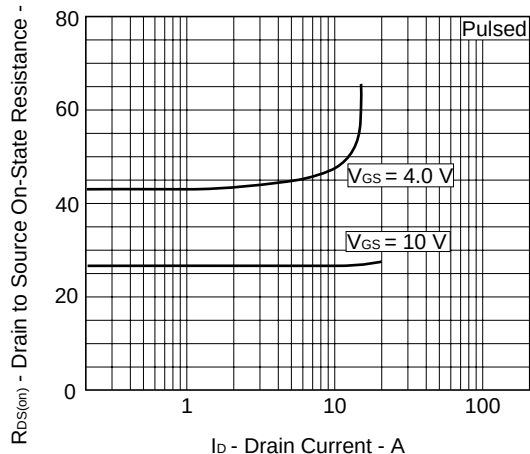
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



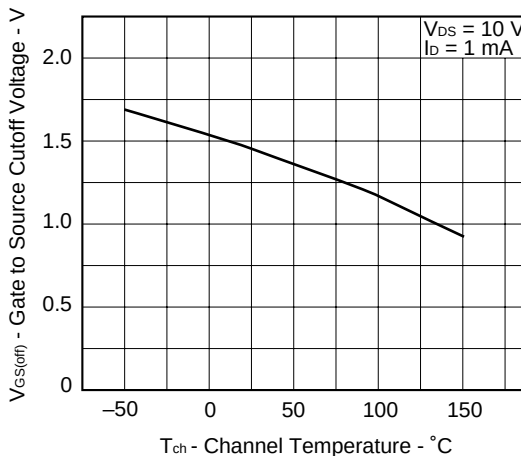
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



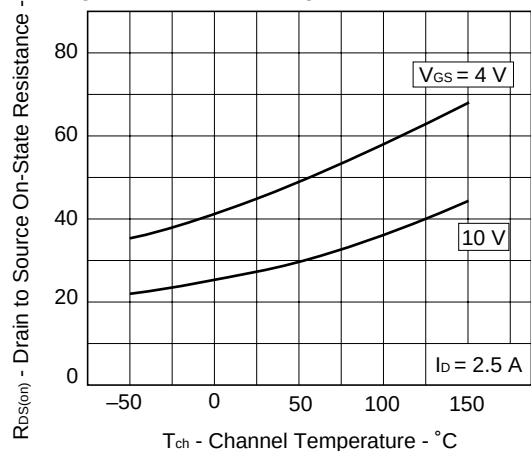
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



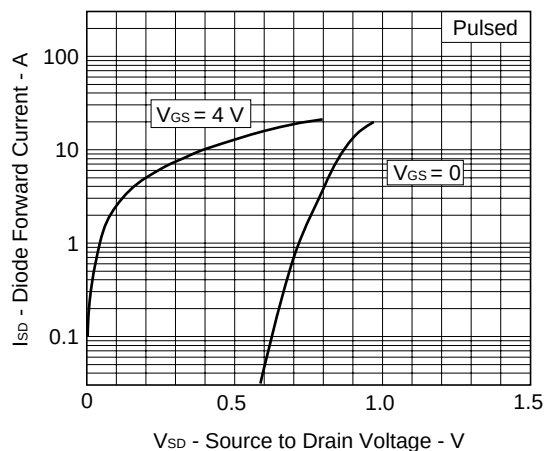
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



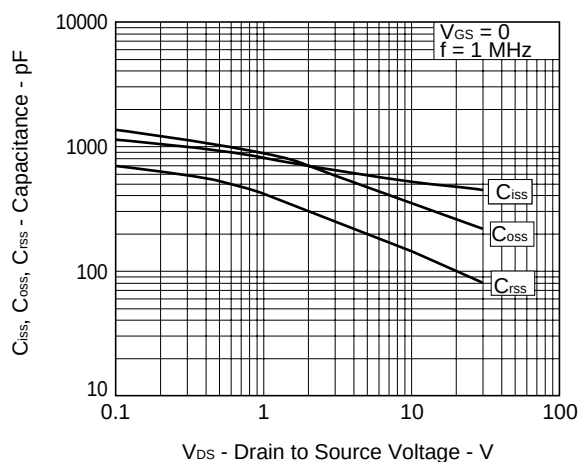
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



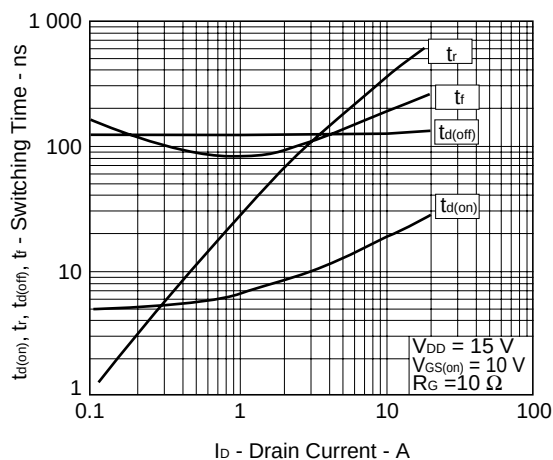
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



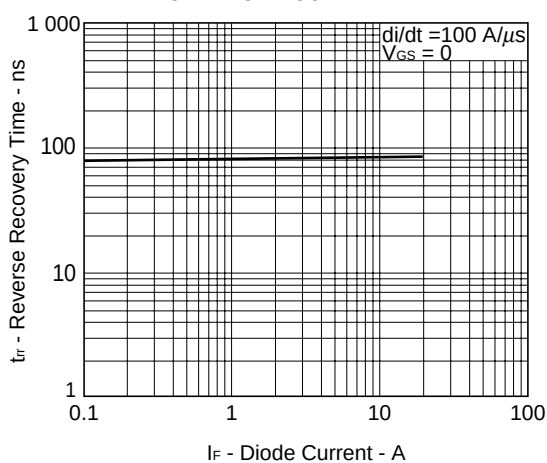
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



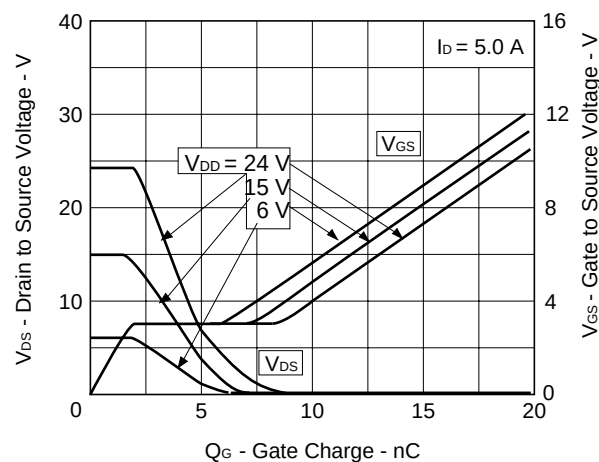
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. BODY DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.