

PRELIMINARY PRODUCT BRIEF

μ PD720121

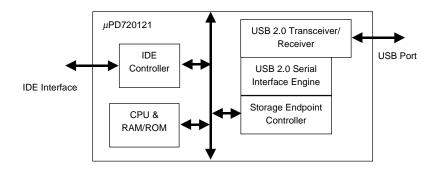
UNIVERSAL SERIAL BUS 2.0 TO IDE BRIDGE

The μ PD720121 is designed to perform a bridge between USB 2.0 to ATA/ATAPI. The μ PD720121 complies with the Universal Serial Bus Specification Revision 2.0 and works up to 480 Mbps. The μ PD720121 integrates RISC processor, IDE controller, Endpoint controller, RAM, serial interface engine, and USB 2.0 transceiver into a single chip. The USB 2.0 protocol and class specific protocol (Bulk only protocol) are handled by USB 2.0 transceiver, serial interface engine, and Endpoint controller. And the transport layer is performed by NB85E RISC processor which is in the μ PD720121. The software to control the μ PD720121 is located in the external ROM (Flash or Mask ROM).

FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps)
- Compliant with ATA/ATAPI-4 (PIO Mode 0-4, DMA Mode 0-2, Ultra DMA/33 Mode 0-2)
- One USB 2.0 high-speed transceiver / receiver with full-speed transceiver / receiver
- USB 2.0 High-speed or Full-speed packet protocol sequencer (Serial Interface Engine)
- Automatic chirp assertion and full-/high-speed mode change
- USB Reset, Suspend and Resume signaling detection
- Can support remote wakeup functionality.
- Supports power control functionality for ATAPI device as CD-ROM.
- Supports set feature (TEST_MODE) functionality.
- System clock is generated by 30 MHz X'tal
- 3.3 V power supply

BLOCK DIAGRAM



PACKAGE

- 120-pin plastic TQFP (Fine pitch) (14×14)
- 144-pin plastic LQFP (Fine pitch) (20×20)



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