U62H256S

Automotive Fast 32K x 8 SRAM

Features

- 32768 x 8 bit static CMOS RAM
- 35 and 55 ns Access Time
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current
  - 35 ns: 45mA
  - 55 ns: 30mA
- Standby current < 1mA at 125°C
- TTL/CMOS-compatible
- Automatic reduction of power dissipation in long Read or Write cycles
- Power supply voltage 5 V
- Operating temperature range
  - -40 °C to 85 °C
  - -40 °C to 125 °C
- CECC 90000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Package: SOP28 (300/330 mil)

Description

The U62H256S is a static RAM manufactured using a CMOS process technology with the following operating modes:

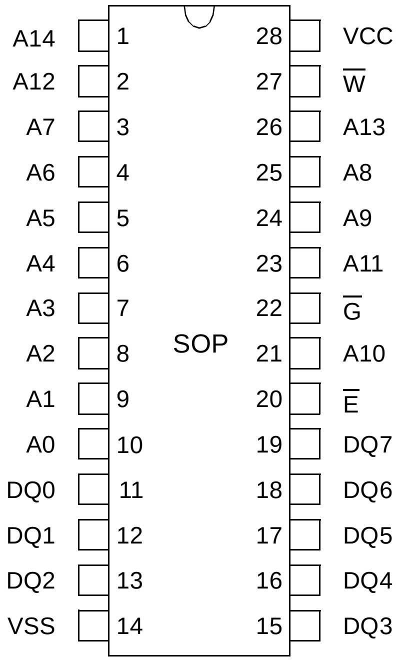
- Read	- Standby
- Write	- Data Retention

The memory array is based on a MIXMOS cell.

The circuit is activated by the falling edge of $\overline{E}$. The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. During the active state $\overline{E}$ = L each address change leads to a new Read or Write cycle. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word will be available at the outputs DQ0-DQ7. After the address change, the data outputs go High-Z until the new information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals $\overline{W}$ or $\overline{G}$, the operating current ($I_O = 0$ mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of $\overline{W}$, or by the rising edge of $\overline{E}$, respectively.

Data retention is guaranteed down to 2 V. With the exception of $\overline{E}$, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration

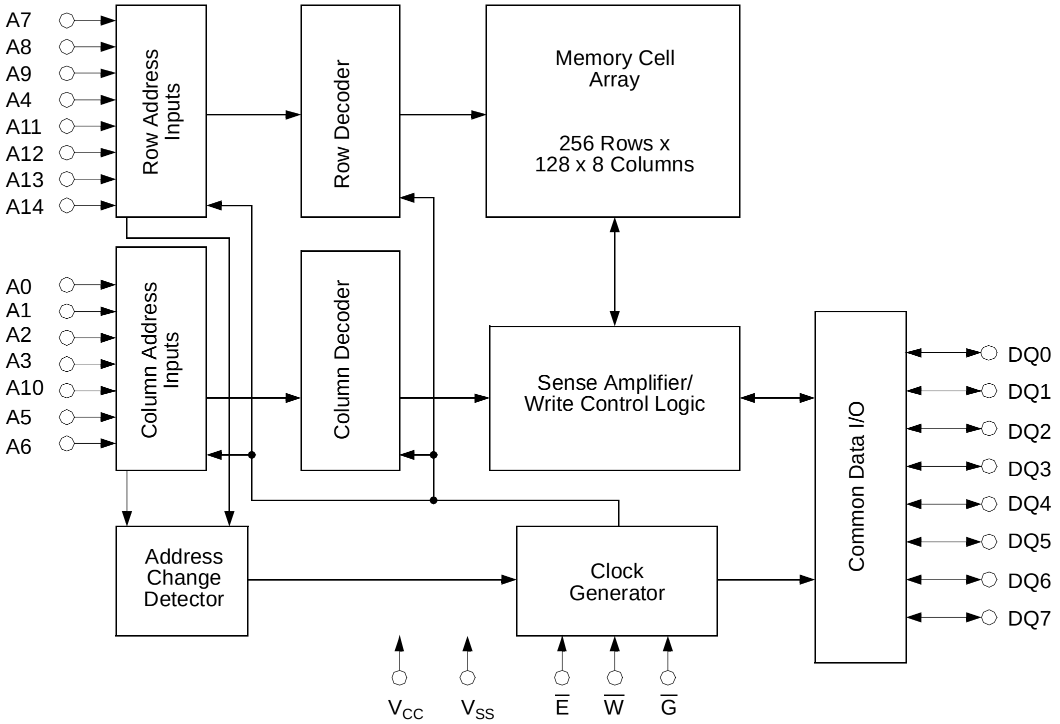


Top View

Pin Description

Signal Name	Signal Description
A0 - A14	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

Block Diagram



Truth Table

Operating Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured ±200 mV from steady-state voltage.

Maximum Ratings	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	-0.5	7	V
Input Voltage	V_I	-0.5	V_{CC} + 0.5	V
Output Voltage	V_O	-0.5	V_{CC} + 0.5	V
Power Dissipation	P_D	-	1	W
Operating Temperature K-Type	T_a	-40	85	°C
A-Type		-40	125	
Storage Temperature	T_{stg}	-65	150	°C
Output Short-Circuit Current at V_{CC} = 5 V and V_O = 0 V**	$\mid I_{OS} \mid$		200	mA

**Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		4.5	5.5	V
Input Low Voltage*	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC} + 0.3	V

* -2 V at Pulse Width 10 ns

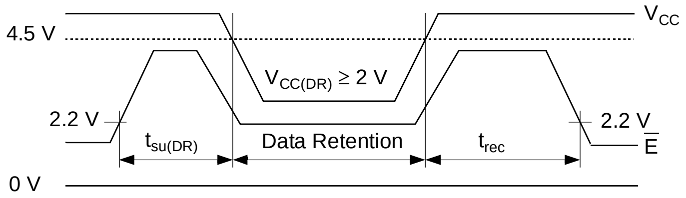
Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} = 5.5 V			
		V_{IL} = 0.8 V			
		V_{IH} = 2.2 V			
		t_{cW} = 35 ns		90	mA
		t_{cW} = 55 ns		70	mA
Supply Current - Standby Mode	$I_{CC(SB)}$	V_{CC} = 5.5 V			
(CMOS level)		$V_{\overline{E}}$ = V_{CC} - 0.2 V			
		T = 40 °C		8	µA
		T = 85 °C		150	µA
		T = 110 °C		500	µA
		T = 125 °C		1000	µA
Supply Current - Standby Mode	$I_{CC(SB)1}$	V_{CC} = 5.5 V			
(TTL level)		$V_{\overline{E}}$ = 2.2 V			
		K-Type		10	mA
		A-Type		20	mA
Output High Voltage	V_{OH}	V_{CC} = 4.5 V	2.4		V
		I_{OH} = -4.0 mA			
Output Low Voltage	V_{OL}	V_{CC} = 4.5 V		0.4	V
		I_{OL} = 8.0 mA			
Input High Leakage Current	I_{IH}	V_{CC} = 5.5 V		2	µA
		V_{IH} = 5.5 V			
Input Low Leakage Current	I_{IL}	V_{CC} = 5.5 V	-2		µA
		V_{IL} = 0 V			
Output High Current	I_{OH}	V_{CC} = 4.5 V		-4	mA
		V_{OH} = 2.4 V			
Output Low Current	I_{OL}	V_{CC} = 4.5 V	8		mA
		V_{OL} = 0.4 V			
Output Leakage Current					
High at Three-State Outputs	I_{OHZ}	V_{CC} = 5.5 V		2	µA
		V_{OH} = 5.5 V			
Low at Three-State Outputs	I_{OLZ}	V_{CC} = 5.5 V	-2		µA
		V_{OL} = 0 V			

Switching Characteristics Read Cycle	**Symbol**		**35**		**55**		**Unit**
	Alt.	**IEC**	**Min.**	**Max.**	**Min.**	**Max.**	
Read Cycle Time	t_{RC}	t_{cR}	35		55		ns
Address Access Time to Data Valid	t_{AA}	$t_{a(A)}$		35		55	ns
Chip Enable Access Time to Data Valid	t_{ACE}	$t_{a(E)}$		35		55	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$		15		25	ns
$\overline{E}$ HIGH to Output in High-Z	t_{HZCE}	$t_{dis(E)}$		12		15	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		12		15	ns
$\overline{E}$ LOW to Output in Low-Z	t_{LZCE}	$t_{en(E)}$	3		3		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	3		3		ns
$\overline{E}$ LOW to Power-Up Time	t_{PU}		0		0		ns
$\overline{E}$ HIGH to Power-Down Time	t_{PD}			35		55	ns

Switching Characteristics Write Cycle	**Symbol**		**35**		**55**		**Unit**
	Alt.	**IEC**	**Min.**	**Max.**	**Min.**	**Max.**	
Write Cycle Time	t_{WC}	t_{cW}	35		55		ns
Write Pulse Width	t_{WP}	$t_{w(W)}$	20		35		ns
Write Setup Time	t_{WP}	$t_{su(W)}$	20		35		ns
Address Setup Time	t_{AS}	$t_{su(A)}$	0		0		ns
Address Valid to End of Write	t_{AW}	$t_{su(A-WH)}$	20		40		ns
Chip Enable Setup Time	t_{CW}	$t_{su(E)}$	25		40		ns
Pulse Width Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	25		40		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	15		25		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		0		ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$		15		20	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		12		15	ns
$\overline{W}$ HIGH to Output in Low-Z	t_{LZWE}	$t_{en(W)}$	0		0		ns
$\overline{G}$ LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns

Data Retention Mode

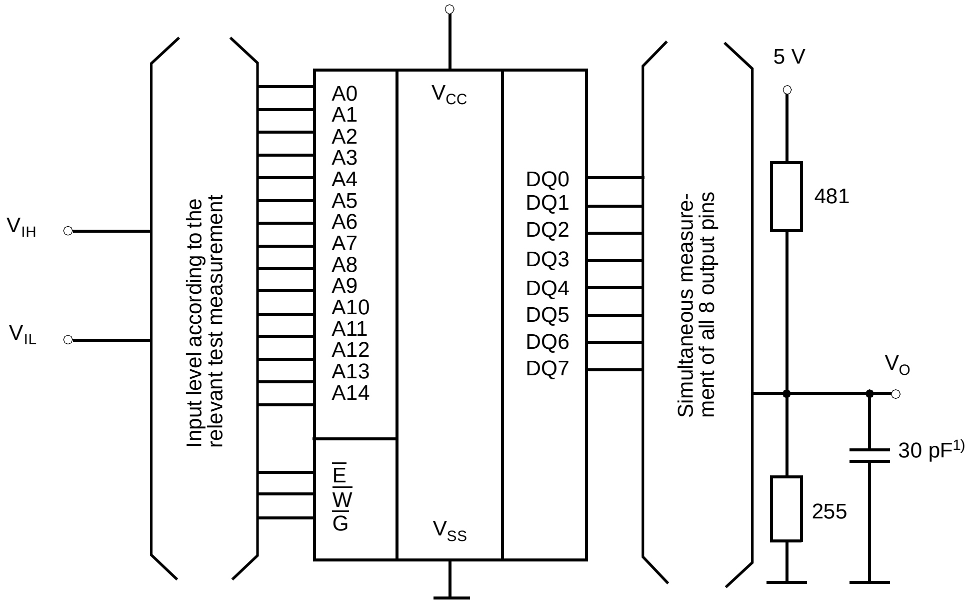
$\overline{E}$ - controlled



$$V_{CC(DR)} - 0.2\ V \le V_{\overline{E}(DR)} \le V_{CC(DR)} + 0.3\ V$$

Data Retention Characteristics	**Symbol**		**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
	Alt.	**IEC**					
Data Retention Supply Voltage		$V_{CC(DR)}$		2		5.5	V
Data Retention Supply Current		$I_{CC(DR)}$	$V_{CC(DR)} = 3$ V $V_{\overline{E}} = V_{CC(DR)} - 0.2$ V T = 40 °C T = 85 °C T = 110 °C T = 125 °C			 5 90 300 600	 µA µA µA µA
Data Retention Setup Time	t_{CDR}	$t_{su(DR)}$	See Data Retention Waveforms (above)	0			ns
Operating Recovery Time	t_R	t_{rec}		t_{cR}			ns

Test Configuration for Functional Check

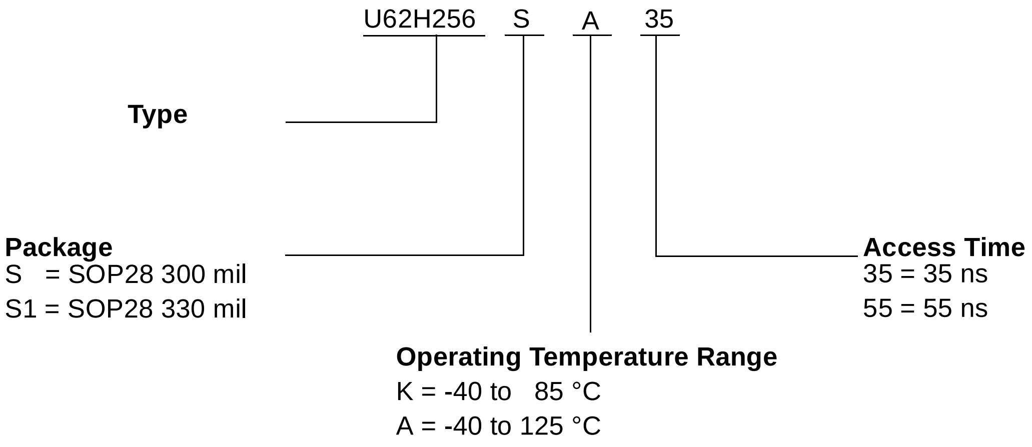


[1)] In measurement of $t_{dis(E)}$,$t_{dis(W)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 5.0 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_I		7	pF
Output Capacitance		C_o		7	pF

All pins not under test must be connected with ground by capacitors.

IC Code Numbers



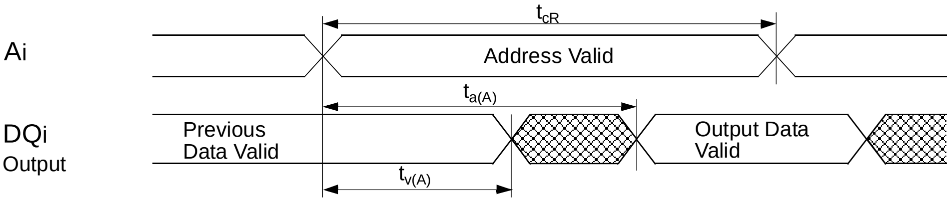
Package
S = SOP28 300 mil
S1 = SOP28 330 mil

Access Time
35 = 35 ns
55 = 55 ns

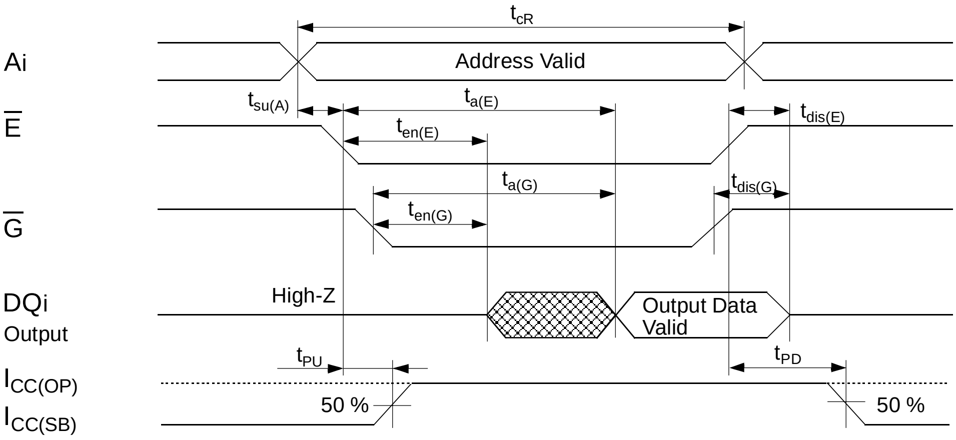
Operating Temperature Range
K = -40 to 85 °C
A = -40 to 125 °C

The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

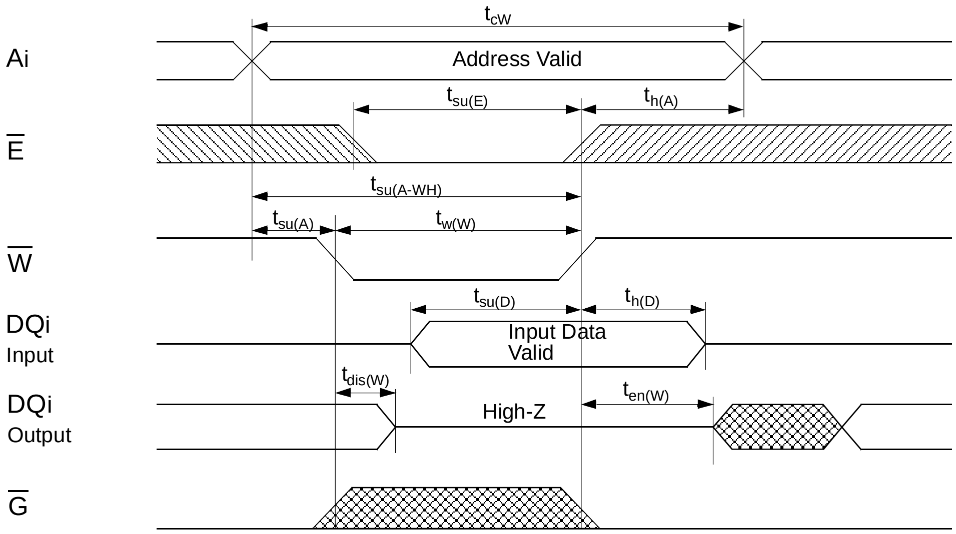
Read Cycle 1: A_i-controlled (during Read Cycle : $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$)



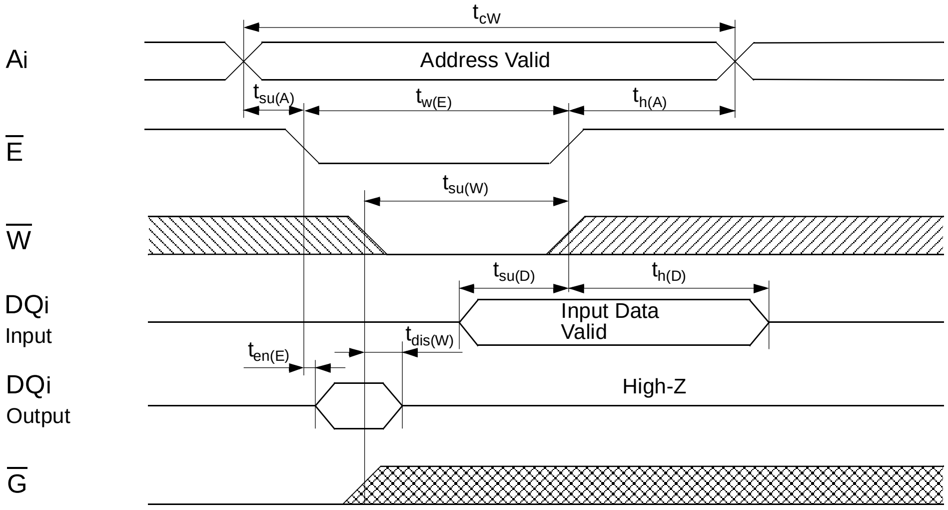
Read Cycle 2: $\overline{G}$-, $\overline{E}$-controlled (during Read Cycle: $\overline{W} = V_{IH}$)



Write Cycle1: $\overline{W}$-controlled



Write Cycle 2: $\overline{E}$-controlled



undefined ▩ L- to H-level ▨ H- to L-level ▧

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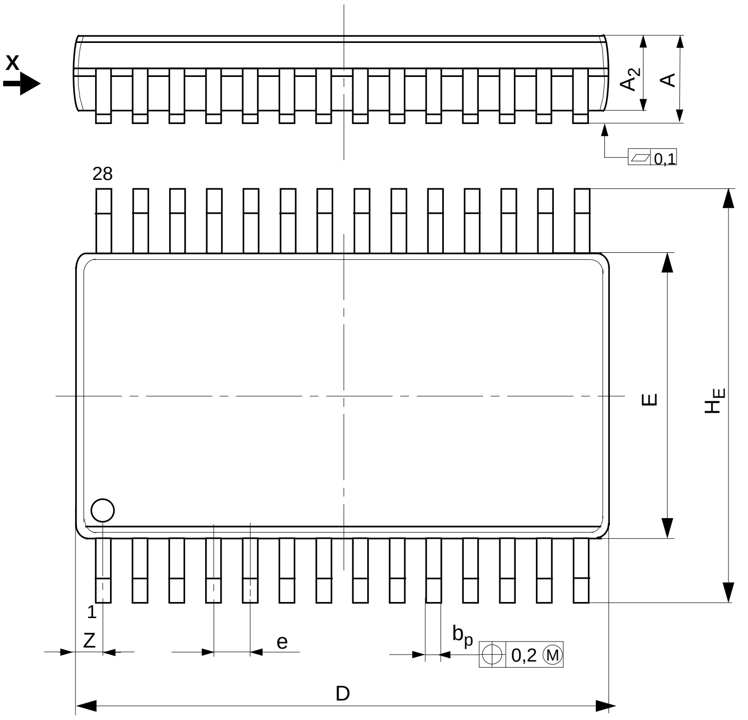
ZMD	**Package SOP28** (300 mil)	**MDS** **715**

Supersedes
Edition 06.92
1. Amendment 09.93

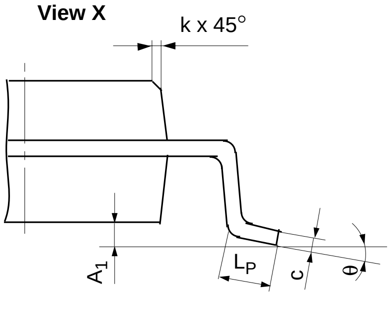
Dimensions in millimetres

Based on IEC 191-2Q: Type 075E06 B

1 Dimensions



View X



Dimensions of Sub-Group B1	
A_{max}	2,65
b_{Pmin}	0,35
b_{Pmax}	0,49
e_{nom}	1,27
H_{Emin}	10,00
H_{Emax}	10,65
L_{Pmin}	0,40
Z_{max}	0,81

Dimensions of Sub-Group C1	
A_{min}	2,35
A_{1min}	0,10
A_{1max}	0,30
A_{2min}	2,25
A_{2max}	2,45
c_{min}	0,23
c_{max}	0,32
D_{min}*	17,70
D_{max}*	18,10
E_{min}*	7,40
E_{max}*	7,60
k_{min}	0,25
θ_{min}	0°
θ_{max}	8°

* without mold-flash

2 Weight	≤ 0,8 g
3 Package Body Material	Low Stress Epoxy
4 Lead Material	FeNi-Alloy or Cu-Alloy
5 Lead Finish	solder plating
6 Lead Form	Z-bends

Package SOP28
(330 mil)

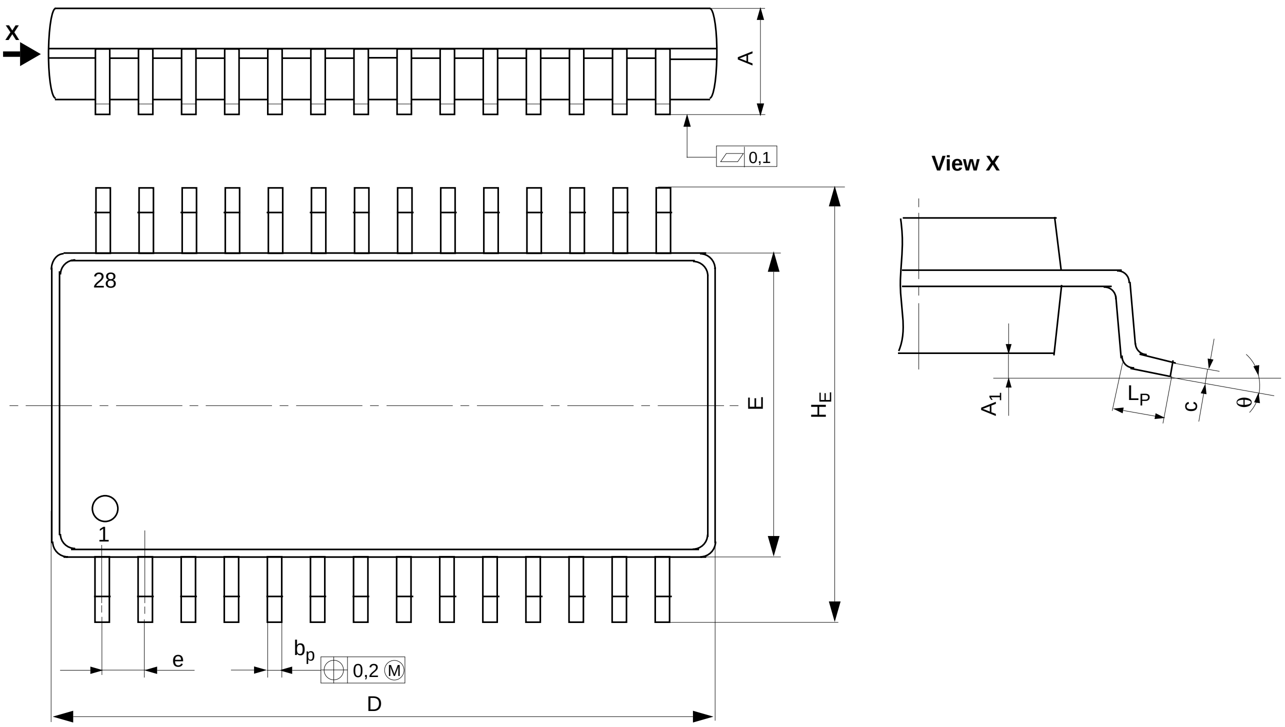
MDS
733

Supersedes
Edition 09.93

Dimensions in millimetres

Based on JEDEC: JEP95 MO-059 AC

1 Dimensions



Dimensions of Sub-Group B1	
A_{max}	2,54
b_{Pmin}	0,35
b_{Pmax}	0,50
e_{nom}	1,27
H_{Emin}	11,76
H_{Emax}	12,12
L_{Pmin}	0,50

Dimensions of Sub-Group C1	
A_{min}	2,25
A_{1min}	0,10
A_{1max}	0,30
c_{min}	0,14
c_{max}	0,32
D_{min}	17,90
D_{max}*	18,30
E_{min}	8,60
E_{max}*	8,90
θ_{min}	0°
θ_{max}	8°

* without mold-flash

2 Weight	≤ 0,8 g
3 Package Body Material	Low Stress Epoxy
4 Lead Material	FeNi-Alloy or Cu-Alloy
5 Lead Finish	solder plating
6 Lead Form	Z-bends

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