UAA3535

Low-power GSM GPRS triple-band Near-Zero IF transceiver

Overview

The UAA3535 is a low-power GSM triple-band transceiver and is the first product based on the new Philips Semiconductors N-ZIF (Near-Zero Intermediate Frequency) RF architecture. The UAA3535 is a GSM900/1800/1900 GPRS Class 12 -capable single-chip RF solution.

Features

- Triple-band RF solution for GSM900/1800/1900 cellular phone systems
- Integrated on-chip data services: GPRS Class 12 (4RX-4TX)
- Low-cost N-ZIF architecture because of the low external components count
- Excellent power consumption performance
- Low noise and wide dynamic range Near Zero IF receiver:
  - More than 35-dB on-chip image rejection in receiver
  - More than 64-dB gain control range in receiver
- Integrated IF channel filter
- Integrated TX low pass filters
- High precision I.Q modulator
- Multi-Band Tx modulation loop architecture including offset mixer and phase-frequency detector
- Dual PLL with on chip fully integrated IF VCO
- Fully differential design minimizing cross-talk and spurs
- Functional down to 2.5V and up to 3.6 V
- 3-wire serial bus interface
- LQFP48 package.

This new architecture removes a conversion step between the RF and the baseband. Compared to a traditional double conversion architecture, it is a major breakthrough towards higher integration since N-ZIF also allows to remove the costly external IF channel filter.

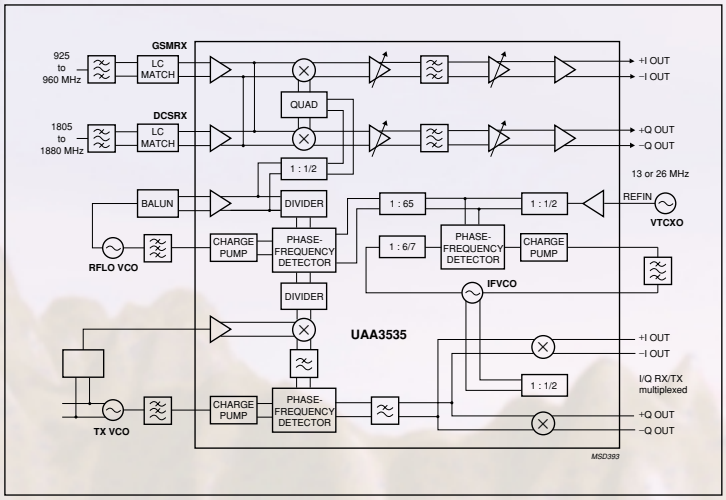
The UAA3535 enables class 12 (4RX, 4TX) GPRS (General Packet Radio Service), meaning faster data rates and thus enabling more data communications applications, combining low-cost and high performance.

It integrates the receiver and most of the transmitter section of GSM900/1800/1900 hand-held transceiver. It also includes the IF channel filter with high-dynamic range, the LNA with image rejection mixer, the frequency synthesisers, as well as the Transmit Offset Loop with all filters integrated. The UAA3535, running at 2.5V, interfaces with standard A/D converters.

Availability

The UAA3535 RF is Full-Type-Approved and is available immediately. This single-chip solution is manufactured in BiCMOS 0.5µm and is packaged in LQFP48. The UAA3535 interfaces with current and future Philips Semiconductors' products and will be at the heart of our system solution offering.

Functional Description



RF Receiver

The receiver front-end converts the aerial RF signal from EGSM (925 - 960 MHz), DCS (1805 - 1880 MHz) or PCS (1930 - 1990 MHz) bands down to a Near-Zero intermediate frequency (IF). The first stages are symmetrical low noise amplifiers (LNAs), followed by an IQ down-mixer. The IQ down-mixer consists of two mixers in parallel but is driven by quadrature out of phase LO signals. The In phase (I) and Quadrature phase (Q) IF signals are then low pass filtered to provide protection from high frequency offset interferers. The Near-Zero IF I and Q signals are then fed into the channel filter.

Channel filter and AGC

The front-end near Zero IF I and Q outputs enters the integrated bandpass channel filter. Being filtered the Near-Zero IF I and Q are further amplified with provision for 68dB Automatic Gain Control (AGC) and DC offset compensation.

IQ modulator

I and Q baseband signals are applied to the IQ modulator that shifts the modulation spectrum up to the transmit IF. It is designed for low harmonic distortion, low carrier leakage and high image rejection to keep the phase error as small as possible. The modulator is loaded at its IF output by an integrated low pass filter that suppress unwanted spurs prior to get into the phase detector.

Transmit modulation loop

The analog transmit modulation loop is composed by on-chip offset mixer, a phase/frequency detector working in and by off-chip loop filter and transmit VCO. The analog PLL copies the modulation to the off-chip transmit VCO and acts as a tracking filter. A PLL of at least third order is required to meet noise requirements at 20 MHz offset from carrier. The PLL bandwidth must be greater than 600 kHz in order to keep a low dynamic phase error and to minimize the acquisition time.

RF and IF LO sections

The RF LO input covering the 1788 to 2002 MHz bandwidth is connected to an external RF VCO module. The RF LO section includes the LO buffering for the RF PLL, a divider by two or one for GSM and DCS/PCS respectively which drives a quadrature generation network for use in the RX IQ down-mixer or the transmit modulation loop offset mixer. The IF LO section consists in a fully integrated IF VCO which internally provides the IQ modulator with the necessary quadrature signals.

Dual PLL

A high performance dual PLL is included on chip which allows to synthesize the frequencies of the RF VCO off chip and that of the IF VCO on chip. Very low close-in phase noise is achieved allowing to widen the PLL loop bandwidth for shorter settling time, providing GPRS Class 12 capabilities in terms of hardware. The charge pump circuit has very low leakage current, in the nA range, so that the spurs are hardly detectable. The 'main' path consists in a programmable dividers chain that divide the RF and IF LO signals down to frequencies of 200 kHz and 13 MHz respectively. Their phase is then compared into a digital phase/frequency detector (PFD) to that of a reference signal divided from an external 13 MHz (or 26 MHz) clock signal. The phase error information is fed back to the VCO via the charge pump circuit that 'sinks' into or 'sources' current from the loop filter capacitor, changing the VCO frequency such that the loop gets finally 'phase locked'.

N-ZIF architecture

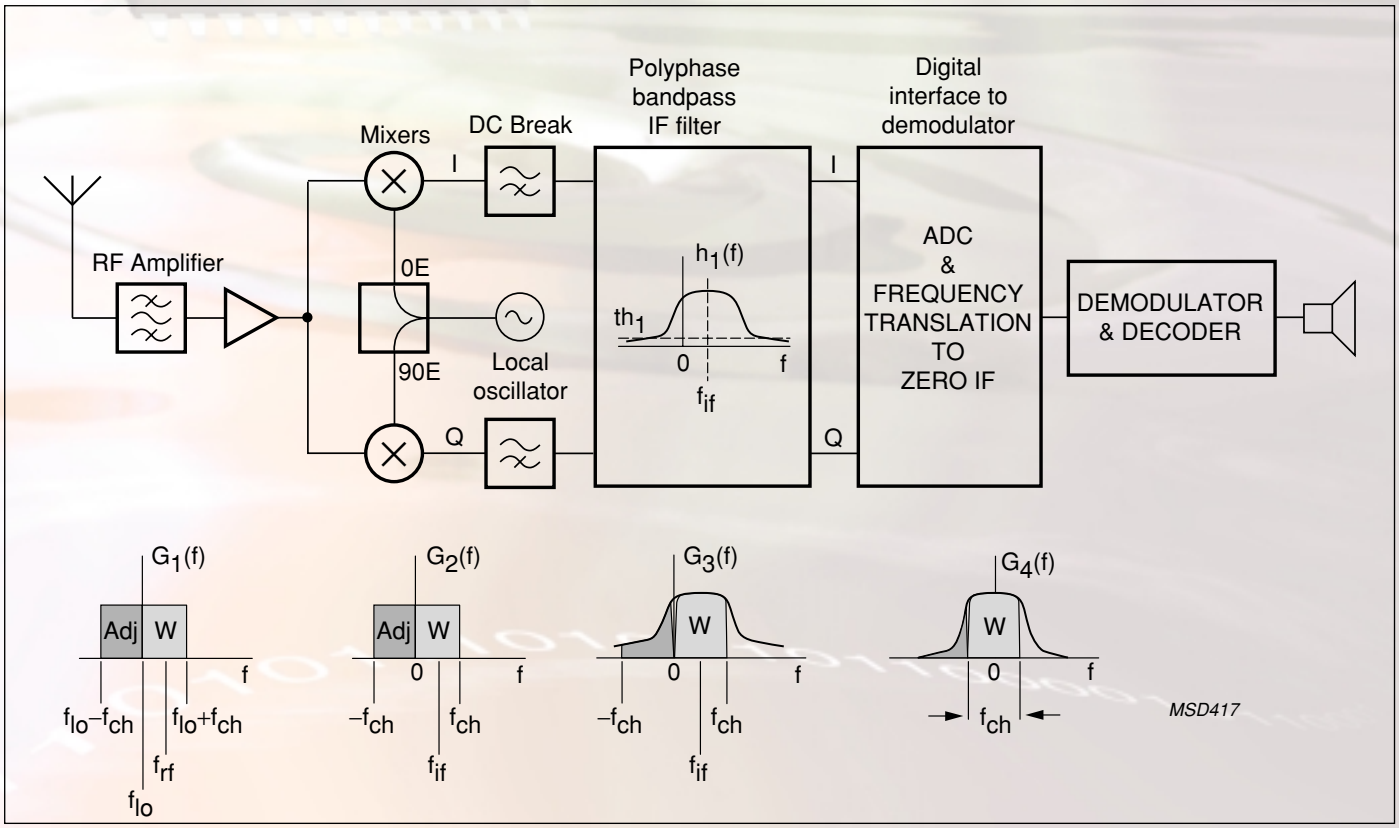
The N-ZIF architecture integrates many different features including a high dynamic range IF channel filter, a low-noise amplifier (LNA) with image rejecting front end, frequency synthesizers and a transmit offset loop with integrated filters. It provides a definitive advantage compared to Zero-IF (ZIF) solutions in terms of immunity to interference, RF development cost, time and manufacturing. In addition to providing simplified signal processing for GSM applications, the high integration level it achieves provides significant cost and size reductions.

Future

This architecture will pave the way towards 3G. The next integration step will allow EDGE (Enhanced Data rates for GSM Evolution), with an even higher integration level to stay on the leading edge with our cellular product offering and with significant advantages compared to double conversion or ZIF architectures.

Philips Semiconductors is already working on the forthcoming generations of cellular products.

In addition to enhanced data rates, Philips Semiconductor's next generation of chipsets will integrate new capabilities such as Bluetooth or FM radio and will directly address 3G standards such as UMTS and W-CDMA.



Near-Zero IF architecture - it eliminates the need for an external SAW filter and also prevents DC errors by allowing a DC break to be inserted into the IF path. The filters that are required are non-critical and can seasily be implemented on-chip.

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