Semicustom Products

UT0.6µ Gate Array Family

Data Sheet

Jan. 2000

FEATURES

- ❑ Multiple gate array sizes up to 600,000 usable equivalent gates
- ❑ Toggle rates up to 215 MHz
- ❑ Advanced 0.6µ (0.5µL_{eff}) silicon gate CMOS processed in a commercial fab
- ❑ Operating voltage of 5V and 3.3V
- ❑ Multiple product assurance levels available, i.e. QML, military, industrial, etc.
- ❑ Designed specifically for high reliability applications
- ❑ JTAG (IEEE 1149.1) boundary-scan supported
- ❑ Extensive package offerings including PQFP, CQFP, PGA and BGA
- ❑ Design support using Mentor Graphics®, and Synopsys™ in VHDL or Verilog design languages on HP®, NT and Sun® workstations❑Supports cold sparing for low power down applications
- ❑ Supports voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus

PRODUCT DESCRIPTION

The high-performance UT0.6µ gate array family features densities up to 600,000 equivalent gates and is available in multiple product assurance levels such as QML, military and industrial grades.

The UT0.6µ gate array family silicon is fabricated at American Microsystems Incorporated (AMI). Developed using UTMC's patented architectures, the UT0.6µ array family uses a highly efficient continuous column transistor architecture for the internal cell construction. Combined with state-of-the-art placement and routing tools, the utilization of available transistors is maximized using three levels of metal interconnect.

The UT0.6µ family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX equivalent functions, as well as, configurable RAM and other cores. UTMC's core library includes the following functions:

- Intel 80C31® equivalent
- Intel 80C196® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- Configurable RAM

Table 1. Gate Densities

DEVICE PART NUMBERS	EQUIVALENT USABLE GATES[1]	SIGNAL I/O[2]	POWER & GROUND PADS[3]
UT25	3,400 - 25,000	177	40
UT50	50,000	177	40
UT75	75,000	259	86
UT100	100,000	259	86
UT150	150,000	259	86
UT200	200,000	400	152
UT250	250,000	400	152
UT300	300,000	400	152
UT350	350,000	450	170
UT400	400,000	450	170
UT450	450,000	450	170
UT500	500,000	450	170
UT550	550,000	450	170
UT600	600,000	450	170

Notes:
1. Based on NAND2 equivalents. Actual usable gate count is design-dependent. Estimates reflect a mix of functions including RAM.
2. Includes five pins that may or may not be reserved for JTAG boundary-scan, depending on user requirements.
3. Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.

Low-noise Device and Package Solutions

The UT0.6µ array family's output drivers feature programmable slew rate control for minimizing noise and switching transients. This feature allows the user to optimize edge characteristics to match system requirements. Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, UTMC offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes. These planes provide lower overall resistance/inductance through power and ground-paths which minimize voltage drops during periods of heavy switching.

UTMC's CQFP packages feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. PQFP packages are available for applications that require plastic for automatic insertion, weight and cost considerations. For high pin count applications, a full line of PGA and BGA packages are available.

In addition to the packages listed in Table 2, UTMC offers custom package development and package tooling modification services for individual requirements.

Table 2. Packages

PACKAGE TYPE/ LEADCOUNT[1]	UT25	UT50	UT75	UT100	UT150	UT200	UT250	UT300	UT350	UT400	UT450	UT500	UT550	UT600
CQFP														
68	X	X												
84	X	X												
132	X	X	X	X	X									
172	X	X	X	X	X	X	X	X						
196	X	X	X	X	X	X	X	X						
224			X	X	X	X	X	X						
256			X	X	X	X	X	X	X	X	X	X	X	X
304			X	X	X	X	X	X	X	X	X	X	X	X
340						X	X	X	X	X	X	X	X	X
PQFP														
128	X	X												
144	X	X												
160	X	X	X	X	X									
208	X	X	X	X	X	X	X	X						
PGA[2]														
84	X	X												
120	X	X	X	X	X									
209	X	X	X	X	X									
281			X	X	X	X	X	X	X	X	X	X	X	X
299			X	X	X	X	X	X	X	X	X	X	X	X
447						X	X	X	X	X	X	X	X	X
BGA														
352			X	X	X	X	X	X	X	X	X	X	X	X
456						X	X	X	X	X	X	X	X	X
512											X	X	X	X

Notes:
1. The number of device I/O pads available may be restricted by the selected package.
2. PGA packages have one additional non-connected index pin (i.e., 84 + 1 index pin = 85 total package pins for the 85 PGA). Contact UTMC for specific package drawings.

Extensive Cell Library
The UT0.6µ family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as, RAM and other library functions. User-selectable options for cell configurations include scan for all register elements, as well as output drive strength. UTMC's core library includes the following functions:

- Intel® 80C31 equivalent
- Intel® 80C196 equivalent
- MIL-STD-1553 functions (BCRTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- Standard microprocessor peripheral functions
- Configurable RAM
- RISC Microcontroller

Refer to UTMC's UT0.6µ Design Manual for complete cell listing and details.

I/O Buffers
The UT0.6µ gate array family offers up to 442 signal I/O locations (note: device signal I/O availability is affected by package selection and pinout.) The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 2 to 16mA. To drive larger off-chip loads, output drivers may be combined in parallel to provide additional drive up to 32mA.

Other I/O buffer features and options include:

- Slew rate control
- Pull-up and pull-down resistors
- TTL, CMOS, and Schmitt levels
- Cold sparing
- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus

JTAG Boundary-Scan
The UT0.6µ arrays provide for a test access port and boundary-scan that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits this capability offers include the following:

- Allows easy test of complex assembled printed circuit boards
- Can be used to gain access to and control internal scan paths
- Can be used to initiate Built-In Self Test

Clock Driver Distribution

UTMC design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance
UTMC specializes in high-performance circuits designed to operate in high reliability environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, supply voltage, operating temperature, and processing tolerance. The UT0.6µ array family simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation
Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. For a rigorous power estimating methodology, refer to the UTMC UT0.6µ Design Manual or consult with a UTMC Applications Engineer.

Typical Power Dissipation

1.1µW/Gate-MHz@5.0V	0.4µW/Gate-MHz@3.3V

Table 3. Typical Cell Delays

CELL	OUTPUT TRANSITION	PROPAGATION DELAY [1]	
Internal Gates		**V_{DD} = 5.0V**	**V_{DD} = 3.3V**
INV1, Inverter	HL	.19	.26
	LH	.30	.40
INV4, Inverter 4X	HL	.10	.11
	LH	.199	.24
NAND2, 2-Input NAND	HL	.29	.38
	LH	.30	.40
NOR2, 2-Input NOR	HL	.18	.27
	LH	.44	.62
DFF - CLK to Q	HL	1.23	1.73
	LH	1.13	1.65
Latch - CLK to Q	HL	1.18	1.70
	LH	.91	1.29
Output Buffers			
OC5050N4, CMOS	HL	2.45	2.90
	LH	2.06	4.20
OT5050N4, TTL, 4mA	HL	5.45	6.52
	LH	4.42	7.94
OT5050N12, TTL, 12mA	HL	4.35	5.87
	LH	3.36	5.66
Input Buffers			
IC5050, CMOS	HL	.66	.93
	LH	.46	.73
IC5050, TTL	HL	.88	1.73
	LH	.71	1.63

Note:
1. All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads.

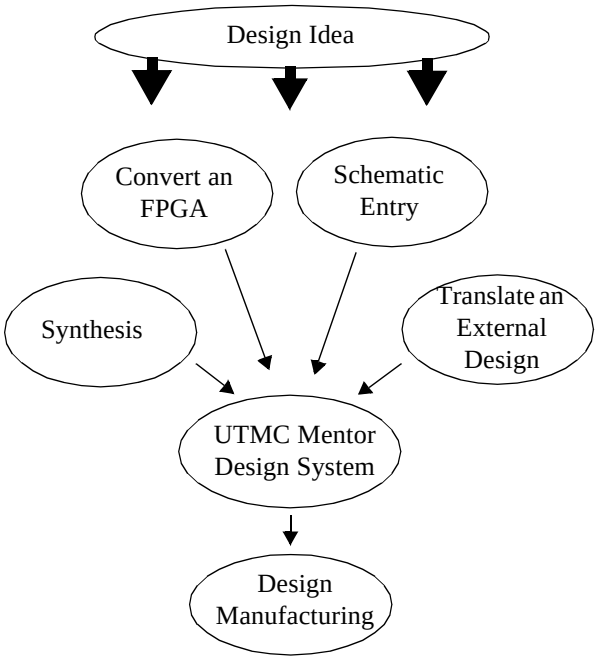
ASIC DESIGN SOFTWARE

Using a combination of state-of-the-art third-party and proprietary design tools, UTMC delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

UTMC's flexible circuit creation methodology supports high level design by providing UT0.6µ libraries for Mentor Graphics and Synopsys synthesis tools. Design verification is performed in the Mentor Graphics environment or with any VHDL VITAL-compliant simulator using UTMC's robust libraries. UTMC also supports Automatic Test Program Generation to improve design testing.

UTMC MENTOR GRAPHICS DESIGN SYSTEM

The UTMC Mentor Graphics Design System software is fully integrated into the Mentor Graphics design environment, making it familiar and easy to use. UTMC tools support Mentor functions such as cross-highlighting, graphical menus, and design navigation.



UTMC Mentor Graphics Design Flow

After creating a design in the Mentor Graphics environment, you can easily verify the design for electrical rules compliance with the UTMC Logic Rules Checker. Testability can be verified with the UTMC Tester Rules Checker. Both of these tools are fully integrated into the Mentor Graphics Environment.

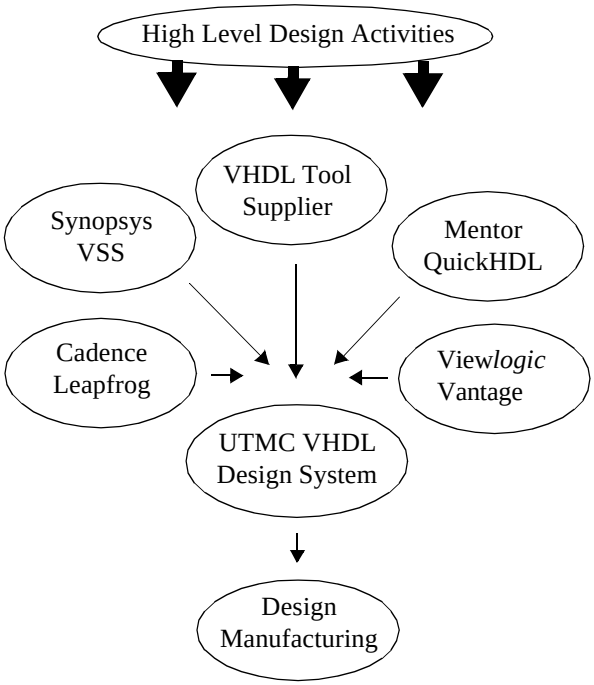
When you have completed all design activities, UTMC's Design Transfer tool captures all the required files and prepares them for easy transfer to UTMC. UTMC uses this data to convert your design into a packaged and tested device.

ADVANTAGES OF THE UTMC MENTOR DESIGN SYSTEM

- The UTMC Mentor Graphics Design System is among the most powerful and respected tool systems in the industry.
- UTMC customers have successfully used the UTMC Mentor Graphics Design System for over 5 years.
- UTMC's Logic and Tester Rules Checker tools allow you to verify partial or complete designs for compliance with UTMC manufacturing practices and procedures.
- The Design System accepts pre-and post-layout timing information to ensure your design results in devices that meet your specifications.
- The Design System supports Autologic II, and database transfer between Synopsys and Mentor.
- The Design System supports powerful Mentor Graphics ATPG capabilities.

UTMC VHDL DESIGN SYSTEM

The UTMC VHDL Design System provides VITAL- compliant sign-off quality libraries. You can use these libraries to verify an ASIC design you have created in most popular VHDL design environments.



UTMC VHDL Design Flow

With the library capabilities UTMC provides, you can use High Level Design methods to synthesize your design for simulation. UTMC also provides tools to verify that your VHDL design can be manufactured at UTMC - completely in your VHDL environment.

ADVANTAGES OF THE UTMC VHDL DESIGN SYSTEM

- The UTMC VHDL Design System gives you the freedom to use tools from Synopsys, Mentor Graphics, Cadence, View*logic*, and other VHDL VITAL-compliant vendors to help you synthesize and simulate a design in VHDL.
- UTMC's Logic and Tester Rules Checker allow you to verify partial or complete designs for compliance with UTMC manufacturing rules.
- The Design System accepts back-annotation of timing information through SDF.
- Your design stays entirely within VHDL, preventing conversion problems and issues.

XDT^{sm} (eXternal Design Translation)

Through UTMC's XDT services, customers can convert an existing non-UTMC design to UTMC's processes. The XDT tool is particularly useful for converting an FPGA to a UTMC gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to UTMC formats and libraries. Industry standard netlist formats supported by UTMC include:

- VHDL
- Verilog HDL^{TM}
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

TOOLS SUPPORTED BY UTMC

Mentor Graphics	Synopsys	VHDL
Autologic II®	Design Compiler^{TM}	Synopsys VSS^{TM}
QuickSimII®	VHDL Compiler^{TM}	Mentor Graphics QuickHDL™
QuickfaultII®	TestSim^{TM}	Cadence Leapfrog
QuickGradeII®	Verilog HDL Compiler^{TM}	Viewlogic Vantage^{TM}
FastScan / Flextest / DFTAdvisor®	Test Compiler Plus^{TM}	Any VITAL-compliant VHDL Tool

TRAINING AND SUPPORT

Qualified UTMC instructors conduct training classes tailored to meet individual needs. These classes can address a wide mix of engineering backgrounds and specific customer concerns. Applications assistance is also available through all phases of ASIC Design.

PHYSICAL DESIGN

Using three layers of metal interconnect, UTMC achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 600,000 equivalent gates.

Test Capability

UTMC supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Scan design options are available on all UT0.6µ storage elements. Automatic test program development capabilities handle large vector sets for use with UTMC's LTX/Trillium MicroMasters, supporting high-speed testing (up to 80MHz with pin multiplexing).

Unparalleled Quality and Reliability

UTMC is dedicated to meeting the stringent performance requirements of avionics and defense systems suppliers. UTMC maintains the highest level of quality and reliability through our Quality Management Program under MIL-PRF-38535 and ISO-9001. In 1988, we were the first gate array manufacturer to achieve QPL certification and qualification of our technology families. Our product assurance program has kept pace with the demands of certification and qualification.

Our quality management plan includes the following activities and initiatives.

- Quality improvement plan
- Failure analysis program
- SPC plan
- Corrective action plan
- Change control program
- Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV) assessment program
- Certification and qualification program

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). The TCV utilizes test structures to evaluate hot carrier aging, electromigration, and time dependent test samples for reliability testing. Data from the wafer-level testing can provide rapid feedback to the fabrication process, as well as establish the reliability performance of the product before it is packaged and shipped.

ABSOLUTE MAXIMUM RATINGS [1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 6.0V
$V_{I/O}$	Voltage on any pin	-0.3V to V_{DD} + 0.3
T_{STG}	Storage temperature	-65 to +150°C
T_J	Maximum junction temperature	+175°C
I_{LU}	Latchup immunity	$\pm$150mA
I_I	DC input current	$\pm$10mA
T_{LS}	Lead temperature (soldering 5 sec)	+300°C

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	3.0 to 5.5V
T_C	Case temperature range	-55 to +125C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] TTL inputs CMOS, OSC inputs				 0.8 $.3V_{DD}$	V
V_{IH}	High-level input voltage [1] TTL inputs CMOS, OSC inputs		 2.2 $.7V_{DD}$			V
V_T+	Schmitt Trigger, positive going [1] threshold				4.0	V
V_T-	Schmitt Trigger, negative going [1] threshold		1.0			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		1.5		2.0	V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors, OSC Inputs with pull-up resistors Inputs with pull-up resistors, OSC	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{DD}$	 -1 +150 -10 -900 -10		 1 +900 +10 -150 +10	µA
V_{OL}	Low-level output voltage [3] TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	 I_{OL} = 2.0mA I_{OL} = 4.0mA I_{OL} = 8.0mA I_{OL} = 12.0mA I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			 0.4 0.4 0.4 0.4 0.05 0.25 1.0	V
V_{OH}	High-level output voltage [3] TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	 I_{OH} = -2.0mA I_{OH} = -4.0mA I_{OH} = -8.0mA I_{OH} = -12.0mA I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	 2.4 2.4 2.4 2.4 V_{DD}-0.05 V_{DD}-0.25 3.5			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	$V_O = V_{DD}$ and V_{SS}	 -5 -10 -20 -30		 5 10 20 30	µA
I_{OS}	Short-circuit output current [2,4] TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	$V_O = V_{DD}$ and V_{SS}	 -50 -100 -200 -300		 50 100 200 300	mA
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V			1	mA
C_{IN}	Input capacitance [5]	*f* = 1MHz @ 0V		12		pF
C_{OUT}	Output capacitance [5] TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	*f* = 1MHz @ 0V		 11 12 14 22		pF
C_{IO}	Bidirect I/O capacitance [5] TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	*f* = 1MHz @ 0V		 13 15 23		pF

Notes:

* Contact UTMC prior to usage.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq$ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V ±.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] TTL inputs CMOS, OSC inputs				 0.8 $.3V_{DD}$	V
V_{IH}	High-level input voltage [1] TTL inputs CMOS, OSC inputs		 2.2 $.7V_{DD}$			V
V_T+	Schmitt Trigger, positive going [1] threshold				2.2	V
V_T-	Schmitt Trigger, negative going [1] threshold		.5			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		.4		1.0	V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors, OSC Inputs with pull-up resistors Inputs with pull-up resistors, OSC	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{DD}$	 -1 +100 -10 -700 -10		 1 +700 +10 -100 +10	µA
V_{OL}	Low-level output voltage [3] TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	 I_{OL} = 1.4mA I_{OL} = 2.8mA I_{OL} = 5.6mA I_{OL} = 8.4mA I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			 0.4 0.4 0.4 0.4 0.05 0.25 1.0	V
V_{OH}	High-level output voltage [3] TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	 I_{OH} = -1.4mA I_{OH} = -2.8mA I_{OH} = -5.6mA I_{OH} = -8.4mA I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	 2.4 2.4 2.4 2.4 V_{DD}-0.05 V_{DD}-0.25 2.0			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	$V_O = V_{DD}$ and V_{SS}	 -5 -10 -20 -30		 5 10 20 30	µA
I_{OS}	Short-circuit output current [2,4] TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	$V_O = V_{DD}$ and V_{SS}	 -50 -100 -200 -300		 50 100 200 300	mA
I_{DDQ}	Quiescent Supply Current	V_{DD} = 3.6V			1	mA
C_{IN}	Input capacitance [5]	*f* = 1MHz @ 0V		12		pF
C_{OUT}	Output capacitance [5] TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	*f* = 1MHz @ 0V		 11 12 14 22		pF
C_{IO}	Bidirect I/O capacitance [5] TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	*f* = 1MHz @ 0V		 13 15 23		pF

Notes:

* Contact UTMC prior to usage.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq$ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

Notes