Standard Products

UT908 MIL-STD-1553 PCI Interface Card

Advanced Product Information

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FEATURES

- 32-bit, 33MHz PCI (PCI Specification 2.1 compliant) to MIL-STD-1553 A/B Bus Controller, Remote Terminal, and Monitor
- Variety of customizable PCI connector configurations
  - 5.0V, 3.3V and universal add-in card
  - PMC (IEEE Std. P1386), PCMCIA
- Low operating and standby current by virtue of the UT69151 SµMMIT XTE power saving architecture
- MIL-STD-1553B Notice II RT
  - Internal command illegalization in RT mode, 16-bit read/write time-tag with user defined resolution, subaddress data buffereing
- Flexible Bus Controller architecture
  - Minor frame timing, efficient command chaining, status word polling
- Simultaneous RT/MT mode of operation
- Internal Memory Management Unit (MMU) interfaces host subsystem to 512Kbit SRAM
- Flexible Interrupt generation from the 1553 bus to PCI host
  - Programmable interrupt architecture, automatic interrupt logging available in all modes
- Built-In test capability
  - Supports IEEE Standard 1149.1 (JTAG)

INTRODUCTION

To solve the problem of interfacing multiple MIL-STD-1553 buses with a 32-bit, 33MHz PCI host, UTMC offers the UT908 MIL-STD-1553 PCI Interface Card. UTMC utilizes a pair of the SµMMIT XTEs to a PCI bridge device for intelligent interfacing between these two bus architectures. The card is offered with a variety of form factors such as PCI add-in card or PMC (pending IEEE Std. P1386) including both 3.3 and 5.0-Volt connectors and operation.

The UT908 implements dual redundant 1553 interface by utilizing multiple UT69151 SµMMIT XTEs. Each redundant 1553 channel may be configured as a full-featured bus controller, remote terminal, and monitor to meet the flexibility requirements of the latest avionic and satellite systems. Each of the SµMMIT device's configuration registers, status registers, and data memories are mapped to the local bus. Each of the SµMMITs has a powerful RISC processing unit providing automatic message handling, message status, general status, and interrupt information. The SµMMIT's register-based interface architecture provides many programmable functions, as well as extensive information relating device maintenance to the PCI host.