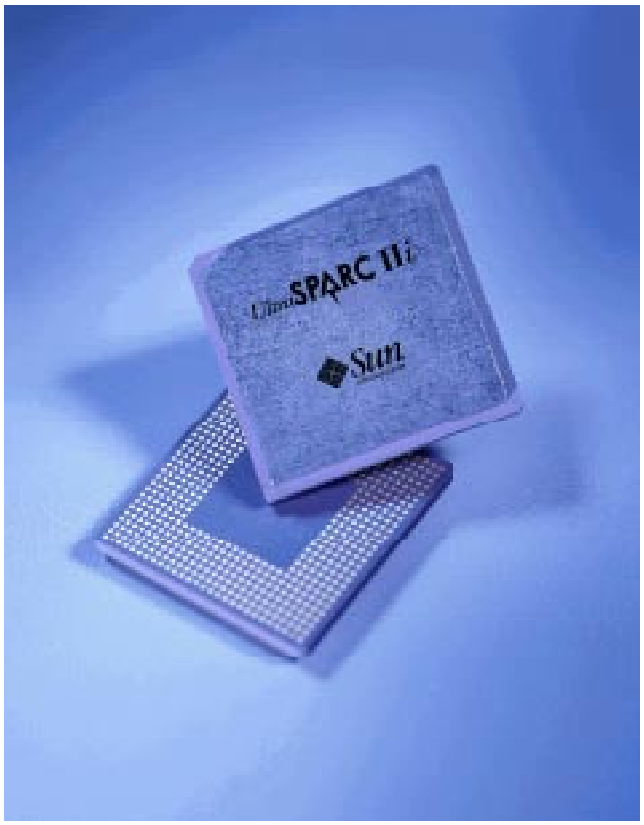
UltraSPARC™ i-Series

Integrated 270/300/333 MHz 64-bit RISC Single Chip Solution



UltraSparc™ i-Series Features

VIS™ Instruction Set for Data Networking Java Acceleration

All family members feature Sun's widely-acclaimed VIS™ V9 extended instruction set for new-media and data networking application acceleration: as fast as seven times the performance of traditional processors.

Software Support

The UltraSPARC IIi processor supports Sun's popular Solaris™ operating system and is binary-compatible with the broad array of existing SPARC™ applications. In addition, Sun is working with leading third-party real-time operating system (RTOS) suppliers for embedded applications.

The UltraSPARC i-Series family consists of processors at 270, 300, and 333MHz and modules at 270MHz/256Kb, 300MHz/512Kb, and 333MHz/2MB.

This innovative processor was designed to deliver proven system performance and features the award-winning UltraSPARC processor in a single-chip system solution. The UltraSPARC IIi processor incorporates a CPU, PCI bus interface, and memory controller to deliver the highest system performance at the lowest system implementation cost.

Its unmatched bandwidth performance makes it the ideal processor for network server solutions. It is also the optimal solution for the emerging high performance embedded market segment which includes new generations of Internet communication systems and advanced imaging technology.

Optimizing Overall System Performance

The UltraSPARC IIi processor series addresses traditional system performance degradation by integrating the complex, high speed communication within the IIi processor. Sun has eliminated these bandwidth-dependent bottlenecks by minimizing memory latency and maximizing I/O throughput, significantly boosting overall system performance.

Ease of Design

System design is eased with all high speed interconnects integrated into the IIi processor. System designers are thus able to harness the extremely high performance of the UltraSPARC IIi, while using PC-class, PCI-based mother boards and components. In addition, Sun offers a family of UltraSPARC IIi modules with fully integrated external cache.

PCI and UPA Support: Uncompromising Flexibility

The i-Series processors leverage standard high-performance memory and PCI components. The UltraSPARC IIi processor incorporates a high performance dual-mode 33/66 MHz 3.3-volt PCI bus that is version 2.1 PCI bus-compliant and delivers up to 200 MByte/sec of PIO data throughput. This interface can be connected to Sun's exclusive Advanced PCI Bridge (APB) chip to provide two fully independent 33 MHz 5-volt PCI buses that support a broad family of devices including Super IO, SCSI networking and graphics interface cards. Up to four of the optional APB chips can be used to support up to 32 PCI devices. The IIi maintains support of Sun's high-performance 800 MBytes/sec Ultra™ Port Architecture (UPA) high bandwidth bus interface for graphics and robust data applications at 300MHz operating frequency.

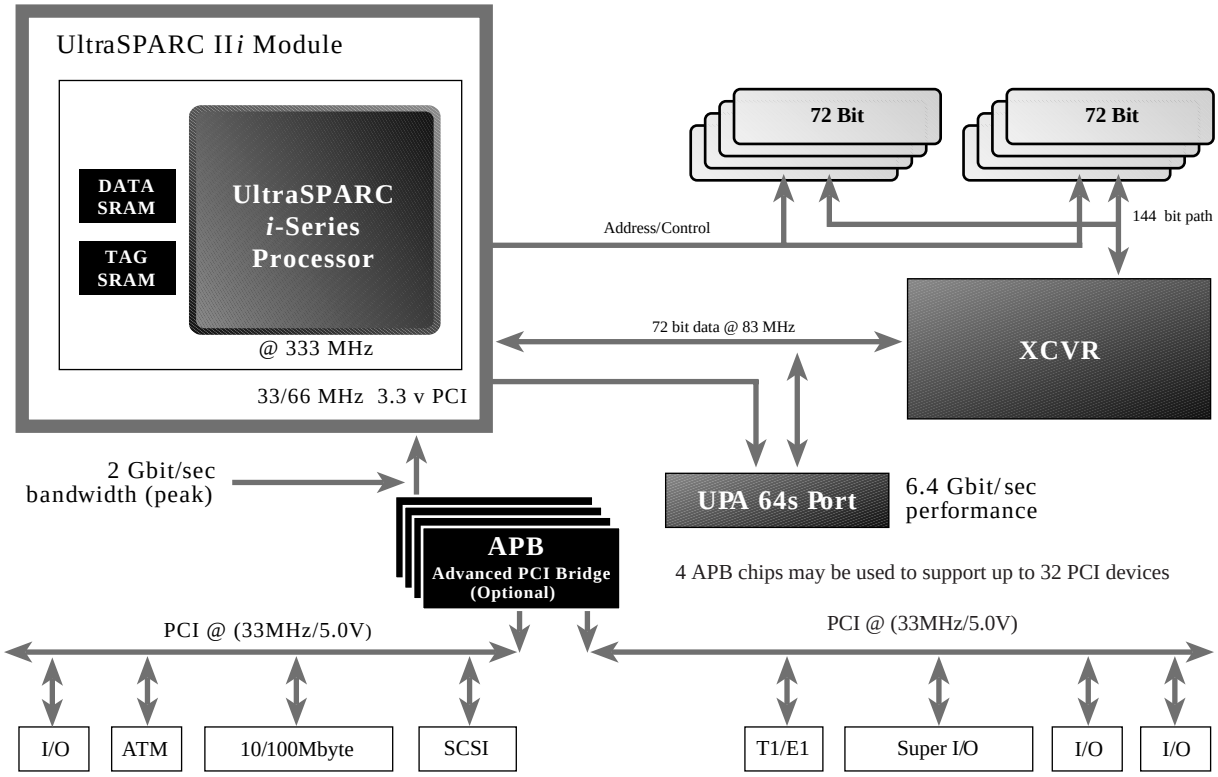
Dual-Mode Cache Support

The UltraSPARC i-Series incorporates a dual-mode cache capability. The standard performance mode enables the processor to take advantage of widely-available, lower cost cache while the performance mode supports the use of high-speed cache to optimize overall system performance.

An Incredible Value

The combination of UltraSPARC microprocessor performance, single chip integration and support for industry standard PCI devices delivers unbeatable performance from the leader in advanced computing.

UltraSPARC i-Series Architecture



UltraSPARC IIi Specifications

- SPARC V9 Architecture/Uniprocessor Design
- 333 MHz processor clock (lower speeds are also available)
- Binary Compatible with all SPARC Application code
- VIS (V9) Instruction Set
- 4-way SuperScalar Design, 64-bit Architecture
- 64-Bit Address Pointers
- External Cache Size: 256 Kbyte – 2MB
- External Cache Speed: 135–167 MHz
- DRAM Configurations: 16 MByte – 1Gbyte
- 144-bit Dram data bus with 8-bit ECC on each 64-bits of data
- 16 Kbyte Non-blocking Data Cache
- 16 Kbyte Instruction Cache
- Integrated 2nd Level Cache Controller Supports up to 2 Mbytes of synchronous SRAM
- 400 Mbyte/sec EDO Dram Memory subsystem
- 64-byte Block Load/Store Instructions
- Supports software data prefetch into L2 cache.
- Supports 800 Mbyte/sec UPA64s 64-bit slave interface for graphics or similar subsystems
- Integrated Rev 2.1 PCI compliant and JTAG support
- PCI DMA is cache coherent, with its own TLB to provide mapping and protection
- Power Supply is 2.5V core/3.3V I/O
- Advanced.35 micron CMOS technology
- Available on 256 Kbyte, 512 Kbyte and 2 Mbyte integrated modules

Estimated Performance:

- System Performance at 333 MHz with 2 Mbyte external cache:
  - SpecInt95 — 14.2
  - SpecFP95 — 16.9
- VIS performance 3-7X the performance of a traditional processor
- Bandwidth Performance
  - PCI bus DMA bandwidth —150 MBytes/sec @ 300MHz core
  - PCI bus PIO bandwidth — 200 MBytes/sec @ 300MHz core
  - UPA64 bandwidth — 800 MBytes/sec @ 300MHz core
  - Memory read/write bandwidth — 400 MBytes/sec @ 300MHz core

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