

Small switching (–20V, –1A)

US6J2

●Features

- 1) Two 2SK3018 transistors in a single TUMT package.
- 2) Mounting cost and area can be cut in half.
- 3) Low on-resistance.
- 4) Low voltage drive (2.5V) makes this device ideal for portable equipment.
- 5) Easily designed drive circuits.

●Applications

Interfacing, switching (–20V, –1A)

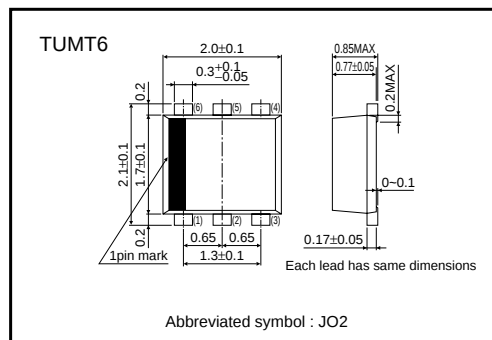
●Structure

Silicon P-channel
MOS FET

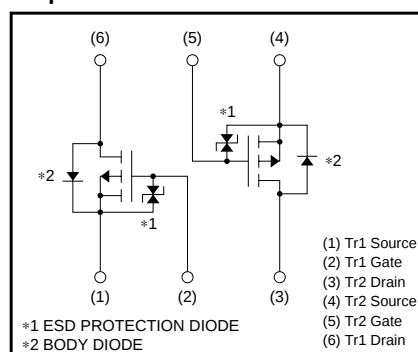
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6J2		○

●External dimensions (Unit : mm)



●Equivalent circuit



*A protection diode has been in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

Transistors

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	−20	V
Gate-source voltage		V _{GSS}	−12	V
Drain current	Continuous	I _D	±1	A
	Pulsed	I _{DP}	±4	A *1
Reverse drain current	Continuous	I _{DR}	−0.4	A *1
	Pulsed	I _{DRP}	−1.6	A
Total power dissipation (Tc=25°C)		P _D	1.0	W *2
Channel temperature		T _{ch}	150	°C
Range of Storage temperature		T _{stg}	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤50%

*2 With each pin mounted on the recommended lands.

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	−	−	±10	μA	V _{GS} =±12V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	−20	−	−	V	I _D = −1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	−	−	−1.0	μA	V _{DS} = −20V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	−0.7	−	−2.0	V	V _{DS} = −10V, I _D = −1mA
Static drain-source on-state resistance	R _{DS(on)}	−	280	390	mΩ	I _D = −1A, V _{GS} = −4.5V
		−	310	430	mΩ	I _D = −1A, V _{GS} = −4V
		−	570	800	mΩ	I _D = −0.5A, V _{GS} = −2.5V
Forward transfer admittance	Y _{fs}	0.7	−	−	S	V _{DS} = −10V, I _D = −0.5A
Input capacitance	C _{iss}	−	150	−	pF	V _{DS} = −10V
Output capacitance	C _{oss}	−	20	−	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	−	20	−	pF	f=1MHz
Turn-on delay time	t _{d(on)}	−	9	−	ns	I _D = −0.5A
Rise time	t _r	−	8	−	ns	V _{DD} ≐ −15V V _{GS} = −4.5V
Turn-off delay time	t _{d(off)}	−	5	−	ns	R _L =30Ω
Fall time	t _f	−	10	−	ns	R _G =10Ω
Total gate charge	Q _g	−	2.1	−	nc	V _{DD} ≐ −15V R _L =15Ω
Gate-source charge	Q _{gs}	−	0.5	−	nc	V _{GS} = −4.5V R _G =10Ω
Gate-drain charge	Q _{gd}	−	0.5	−	nc	I _D = −1A

Transistors

●Electrical characteristic curves

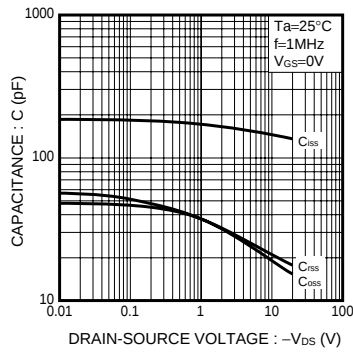


Fig.1 Typical Capacitance vs. Drain-Source Voltage

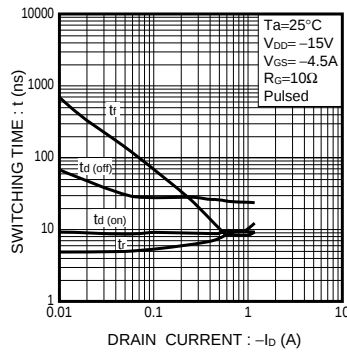


Fig.2 Switching Characteristics

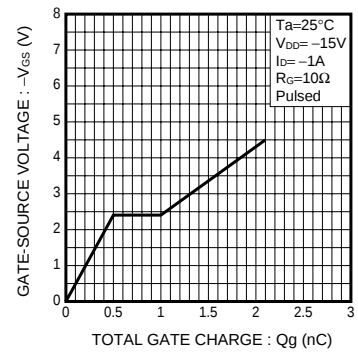


Fig.3 Dynamic Input Characteristics

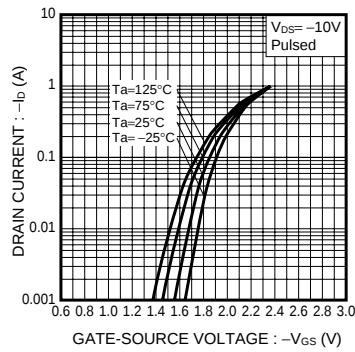


Fig.4 Typical Transfer Characteristics

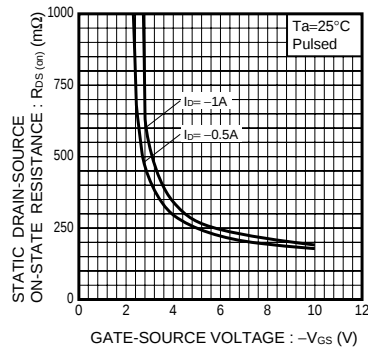


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

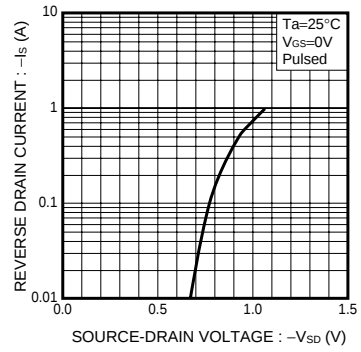


Fig.6 Reverse Drain Current vs. Source-Drain Voltage

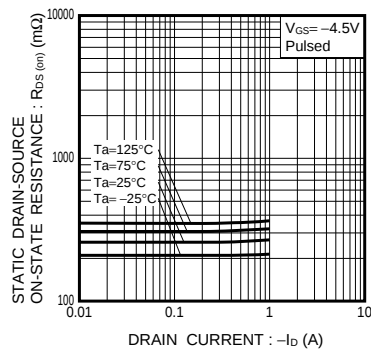


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (II)

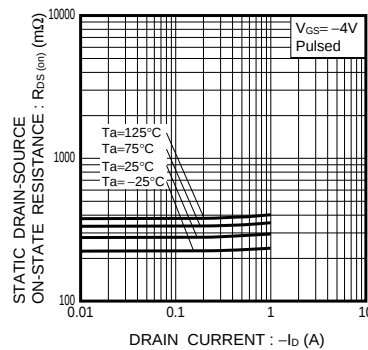


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (III)

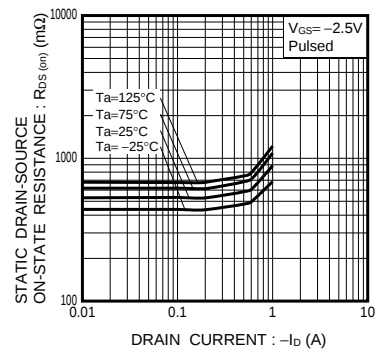


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (I)

Transistors

●Measurement circuits

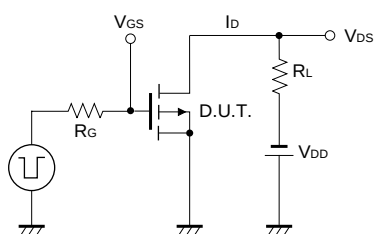


Fig.10 Switching Time Measurement Circuit

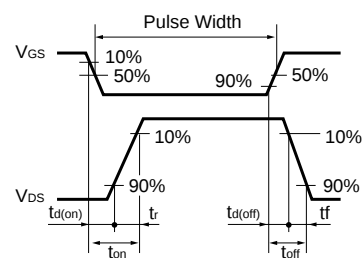


Fig.11 Switching Waveforms

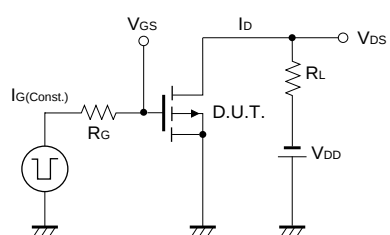


Fig.12 Gate Charge Measurement Circuit

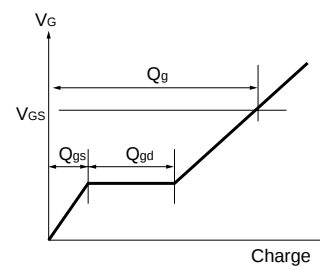


Fig.13 Gate Charge Waveform