UC1607(i)

Single-Chip, Ultra-Low Power
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1607(i) is an advanced high-voltage mixedsignal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1607(i) contain all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

M AIN APPLICATIONS

 Cellular Phones, Smart Phones, PDA and other battery operated palm top devices and/or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver supports 4shade-per-pixel, 128 COM x 128 SEG LCD, with vertical scroll support.
- Available either with or without I2C license.
- Support industry standard 8-bit parallel interface (8080 or 6800), 4-wire SPI (S8), and 2-wire I²C serial interface.
- Special driver structure and gray shade

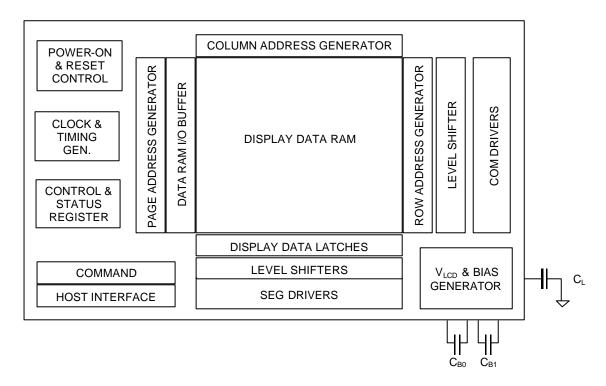
modulation scheme. Sharp image and ultralow power consumption under all display patterns.

- Support four multiplexing rates (64, 80, 102, 128), four frame rates and 48-32-48 partial display function.
- Self-configuring 8x charge pump with onchip pumping capacitor requires only 3 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Software programmable 4 temperature compensation coefficients.
- On-chip bypass capacitor for V_{LCD} makes V_{LCD} bypass capacitor optional for small LCD panels.
- On-chip Power-ON Reset and Software Reset commands, make RST pin optional.
- Very low pin count (9-pin, with I2C) allows exceptional image quality in COG format on conventional ITO glass.

 V_{DD} (digital) range: $2.4 \text{ V} \sim 3.3 \text{ V}$ V_{DD} (analog) range: $2.4 \text{ V} \sim 3.3 \text{ V}$ V_{DD} (analog) range: $2.4 \text{ V} \sim 3.3 \text{ V}$ V_{DD} (analog) range: $0.5 \text{ V} \sim 13.5 \text{ V}$

 Available in gold bump dies Bump pitch: 55µM min. Bump gap: 20µM min.

BLOCK DIAGRAM



1607 v1.3B