UC1602(i)

Single-Chip, Ultra-Low Power

65COM x 102SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1602(i) is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power COM and SEG drivers, UC1602(i) contain all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, and other battery operated devices and/or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver supports 65 COM x 102 SEG LCD.
- Support industry standard 8-bit parallel interface (8080 or 6800), 4-wire SPI (S8), and 2-wire I^2C serial interface.
- Two multiplexing rates (49, 65).
- Self-configuring 6x charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Software programmable 4 temperature compensation coefficients.
- On-chip bypass capacitor for V_{LCD} makes V_{LCD} bypass capacitor optional for small LCD panels.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- V_{DD} (digital) range: 2.4V ~ 3.3V
  V_{DD} (analog) range: 2.4V ~ 3.3V
  LCD V_{OP} range: 4.5V ~ 10.5V
- Available in gold bump dies
  Bump pitch: 55uM min.
  Bump gap: 20uM min.

ORDERING INFORMATION

Product ID	Description
UC1602iGAD	65 COM x 102 SEG LCD driver, with I^2C interface license.
UC1602xGAD	65 COM x 102 SEG LCD driver, no I^2C interface license.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon. However, unless I^2C licensing obligation is executed satisfactorily, it is not legal to use UltraChip product for I^2C applications. Unless I^2C version is ordered from UltraChip, the customer will take the responsibility for all such licensing liabilities.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and quality their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

TABLE OF REVISION HISTORY

Version	CONTENTS	DATE OF REVISION
1.0	First release	Jun. 07, 2001
1.1	Overall revision	Aug. 26, 2002
	(1) Recommended C_L value is adjusted to 5nF ~ 20nF (Page 5)	
	(2) V_{DD1} is renamed to V_{DD} (Page 5)	
	(3) TP3 is renamed to TST4 (Page 7)	
	(4) TP[2:0] is renamed to TP[3:1] (Page 7)	
	(5) C[0:101] is renamed to SEG[1:102] (Page 7)	
	(6) R[1~64] is renamed to COM[1~64] (Page 7)	
	(7) RIC is renamed to CIC (Page 7)	
	(8) Application circuits are added. (Page 17, 22, 23)	
	(9) Alignment Mark Information is presented (Page 39)	
	(10) Tray Information is presented. (Page 43)	

BLOCK DIAGRAM