Preliminary Rev 1.0

CLOCK GENERATOR FOR PENTIUM BASED SYSTEM

FEATURES

- Eight selectable CPU clocks operate up to 83.3 MHz
- Six PCI bus clocks support synchronous or asynchronous mode
- A 48MHz clock for USB requirement
- A 24MHz clock for I/O requirement
- A 14.318MHz clock for system reference
- Low-frequency test mode support
- Internal driving force adjustment for output clocks
- Frequency selection inputs were latched at Power-On Reset interval
- Low CPU/PCI clock skew
- 2.5V to 5V operation
- 50 percent duty cycle
- 28-pin 300mil SOP package

GENERAL DESCRIPTION

The UT8586SC is Phase-Locked-Loop frequency synthesizer designed specially for Pentium-based chip set systems. The integrated buffer minimizes skew and provides all the clocks required. A 14.318MHz Crystal oscillator provides the reference clock to the Phase-Locked-Loop for the standard Pentium mother board frequencies generation.

Either synchronous (CPU/2) or asynchronous (32MHz) PCI bus operation can be selected by latching data on BSEL input. Also UT8586SC provide low-frequency test mode for chip verification and output clock driving adjustment. It's pin-to-pin replacements for the ICW48C61-01, ICS9169C-23, CY2961 and PLL52C61-01.

The UT8586SC clock outputs can adjust the driving force internally. Inside UT8586SC, it supports 5 different speed VCO to accommodate different operation voltage supply from 2.5 Volt to 5.0 Volt.

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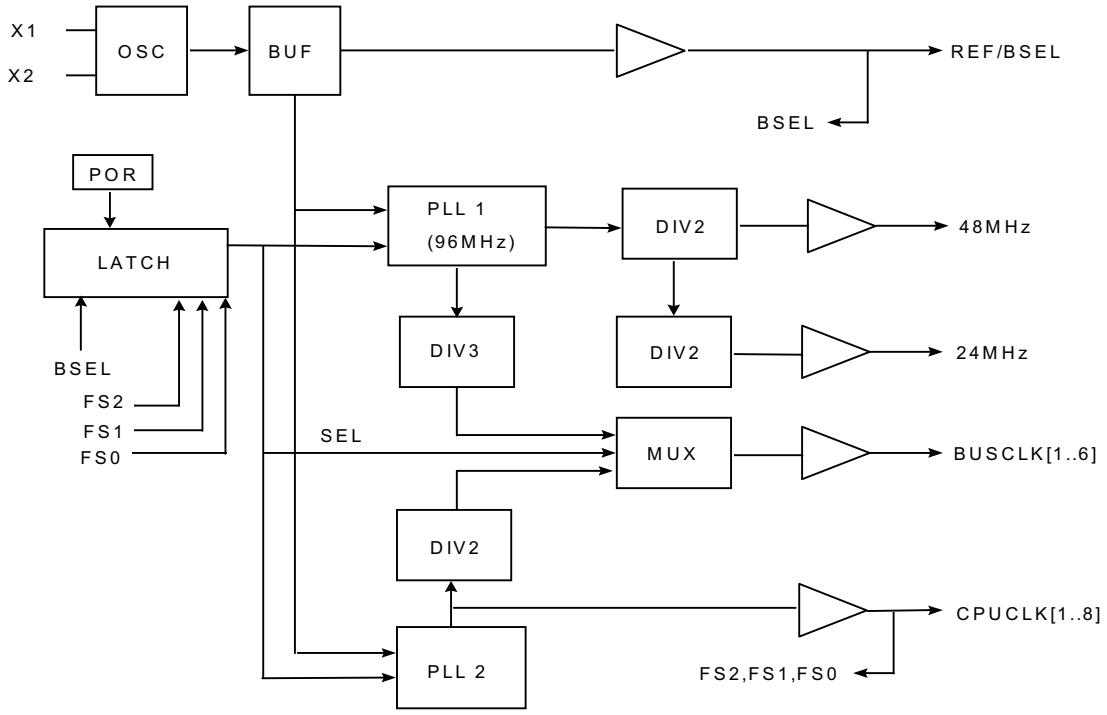
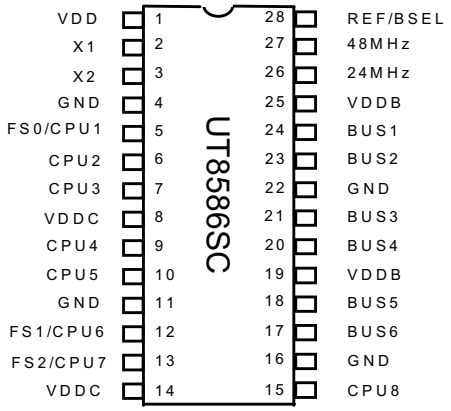
BLOCK DIAGRAM



PIN CONFIGURATION



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PIN DESCRIPTION

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD	PWR	Power for control logic
2	X1	IN	XTAL or external reference input to device
3	X2	OUT	XTAL output drive from device
4,11,16,22	GND	PWR	Ground for control logic
6,7,9,10,15	CPU(2:5) & CPU8	OUT	CPU clock outputs which are a multiple of the input reference clock as shown in preceding table
8,14	VDDC	PWR	Power for CPU clock buffers only
17,18,20,21,23,24	BUS(1:6)	OUT	PCI BUS clock outputs which are a multiple of the input reference clock as shown in the preceding table
19,25	VDDB	PWR	Power for BUS & fixed clock output buffers
26	24MHz	OUT	Fixed 24MHz clock for IOCLK
27	48MHz	OUT	Fixed 48MHz clock for USBCLK
28	REF	OUT	Fixed 14.318MHz clock
	BSEL	IN	Selection for synchronous or asynchronous PCI bus clock operation
5	CPU1	OUT	CPU clock outputs which are a multiple of the input reference clock as shown in preceding table
	FS0	IN	Frequency selection address pin
12,13	CPU(6:7)	OUT	CPU clock outputs which are a multiple of the input reference clock as shown in preceding table
	FS(1:2)	IN	Frequency selection address pin

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I/O PIN DESIGN METHODOLOGY

The frequency selection functions are achieved by pins 5, 12, 13 and 28 upon power up interval. After power up for a short while (≈ 5ms), these pins turn into clock outputs for maximum usage of pin assignments. Such feature reduces device pin count by combining clock outputs with input select pins.

The PLL start tracking the selected frequency since the power on reset according to selection inputs. Upon UT8586SC power up, the first 1msec is used as input logic selection. After 1msec of power up, the selection inputs were blocked outside the chip (to prevent error input selection data). During this period, the CPU / BUS clock output buffers and fixed frequency output buffers are tri-stated until 5ms past power up. Next the output buffers are enabled which converts the PLL locked frequency to each output clock pins.

LOW-FREQUENCY TEST MODE

The UT8586SC support a special low-frequency test mode for production system verification. When the selection inputs FS2= 0 , FS1=1, FS0=1, and Ref. = Frequency input to pin X1 then the frequency of each output pins act as follow:

CPU(1-8)	BUS(1-6)		48MHz	24MHz	REF
(MHz)	BSEL=1	BSEL=0	(USB)	(IO)	
REF/2	REF/4	REF/3	REF/2	REF/4	REF

FUNCTION TABLE

ADDRESS SELECT			CPU(1-8)	BUS(1-6)		48MHz	24MHz	REF
FS2	FS1	FS0	(MHz)	BSEL=1	BSEL=0			
0	0	0	50	25	32	48	24	REF
0	0	1	60	30	32	48	24	REF
0	1	0	66.6	33.3	32	48	24	REF
0	1	1	REF/2	REF/4	REF/3	REF/2	REF/4	REF
1	0	0	55	27.5	32	48	24	REF
1	0	1	75	37.5	32	48	24	REF
1	1	0	83	41.7	32	48	24	REF
1	1	1	68.4	34.2	32	48	24	REF

* NOTE : Crystal (X1, X2) = 14.318MHz
* REF = 14.318MHz
* 66.6MHz x (1+2.5%) = 68.265MHz

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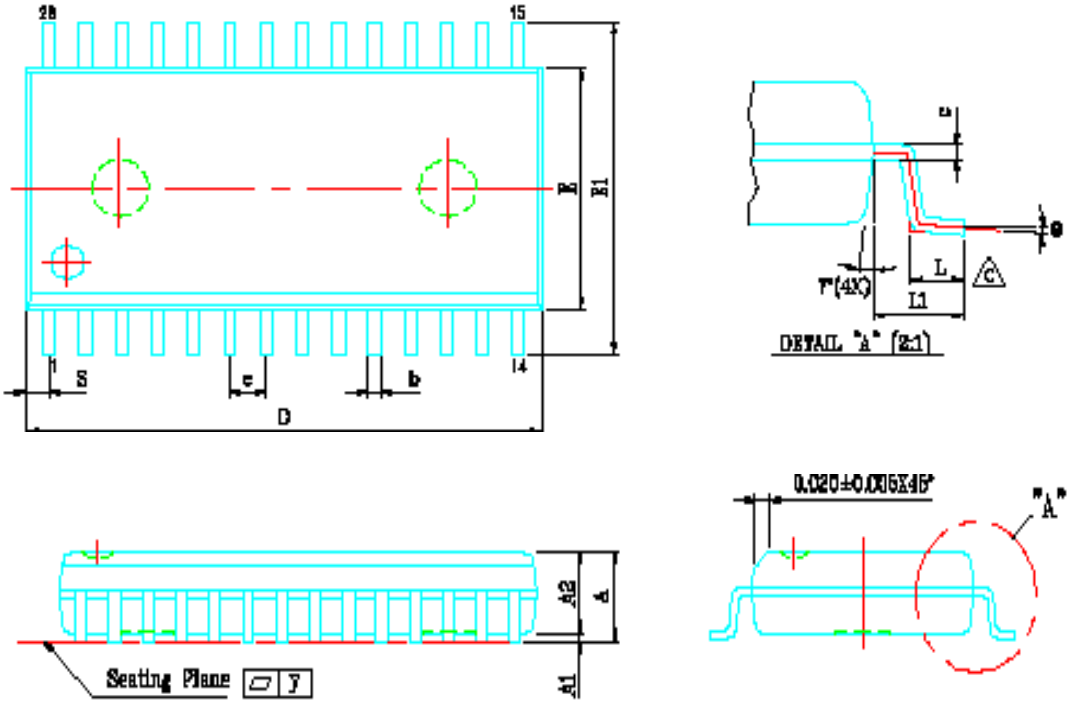
PACKAGE OUTLINE DIMENSION

28 pin 300 mil SOP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.120 (MAX)	3.048 (MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098± 0.005	2.489± 0.127
b	0.0016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.728 (MAX)	18.491 (MAX)
E	0.0350 (MAX)	8.890 (MAX)
△B E1	0.465± 0.012	11.811± 0.305
e	0.050 (TYP)	1.270(TYP)
△C L	0.05 (MAX)	1.270 (MAX)
L1	0.067± 0.008	1.702± 0.203
S	0.047 (MAX)	1.194 (MAX)
△E y	0.003(MAX)	0.076(MAX)
θ	0°～10°	0°～10°

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ORDERING INFORMATION

PART NO.	PACKAGE	PRODUCTION FLOW
UT8586SC	28PIN SOP	Commercial 0℃to +70℃

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