## REVISION HISTORY

| REVISION | DESCRIPTION | Release Date |
|---|---|---|
| Preliminary Rev. 0.1 | Original. | Jun 18, 2001 |
| Rev. 1.0 | 1. Revised Power supply<br>a、 55ns (max.) for Vcc=2.7V~3.6V<br>b、 70/100ns (max.) for Vcc=2.5V~3.6V<br>2. Revised DC ELECTRICAL CHARACTERISTICS：<br>a、 Revised $V_{IH}$ as 2.2V<br>b、 Revised standby current $I_{SB1}$ of LL-version<br>Typical : 3uA⇨2uA<br>Maximum : 25uA⇨20uA<br>3. Revised AC ELECTRICAL CHARACTERISTICS：<br>a、 Revised $t_{OH}$ as 10ns (min.)<br>4. Revised 36-pin TFBGA package outline dimension：<br>a、 Rev. 0.1 ball diameter=0.3mm<br>b、 Rev. 1.0 ball diameter=0.35mm | Jul 30, 2002 |
| Rev. 1.1 | 1.Revised “FEATURES” Operating current :<br>40/35/25mA($I_{CC}$ max)→20/18/15mA ($I_{CC}$ typ.)<br>2.TRUTH TABLE & DC ELECTRICAL : Delete $I_{SB2}$<br>3.Revised $V_{TERM}$ : -0.5 to Vcc+0.3V → -0.5 to 4.6V<br>4.Added $V_{OH}$ : 2.7V at Vcc=3.0V<br>5.Revised DC ($I_{CC}$ max) 45/35/25mA→35/30/25mA<br>($I_{CC}$ typ.) 30/25/20mA→20/18/15mA<br>6.Add under/overshoot range of $V_{IL}$ & $V_{IH}$<br>7.Revised AC $t_{OHZ}$*@100ns (max): 35ns→30ns<br>$t_{WHZ}$*(max) :30/30/40→20/25/30ns<br>8.Revised “Data retention Characteristics” :<br>$I_{DR}$-LL (Typ.) : NA→1uA, $I_{DR}$-L (Typ.) : NA→10uA<br>$I_{DR}$-LL (Max.) : 25uA→6uA<br>$t_R$(min) : 5ns→”$t_{RC}$”<br>9.Add order information for lead free product | Apr 28, 2003 |

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## FEATURES

- Fast access time :
  55ns(max.) for Vcc=2.7V~3.6V
  70/100ns(max.) for Vcc=2.5V~3.6V
- CMOS low power operation
  Operating : 20/18/15mA (TYP.)
  Standby : 20 uA(TYP.) L -version
  2 uA(TYP.) LL-version
- Single 2.5V~3.6V power supply
- Operating temperature:
  Commercial : 0℃~70℃
  Extended : -20℃~80℃
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage: 1.5V (min)
- Package : 32-pin 8mm x 20mm TSOP-Ⅰ
  32-pin 8mm x 13.4mm STSOP
  36-pin 6mm × 8mm TFBGA

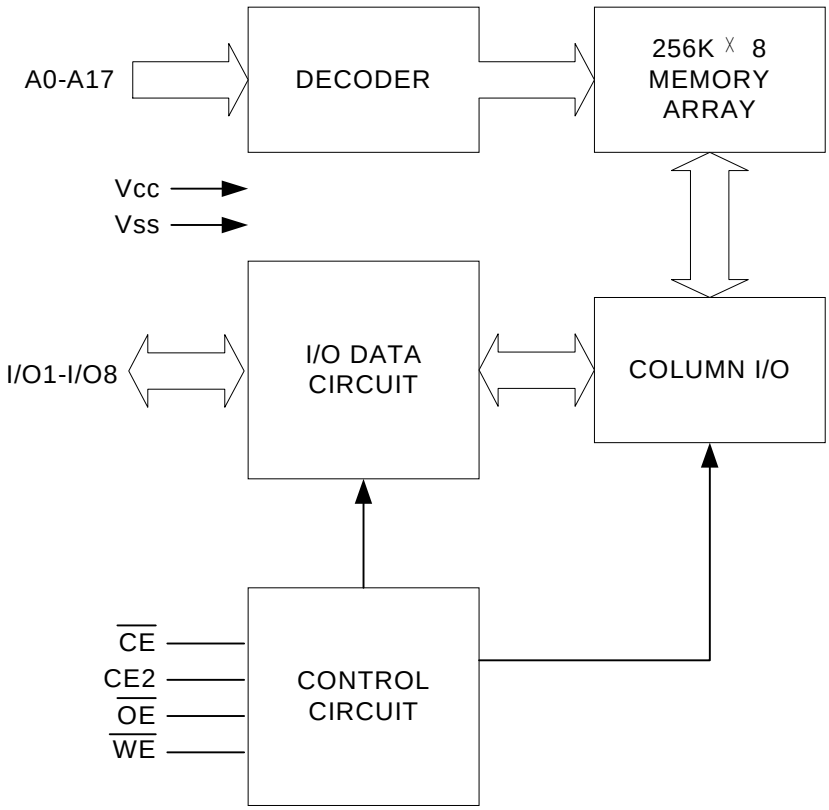
## GENERAL DESCRIPTION

The UT62L2568 is a 2,097,152-bit low power CMOS static random access memory organized as 262,144 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

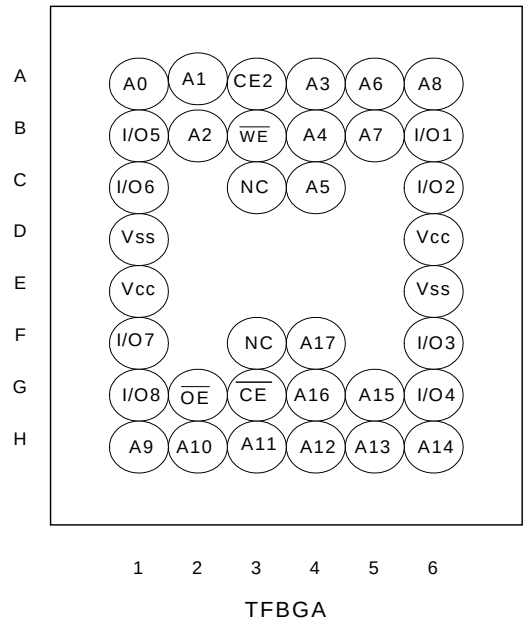
The UT62L2568 is designed for very low power system applications. It is particularly well suited for battery back-up nonvolatile memory applications.

It operates from a wide range of 2.5V~ 3.6V supply voltage. Easy memory expansion is provided by using two chip enable input ($\overline{CE}$,CE2). And all inputs and three-state outputs are fully TTL compatible.

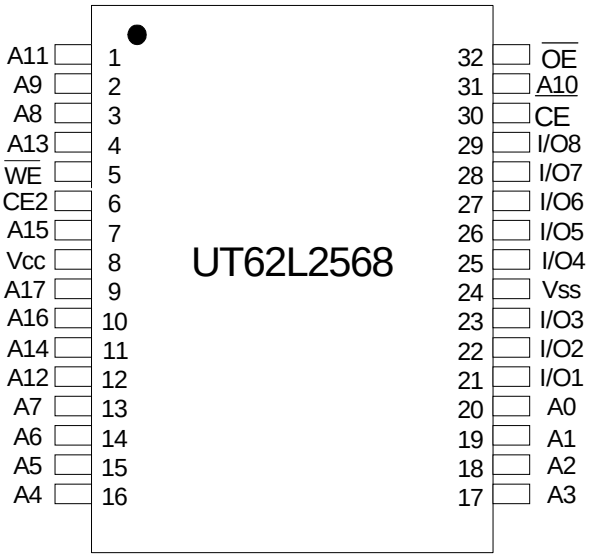
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




TFBGA




TSOP-1 / STSOP

## PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|---|---|
| A0 - A17 | Address Inputs |
| I/O1 - I/O8 | Data Inputs/Outputs |
| $\overline{CE}$ ,CE2 | Chip Enable Inputs |
| $\overline{WE}$ | Write Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |
| NC | No Connection |

## TRUTH TABLE

| MODE | $\overline{CE}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | I/O OPERATION | SUPPLY CURRENT |
|---|---|---|---|---|---|---|
| Standby | H | X | X | X | High - Z | $I_{SB}$,$I_{SB1}$ |
| | X | L | X | X | High - Z | $I_{SB}$,$I_{SB1}$ |
| Output Disable | L | H | H | H | High - Z | $I_{CC}$,$I_{CC1}$,$I_{CC2}$ |
| Read | L | H | L | H | $D_{OUT}$ | $I_{CC}$,$I_{CC1}$,$I_{CC2}$ |
| Write | L | H | X | L | $D_{IN}$ | $I_{CC}$,$I_{CC1}$,$I_{CC2}$ |

Note: H = $V_{IH}$, L=$V_{IL}$, X = Don't care.

## ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|
| Terminal Voltage with Respect to $V_{SS}$ | | $V_{TERM}$ | -0.5 to 4.6 | V |
| Operating Temperature | Commercial | $T_A$ | 0 to 70 | ℃ |
| | Extended | $T_A$ | -20 to 80 | ℃ |
| Storage Temperature | | $T_{STG}$ | -65 to 150 | ℃ |
| Power Dissipation | | $P_D$ | 1 | W |
| DC Output Current | | $I_{OUT}$ | 50 | mA |
| Soldering Temperature (under 10 secs) | | Tsolder | 260 | ℃ |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ =2.5V~3.6V, $T_A$ =0℃ to 70℃ / -20℃ to 80℃(E))

| PARAMETER | SYMBOL | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Power Voltage | $V_{CC}$ | | 55 | 2.7 | 3.0 | 3.6 | V |
| | | | 70/100 | 2.5 | 3.0 | 3.6 | V |
| Input High Voltage | $V_{IH}$ *1 | | | 2.2 | - | Vcc+0.3 | V |
| Input Low Voltage | $V_{IL}$ *2 | | | - 0.2 | - | 0.6 | V |
| Input Leakage Current | $I_{LI}$ | $V_{SS} \leqq V_{IN} \leqq V_{CC}$ | | - 1 | - | 1 | μA |
| Output Leakage Current | $I_{LO}$ | $V_{SS} \leqq V_{I/O} \leqq V_{CC}$, Output Disabled | | - 1 | - | 1 | μA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$= - 1mA ($I_{OH}$= -0.5mA when Vcc<2.7V) | | 2.2 | 2.7 | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$= 2.1mA | | - | - | 0.4 | V |
| Operating Current | $I_{CC}$ | Cycle time=Min.100% duty, $\overline{CE}$ =$V_{IL}$ and CE2 = $V_{IH}$, $I_{I/O}$ =0mA | 55 | - | 20 | 35 | mA |
| | | | 70 | - | 18 | 30 | mA |
| | | | 100 | - | 15 | 25 | mA |
| | $I_{CC1}$ | 100%duty, $I_{I/O}$=0mA, $\overline{CE} \leqq$0.2V and CE2$\geqq$Vcc-0.2V, other pins at 0.2V or Vcc-0.2V | TCycle= 1μs | - | 4 | 5 | mA |
| | $I_{CC2}$ | | TCycle= 500ns | - | 8 | 10 | mA |
| Standby Current (TTL) | $I_{SB}$ | $\overline{CE}$ =$V_{IH}$ or CE2 = $V_{IL}$ | | - | 0.3 | 0.5 | mA |
| Standby Current (CMOS) | $I_{SB1}$ | $\overline{CE}$ =$V_{CC}$-0.2V or CE2=0.2V, other pins at 0.2V or Vcc-0.2V | -L | - | 20 | 80 | μA |
| | | | -LL | - | 2 | 20 | μA |

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 10ns.
2. Undershoot : Vss-3.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

## CAPACITANCE ($T_A$=25°C, f=1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | - | 6 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 8 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | $C_L$ = 30pF+1TTL, $I_{OH}$= -1mA, $I_{OL}$= 2.1mA |

## AC ELECTRICAL CHARACTERISTICS ( $T_A$ = 0°C to 70°C / -20°C to 80°C(E))

### (1) READ CYCLE

| PARAMETER | SYMBOL | UT62L2568-55 $V_{CC}$ = 2.7V~3.6V | | UT62L2568-70 $V_{CC}$ = 2.5V~3.6V | | UT62L2568-100 $V_{CC}$ = 2.5V~3.6V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | $t_{RC}$ | 55 | - | 70 | - | 100 | - | ns |
| Address Access Time | $t_{AA}$ | - | 55 | - | 70 | - | 100 | ns |
| Chip Enable Access Time | $t_{ACE}$ | - | 55 | - | 70 | - | 100 | ns |
| Output Enable Access Time | $t_{OE}$ | - | 30 | - | 35 | - | 50 | ns |
| Chip Enable to Output in Low Z | $t_{CLZ*}$ | 10 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z | $t_{OLZ*}$ | 5 | - | 5 | - | 5 | - | ns |
| Chip Disable to Output in High Z | $t_{CHZ*}$ | - | 20 | - | 25 | - | 30 | ns |
| Output Disable to Output in High Z | $t_{OHZ*}$ | - | 20 | - | 25 | - | 30 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | - | 10 | - | 10 | - | ns |

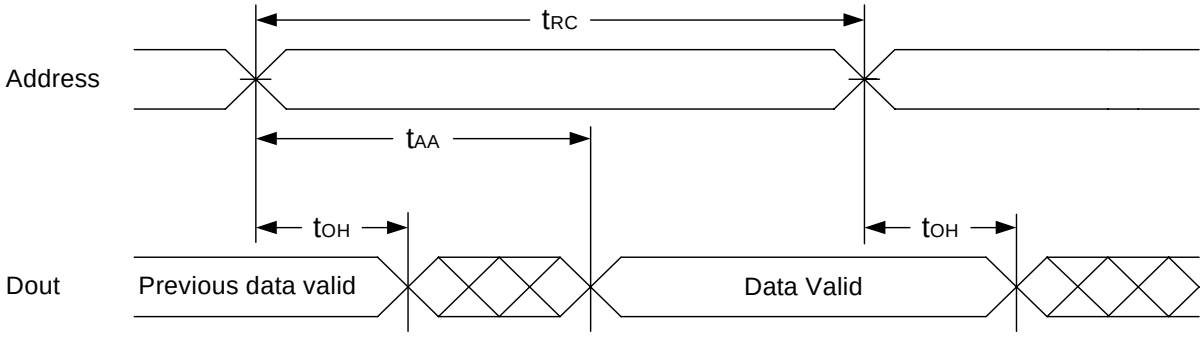
### (2) WRITE CYCLE

| PARAMETER | SYMBOL | UT62L2568-55 $V_{CC}$ = 2.7V~3.6V | | UT62L2568-70 $V_{CC}$ = 2.5V~3.6V | | UT62L2568-100 $V_{CC}$ = 2.5V~3.6V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | $t_{WC}$ | 55 | - | 70 | - | 100 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 50 | - | 60 | - | 80 | - | ns |
| Chip Enable to End of Write | $t_{CW}$ | 50 | - | 60 | - | 80 | - | ns |
| Address Set-up Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 45 | - | 55 | - | 70 | - | ns |
| Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | $t_{DW}$ | 25 | - | 30 | - | 40 | - | ns |
| Data Hold from End of Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | ns |
| Output Active from End of Write | $t_{OW*}$ | 5 | - | 5 | - | 5 | - | ns |
| Write to Output in High Z | $t_{WHZ*}$ | - | 20 | - | 25 | - | 30 | ns |

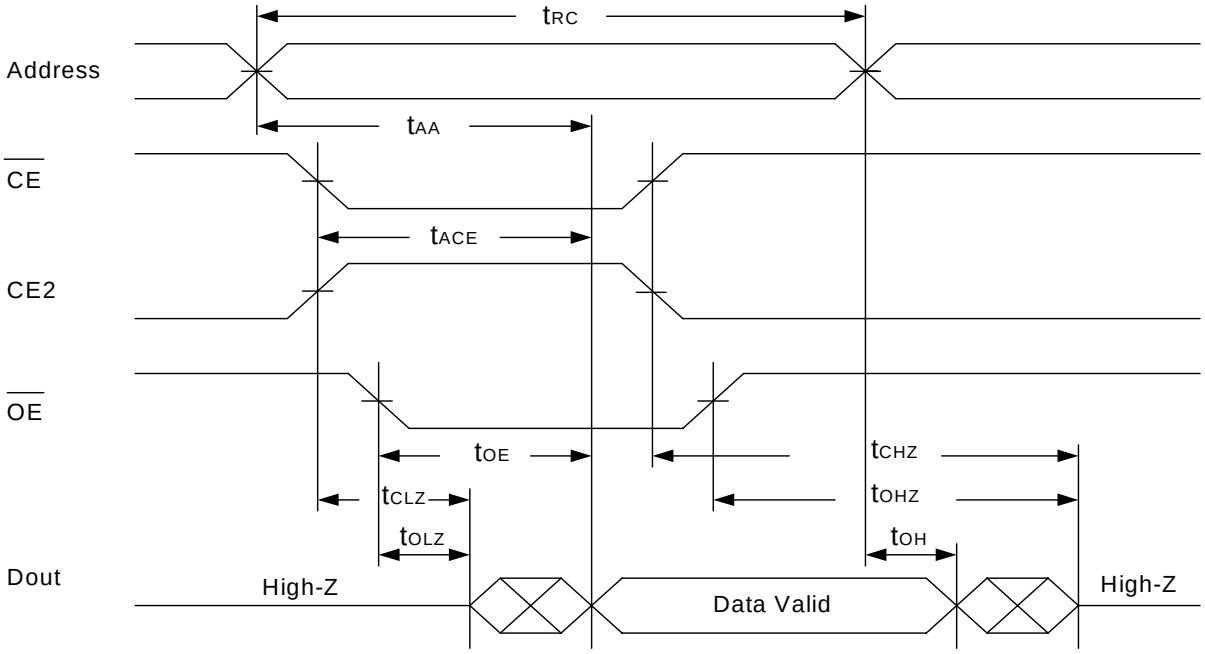
*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

**READ CYCLE 1** (Address Controlled) (1,2)



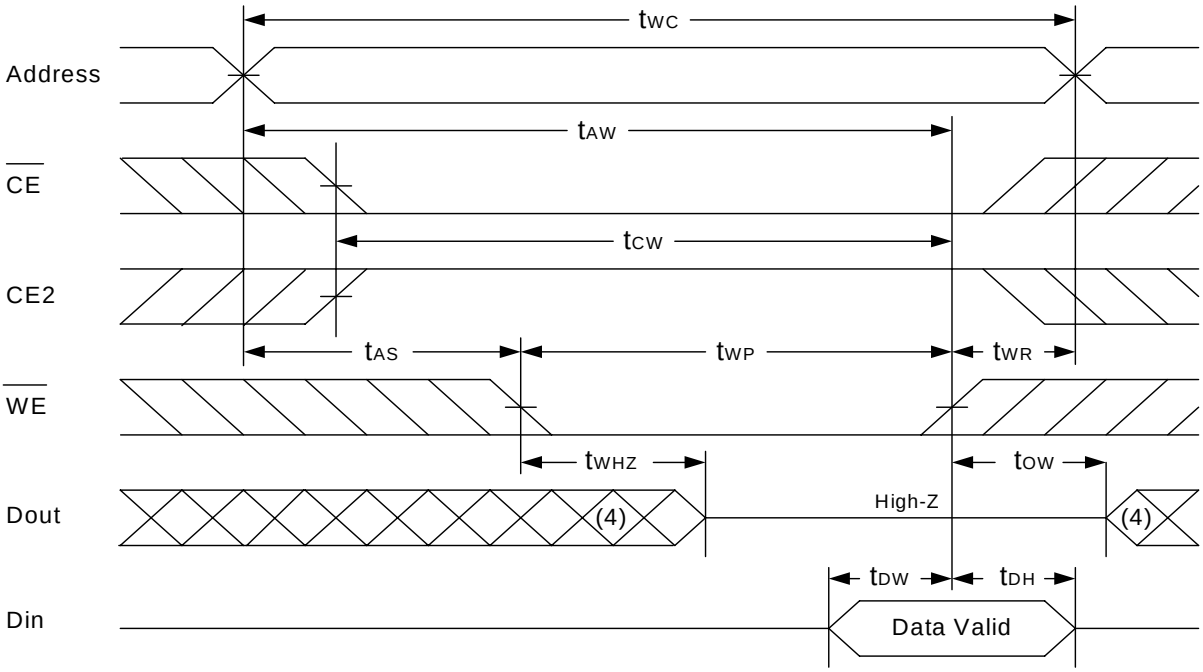

**READ CYCLE 2** ( $\overline{CE}$ and CE2 and $\overline{OE}$ Controlled) (1,3,4,5)



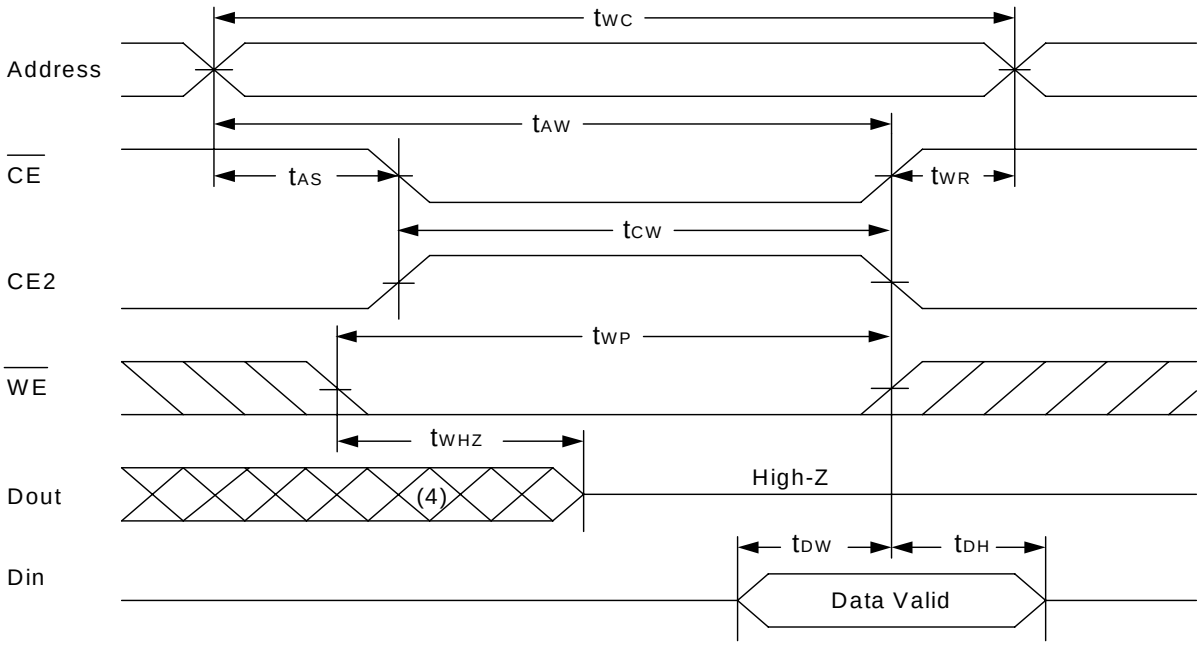

Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low, CE2=high.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, CE2=high; otherwise $t_{AA}$ is the limiting parameter.
4. $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$ and $t_{OHZ}$ are specified with $C_L$=5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, $t_{CHZ}$ is less than $t_{CLZ}$ is less than $t_{OHZ}$ is less than $t_{OLZ}$.

**WRITE CYCLE 1** ( $\overline{WE}$ Controlled) (1,2,3,5,6)




**WRITE CYCLE 2** ( $\overline{CE}$ and CE2 Controlled) (1,2,5,6)



Notes :

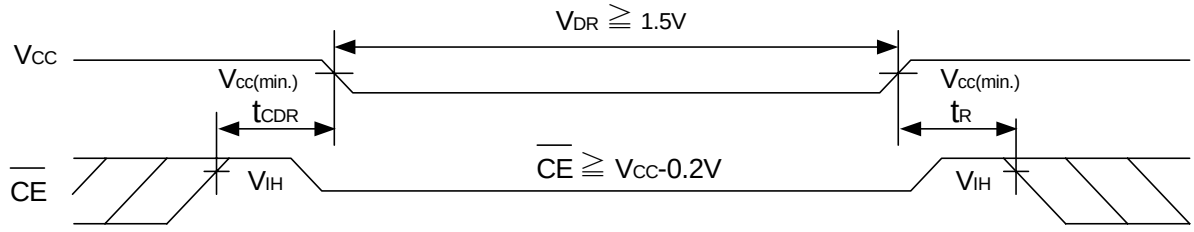
1. $\overline{WE}$ , $\overline{CE}$ must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ , high CE2, low $\overline{WE}$ .
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, $t_{WP}$ must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition and CE2 high transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. $t_{OW}$ and $t_{WHZ}$ are specified with $C_L$ = 5pF. Transition is measured ±500mV from steady state.

## DATA RETENTION CHARACTERISTICS ($T_A$ =0℃ to 70℃ / -20℃ to 80℃(E))

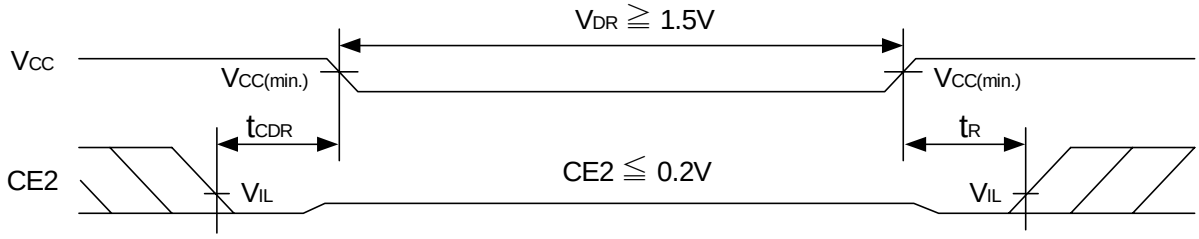
| PARAMETER | SYMBOL | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Vcc for Data Retention | $V_{DR}$ | $\overline{CE} \geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V | | 1.5 | - | 3.6 | V |
| Data Retention Current | $I_{DR}$ | $V_{CC}$=1.5V $\overline{CE} \geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V | - L | - | 10 | 80 | µA |
| | | | - LL | - | 1 | 10 | µA |
| Chip Disable to Data Retention Time | $t_{CDR}$ | See Data Retention Waveforms (below) | | 0 | - | - | ns |
| Recovery Time | $t_R$ | | | $t_{RC}$ | - | - | ns |

## DATA RETENTION WAVEFORM

**Low Vcc Data Retention Waveform (1)** ($\overline{CE}$ controlled)

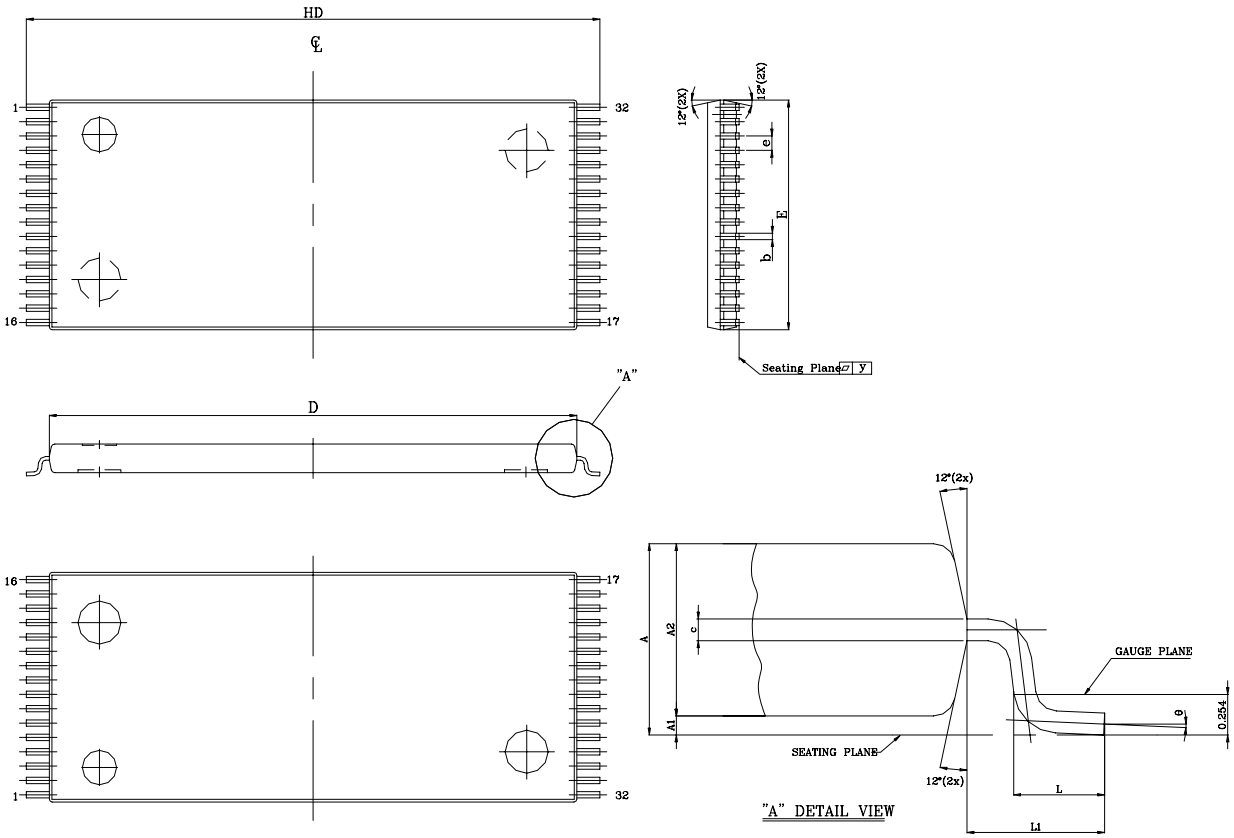



**Low Vcc Data Retention Waveform (2)** (CE2 controlled)



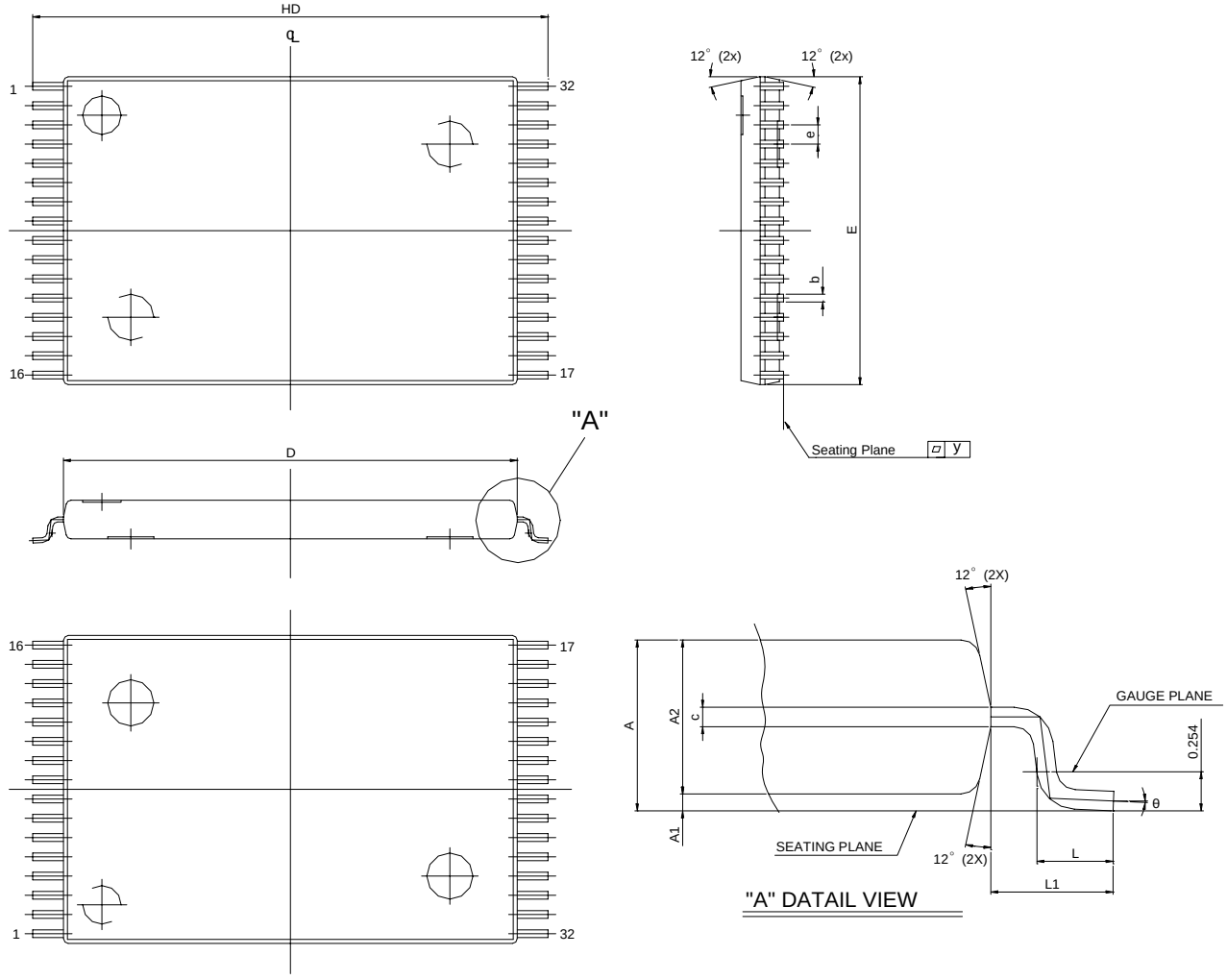
## PACKAGE OUTLINE DIMENSION

### 32 pin 8mm x 20mm TSOP-I Package Outline Dimension



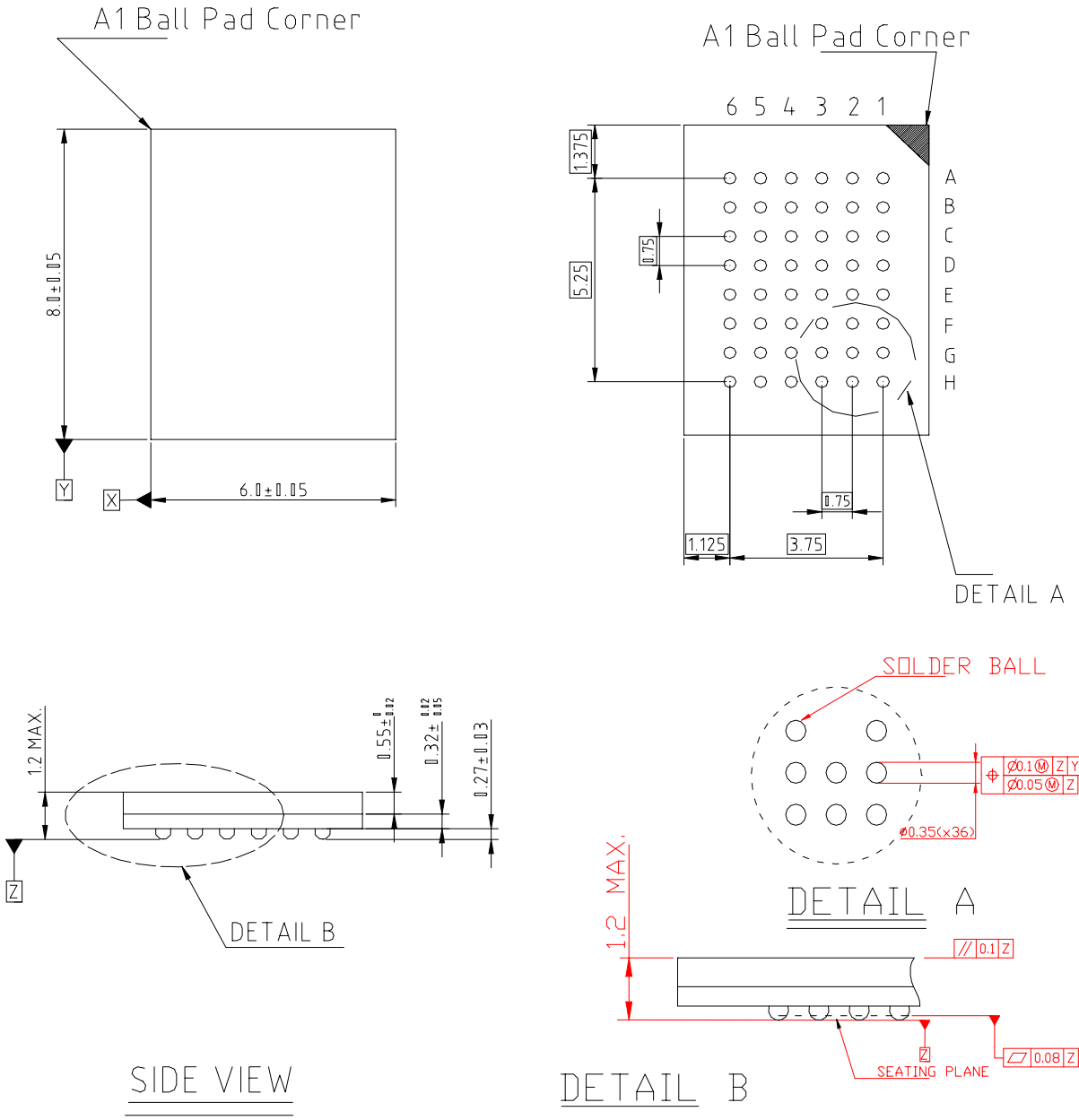

| UNIT / SYMBOL | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.047 (MAX) | 1.20 (MAX) |
| A1 | 0.004 ±0.002 | 0.10 ±0.05 |
| A2 | 0.039 ±0.002 | 1.00 ±0.05 |
| b | 0.008 + 0.002 - 0.001 | 0.20 + 0.05 -0.03 |
| c | 0.005 (TYP) | 0.127 (TYP) |
| D | 0.724 ±0.004 | 18.40 ±0.10 |
| E | 0.315 ±0.004 | 8.00 ±0.10 |
| e | 0.020 (TYP) | 0.50 (TYP) |
| HD | 0.787 ±0.008 | 20.00 ±0.20 |
| L | 0.0197 ±0.004 | 0.50 ±0.10 |
| L1 | 0.0315 ±0.004 | 0.08 ±0.10 |
| y | 0.003 (MAX) | 0.076 (MAX) |
| Θ | $0^o$ $5^o$ | $0^o$ $5^o$ |

**32 pin 8mm x 13.4mm STSOP Package Outline Dimension**




| SYMBOL \ UNIT | INCH(BASE) | MM(REF) |
|---|---|---|
| A | 0.049 (MAX) | 1.25 (MAX) |
| A1 | 0.005 ±0.002 | 0.130 ±0.05 |
| A2 | 0.039 ±0.002 | 1.00 ±0.05 |
| b | 0.008 ±0.01 | 0.20±0.025 |
| c | 0.005 (TYP) | 0.127 (TYP) |
| D | 0.465 ±0.004 | 11.80 ±0.10 |
| E | 0.315 ±0.004 | 8.00 ±0.10 |
| e | 0.020 (TYP) | 0.50 (TYP) |
| HD | 0.528±0.008 | 13.40 ±0.20. |
| L | 0.0197 ±0.004 | 0.50 ±0.10 |
| L1 | 0.0315 ±0.004 | 0.8 ±0.10 |
| y | 0.003 (MAX) | 0.076 (MAX) |
| Θ | $0^o$ $5^o$ | $0^o$ $5^o$ |

**36 pin 6mm×8mm TFBGA Package Outline Dimension**



## ORDERING INFORMATION

**COMMERCIAL TEMPERATURE**

| PART NO. | ACCESS TIME (ns) | STANDBY CURRENT (µA) TYP. | PACKAGE |
|---|---|---|---|
| UT62L2568LC-55L | 55 | 20 | 32 PIN TSOP-I |
| UT62L2568LC-55LL | 55 | 2 | 32 PIN TSOP-I |
| UT62L2568LC-70L | 70 | 20 | 32 PIN TSOP-I |
| UT62L2568LC-70LL | 70 | 2 | 32 PIN TSOP-I |
| UT62L2568LC-100L | 100 | 20 | 32 PIN TSOP-I |
| UT62L2568LC-100LL | 100 | 2 | 32 PIN TSOP-I |
| UT62L2568LS-55L | 55 | 20 | 32 PIN STSOP |
| UT62L2568LS-55LL | 55 | 2 | 32 PIN STSOP |
| UT62L2568LS-70L | 70 | 20 | 32 PIN STSOP |
| UT62L2568LS-70LL | 70 | 2 | 32 PIN STSOP |
| UT62L2568LS-100L | 100 | 20 | 32 PIN STSOP |
| UT62L2568LS-100LL | 100 | 2 | 32 PIN STSOP |
| UT62L2568BS-55L | 55 | 20 | 36 PIN TFBGA |
| UT62L2568BS-55LL | 55 | 2 | 36 PIN TFBGA |
| UT62L2568BS-70L | 70 | 20 | 36 PIN TFBGA |
| UT62L2568BS-70LL | 70 | 2 | 36 PIN TFBGA |
| UT62L2568BS-100L | 100 | 20 | 36 PIN TFBGA |
| UT62L2568BS-100LL | 100 | 2 | 36 PIN TFBGA |

**EXTENDED TEMPERATURE**

| PART NO. | ACCESS TIME (ns) | STANDBY CURRENT (µA) TYP. | PACKAGE |
|---|---|---|---|
| UT62L2568LC-55LE | 55 | 20 | 32 PIN TSOP-I |
| UT62L2568LC-55LLE | 55 | 2 | 32 PIN TSOP-I |
| UT62L2568LC-70LE | 70 | 20 | 32 PIN TSOP-I |
| UT62L2568LC-70LLE | 70 | 2 | 32 PIN TSOP-I |
| UT62L2568LC-100LE | 100 | 20 | 32 PIN TSOP-I |
| UT62L2568LC-100LLE | 100 | 2 | 32 PIN TSOP-I |
| UT62L2568LS-55LE | 55 | 20 | 32 PIN STSOP |
| UT62L2568LS-55LLE | 55 | 2 | 32 PIN STSOP |
| UT62L2568LS-70LE | 70 | 20 | 32 PIN STSOP |
| UT62L2568LS-70LLE | 70 | 2 | 32 PIN STSOP |
| UT62L2568LS-100LE | 100 | 20 | 32 PIN STSOP |
| UT62L2568LS-100LLE | 100 | 2 | 32 PIN STSOP |
| UT62L2568BS-55LE | 55 | 20 | 36 PIN TFBGA |
| UT62L2568BS-55LLE | 55 | 2 | 36 PIN TFBGA |
| UT62L2568BS-70LE | 70 | 20 | 36 PIN TFBGA |
| UT62L2568BS-70LLE | 70 | 2 | 36 PIN TFBGA |
| UT62L2568BS-100LE | 100 | 20 | 36 PIN TFBGA |
| UT62L2568BS-100LLE | 100 | 2 | 36 PIN TFBGA |

## ORDERING INFORMATION (for lead free product)

**COMMERCIAL TEMPERATURE**

| PART NO. | ACCESS TIME (ns) | STANDBY CURRENT (µA) TYP. | PACKAGE |
|---|---|---|---|
| UT62L2568LCL-55L | 55 | 20 | 32 PIN TSOP-I |
| UT62L2568LCL-55LL | 55 | 2 | 32 PIN TSOP-I |
| UT62L2568LCL-70L | 70 | 20 | 32 PIN TSOP-I |
| UT62L2568LCL-70LL | 70 | 2 | 32 PIN TSOP-I |
| UT62L2568LCL-100L | 100 | 20 | 32 PIN TSOP-I |
| UT62L2568LCL-100LL | 100 | 2 | 32 PIN TSOP-I |
| UT62L2568LSL-55L | 55 | 20 | 32 PIN STSOP |
| UT62L2568LSL-55LL | 55 | 2 | 32 PIN STSOP |
| UT62L2568LSL-70L | 70 | 20 | 32 PIN STSOP |
| UT62L2568LSL-70LL | 70 | 2 | 32 PIN STSOP |
| UT62L2568LSL-100L | 100 | 20 | 32 PIN STSOP |
| UT62L2568LSL-100LL | 100 | 2 | 32 PIN STSOP |
| UT62L2568BSL-55L | 55 | 20 | 36 PIN TFBGA |
| UT62L2568BSL-55LL | 55 | 2 | 36 PIN TFBGA |
| UT62L2568BSL-70L | 70 | 20 | 36 PIN TFBGA |
| UT62L2568BSL-70LL | 70 | 2 | 36 PIN TFBGA |
| UT62L2568BSL-100L | 100 | 20 | 36 PIN TFBGA |
| UT62L2568BSL-100LL | 100 | 2 | 36 PIN TFBGA |

**EXTENDED TEMPERATURE**

| PART NO. | ACCESS TIME (ns) | STANDBY CURRENT (µA) TYP. | PACKAGE |
|---|---|---|---|
| UT62L2568LCL-55LE | 55 | 20 | 32 PIN TSOP-I |
| UT62L2568LCL-55LLE | 55 | 2 | 32 PIN TSOP-I |
| UT62L2568LCL-70LE | 70 | 20 | 32 PIN TSOP-I |
| UT62L2568LCL-70LLE | 70 | 2 | 32 PIN TSOP-I |
| UT62L2568LCL-100LE | 100 | 20 | 32 PIN TSOP-I |
| UT62L2568LCL-100LLE | 100 | 2 | 32 PIN TSOP-I |
| UT62L2568LSL-55LE | 55 | 20 | 32 PIN STSOP |
| UT62L2568LSL-55LLE | 55 | 2 | 32 PIN STSOP |
| UT62L2568LSL-70LE | 70 | 20 | 32 PIN STSOP |
| UT62L2568LSL-70LLE | 70 | 2 | 32 PIN STSOP |
| UT62L2568LSL-100LE | 100 | 20 | 32 PIN STSOP |
| UT62L2568LSL-100LLE | 100 | 2 | 32 PIN STSOP |
| UT62L2568BSL-55LE | 55 | 20 | 36 PIN TFBGA |
| UT62L2568BSL-55LLE | 55 | 2 | 36 PIN TFBGA |
| UT62L2568BSL-70LE | 70 | 20 | 36 PIN TFBGA |
| UT62L2568BSL-70LLE | 70 | 2 | 36 PIN TFBGA |
| UT62L2568BSL-100LE | 100 | 20 | 36 PIN TFBGA |
| UT62L2568BSL-100LLE | 100 | 2 | 36 PIN TFBGA |

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