REVISION HISTORY

REVISION	DESCRIPTION	Date
Preliminary Rev. 0.1	Original.	Sep.04,2002
Preliminary Rev. 0.2	1. Revised Pin number	Oct.28,2002
Rev. 1.0	1. Revised Standby current : 10/2mA(max)→0.5mA(typ.) 2. Delete I_{CC1}, I_{CC2} 3. Revised I_{SB} : 30mA→3mA, I_{SB1}:10mA→2mA, 4. Add I_{SB} & I_{SB1} (typ.) : 1mA & 2mA 5. Add Overshoot : $V_{IH} \leq +6.0V$ for $t \leq$ tRC /2. Undershoot : $V_{IL} \leq -2.0V$ for $t \leq$ tRC /2. 6. Revised Data retention I_{DR} (max) : 3mA→1mA 7. Add order information for lead free product	May 20,2003

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FEATURES

- Fast access time : 10/12/15ns
- CMOS Low operating power
  Operating current :
  260/240/220 mA (Icc max.)
  Standby current : 0.5 mA (typ.)
- Single 3.0V~3.6V power supply
- Operating temperature :
  Commercial : 0℃~70℃
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Data byte control : $\overline{LB}$ (I/O1~I/O8)
  $\overline{UB}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP-II

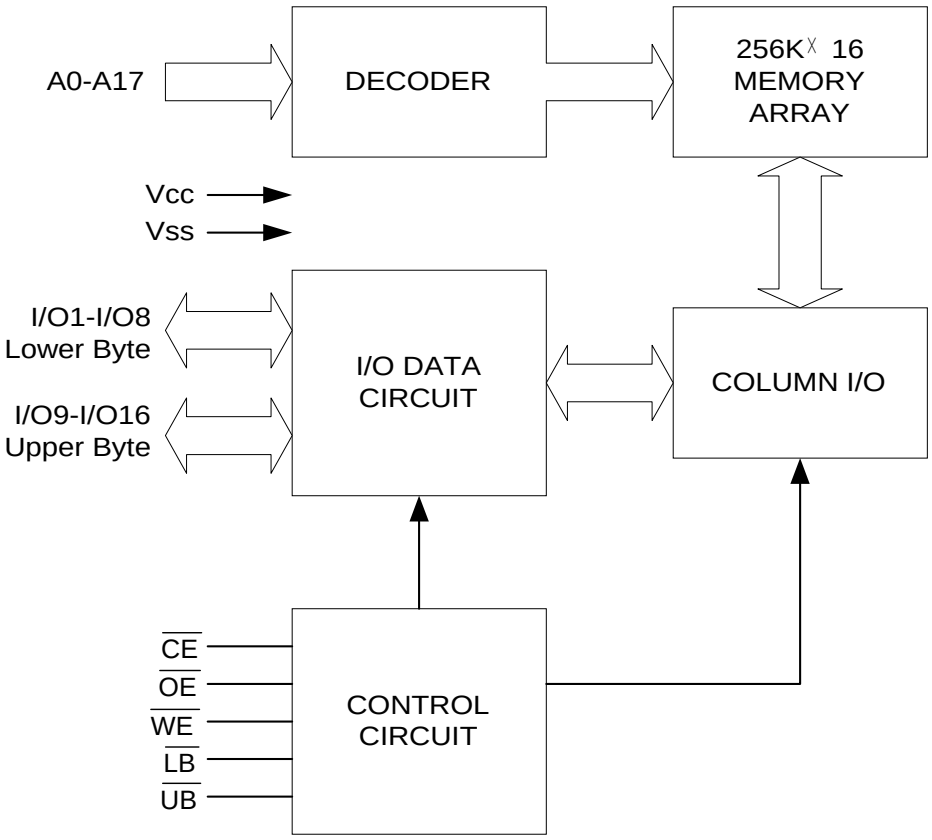
GENERAL DESCRIPTION

The UT61L25616 is a 4,194,304-bit high speed CMOS static random access memory organized as 262,144 words by 16 bits. It is fabricated using high performance and high reliability CMOS technology.

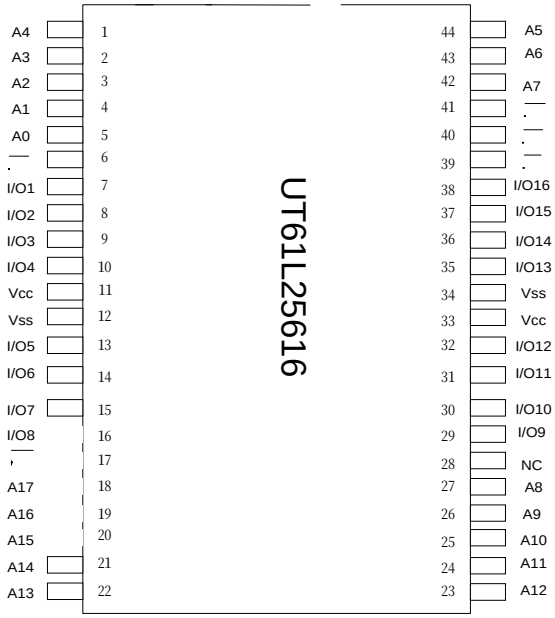
The UT61L25616 operates from a single 3.0V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

It is designed to allow lower and upper byte access by data byte control ($\overline{LB}$、$\overline{UB}$)。

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSOP II

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-Byte Control
$\overline{UB}$	Upper-Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	L	X	High – Z	High – Z	I_{CC}
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D_{OUT}	High – Z	I_{CC}
	L	L	H	H	L	High – Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High – Z	I_{CC}
	L	X	L	H	L	High – Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	Tsolder	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	Vcc			3.0	3.3	3.6	V
Input High Voltage	V_{IH} *1			2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL} *2			-0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC;}$ Output Disabled		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH}= -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 8mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty, I/O=0mA, $\overline{CE}$ =V_{IL}	-10		-	260	mA
			-12		-	240	mA
			-15		-	220	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$ =$V_{IH,}$ other pins =V_{IL} or V_{IH}		-	1	3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}$ =V_{CC}-0.2V, other pins at 0.2V or Vcc-0.2V		-	0.5	2	mA

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 8ns.
2. Undershoot : Vss-3.0v for pulse width less than 8ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -4mA / 8mA

AC ELECTRICAL CHARACTERISTICS (T_A =0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L25616-10		UT61L25616-12		UT61L25616-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ to High-Z Output	t_{BHZ*}	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	t_{BLZ*}	0	-	0	-	0	-	ns

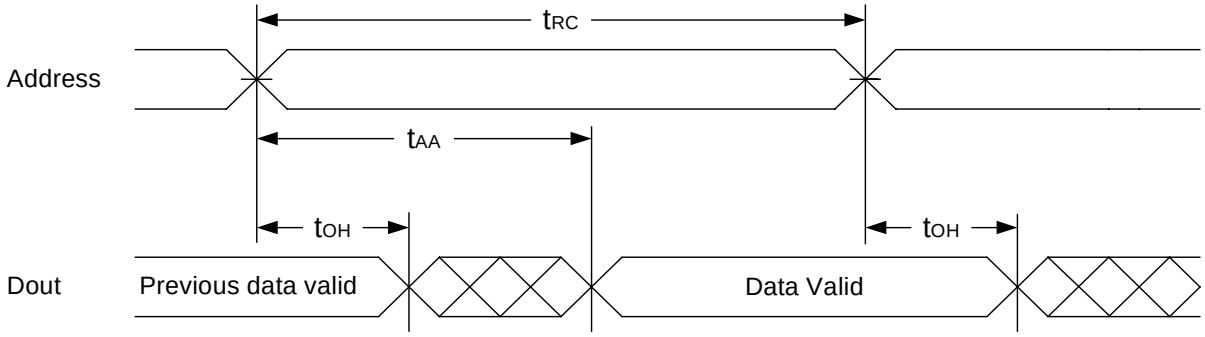
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61L25616-10		UT61L25616-12		UT61L25616-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	9	-	10	-	ns
Chip Enable to End of Write	t_{CW}	8	-	9	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	3	-	3	-	3	-	ns
Write to Output in High Z	t_{WHZ*}	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	8	-	9	-	10	-	ns

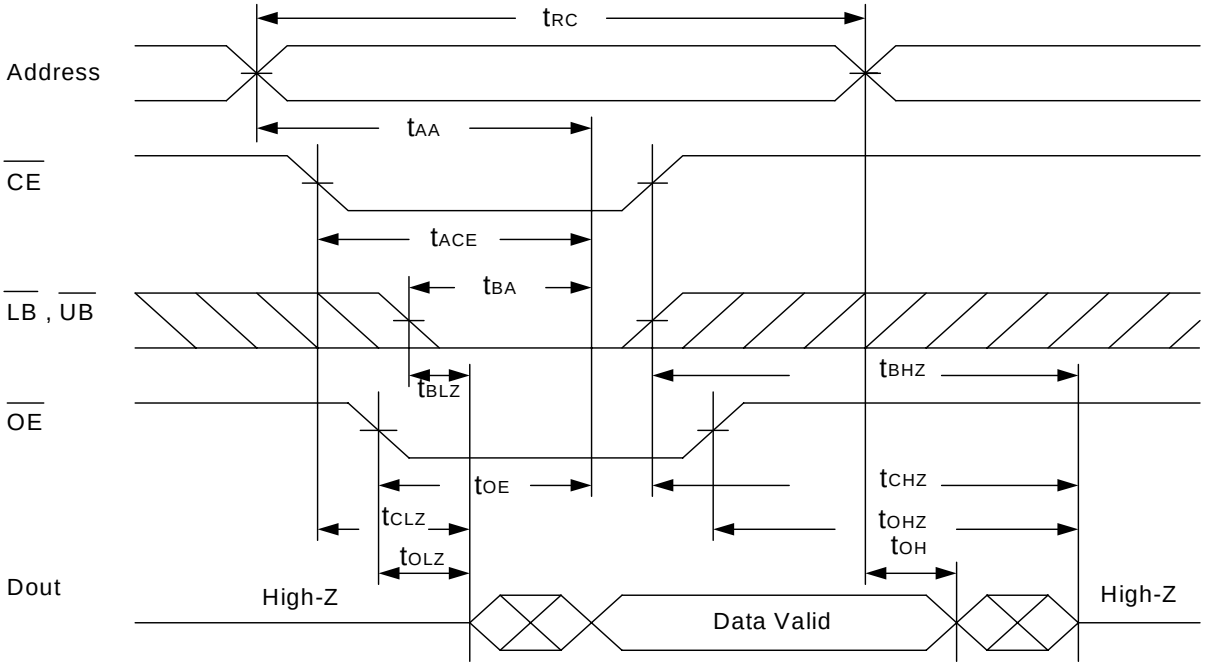
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



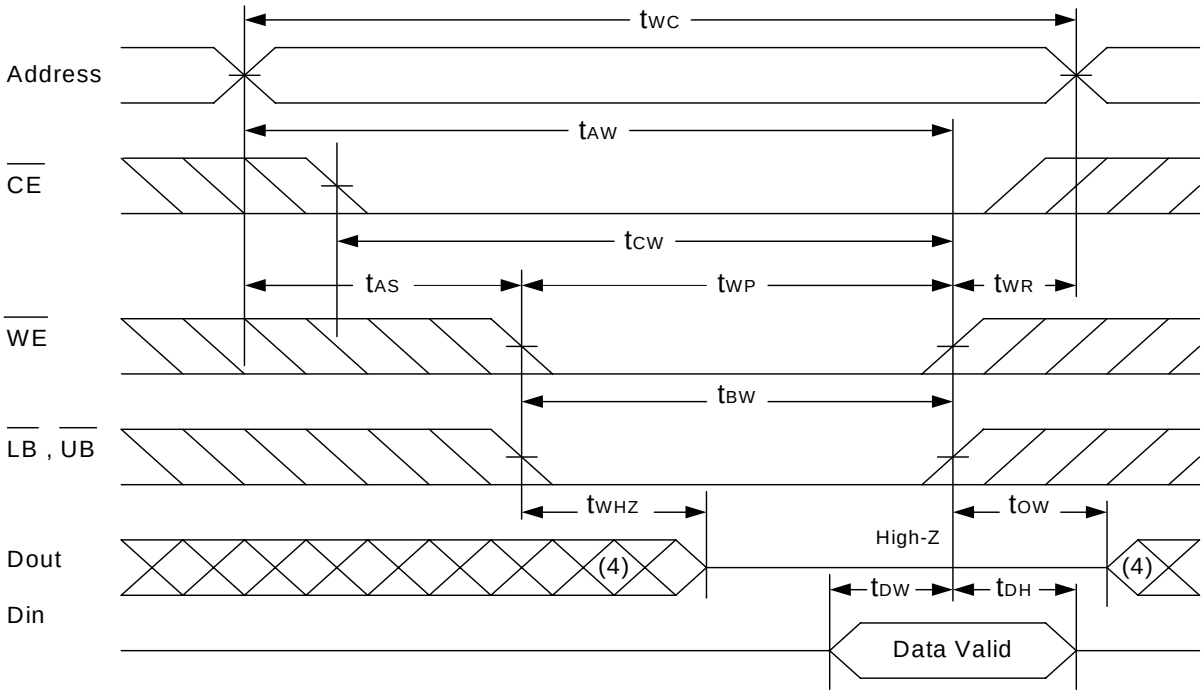
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,4,5)



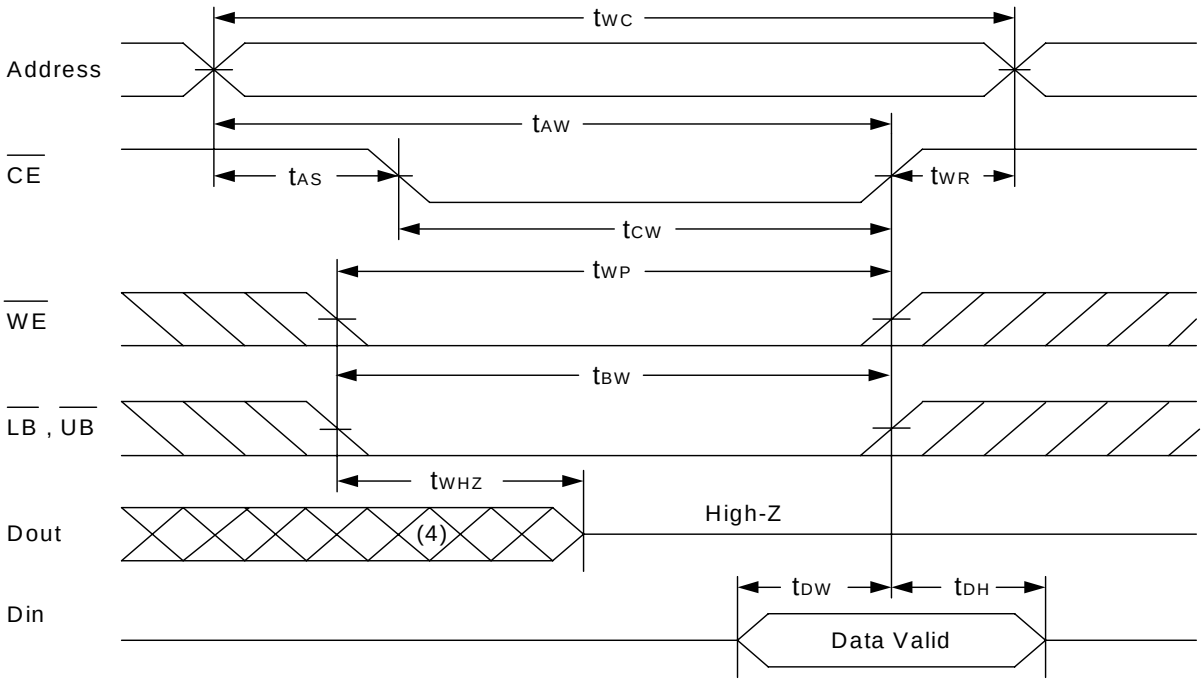
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low, $\overline{LB}$ or $\overline{UB}$ =low.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, $\overline{LB}$ or $\overline{UB}$ =low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{BHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{BHZ} is less than t_{BLZ}, t_{OHZ} is less than t_{OLZ}.

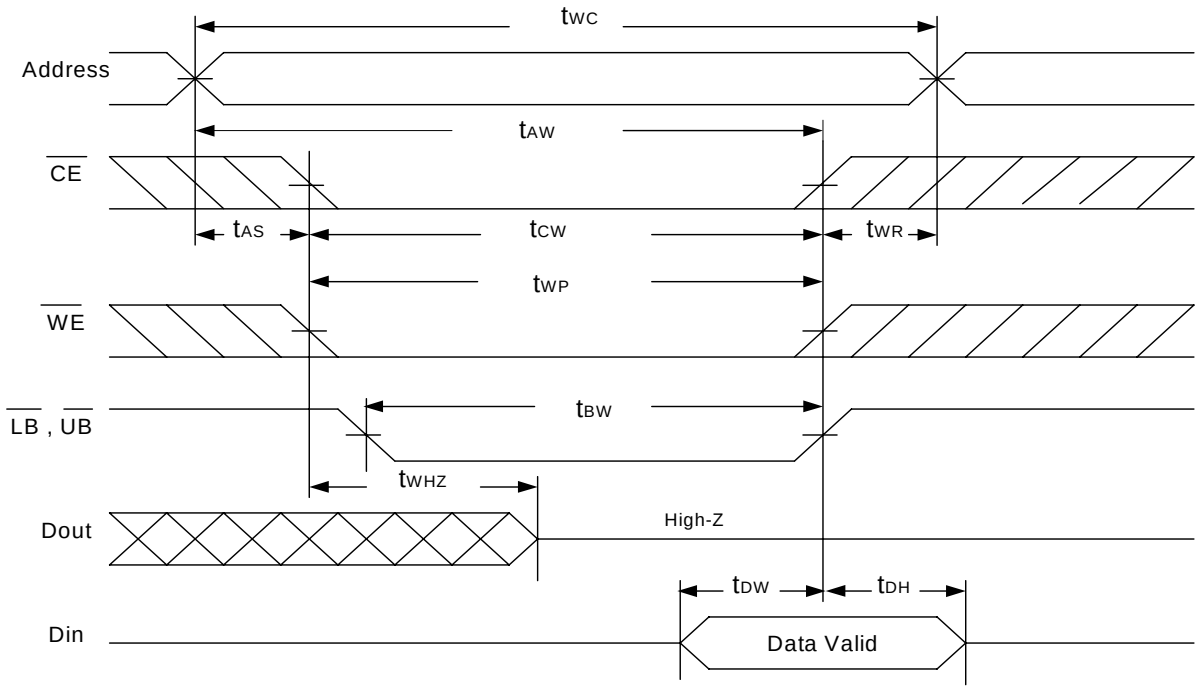
WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5,6)



WRITE CYCLE 3 ($\overline{LB}$, $\overline{UB}$ Controlled) (1,2,5,6)



Notes :

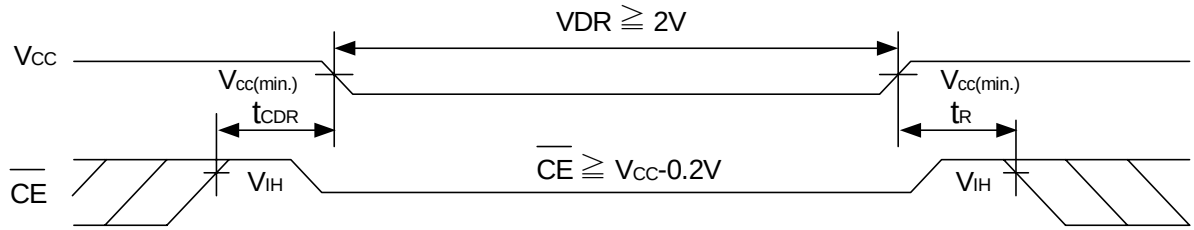
1. $\overline{WE}$, $\overline{CE}$, $\overline{LB}$, $\overline{UB}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, low $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ =low.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$, $\overline{LB}$, $\overline{UB}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = 0℃ to +70℃)

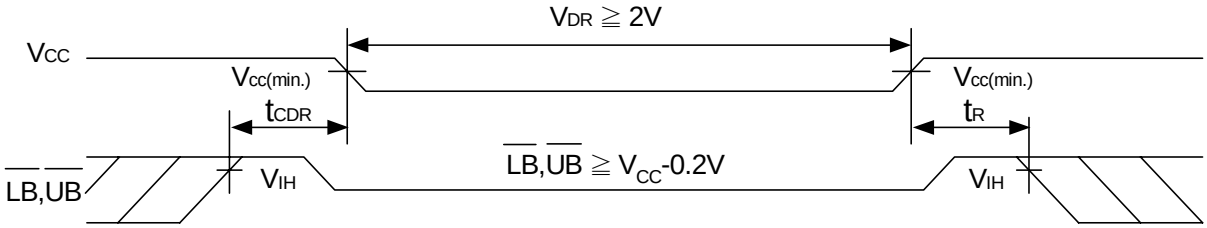
PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V ,	2.0	3.6	V
Data Retention Current	I_{DR}	Vcc=2V $\overline{CE} \geqq V_{CC}$-0.2V ,	-	1	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	ms
Recovery Time	t_R		5	-	ms

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE}$ controlled)

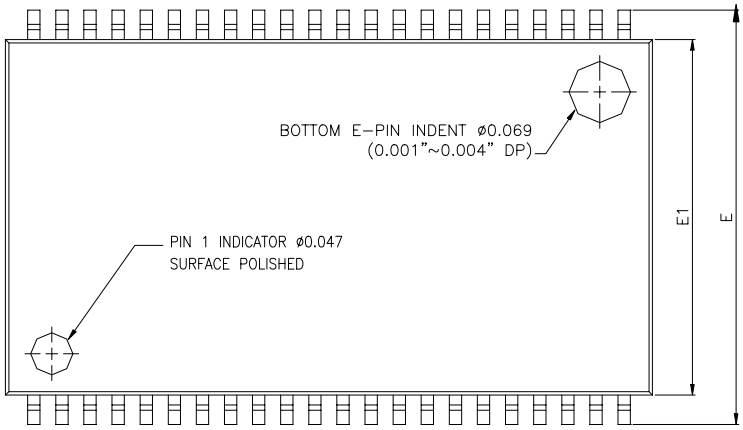


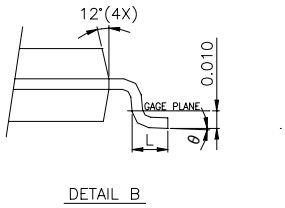
Low Vcc Data Retention Waveform (2) ($\overline{LB}$, $\overline{UB}$ controlled)

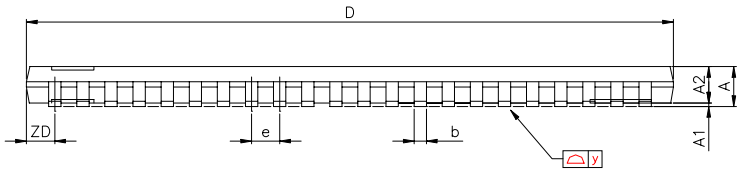


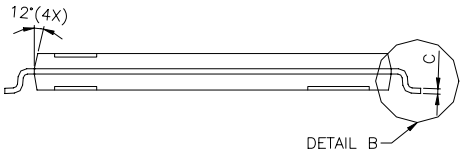
PACKAGE OUTLINE DIMENSION

44pin 400mil TSOP-Ⅱ Package Outline Dimension









SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0^o	-	5^o	0^o	-	5^o

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L25616MC-10	10	44 PIN TSOP-II
UT61L25616MC-12	12	44 PIN TSOP-II
UT61L25616MC-15	15	44 PIN TSOP-II

ORDERING INFORMATION (for lead free product)

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L25616MCL-10	10	44 PIN TSOP-II
UT61L25616MCL-12	12	44 PIN TSOP-II
UT61L25616MCL-15	15	44 PIN TSOP-II

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