



UTRON

Rev. 1.1

UT61L6416

64K X 16 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	Date
Preliminary Rev. 0.4	Original.	Mar, 2001
Preliminary Rev. 0.5	1.The symbols CE# and OE# and WE# are revised as. $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2.Separate Industrial and Commercial SPEC. 3.Add access time 15ns range. 4.Delete SOJ package.	Aug 31,2001
Rev. 1.0	1.Revised CMOS low power operating : Operating current : 195→150mA (max.) Standby current : 30mA (max.) → 1mA (Typ.) 2.Revised power supply : 3.0~3.6V→3.15~3.6V 3.Revised DC CHARACTERISTICE I_{CC} -8ns (max) : 200→150mA I_{CC} -10ns (max) : 195→120mA I_{CC} -12ns (max) : 190→100mA I_{CC} -15ns (max) : 150→80 mA I_{SB} (max) : 30→10mA, I_{SB} (typ) : NA→3mA I_{SB1} (max) : 10→3mA, I_{SB1} (typ) : NA→1mA I_{SB1} (max)<1 mA for special order 4. Add order information for lead free product	May 20,2003
Rev. 1.1	1.Add Extended temperature : -20°C~80°C	Jul 03,2003



UTRON

Rev. 1.1

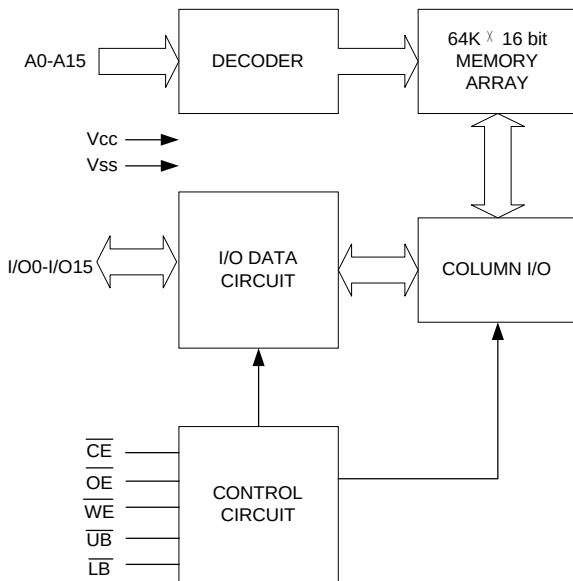
UT61L6416

64K X 16 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time :
8ns for $V_{CC}=3.15V\sim3.6V$
10/12/15ns for $V_{CC}=3.0V\sim3.6V$
- CMOS low power operating :
Operating current : 150mA (max.)
Standby current : 1mA (typ.)
- Single 3.15~3.6V power supply
- Operating temperature :
Commercial : $0^{\circ}C\sim70^{\circ}C$
Extended : $-20^{\circ}C\sim80^{\circ}C$
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data byte control : $\overline{LB}$ (I/O0~I/O7)
 $\overline{UB}$ (I/O8~I/O15)
- Package : 44-pin 400mil TSOP II

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The UT61L6416 is a 1,048,576-bit high speed CMOS static random access memory organized as 65,536 words by 16 bits.

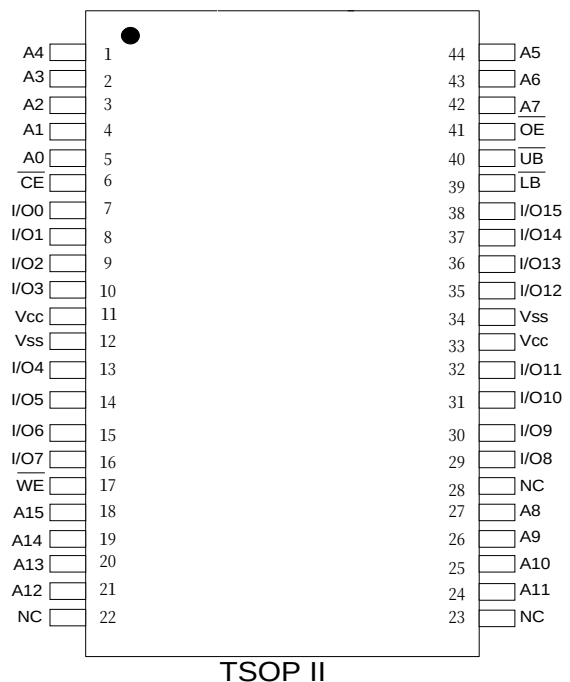
The UT61L6416 operates from a single 3.15 ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT61L6416 is designed for lower and upper byte access by data byte control. ($\overline{LB}$ $\overline{UB}$)

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O0 - I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Control
$\overline{UB}$	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70
	Extended	T_A	-20 to 80
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	T_{solder}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O0-I/O7	I/O8-I/O15	
Standby	H	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	X	X	H	H			
Output Disable	L	H	H	L	X	High – Z	High – Z	I_{CC}
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D_{OUT}	High – Z	I_{CC}
	L	L	H	H	L	High – Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High – Z	I_{CC}
	L	X	L	H	L	High – Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C / -20°C to 80°C (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}	8	3.15	3.3	3.6	V
		10/12/15	3.0	3.3	3.6	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}		-0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$	- 2	-	2	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_{IO} \leq V_{CC}$, Output Disable	- 2	-	2	μA
Output High Voltage	V_{OH}	$I_{OH} = -4\text{mA}$	2.4	-	-	V
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{mA}$	-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty $I/O=0\text{mA}$, $\overline{CE}=V_{IL}$	8	-	-	150
			10	-	-	120
			12	-	-	100
			15	-	-	80
Standby Current (TTL)	I_{SB}	$\overline{CE}=V_{IH}$, other pins = V_{IL} or V_{IH}	-	3	10	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}=V_{CC}-0.2\text{V}$, other pins at 0.2V or $V_{CC}-0.2\text{V}$	-	1	3^{*4}	mA

Notes:

1. Overshoot : $V_{CC}+3.0\text{V}$ for pulse width less than 6ns.
2. Undershoot : $V_{SS}-3.0\text{V}$ for pulse width less than 6ns.
3. Overshoot and Undershoot are sampled, not 100% tested.
4. $I_{SB1} < 1\text{mA}$ for special order or requirement.



UTRON

Rev. 1.1

UT61L6416

64K X 16 BIT HIGH SPEED CMOS SRAM

CAPACITANCE (T_A=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF, I _{OH} /I _{OL} = -4mA / 8mA

AC ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C / -20°C to 80°C(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L6416 -8 V _{CC} =3.15 3.6		UT61L6416 -10 V _{CC} =3.0 3.6		UT61L6416 -12 V _{CC} =3.0 3.6		UT61L6416 -15 V _{CC} =3.0 3.6		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t _{CLZ*}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t _{OLZ*}	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t _{CHZ*}	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t _{OHZ*}	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t _{BA}	-	4	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ to High Z Output	t _{BHZ}	-	4	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ to Low Z Output	t _{BLZ}	0	-	0	-	0	-	0	-	ns

(2) WRITE CYCLE

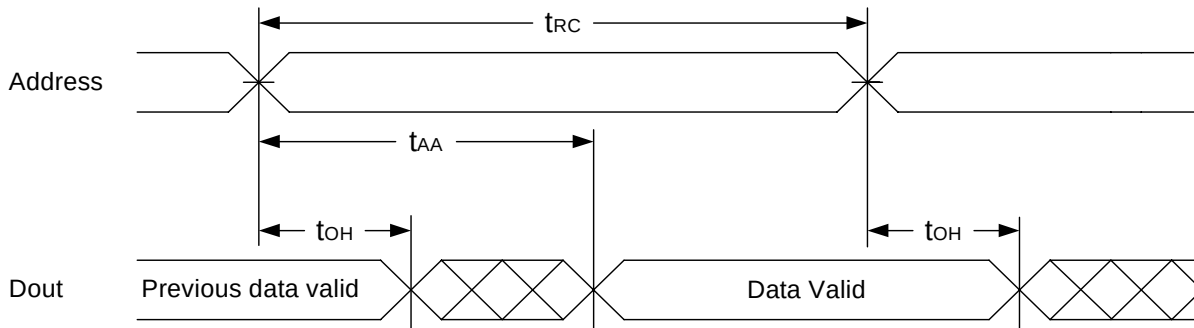
PARAMETER	SYMBOL	UT61L6416 -8 V _{CC} =3.15 3.6		UT61L6416 -10 V _{CC} =3.0 3.6		UT61L6416 -12 V _{CC} =3.0 3.6		UT61L6416 -15 V _{CC} =3.0 3.6		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	9	-	10	-	ns
Chip Enable to End of Write	t _{CW}	7	-	8	-	9	-	10	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	7	-	8	-	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	5.5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW*}	3	-	3	-	3	-	3	-	ns
Write to Output in High Z	t _{WHZ*}	-	4	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t _{BW}	7	-	8	-	9	-	10	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

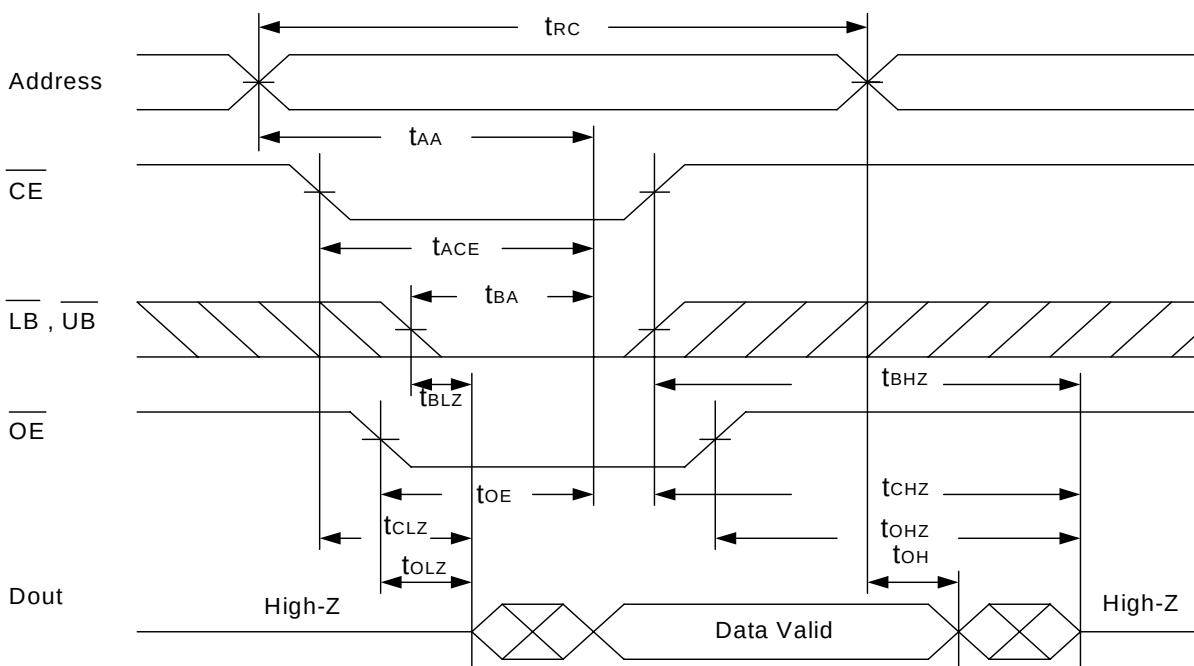


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,4,5)



Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ = low, $\overline{CE}$ = low, $\overline{LB}$ or $\overline{UB}$ = low.
3. Address must be valid prior to or coincident with $\overline{CE}$ = low, $\overline{LB}$ or $\overline{UB}$ = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ± 500 mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

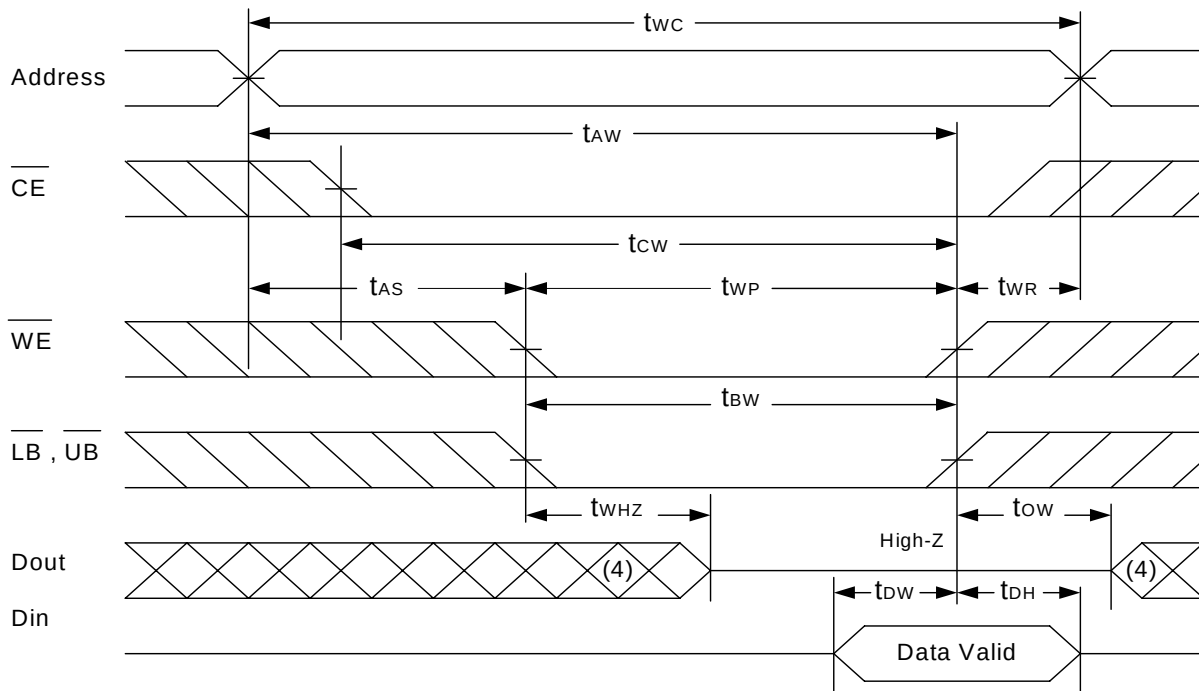


Rev. 1.1

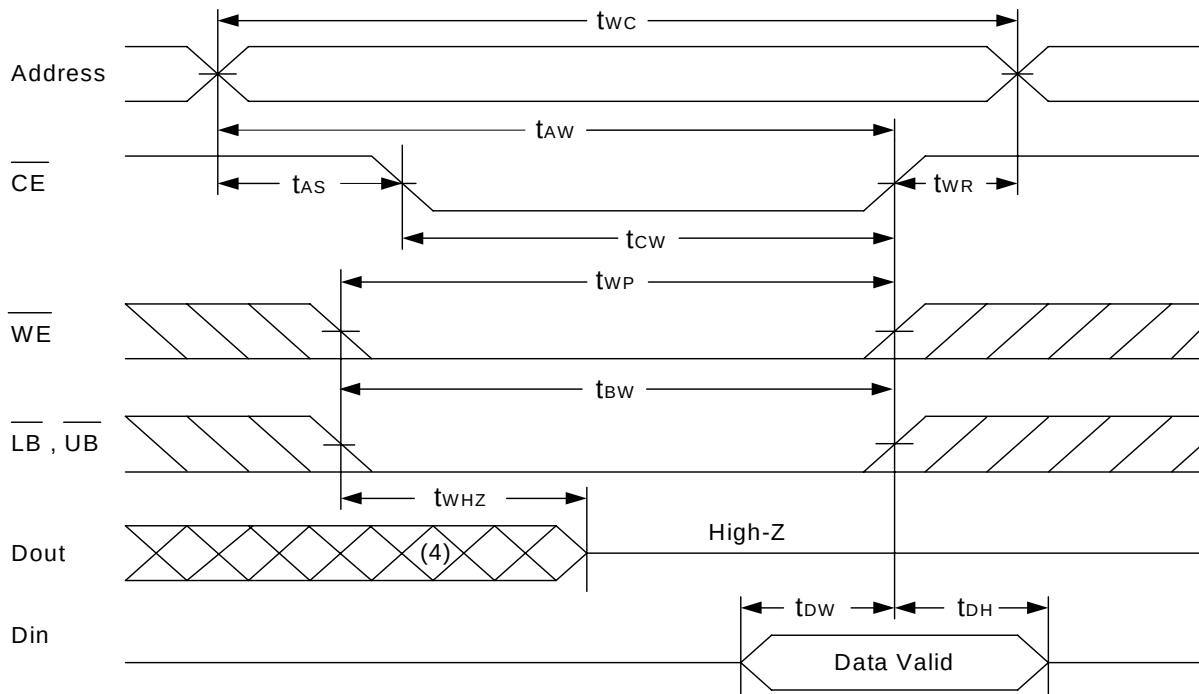
UTRON

UT61L6416
64K X 16 BIT HIGH SPEED CMOS SRAM

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5,6)



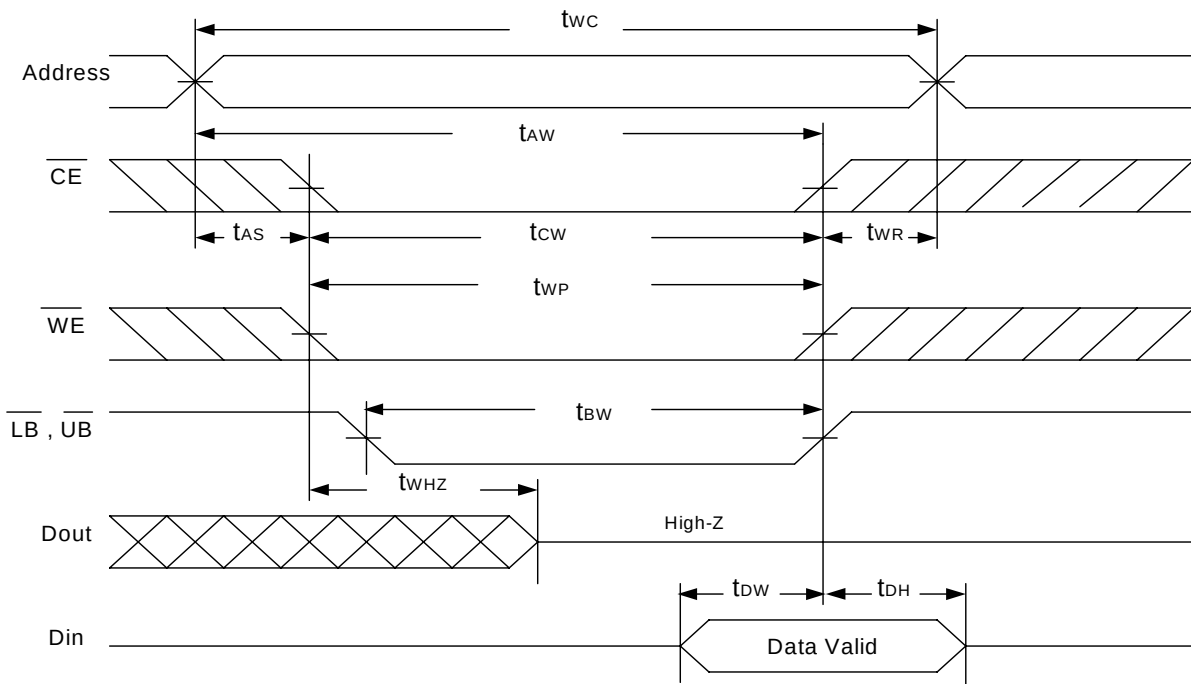


Rev. 1.1

UTRON

UT61L6416
64K X 16 BIT HIGH SPEED CMOS SRAM

WRITE CYCLE 3 ($\overline{LB}$, $\overline{UB}$ Controlled) (1,2,5,6)



Notes :

1. $\overline{WE}$, $\overline{CE}$, $\overline{LB}$, $\overline{UB}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, low $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$ = low.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ} + t_{BW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$, $\overline{LB}$, $\overline{UB}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.



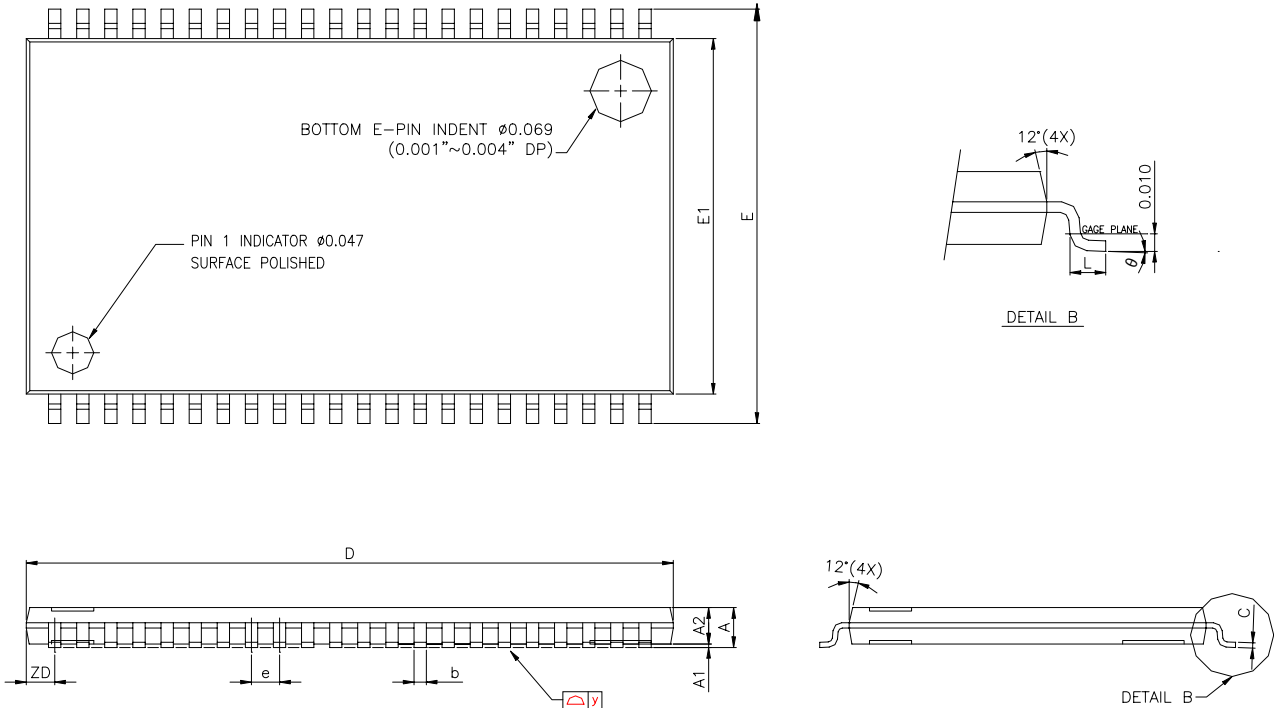
UTRON

Rev. 1.1

UT61L6416
64K X 16 BIT HIGH SPEED CMOS SRAM

PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II PACKAGE OUTLINE DIMENSION



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0°	-	5°	0°	-	5°



Rev. 1.1

UTRON**UT61L6416****64K X 16 BIT HIGH SPEED CMOS SRAM****ORDERING INFORMATION****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L6416MC-8	8	44 PIN TSOP- II
UT61L6416MC-10	10	44 PIN TSOP- II
UT61L6416MC-12	12	44 PIN TSOP- II
UT61L6416MC-15	15	44 PIN TSOP- II

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L6416MC-8E	8	44 PIN TSOP- II
UT61L6416MC-10E	10	44 PIN TSOP- II
UT61L6416MC-12E	12	44 PIN TSOP- II
UT61L6416MC-15E	15	44 PIN TSOP- II

ORDERING INFORMATION (for lead free product)**COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L6416MCL-8	8	44 PIN TSOP- II
UT61L6416MCL-10	10	44 PIN TSOP- II
UT61L6416MCL-12	12	44 PIN TSOP- II
UT61L6416MCL-15	15	44 PIN TSOP- II

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L6416MCL-8E	8	44 PIN TSOP- II
UT61L6416MCL-10E	10	44 PIN TSOP- II
UT61L6416MCL-12E	12	44 PIN TSOP- II
UT61L6416MCL-15E	15	44 PIN TSOP- II



Rev. 1.1

UTRON

UT61L6416

64K X 16 BIT HIGH SPEED CMOS SRAM

THIS PAGE IS LEFT BLANK INTENTIONALLY.