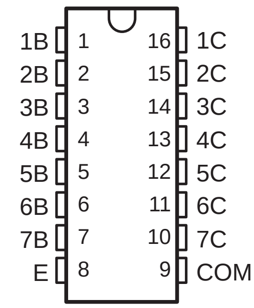
SLRS027 – DECEMBER 1976 – REVISED APRIL 1993

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Designed to Be Interchangeable With Sprague ULN2001A Series**

D OR N PACKAGE
(TOP VIEW)

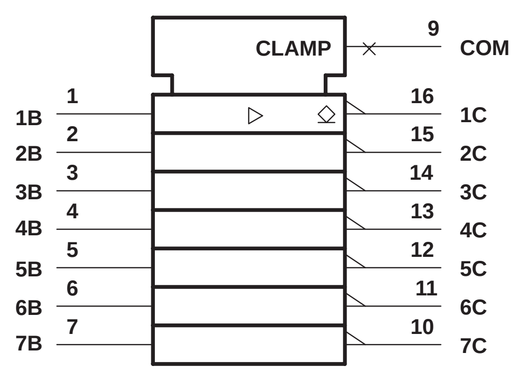


description

The ULN2001A, ULN2002A, ULN2003A, and ULN2004A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

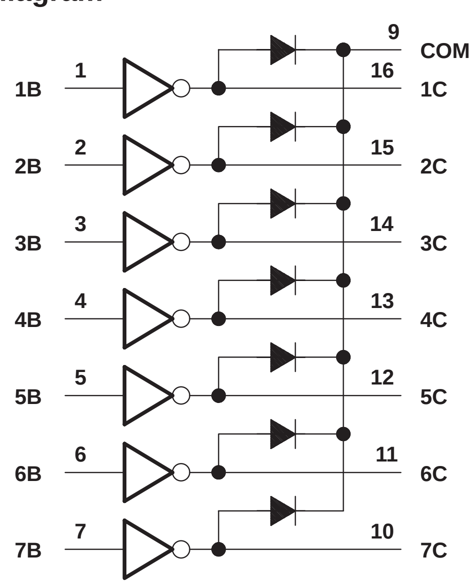
The ULN2001A is a general-purpose array and can be used with TTL and CMOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V PMOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A.

logic symbol†

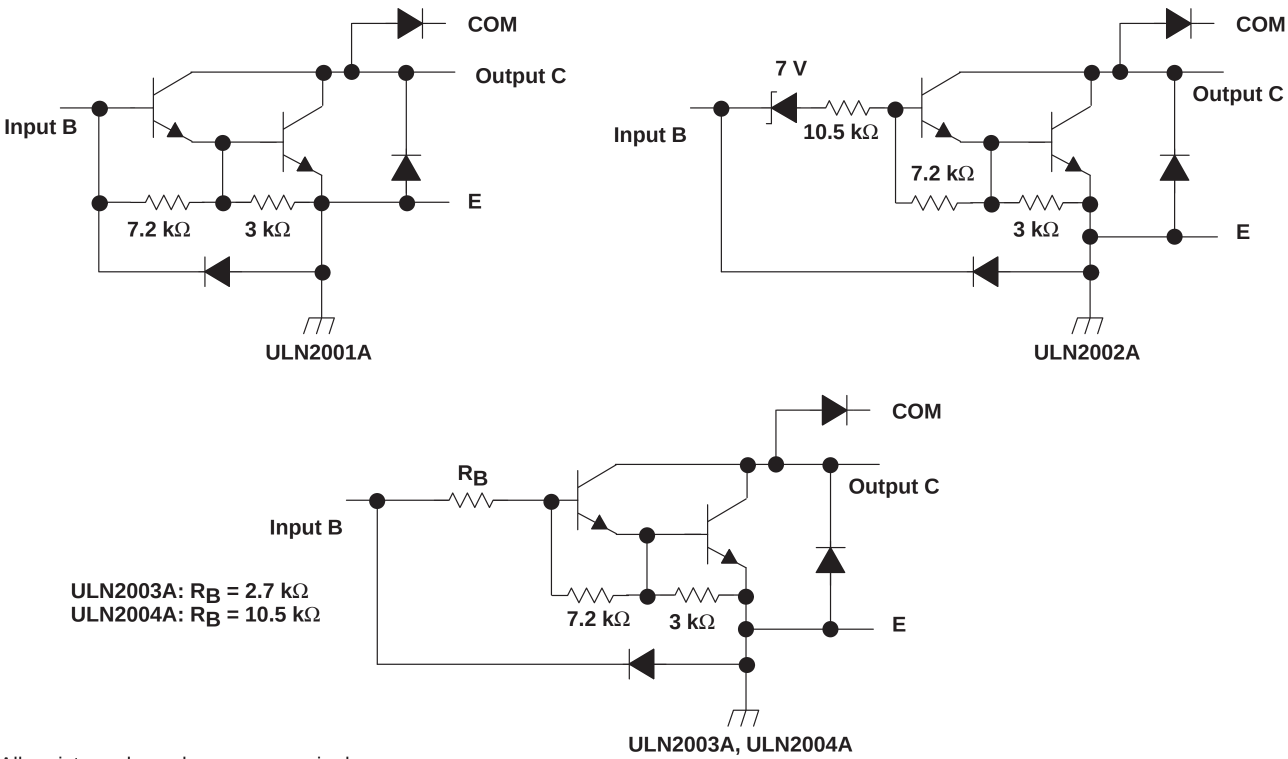


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage . . . . 50 V
Input voltage, V_I (see Note 1) . . . . 30 V
Peak collector current (see Figures 14 and 15) . . . . 500 mA
Output clamp current, I_{OK} . . . . 500 mA
Total emitter-terminal current . . . . –2.5 A
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –20°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2001A MIN	ULN2001A TYP	ULN2001A MAX	ULN2002A MIN	ULN2002A TYP	ULN2002A MAX	UNIT
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
I_R	Clamp reverse current	7	V_R = 50 V,	TA = 70°C			100			100	µA
			V_R = 50 V				50			50	
h_{FE}	Static forward current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A MIN	ULN2003A TYP	ULN2003A MAX	ULN2004A MIN	ULN2004A TYP	ULN2004A MAX	UNIT
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
		2	V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
				V_I = 1 V						500	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	7	V_R = 50 V				50			50	µA
			V_R = 50 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

switching characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	µs
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 9		0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 10	V_S – 20			mV

PARAMETER MEASUREMENT INFORMATION

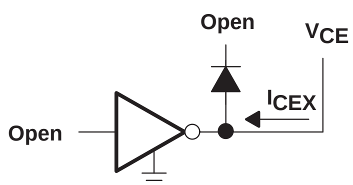


Figure 1. I_{CEX} Test Circuit

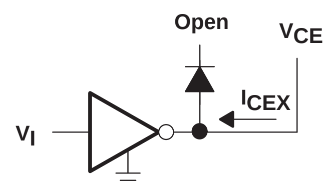


Figure 2. I_{CEX} Test Circuit

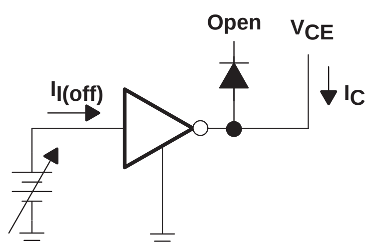


Figure 3. $I_{I(off)}$ Test Circuit

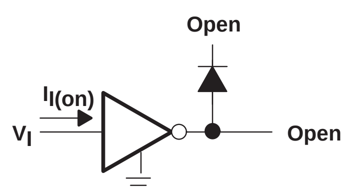
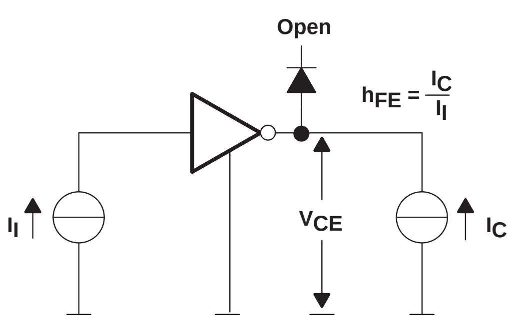


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

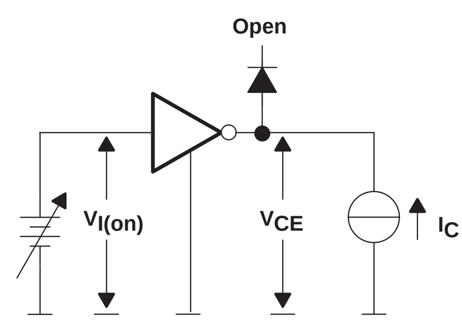


Figure 6. $V_{I(on)}$ Test Circuit

PARAMETER MEASUREMENT INFORMATION

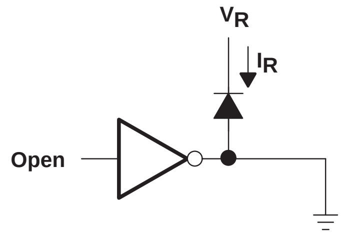


Figure 7. I_R Test Circuit

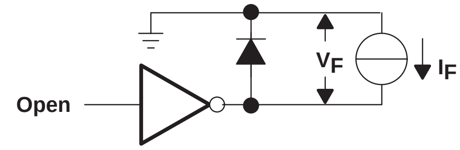
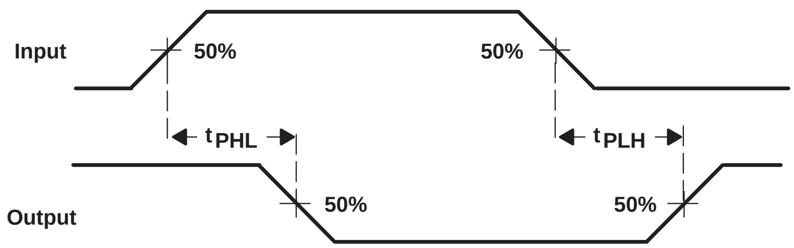
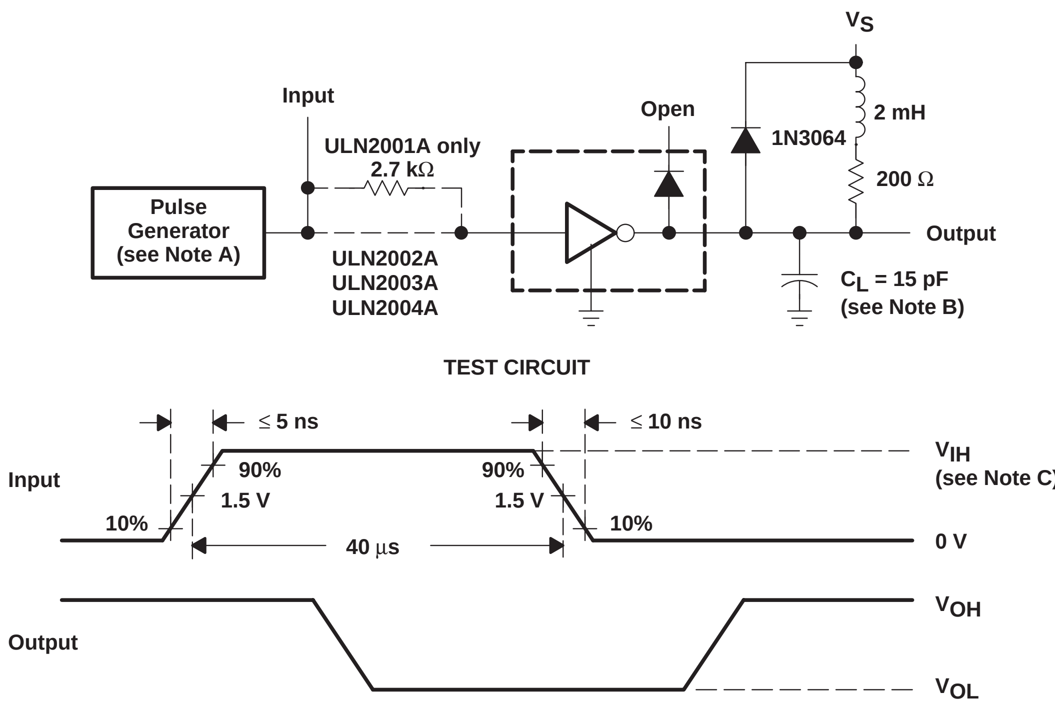


Figure 8. V_F Test Circuit



VOLTAGE WAVEFORMS

Figure 9. Propagation Delay Time Waveforms



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A and the ULN2003A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

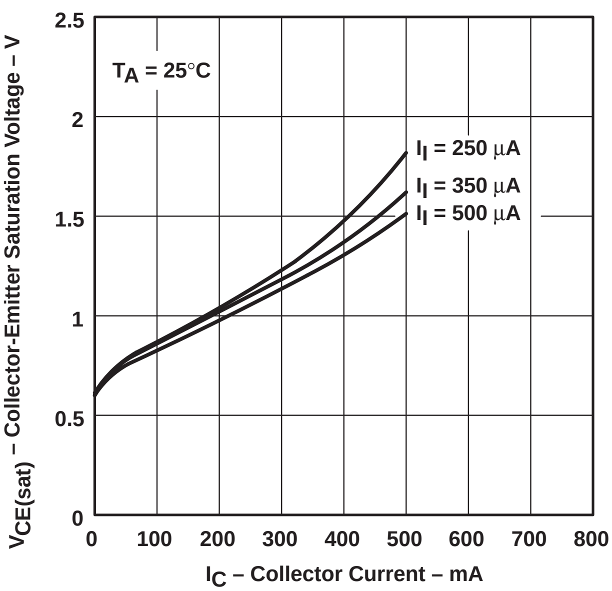


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

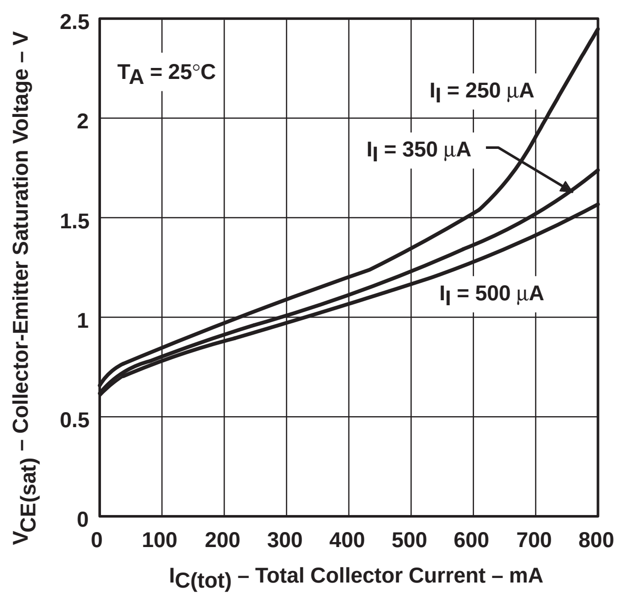


Figure 12

COLLECTOR CURRENT vs INPUT CURRENT

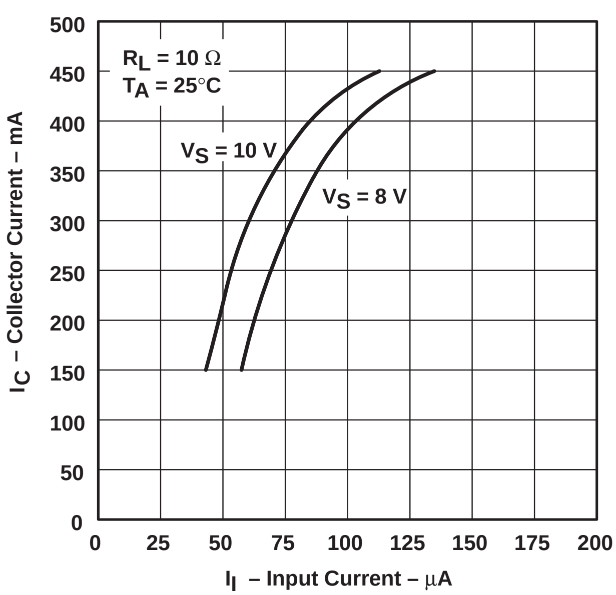


Figure 13

THERMAL INFORMATION

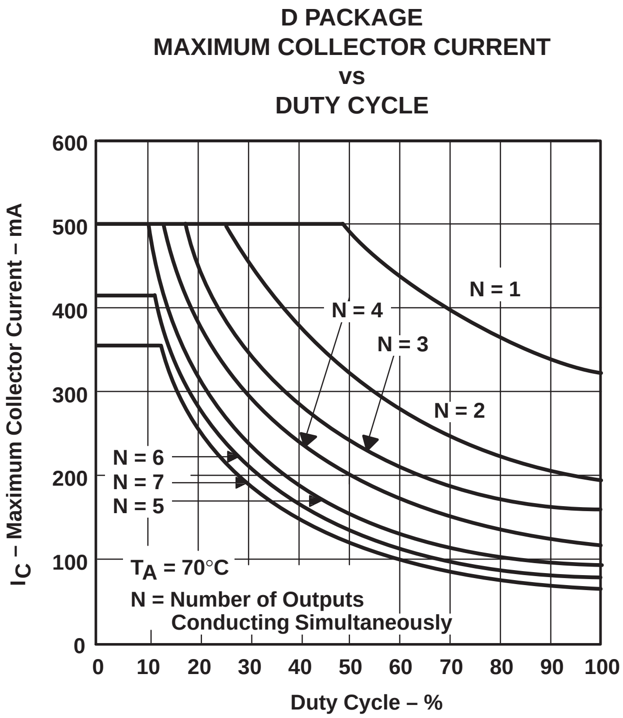


Figure 14

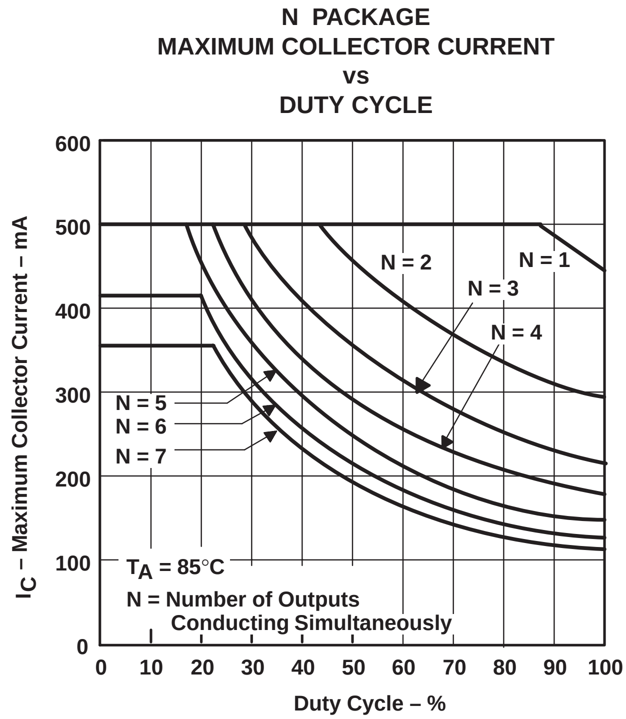


Figure 15

APPLICATION INFORMATION

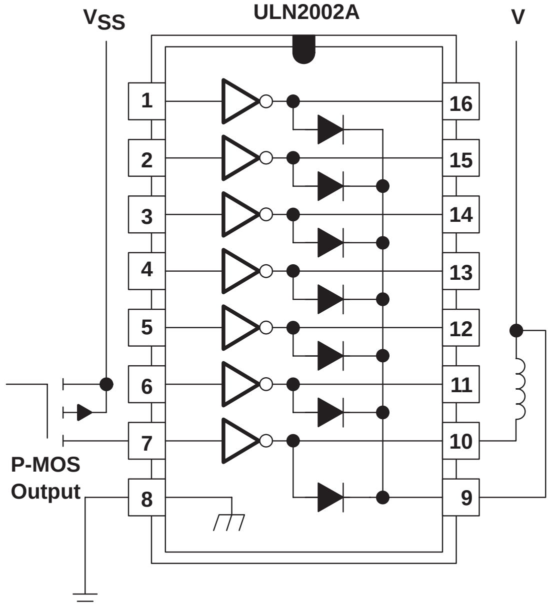


Figure 16. P-MOS to Load

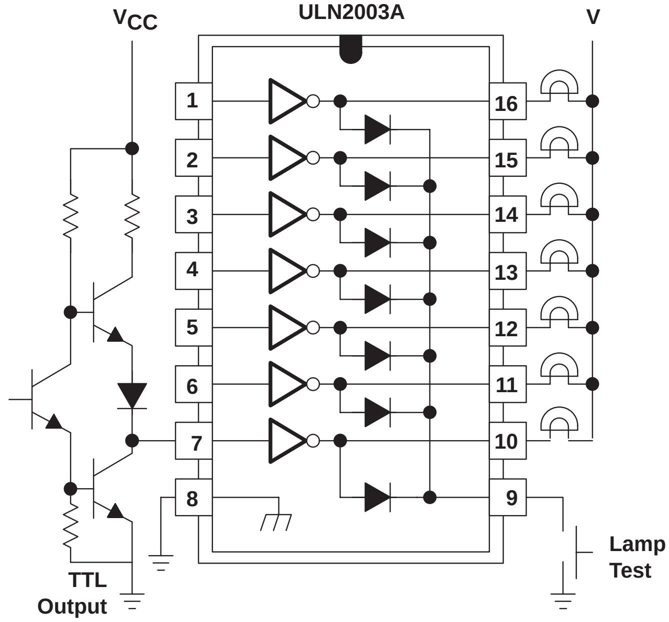


Figure 17. TTL to Load

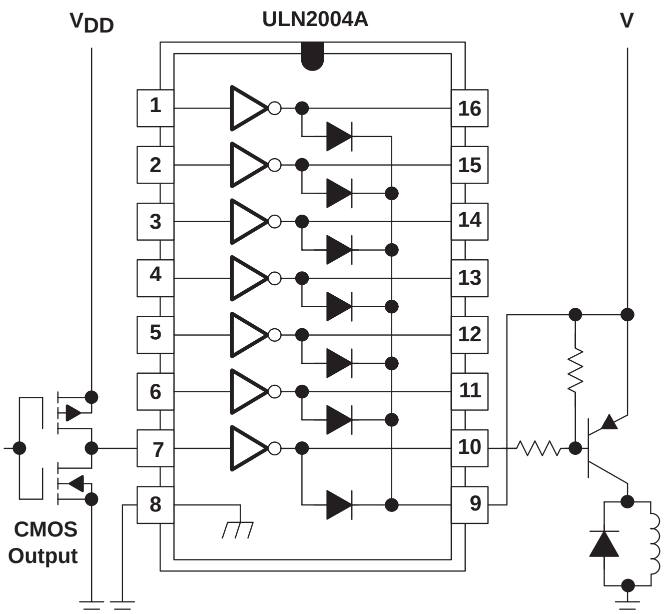


Figure 18. Buffer for Higher Current Loads

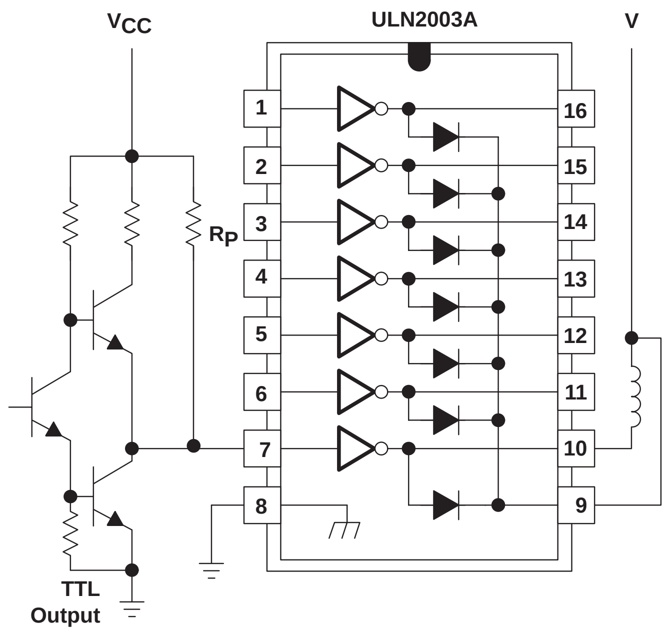


Figure 19. Use of Pullup Resistors to Increase Drive Current

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