APPLICATION NOTE U-158

Larry Spaziani
Applications Engineer
Unitrode Integrated Circuits

THE UC3910 COMBINES PROGRAMMABILITY, ACCURACY AND INTEGRATED FUNCTIONS TO CONTROL AND MONITOR HIGH END PROCESSOR POWER SUPPLIES

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by Larry Spaziani

ABSTRACT

As high performance processors continue to develop, their respective power supply requirements become more stringent, often requiring low, custom voltages and increasingly tighter regulation. Intel's Pentium®Pro power system specification, for instance, demonstrates the need for tight regulation, programmable power supply voltage and programmable voltage monitoring for status reporting to the processor. To help meet these requirements, the UC3910 4-BIT DAC and Voltage Monitor IC is introduced. This application note discusses the architecture and features of the UC3910 and details how this IC is used for an optimal Pentium®Pro power supply solution.

UC3910 4-BIT DAC AND VOLTAGE MONITOR

- High Precision Reference for tight regulation
  - 0.5% Typical combined DAC/Reference precision
- 4-BIT DAC directly compatible with Intel's Pentium®Pro VID function
  - Sixteen steps from 2.0V to 3.5V in 100mV increments
- Undervoltage and Overvoltage Fault Windows
  - User programmed with 2 external resistors
  - Proportional to DAC programmed voltage over the entire operating range
- Overvoltage Protection Comparator
  - Proportional to DAC programmed voltage over the entire operating range
  - Directly drives an external SCR
- Undervoltage Lockout

INTRODUCTION

The UC3910 4-BIT DAC and Voltage Monitor IC contains a 4-BIT Digital to Analog converter which is used to program a precise DC voltage for use in commanding a power supply voltage. The actual power supply voltage is compared against user programmable thresholds, with the comparators providing logic status to the system or protecting the power supply with a crowbar SCR. This IC has been developed to interface with Intel's Pentium® Pro processor, but has widespread uses where precise control and monitoring of a power supply voltage is required.

The high DC accuracy of the UC3910 reference and DAC, typically ±0.5%, makes this IC ideal for controlling and monitoring tightly regulated power supplies, such as high end processors or bus termination voltages. Tight regulation of power supplies can be met without adjusting the power supply voltage at manufacturing. The programmable output can also be used to digitally adjust a power supply voltage in test or manufacturing, allowing a single power supply design to accommodate multiple uses.

The UC3910 offers substantial advantages over discrete solutions when meeting Intel's Pentium®Pro power supply requirements. Its 4-BIT Digital-to-Analog Converter output voltage varies from 2.0V to 3.5V in 100mV increments for direct

compatibility with Intel's VID codes. The many integrated features and the programmability of the UC3910 allow power supply designers to replace discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver. Tight regulation can be met directly because of the excellent DC accuracy of the UC3910 combined DAC and reference voltages.

THE UC3910 4-BIT DAC AND VOLTAGE MONITOR

A block diagram of the UC3910 is shown in Figure 1.

The UC3910 is ideally suited to create a programmable, precision system reference for low voltage power supplies. Figure 2 shows the UC3910 configured with the UC3886 Average Current Mode PWM Controller IC to provide a solution for the

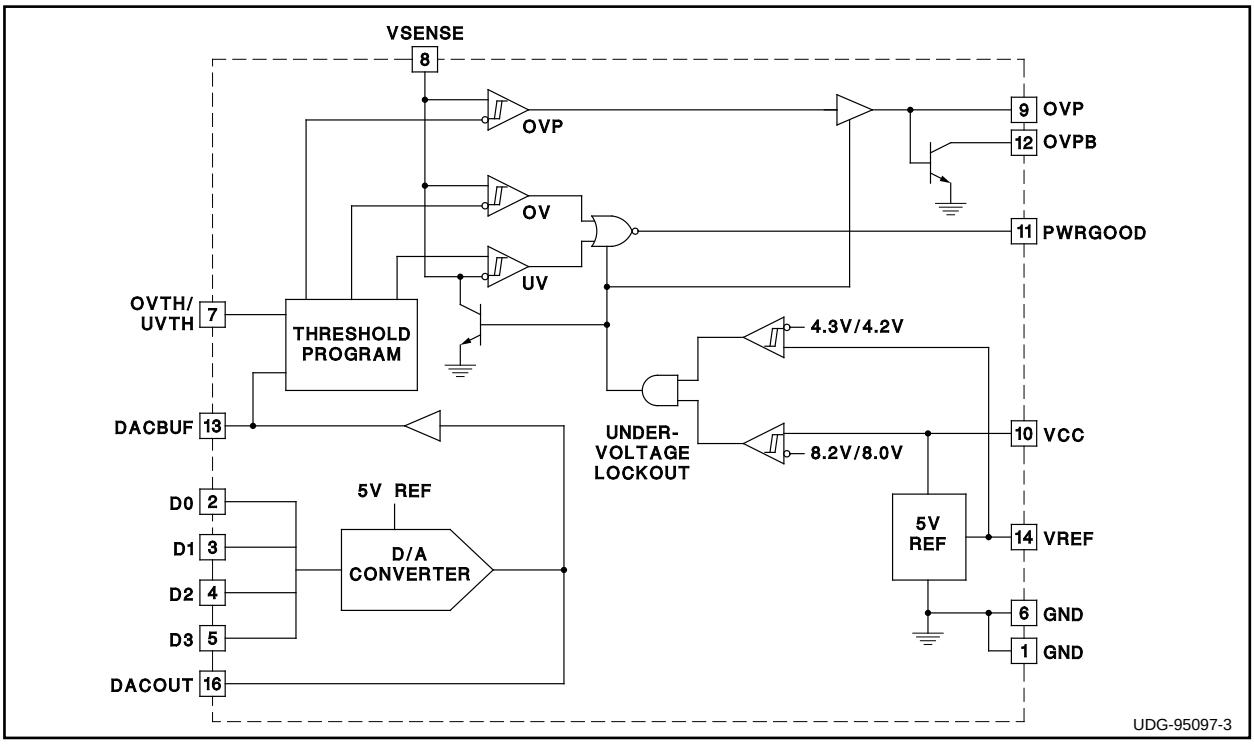

Figure 1. UC3910 4-BIT DAC and Voltage Monitor

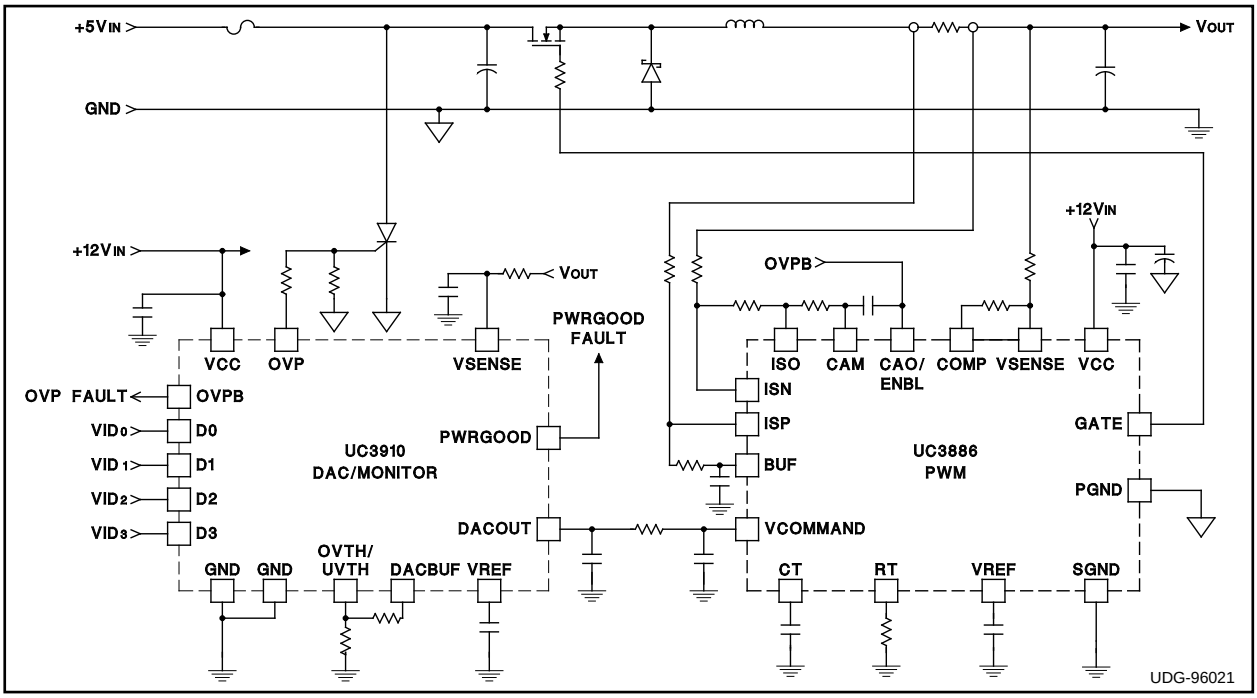

Figure 2. UC3910 Configured with the UC3886 for a Pentium®Pro DC/DC Converter

complex power system requirements of Intel's Pentium®Pro processor. The UC3910 is directly compatible with Intel's Voltage Identification (VID) code as shown in Figure 2.

UC3910 - SUPPLYING POWER

The UC3910 is constructed using a bipolar process allowing the input supply voltage, V_{CC}, to be as high as 20V. Minimum operating voltage is 8.2 volts. The supply voltage provides internal biasing of all circuit blocks including the high precision reference voltage, V_{REF}, which provides a precision reference voltage for the Digital to Analog Converter (DAC). VCC should be decoupled to ground with a 0.1µF to 1.0µF ceramic capacitor located in close proximity to the IC.

Grounding the UC3910

The UC3910 utilizes two ground pins to optimize the layout of the high precision DAC and Reference circuitry. Both ground pins must be connected to ground close to the IC and to each other.

UNDERVOLTAGE LOCKOUT

The UC3910 features an undervoltage lockout protection circuit for controlled operation during power up and power down sequences. Figure 3 shows typical V_{CC} thresholds of the UC3910 UVLO circuitry.

The supply current, I_{CC}, is typically less than 3mA during UVLO and is typically less than 10mA when V_{CC} is above the UVLO thresholds. External loading of the reference voltage will add to the supply current, I_{CC}. The 0.2V hysteresis prevents V_{CC} oscillations during the power up and power down sequences.

During UVLO, V_{REF} and the DAC output, DACOUT, are disabled, the threshold circuitry is disabled and the sense pin, VSENSE, is actively held low. The PWRGOOD signal is actively held LOW, the OVPB signal is forced HIGH (open) and the OVP signal's drive is disabled to insure no false control signals are generated during power up and power down sequencing.

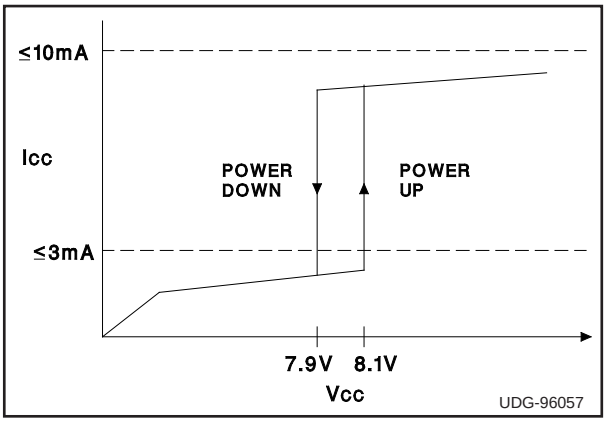

Figure 3. UC3910 UVLO Typical Values

VREF

The UC3910 contains a 5.0V precision trimmed bandgap reference, based on similar technology as that used on many other Unitrode ICs, but is enhanced by the use of precision thin film resistors. Thin film resistors exhibit excellent performance with voltage and temperature variations, and don't shift in value due to packaging stresses. These enhancements result in a reference voltage tolerance of ±0.5% from 0°C to 70°C. V_{REF} provides bias directly to the DAC circuitry, and plays a major role in the precision of the DAC output.

The reference can be used to bias external circuitry, can source up to 10mA and has internal short circuit protection. VREF should be decoupled with a 0.1µF to 1.0µF monolithic ceramic capacitor located close to the IC. Load circuits with high noise content should be avoided, or decoupled very well, as noise on V_{REF} will directly couple to the DACOUT pin.

VREF COMPARATOR

The reference voltage is internally monitored as shown in Figure 4. The 0.1V hysteresis prevents V_{REF} oscillations during the V_{REF} power up and power down sequences. While the reference voltage is below the V_{REF} threshold, VSENSE, PWRGOOD, OVP and OVPB are disabled in the same manner as they are during undervoltage lockout.

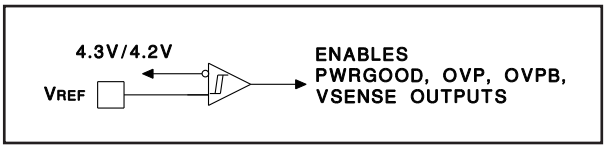

Figure 4. UC3910 V_{REF} Comparator

A typical power up sequence is shown in Figure 5. The voltage monitoring outputs are not enabled until time t_1 at which time V_{CC} and V_{REF} are above their respective thresholds.

PROGRAMMABLE DIGITAL-TO-ANALOG CONVERTER

The UC3910 contains a 4-Bit Digital to Analog Converter with an architecture shown in Figure 6. The DAC output (DACOUT) is a high impedance precision output programmed by the 4 programming pins, D0 (LSB) through D3 (MSB). Each programming bit pin controls a current source which is precisely trimmed to achieve the proper output voltage.

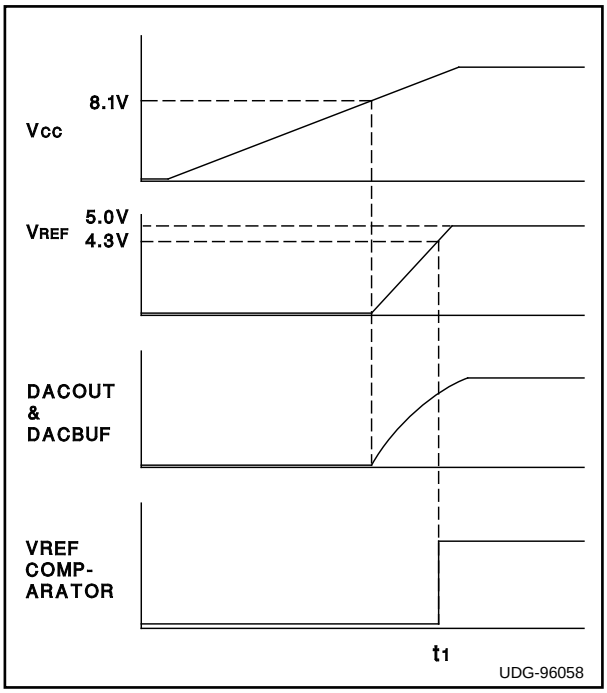

Figure 5. Power Up Sequence

DACOUT

The accuracy of the DACOUT pin, including the tolerance of the reference voltage, V_{REF} (combined accuracy), is typically ±0.5% and is ±0.9% from 0°C to 70°C worst case. DACOUT cannot be loaded externally since it is a high impedance (3kΩ) output. It should be decoupled locally with a 0.01µF to 0.1µF monolithic ceramic capacitor. A larger capacitor can be used to control the rise rate of the DACOUT voltage, where the internal 3kΩ resistor and the external decoupling capacitor form an RC time constant.

DACBUF

The DACBUF pin is a low impedance, buffered output of the DACOUT pin with a total gain/offset error of ±25mV. This pin is used by the UC3910 to set the overvoltage, undervoltage and overvoltage protection comparator threshold voltages. DACOUT cannot be used for this function since the threshold circuitry requires current and DACOUT cannot be loaded. The buffer is internally compensated for unity gain and cannot be decoupled externally. Good decoupling of the DACOUT and VCC pins will insure that the DACBUF signal is not corrupted by noise. DACBUF is internally clamped to 1 diode drop above ground during undervoltage lockout.

PROGRAMMING THE DAC

The DACOUT voltage is directly compatible with Intel's Pentium®Pro coding requirements, as shown in Table 1. The D0-D3 pins are directly equivalent to Intel's VID0 - VID3 signals. Intel requires programmable steps from 2.4V to 3.4V in 100mV increments, whereas the values of 2.0V to 2.3V and 3.5V are optional. The UC3910 DAC is programmable in 100mV increments, from 2.0V to 3.5V, where each decreasing bit represents a 100mV step, as shown Table 1.

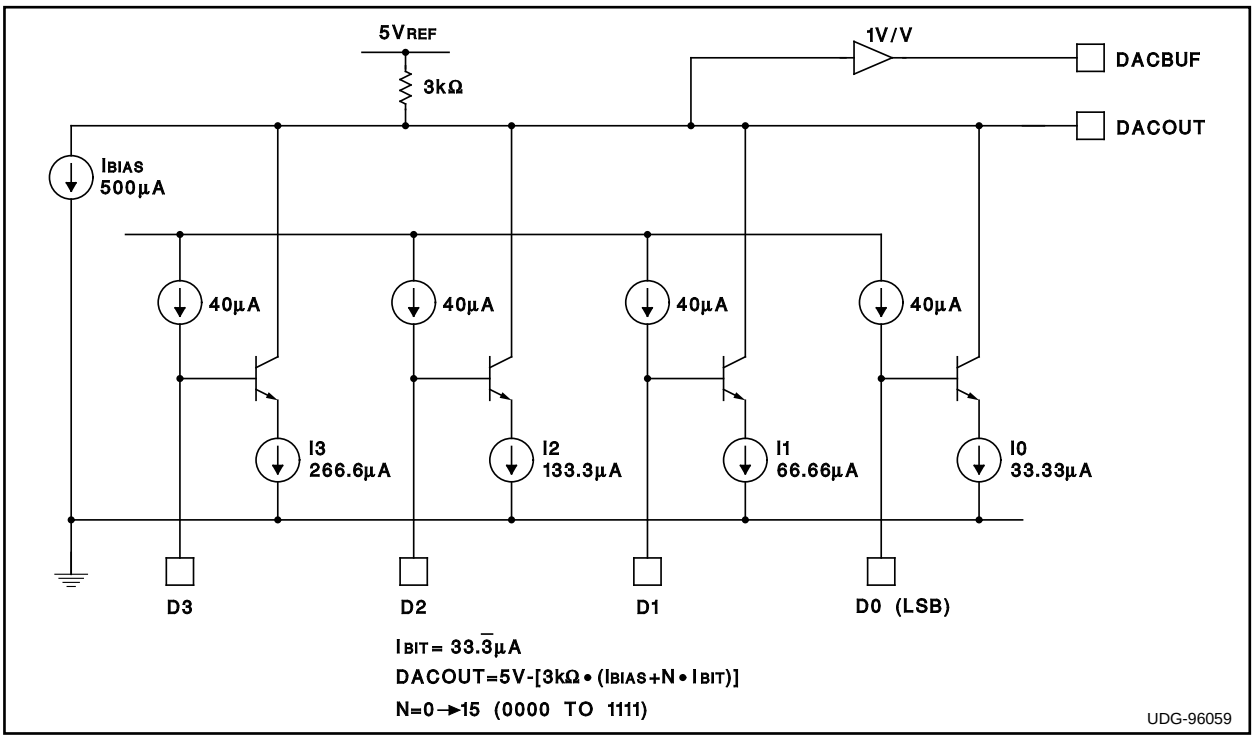

Figure 6. UC3910 Digital to Analog Converter (DAC) Architecture

Decimal Code	D3	D2	D1	D0	DACOUT Voltage	Pentium®Pro Specification	
15	1	1	1	1	2.0	No Processor	
14	1	1	1	0	2.1	2.1	
13	1	1	0	1	2.2	2.2	
12	1	1	0	0	2.3	2.3	
11	1	0	1	1	2.4	2.4	Intel's
10	1	0	1	0	2.5	2.5	|
9	1	0	0	1	2.6	2.6	|
8	1	0	0	0	2.7	2.7	|
7	0	1	1	1	2.8	2.8	↓
6	0	1	1	0	2.9	2.9	Operating
5	0	1	0	1	3.0	3.0	|
4	0	1	0	0	3.1	3.1	|
3	0	0	1	1	3.2	3.2	|
2	0	0	1	0	3.3	3.3	↓
1	0	0	0	1	3.4	3.4	Region
0	0	0	0	0	3.5	3.5	

Table 1. Programming the DACOUT Voltage

Figure 6 shows that each decimal code (0 through 15) represents an addition of 33.33µA of current through the 3kΩ resistor, which results in 100mV steps for each bit. A bias current of 500µA is used to set DACOUT to 3.5V when all four bits are 0s.

Programming pins D0-D3 are designed to accept OPEN = Logic 1 and SHORT = Logic 0 levels, as required by Intel, and will also accept open collector logic inputs. Each bit is pulled up internally to approximately 4.8V by a 40µA current source, as shown in Figure 6.

Some systems may want to control the D0-D3 pins from standard logic gates rather than open collector logic. The UC3910 will accept logic level inputs to the D0-D3 programming pins only if the logic HIGH level is ≥ 3.0 volts. The logic family should be well understood to insure that the driver can sink 40µA even when it is a logic HIGH.

Intel's specification for the Pentium®Pro processor includes all "1s" as an indicator that no processor is present. The UC3910 generates 2.0V on the DACOUT pin when all "1s" are present, thus insuring a safe low voltage level is present in a system should the programming pins be opened for any reason.

Dynamically Programming the DAC

The UC3910 is designed to accept the 4 bits as hardwired inputs prior to or at the same time power is applied to the UC3910. Dynamically changing the 4 bits is not recommended, as the characteristics (response time, overshoot, etc.) of the UC3910 DAC output under these conditions is highly dependent on external components. The time constant of the internal 3kΩ resistor and the DACOUT decoupling capacitor directly affect the rate at which DACOUT can dynamically change.

Changing the DAC Voltage Increments/Range

The UC3910 is designed to meet the Intel Pentium®Pro specification which requires programmable voltages from 2.4V to 3.4V in 100mV steps. Some systems may require exact power supply voltage outputs in ranges or increments other than those above in order to compensate for losses or to fine tune performance.

Upon inspection of Figure 6, a designer may opt to place an external resistor from DACOUT to VREF or to GND to adjust the DACOUT voltage up or down, respectively, as shown in Figure 7. This method, however, is NOT recommended. The UC3910 DAC is precisely trimmed to achieve it's accuracy, but the internal 3kΩ resistor IS NOT a precision resistor, and may be only accurate to ±20%. Designing an offset based on this internal resistor may therefore result in large errors. Should this method be used, the programmed voltage increment is no longer 100mV, but is proportional to the value of the external resistor used.

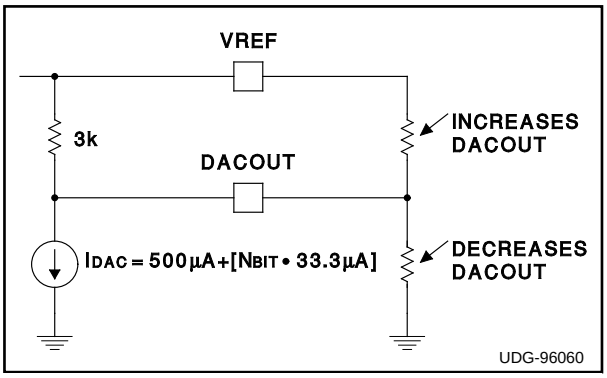

Figure 7. Using External Resistors to Adjust DACOUT is NOT recommended

A power supply's output voltage, controlled by the UC3910, may be adjusted when used in conjunction with the UC3886 PWM controller, as shown in Figures 8 (a) and (b). Increasing the voltage as shown in Figure 8 (a) can be accomplished with good accuracy by using precision resistors. Decreasing the voltage, as shown in Figure 8 (b) however, results in less accuracy, as the DACBUF buffered output includes gain/offset error of ±25mV (DACBUF = DACOUT ±25mV).

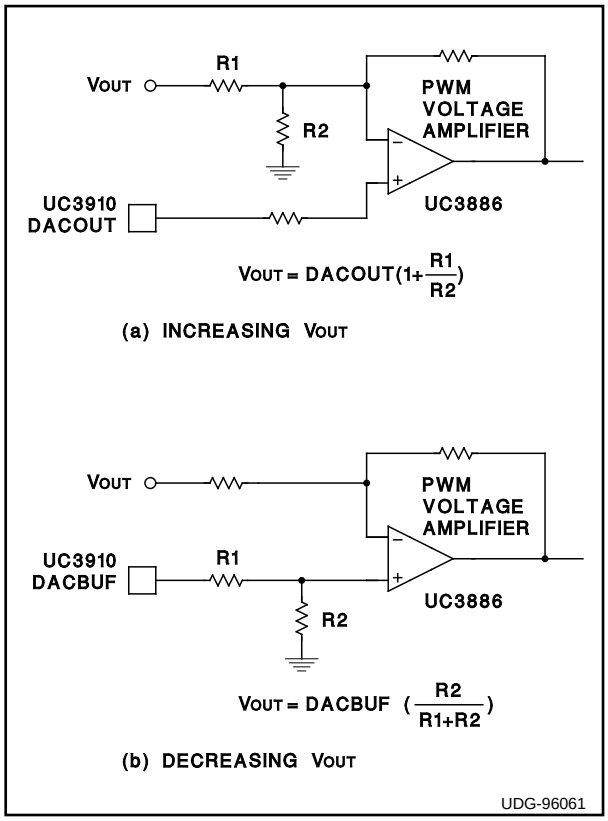

Figure 8. Recommended Methods for Adjusting a Power Supply's Output Voltage

VOLTAGE MONITORING SECTION

The UC3910's voltage monitoring section contains programmable window comparators which enable a power supply's output voltage to be closely monitored. The power supply's output voltage, as seen at the UC3910 VSENSE pin, is compared to three programmable thresholds; undervoltage, overvoltage, and overvoltage protection. The undervoltage and overvoltage comparators control the PWRGOOD signal to indicate that the output voltage is within a specified operating range. The overvoltage protection comparator controls the OVPB and OVP signals, which can be used to disable the power supply or to fire an external crowbar SCR.

The undervoltage, overvoltage, and overvoltage protection thresholds are programmed as a percentage above and below the programmed output (DACOUT), so that as the UC3910 DAC output voltage varies (various Pentium®Pro voltages for instance), so do the thresholds as a percentage of the DACOUT voltage.

Figure 9 shows a simplified schematic of the internal voltage monitor section. The voltage monitor section is programmable by the external resistors RS1 and RS2 at the threshold programming pin, OVTH/UVTH. RS1 and RS2 set the internal voltage thresholds which become inputs to the overvoltage, undervoltage and overvoltage protection comparators. The buffered DAC output, DACBUF, is used as the reference for the voltage monitoring thresholds.

VSENSE

The sense pin, VSENSE, is one input to the overvoltage, undervoltage and overvoltage protection comparators (OV, UV and OVP) which is compared to the set thresholds, as shown in Figure 9. VSENSE is typically connected to the output of the power supply which is controlled by the UC3910's precision output, DACOUT.

The hysteresis levels on the voltage monitor comparators can be as low as 20mV. VSENSE should be filtered externally with an RC filter, as shown in Figure 9, to insure that noise and ripple voltage does not cause false signals at the PWRGOOD and OVP pins. A filter frequency of 1/10th the power supply switching frequency is recommended, to reduce switching ripple by 20dB. The filter resistor and capacitor product is therefore

$$R_F \bullet C_F = \frac{1}{2 \bullet \pi \bullet (F_{SWITCH}/10)}$$

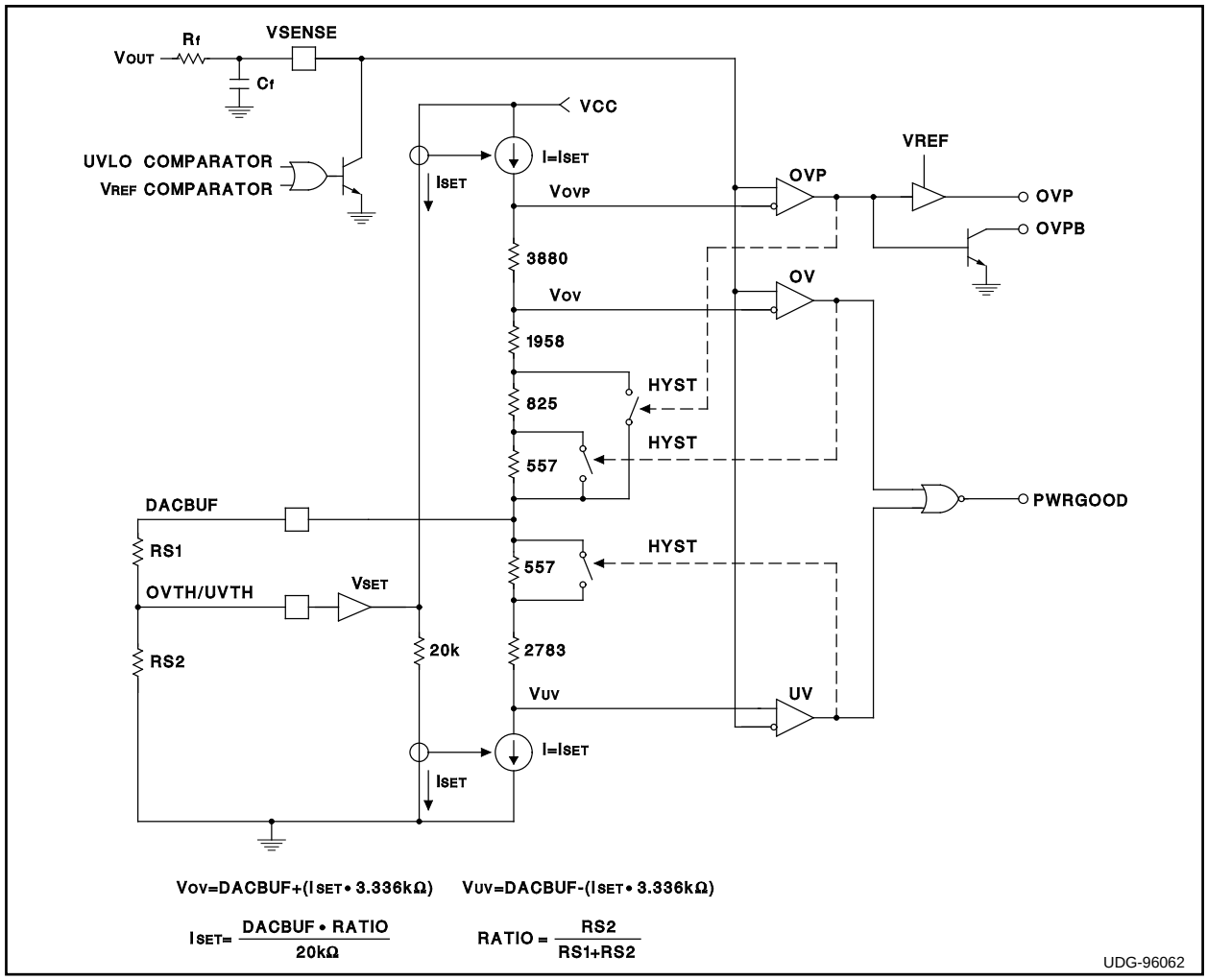

Figure 9. Voltage Monitor Section

VSENSE During UVLO - Protecting Against False OVP Signals

The UC3910 is designed to actively pull down VSENSE until V_{CC} and V_{REF} are above their respective thresholds during startup of the UC3910. This feature insures that during V_{CC} "brown-out" conditions, or when power supplies are powered up onto a live output bus, that the value of VSENSE will be below the DAC voltage, and will not trigger a false overvoltage protection signal. A V_{CC} "brown-out" situation is illustrated in Figure 10.

VSENSE can actively sink up to 500µA. The external filter resistor must therefore limit the current into VSENSE, such that

$$R_F \geq \frac{V_{OUT}}{500\mu A}$$

To insure that VSENSE does not falsely trigger an OVP condition, DACOUT must rise to its programmed level faster than VSENSE can rise. This restriction governs the two time constants on the VSENSE and the DACOUT pins. The DACOUT time constant is determined by the internal 3kΩ resistor and the DACOUT decoupling capacitor,

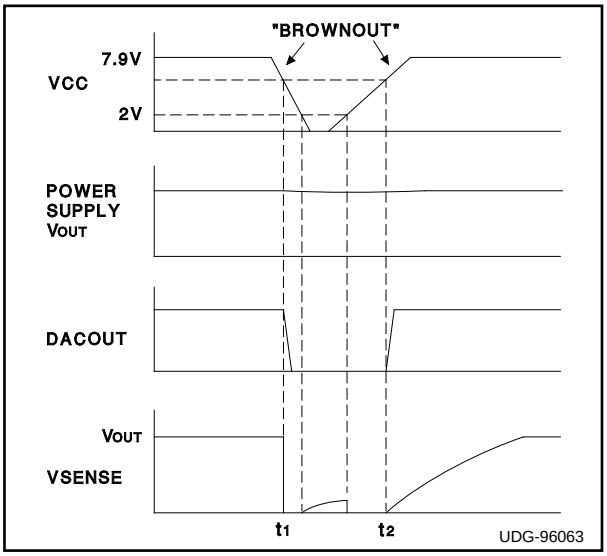

Figure 10. VSENSE is Pulled Low During UVLO Insuring that no False OVP Conditions Occur

whereas the VSENSE time constant is controlled by the external filter components R_F and C_F. From Figure 11, it can be seen that

$$R_F \bullet C_F > 3k\Omega \bullet C_{DACOUT}$$

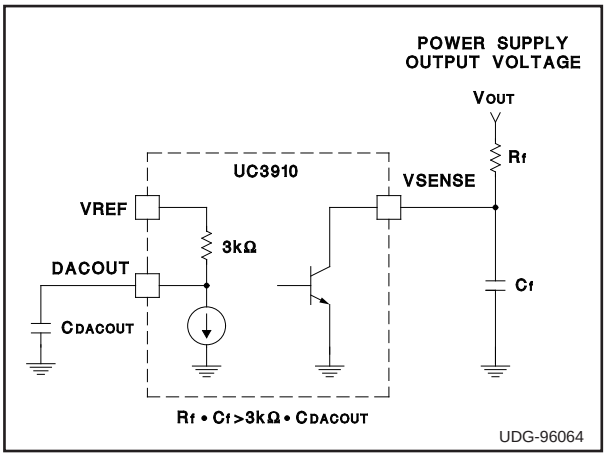

Figure 11. DACOUT Must Rise Faster than VSENSE

OVTH/UVTH Pin: Programming the OV, UV and OVP Thresholds

The UC3910 percentage thresholds are set above or below the nominal DAC output voltage, and are programmed by the ratio of the external resistors RS1 and RS2, R_{DIV}, where R_{DIV} is defined as

$$R_{DIV} = \frac{RS2}{RS1 + RS2}$$

The UC3910 allows a ratio R_{DIV} at the OVTH/UVTH pin from 0.3 to 0.9, which corresponds to overvoltage and undervoltage percentage thresholds from 5% to 15% and an OVP percentage threshold from 10% to 30%. These thresholds are shown in Figure 12.

The undervoltage, overvoltage and overvoltage protection (UV, OV and OVP) percentage thresholds are given by

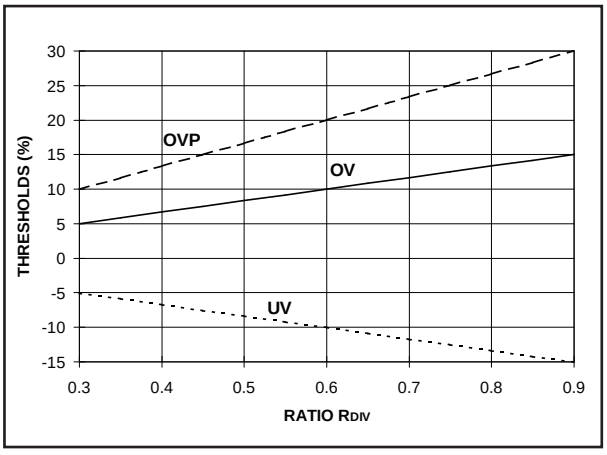

Figure 12. OV, UV and OVP Percentage Thresholds as a Function of the Divider Ratio R_{DIV}

$$\%V_{OV} = R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega} \bullet 100 = R_{DIV} \bullet 16.7$$

$$\%V_{UV} = -\%V_{OV} = -(R_{DIV} \bullet 16.7)$$

$$\%V_{OVP} = \%V_{OV} \bullet 2.0 = R_{DIV} \bullet 33.4$$

Refer to Figure 9 for the following derivation of how these UC3910 thresholds are set.

The voltage at the OVTH/UVTH pin, V_{SET}, is obtained by dividing DACBUF using RS1 and RS2, such that

$$V_{SET} = DACBUF \bullet \left[\frac{RS2}{RS1+RS} \right]$$

$$= DACBUF \bullet R_{DIV}$$

V_{SET} is internally buffered and then fed to a 20kΩ resistor to set the current I_{SET}, giving

$$I_{SET} = \frac{V_{SET}}{20k\Omega}$$

I_{SET} is then mirrored to the overvoltage and undervoltage resistive chains shown in Figure 9. The total resistance in the overvoltage and undervoltage chains is 3.34kΩ, whereas the total resistance in the overvoltage protection chain is 6.663kΩ. DACBUF is internally tied to the "center" point of the resistive chains as a reference voltage for the thresholds. The UV, OV, and OVP threshold voltages, at their respective comparators, are therefore given by:

$$V_{OV} = DACBUF + I_{SET} \bullet 3.34k\Omega$$

$$V_{UV} = DACBUF - I_{SET} \bullet 3.34k\Omega$$

$$V_{OVP} = DACBUF + I_{SET} \bullet 6.663k\Omega$$

These threshold voltages can be expressed in terms of percentages above or below the nominal DACBUF voltage since they are all biased by the programmed DACBUF voltage. The overvoltage percentage is determined by

$$\%V_{OV} = \left(\frac{V_{OV} - DACBUF}{DACBUF} \right) \bullet 100$$

which can be simplified to

$$\%V_{OV} = \left(R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega} \right) \bullet 100 = R_{DIV} \bullet 16.7$$

Likewise, the undervoltage and overvoltage protection percentage thresholds can be expressed as

$$\%V_{UV} = -(R_{DIV} \bullet 16.7) \text{ and}$$

$$\%V_{OVP} = R_{DIV} \bullet 33.4 = \%V_{OV} \bullet 2.0$$

(The OVP threshold percentage is 2.0 times the OV threshold percentage)

These percentage thresholds are shown graphically in Figure 12.

Hysteresis and Tolerances in the OV, UV and OVP Thresholds:

Each of the UV, OV and OVP threshold circuits in the resistive chain of Figure 9 contains a hysteresis resistor, which is switched in or out by the output of the respective comparator. The result is that the threshold voltages change (in voltage, not percent) by

$$UV_{HYS} = -(I_{SET} \bullet 557\Omega)$$

$$OV_{HYS} = I_{SET} \bullet 557\Omega$$

$$OVP_{HYS} = I_{SET} \bullet 1382\Omega$$

I_{SET} is proportional to both the programmed DAC voltage DACBUF as well as the ratio R_{DIV} which sets the thresholds. For an Intel Pentium®Pro application with voltages ranging from 2.4V to 3.4V and R_{DIV} ranging from 0.3 to 0.9, the hysteresis can range from 20mV to 85mV on OV and UV and from 50mV to 211mV on OVP. The effects of hysteresis are shown graphically in Figure 13.

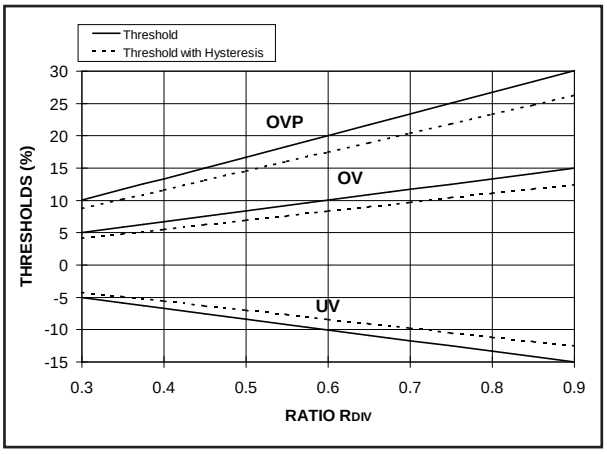

Figure 13. OV/UV and OVP Thresholds Including Hysteresis

There are tolerance factors that a circuit designer should consider when programming the voltage monitor threshold percentages. They are:

- UC3910 DACBUF error of ± 25mV
- UC3910 OV, UV and OVP Comparator off set voltages of ±10mV
- UC3910 Bias current from the OVTH/UVTH pins of ±30% of the value Iset
- UC3910 Threshold detection tolerance of ±10% of the percentage set
- External Resistor tolerances
- Non-ideal External resistor Values (The perfect divider ratio may not be achievable)

The designer can reduce the error due to external resistors by using precision values. Errors due to bias current from the OVTH/UVTH pin can also be minimized by using external values which draw approximately 1.0mA from DACBUF (presents a low impedance to the leakage current source), or

$$\frac{DACBUF}{RS1 + RS2} \approx 1.0mA$$

Unitrode has performed a Worst Case and an Root Sum Square (RSS) error analysis including all the abovementioned factors, for a set Ratio of R_{DIV}=0.45 (7.5% OV/UV thresholds), and using 1% resistors, with the results shown in Figure 14.

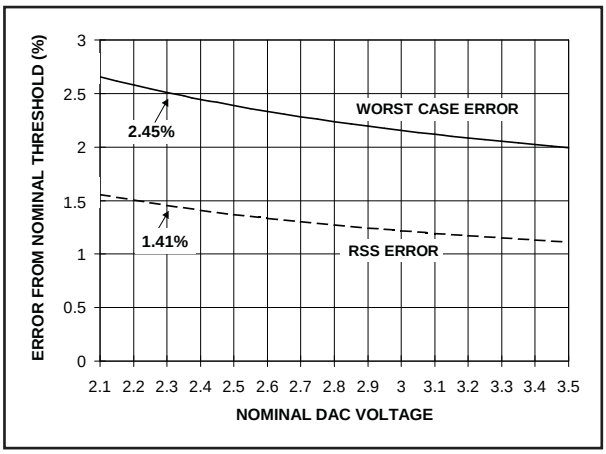

Figure 14. Error Analysis for a Nominal 7.5% OV/UV Threshold Setting - Varies with V_{OUT}

Should higher accuracy be required for the thresholds, the stability of the offset voltages and bias currents of the UC3910 with life and temperature is such that a voltage divider, RS1 and RS2, can be set up at manufacturing to set the thresholds very precisely, with little drift expected over the life of the power supply.

PWRGOOD

The PWRGOOD signal is an open collector logic level that is HIGH when the voltage at the UC3910 VSENSE pin is above the UV threshold and below the OV threshold, as indicated in Figure 9. The PWRGOOD signal must be pulled up externally to a voltage less than V_{CC}(max) and can sink 10mA.

Figure 15 illustrates the PWRGOOD comparator and drive stage. PWRGOOD is held low until the UC3910 supply voltage is above the UVLO threshold and the reference voltage is above the V_{REF} threshold, as indicated in Figure 15.

The PWRGOOD comparator output, during power up and power down sequencing, gets “smart” with V_{CC} at approximately 2.0 volts. Until V_{CC} reaches this level, there is not enough bias current (Figure 15, I1) to keep the PWRGOOD signal held in its low state. In most systems, where the PWRGOOD signal will act as the reset for the processor, this will

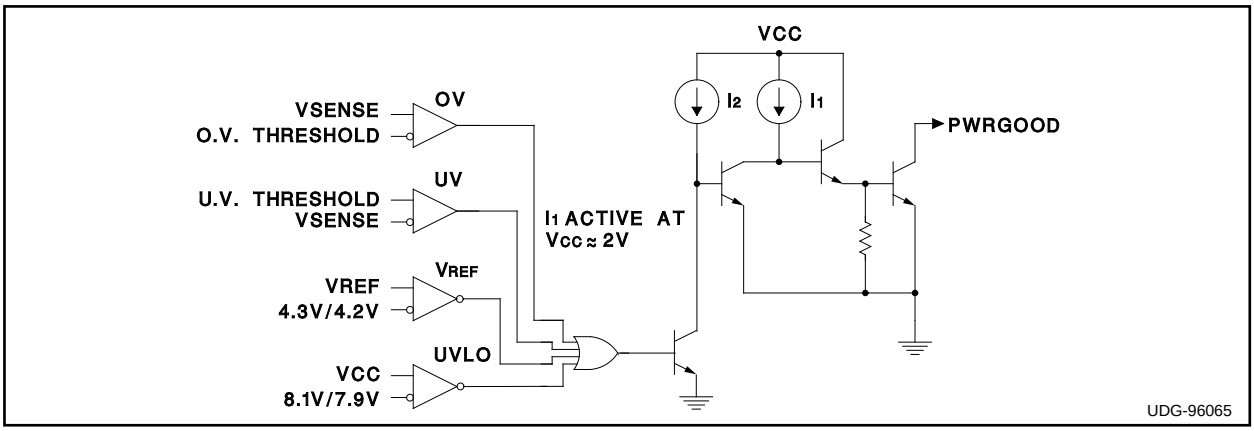

Figure 15. PWRGOOD Comparator and Drive

not matter since the processor itself will have no power during the time V_{CC} is lower than 2.0 volts.

Resistor R2 shown in Figure 16 can be used to pull down the PWRGOOD signal, thus insuring that even with VCC at 0 volts, the PWRGOOD signal will not provide an erroneous signal. R2 should be chosen such that it can sink a small amount of leakage current from the logic receiving circuit and still maintain logic low level. R1 must be chosen to limit the current into PWRGOOD to less than 10mA, and also to provide the proper level HIGH voltage. V_{REF} is disabled during UVLO, thus insuring there will be no pull-up voltage. Low voltage logic families can also be accommodated by using the circuit of Figure 16.

The PWRGOOD signal may be used as a reset signal to processor which is controlled by the UC3910 itself. A reset delay may be added to allow the processor to boot some time after the PWRGOOD signal. A typical reset circuit is shown in Figure 17.

OVP and OVPB Overvoltage Protection Signals

The OVP output signal is designed to directly trigger a silicon controlled rectifier (SCR) thyristor when a severe overvoltage condition occurs. OVPB is an open collector signal designed to go LOW under the same conditions, which can be used to disable a PWM such as the UC3886. The OVP comparator (see Figure 9) is tripped when the output voltage has reached a voltage equal to two times the programmed overvoltage threshold.

Figure 18 illustrates the OVP comparator and drive stage. The OVP and OVPB signals are disabled until the UC3910 supply voltage is above the UVLO threshold and the reference voltage is above the V_{REF} threshold, as indicated in Figure 18, by removing the bias current from the drive stage.

The OVP output drive, during power up and power down sequencing, gets "smart" with V_{CC} at approximately 2.0 volts. A minor amount of drive current can leak through to the OVP output while V_{CC} is lower than 2.0V. It is recommended that a 1kΩ maximum resistor be connected from OVP to ground, to insure that this leakage current does not charge an external SCR gate.

Figure 19 shows the UC3910 driving an external SCR. The UC3910 OVP signal, when high, will source a minimum of 65mA. Many SCRs require a

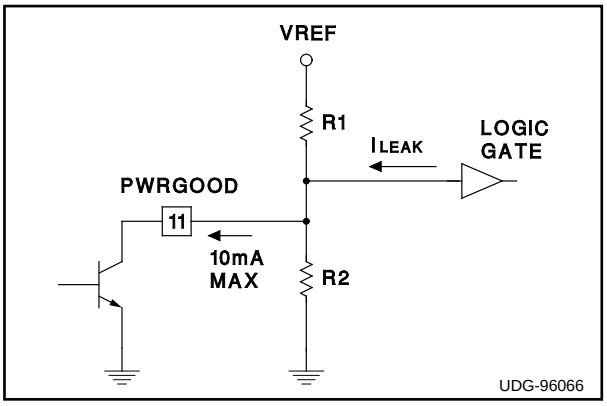

Figure 16. Add a Pull-down Resistor to PWRGOOD to Insure Proper Signal at $V_{CC} \leq 2$ Volts

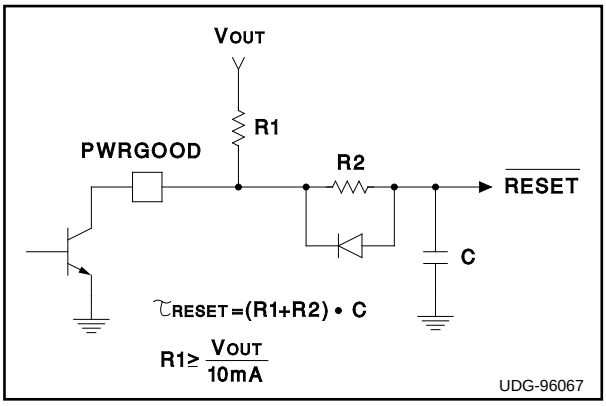

Figure 17. Using PWRGOOD to Reset the Processor

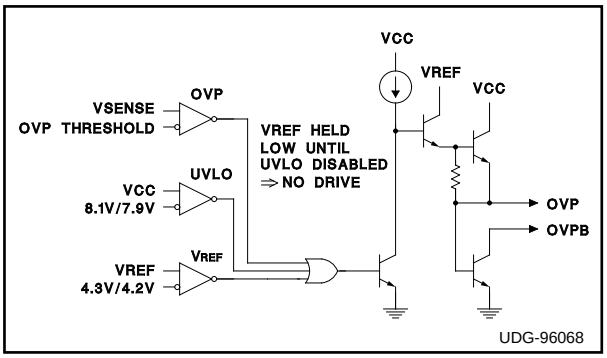

Figure 18. OVP Comparator and Drive

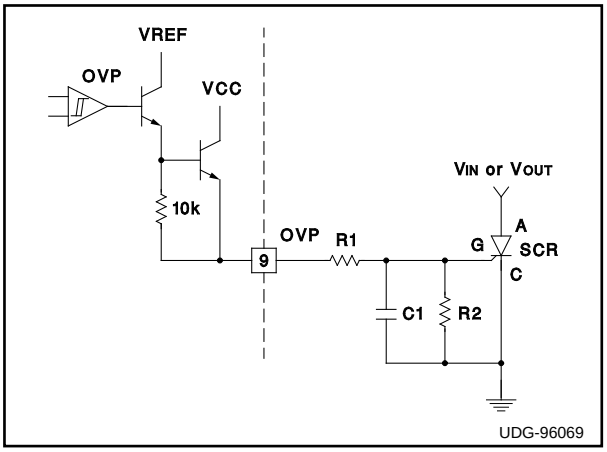

Figure 19. Driving an SCR using the UC3910 OVP Signal

gate trigger current (IGT) between 30mA and 50mA. The output high voltage will be approximately 4.3V maximum. The OVP signal is not pulled low internally to the UC3910.

Resistor R1 in Figure 19 is chosen to limit the gate current to minimize current draw on V_{CC} while insuring that the rated gate current is met. Resistor R2 is required to insure that the SCR is not inadvertently fired due to dc leakage currents or parasitic dv/dt effects through the SCR itself. C1 can be used to provide additional gate filtering, but should not be so large that the SCR gate signal is significantly delayed.

There are many tradeoffs to consider when choosing which SCR to use and where to use it to best protect critical electronics. SCR theory and various crowbar circuits are discussed extensively in literature [1] and in device data books [2].

The OVPB signal can be used to disable a power supply through a logic disable signal. This is easily accomplished when the UC3910 is used in conjunction with the UC3886 PWM controller IC, as demonstrated in Figure 20.

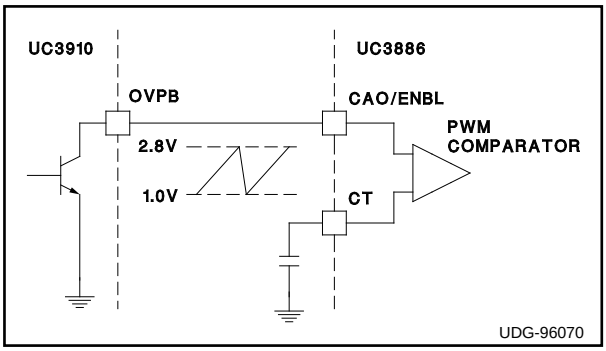

Figure 20. Disabling the UC3886 Switching Using the OVPB Signal

Circuit Example - Programming the Voltage Monitor Thresholds

Refer to Figure 9 and Figure 11, and program the UC3910 Voltage Monitor Section for the following requirements:

V_{OUTPUT} ranges from 2.4V to 3.4V (i.e., Pentium®Pro application)

F_{SWITCH} = 200kHz

Ripple voltage = 2% peak-to-peak

OV and UV Thresholds must be ±5% MINIMUM

OVP is to be set at 20% Maximum

Step 1: Choose to set the nominal overvoltage and undervoltage thresholds at 7.5% to insure that the ±5% thresholds are met.

Step 2: Calculate the ratio R_{DIV}, based on the desired 7.5%:

R_{DIV} = 7.5/16.7 = 0.45

Step 3: Find nominal values for RS1 and RS2

Let RS1 + RS2 draw ≈ 1.0mA at the maximum DACBUF voltage. Therefore

$$RS1+RS2 \approx \frac{3.4V}{1.0mA} \approx 3.4k\Omega$$

$$R_{DIV} = 0.45 = \frac{RS2}{RS1+RS2}$$

RS2 = 1.54kΩ RS1 = 1.91kΩ

RS1+RS2 = 3.45kΩ R_{DIV} = 0.446

Step 4: Find the hysteresis in terms of percentage, over the 2.4V to 3.4V range:

$$OV_{HYS} = I_{SET} \bullet 557\Omega$$

$$= DACBUF \bullet R_{DIV} \bullet \frac{557\Omega}{20k\Omega}$$

$$UV_{HYS} = -OV_{HYS}$$

$$OVP_{HYS} = I_{SET} \bullet 1382\Omega$$

$$= DACBUF \bullet R_{DIV} \bullet \frac{1382\Omega}{20k\Omega}$$

The OV and UV hysteresis is 30mV @ 2.4V and 42mV @ 3.4V

The OVP hysteresis is 74mV @ 2.4V and 105mV @ 3.4V

Hysteresis on the OV and UV is ± 1.25%, and on the OVP is ± 3.1%

Step 5: Find V_{SENSE} filter components and calculate effective ripple at the VSENSE pin.

$$R_F \geq \frac{V_{OUTmax}}{500\mu A} \geq \frac{3.4V}{500\mu A} \geq 6.8k\Omega$$

Let $R_F = 6.8k\Omega$ as a standard 5% value.

$$C_F \geq \frac{1}{2 \bullet \pi \bullet (F_{SWITCH}/10)}$$

$$\geq \frac{1}{2 \bullet \pi \bullet (200kHz/10) \bullet 6.8k\Omega}$$

$$\geq 1170pF$$

Let $C_F = 1200pF$ as a standard value, giving a filter corner frequency of < 20kHz.

V_{RIPPLE} = 2% peak-to-peak • 1/10 = 4.8mV to 6.8mV peak to peak. This is well below the hysteresis ranges found in step 4.

Step 6: Solve for the thresholds. Use Figure 14 to estimate tolerances.

Nominal: $UV = -R_{DIV} \bullet 16.7 = -7.45\%$

$OV = R_{DIV} \bullet 16.7 = 7.45\%$

$OVP = OV \bullet 2.0 = 14.9\%$

Minimum OV/UV 7.45% - 2.45% = 5.00%

Maximum OV/UV 7.45% + 2.45% = 9.90%

Maximum OVP: 14.9% + 2.45% =17.35%

Step 7: Insure the time constant on VSENSE is slower than that on DACOUT

$$C_{DACOUT} \leq \frac{R_F \bullet C_F}{3k\Omega}$$

$$\leq \frac{6.8k\Omega \bullet 1200pF}{3k\Omega}$$

$$\leq 2720pF$$

Let $C_{DACOUT} = 2700pF$ as a standard value.

SUMMARY

The UC3910 contains all the features required to command power supplies requiring custom voltages, precise regulation, programmable voltage monitoring and circuit protection. The high DC accuracy of the UC3910 reference and DAC makes this IC ideal for controlling and monitoring tightly regulated power supplies, such as high end processors or bus termination voltages. Multiple discrete precision components can be replaced by the many integrated functions of the UC3910. Voltage programming is directly compatible with Intel's Pentium®Pro processor and voltage monitor threshold programming is precisely controlled with only two external resistors. Protecting the load against overvoltage can be performed with a logical shutdown or by driving a crowbar SCR.

Together with the UC3886 Average Current Mode PWM Controller IC, an optimal power supply can be designed to meet the stringent requirements of the Intel Pentium®Pro processor. For additional information on the UC3886 Average Current Mode PWM Controller IC, refer to application note U-156 [3]. For additional information on a detailed circuit design and performance of the UC3886/UC3910 chip pair, refer to application note U-157 [4].

REFERENCES

[1] Abraham I. Pressman, "Switching and Linear Power Supply, Power Converter Design" Switchtronix Press, 1987

[2] Thyristor Device Data Book, Motorola, Phoenix, Arizona.

[3] U-156 The UC3886 PWM Controller Uses Average Current Mode Control to Meet the Transient Regulation Performance of High End Processors, L. Spaziani

[4] U-157 Fueling the Megaprocessor - A DC/DC Converter Design Review Featuring the UC3886 and UC3910, L. Spaziani

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

UNITRODE 7 CONTINENTAL BLVD. • MERRIMACK, NH 03054 • TEL (603) 424-2410 • FAX (603) 424-3460

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