APPLICATION NOTE U-166

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AN OFF-LINE LEAD ACID CHARGER BASED ON THE UC3909

UNITRODE

INTRODUCTION

Lead-acid batteries are the most commonly used batteries where large amounts of energy must be stored and low cost is more important than weight or physical size. Typical applications include UPS systems, alarm system backup power, telephone system backup power and larger portable electronic devices such as a bag-phone. This paper presents an isolated switch-mode charging circuit for lead-acid batteries that operates from a 115V_{ac} circuit.

The reader is encouraged to read the references listed at the end of this paper. There is much useful information there that will not be repeated here.

DESIGN REQUIREMENTS

For this design, the goal is to charge an Eagle-Picher HE12V12.7 battery as quickly and safely as possible to the highest practically attainable capacity, and maintain this capacity indefinitely. From the battery manufacturer's data sheet, this battery may be charged from a 14.6 to 15.0 volt source that is current limited to 4.0 amps. Therefore, the bulk charge current for this charger (I_{bulk}) will be 4.0 amps and the maximum overcharge voltage (V_{oc}) will be 14.8 volts. The float voltage is specified to be 13.6 to 13.8 volts. This charger will float the battery at 13.8 volts (V_{float}). The battery is specified to a discharge voltage of 10.5 volts so this value will be used as the bulk charge enable threshold (V_{CHGENB}).

The remaining parameters that must be specified for the circuit (I_{OCT} and I_{TC}) are up to the circuit designer. In this design, the over charge terminate current threshold (I_{OCT}) is picked to be 10% of I_{BULK} or 400mA. The trickle current (I_{TC}) is picked to be 2% of the bulk current or 80mA.

The power source for this charger will be a standard 125 V_{ac} circuit. The tolerances on this input voltage will be +10/–25%. This means that the bulk supply on the primary side can range from 130 to 195 V_{dc}.

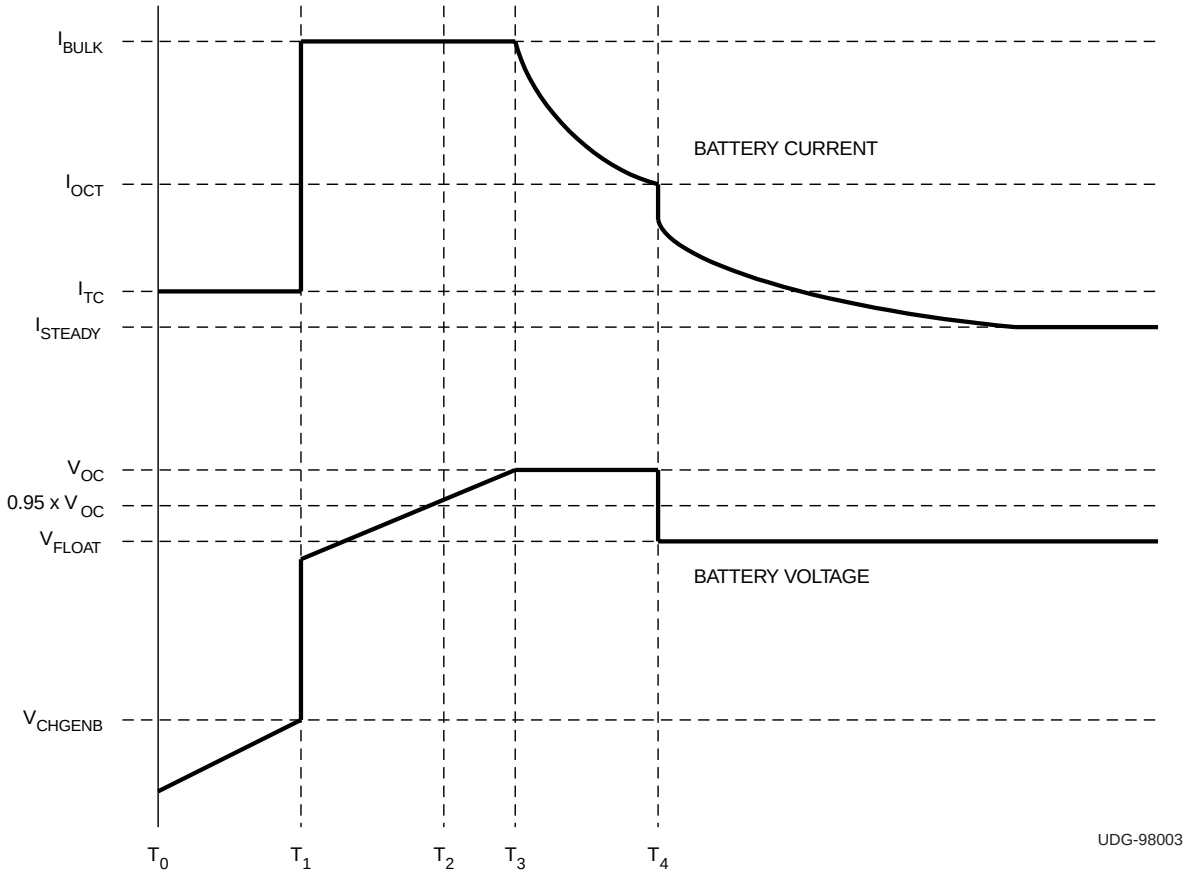

Figure 1. Battery voltage and current over one charging cycle.

DESIGN OVERVIEW

The UC3909 implements a four-stage charging algorithm. The four stages are trickle charge, bulk charge, over charge and float charge. The stages operate as follows in Fig. 1.

Trickle Charge

(T_0 to T_1) The charger will supply a small current, typically C/100 (I_{TC}) to the battery until the battery voltage reaches a predetermined threshold value (V_{CHGENB}). The purpose behind trickle charging is to prevent a potentially hazardous condition caused by continuously pumping bulk charge current into a damaged battery. Note that trickle charging may be skipped depending upon the battery voltage when the charger is powered. In some applications, it may be necessary to disable the trickle charge portion of the algorithm entirely. An example of this might be a device that normally operates from the incoming line and needs more current than can be programmed in the trickle charge state. The trickle charge stage can be permanently disabled by connecting CHGENB to VLOGIC.

Bulk Charge

(T_1 to T_2) The charger will supply a constant current to the battery if the battery voltage is above a given threshold. This current will be applied until the battery voltage rises above 95% of the maximum overcharge voltage.

Over Charge

(T_2 to T_4) During the over charge state, the charger tries to regulate the battery voltage to a constant voltage, V_{oc}. When the charger enters the over charge state, the current control loop will likely be dominant and a constant current will continue to be applied to the battery. As the battery voltage rises, the voltage control loop will begin to take over and regulate the battery voltage to the over charge voltage V_{oc} (Shown at T_3).

Float Charge

(T_4 and beyond) The float charge is entered when the battery current falls below a preset threshold while its voltage is held at V_{oc}. While in the float state, the charger will supply up to I_{bulk} amperes to a load and the battery. The charger will remain in the float state until power to the UC3909 is cycled or until the battery voltage drops below 90% of V_{oc}.

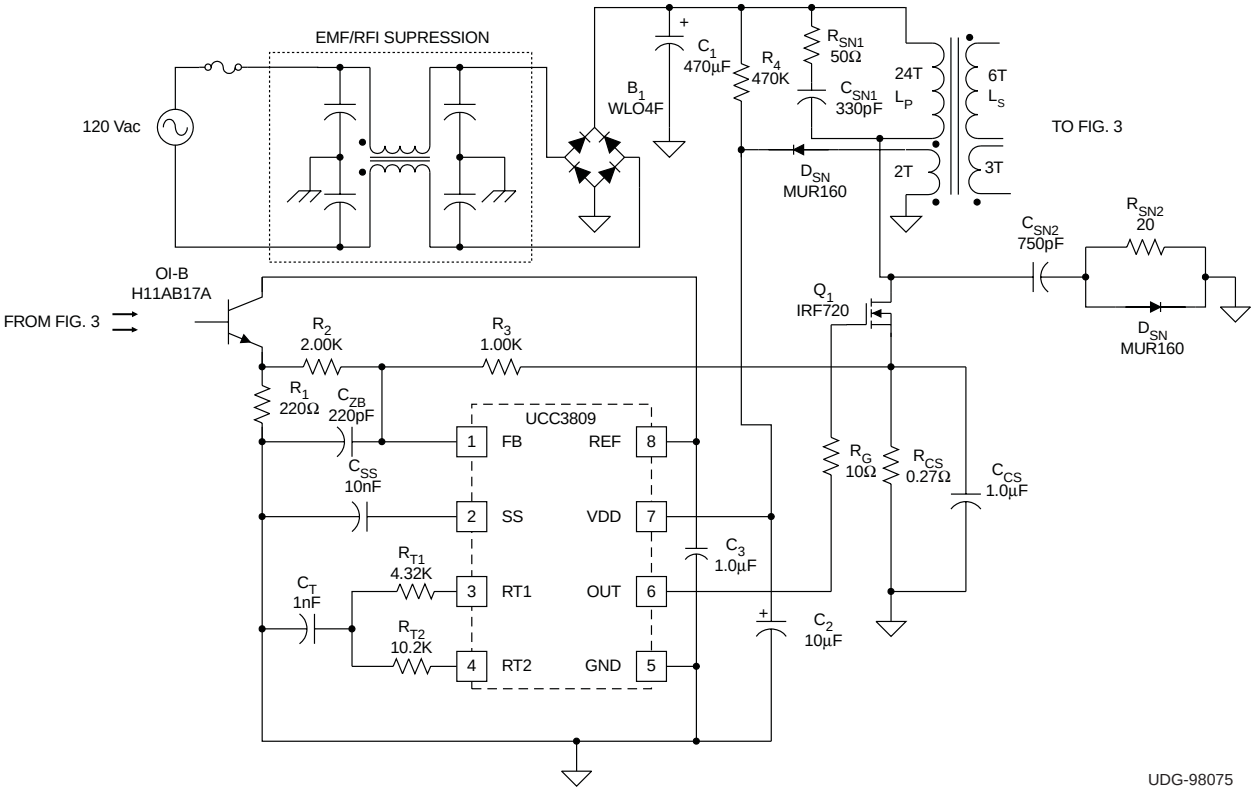

Figure 2. Primary side schematic.

If power is cycled, the charger will wake up in either the trickle or the bulk charge states, depending upon the battery voltage. If the battery voltage drops to 90% of V_{OC}, the charger will re-enter the bulk charge sate.

CIRCUIT DESCRIPTION

The circuit description presented is a discontinuous flyback with peak forward rectifiers on auxiliary windings to derive power for the control IC's. See Figs. 2 and 3.

The primary side schematic Fig. 2 shows a UCC3809 primary side controller being used as a peak current controller. The operating frequency and maximum switch on time are determined by components R_{T1}, R_{T2} and C_T. C_{SS} determines the soft start interval. R_{CS}, R_1, R_2, R_3, C_{ZB} and OI-B form the feedback and ramp circuit. C_3 is simply a bypass capacitor for the chip reference. R_4, D_1 and C_2 form the power supply for the UCC3809. R_{SN1}, C_{SN1}, R_{SN2}, C_{SN2} and D_{SN} are ring and dV/dt snubbers.

The secondary side schematic, Fig. 3, shows the UC3909 and its associated support components. D_4 and C_4 form the power supply circuit for the secondary side electronics. Q_2, Q_3, R_6 and R_7 disconnect the battery from the voltage divider string when the charger is not powered from the line. The resistor divider string R_{S1} through R_{S4} determines all voltage thresholds. R_{OVC1} and R_{OVC2} determine the current level for the transition from bulk charging to float charging.

The nature of the application demands that the UC3909 reside on the secondary side of the circuit with the battery. In order not to cause a current drain on the battery, the UC3909 will not be powered and the resistor divider string will be disconnected when the charger is not powered from the line. When line power is applied to the charger, several events take place. First, the startup resistor, R_4, supplies a small current to charge the supply capacitor, C_2, for the UCC3809. Second, when the voltage on this capacitor reaches the turn-on threshold for the UCC3809, the UCC3809 wakes up and begins charging the soft-start capacitor,

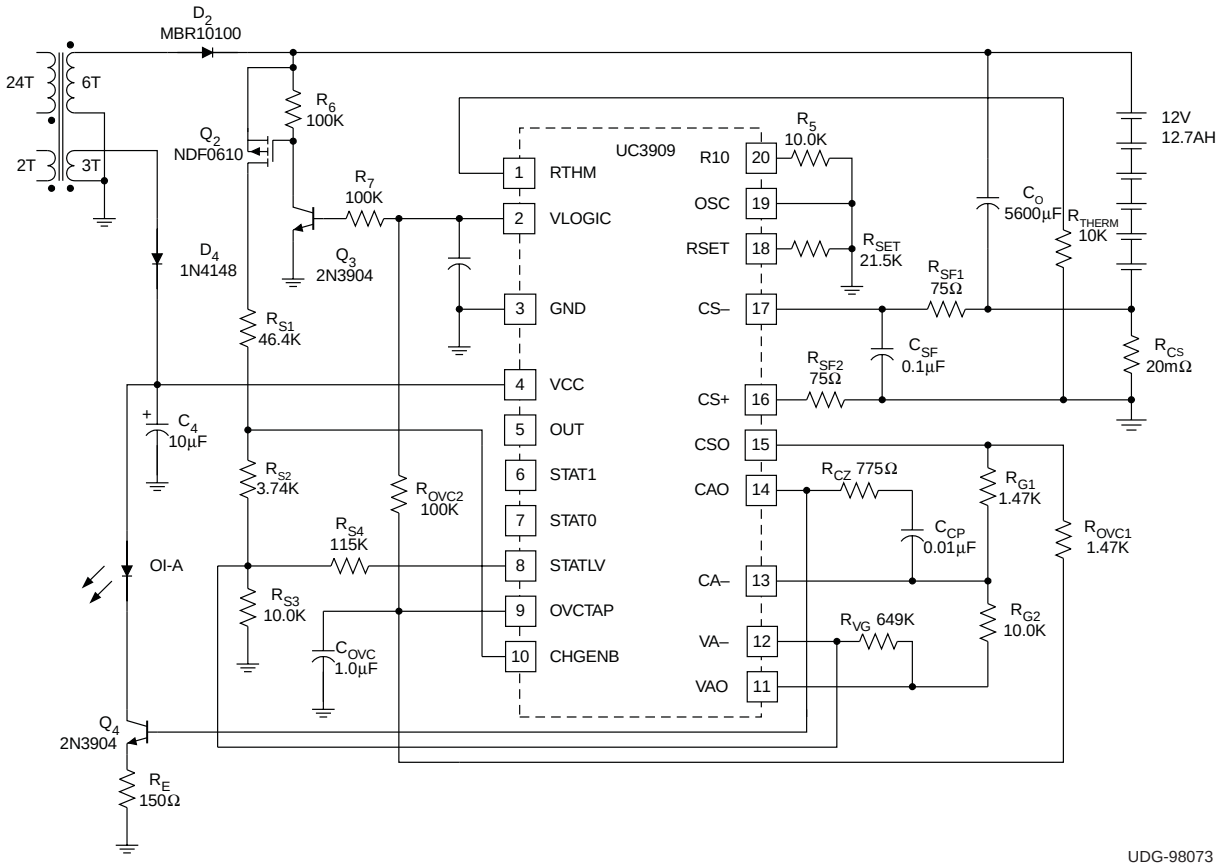

Figure 3. Secondary side schematic.

C_{SS}. Third, the UCC3809 issues no output pulses until the voltage on the soft-start capacitor reaches 0.7V. At this time, the UCC3809 will begin to issue output pulses. These pulses will be clamped to a width that is less than the maximum pulse width until the voltage on C_{SS} reaches 1.7V. Fourth, the bootstrap supplies for both the UCC3809 and the UC3909 come up and the charger begins charging the battery according to the charge algorithm described above and in the references.

The circuit is guaranteed to start (provided that the soft start capacitor is not chosen too large and cannot be charged to the 0.7V level before the voltage on C_4 falls to the UCC38098 UVLO threshold) since the feedback mechanism is commanding maximum pulse width until the opto-isolator is made to pass current into R_1. This cannot happen until the bootstrap supply for the UC3909 comes up. When the bootstrap supplies come up, the feedback circuit can then command shorter pulse widths from the UCC3809 and regulate the current and voltage output.

POWER STAGE DESIGN

Notation

Throughout this paper the following notation will be used.

Overbar: $\overline{V_{dc}}$ – a maximum value

Underbar: $\underline{I_{ls}}$ – a minimum value

Carat: $\hat{I}_{out}$ – an average value

Flyback Inductor Turns Ratio

The maximum turns ratio (N_p/N_s) is determined by the maximum voltage stress that is to be allowed on the power switching device, the maximum voltage that will be seen across the terminals of the secondary inductor winding and the amount of overshoot that will occur on the primary inductor when the power switch turns off. The peak power switch voltage is given by:

$$\overline{V_{ps}} = \overline{V_{dc}} + \overline{V_{ls}}\left(\frac{N_p}{N_s}\right) + V_{spike}$$

Where:

V_{ps} is the maximum power switch voltage (400V)

V_{dc} is the maximum dc voltage on the input filter capacitor C_1 (195V)

V_{ls} is the maximum voltage across the secondary inductor (15V + 1V for the diode)

N_p/N_s is the inductor turns ratio

V_{spike} is the leakage spike expected on switch turn-off (~ 30% of V_{dc})

With these values, taking a maximum N_p/N_s of 4 gives a maximum switch voltage of about 320 volts. This is well within safety margins for a 400 volt power switch.

Power Requirements

The maximum output power required from the flyback inductor is:

$$\overline{P_{out}} = \hat{I}_{out}\left(\overline{V_{batt}} + V_{diode}\right)$$

Where:

P_{out} is the output power of the flyback inductor

I_{out} is the maximum average output current (I_{bulk} or 4A)

V_{batt} is the maximum battery voltage (use 15V to allow for temperature correction)

V_{diode} is the voltage across the rectifier diode (use 1V to be conservative)

The input power to the inductor is the output plus an allowance for losses in the inductor and power switch. A conservative estimate is (based on 80% efficiency up to the output rectifier diode):

$$P_{IN} = \frac{P_{OUT}}{0.8}$$

In this application, the output power is 64W and the input power is 80W.

Inductor Values, Maximum "On" and "Reset" times, Peak Currents and Switching Frequency

The switching frequency was chosen to be 100 kHz as a compromise between switching losses and energy storage component size. To assure that the circuit remains discontinuous, the sum of the maximum on and reset times will only be allowed to be 85% of a switching period. The turns ratio, power requirements, discontinuity requirement and switching frequency define the values of the primary and secondary inductors, the peak currents and the on and reset times. From the following relationships, these values can be determined:

$$P_{in} = \frac{1}{2}\overline{I_p}^2 L_p F_s \qquad (1)$$

$$\overline{I_p} = \overline{\tau_{on}} \frac{V_{dc}}{L_p} \quad (2)$$

$$\overline{I_s} = \overline{I_p} \frac{N_p}{N_s} \quad (3)$$

$$L_p = \left(\frac{N_p}{N_s}\right)^2 L_s \quad (4)$$

$$\tau_{rst} = \frac{\overline{I_s} L_s}{V_{batt} + V_{diode}} \quad (5)$$

$$\overline{\tau_{on}} + \overline{\tau_{rst}} \le \frac{0.85}{F_s} \quad (6)$$

Where:

I_p is the primary inductor peak current.

L_p is the primary inductance.

I_s is the secondary inductor peak current.

L_s is the secondary inductance.

τ_{on} is the on time.

τ_{rst} is the reset time.

F_s is the switching frequency

After some algebraic manipulation, it is obvious that (I couldn't resist.):

$$\overline{\tau_{on}} = \left(1 + \frac{V_{dc} N_s}{N_p \left(V_{batt} + V_{diode}\right)}\right) \le \frac{0.85}{F_s} \quad (7)$$

From this, τ_{on} will be less than about 2.97µs and τ_{rst} will be less than about 6.03µs. Note that these numbers are "ideal out of the math" and will change somewhat when the real world primary and secondary inductances are known.

Again, after some manipulation of equations (1) and (2),

$$L_p = \frac{\left(\overline{\tau_{on}} V_{dc}\right)^2 F_s}{2 P_{in}} \quad (8)$$

L_p is then about 93µH. From (4), L_s is then about 5.8µH. From (2), the peak primary inductor current is 4.15A. From (3), the peak secondary inductor current is 16.6A.

RMS Inductor Currents

The RMS value of a periodic triangular pulse is:

$$I_{RMS} = I_p \sqrt{\frac{\tau}{3T}} \quad (9)$$

Where:

I_p is the peak value of the current

τ is the width of the base of the pulse

T is the period of the waveform

The RMS primary and secondary currents are then 1.3A and less than 7.44A respectively. At 500A/cm^2, the primary inductor should be wound with #24 or equivalent and the secondary inductor with #15 or equivalent.

Core Selection and Calculations

Inductance may be written as:

$$L = \frac{N \Phi}{I}$$

Where:

L is the inductance in Henries.

N is the number of turns of wire in the inductor.

Φ is the total flux linked by the N turns in Webers.

I is the current in the inductor in Amperes.

Since Φ is also equal to $A_e B$ where A_e is the effective area of the inductor core (m^2) and B is the flux density (Tesla):

$$\overline{B} = \frac{L \overline{I}}{N A_e} \quad (10)$$

From the core data for the Philips EFD30 core:

$$A_e = 69\, mm^2 = 6.9 \times 10^{-5}\, m^2 \quad (11)$$

If B is limited to 250mT (approaching roll-off in the B-H curve), N_p must be 23 or more turns. If N_p is set to 24, then N_s is 6.

These cores are ordered specifying the gap in terms of nH/Turn^2 (the A_L value). Obtaining an inductance of 93µH from 24 turns requires an A_L of 161nH. Since an A_L of 150nH is a standard value, this is what will be used. Note that since the core is gapped, the remanent flux density in the core will be approximately reduced by the ratio of the un-gapped A_L to the gapped A_L. The un-gapped A_L for the EFD30 is about 2100 in 3C85 material. The remanent flux density in a 3C85 un-gapped core is about 160mT at room temperature. Therefore the remanent flux density in the gapped core will be:

$$Brem_{gapped} \approx \frac{A_{L\,gapped}}{A_{L\,un-gapped}} Brem_{un-gapped} \quad (12)$$

$$= \frac{150}{2100} 160\,mT = 11.4\,mT$$

Since the saturation flux density of 3C85 material is well above 250mT, a flux swing of 250mT will not saturate the core with a remanent flux density of only 11.4mT.

Windings

The inductor in the schematic shows 4 separate windings. The primary inductor winding is wound from #24 magnet wire. The 2 turn winding that supplies the bootstrap power to the primary side of the circuit can be of practically any small gauge wire as the current level is low. In the prototype inductor this winding was wound with #30 wire simply because it was readily available. The primary side windings were placed side by side against the bobbin with a layer of kapton tape, 3M #5413, to isolate the high voltage primary inductor winding from the low voltage bootstrap winding.

The secondary side of the inductor shows two windings, the secondary inductor winding and a bootstrap winding for the secondary side electronics. The secondary inductor cannot be wound from (at least not easily and maintain creepage distances) from bundles of discrete wires or from litz and still fit the winding in the window of the EFD30 bobbin. Therefore, the secondary inductor was wound from foil. A 0.5 inch wide by 0.007 inch thick strip of copper foil was used. This gives a current density of about 330A/cm^2 in the winding. This low value of current density was used to help offset losses caused by the high number of layers in the winding. The secondary bootstrap winding was wound on top of the secondary inductor.

To satisfy insulation requirements, three layers of kapton tape were used between the primary side and secondary side windings.

The bootstrap windings in Figs. 2 and 3 are connected so that they will supply current when the main power switch is on, not off, as the secondary inductor will. This means that the voltage applied to the primary and secondary electronics will be equal to:

$$V_{boot} = \frac{N_{boot}}{N_p} V_{dc} - V_{diode} \quad (13)$$

For the primary side, the bootstrap voltage will be between 10.1 and 15.5 volts. Likewise, the secondary bootstrap voltage will be between 15.5 and 23.75 volts.

The prototype charger was built using two different inductors using different winding arrangements. One inductor had the primary winding on one layer, and the other sandwiched the secondary between a primary split between two layers. While both arrangements produce satisfactory results, the split primary does have lower leakage inductance and places less stress on the power switch at turn-off. In the prototype, the single layer primary produced leakage spikes that were high enough to make a 400V Vds MOSFET a marginal choice. If the single layer primary is used, a 500V Vds MOSFET would be a better choice for the power switch.

PRIMARY SIDE COMPONENT VALUES

Current Sensing and Feedback

To be certain that the flyback inductor never saturates, some resistor values on the primary side can be adjusted to limit the primary current to a level on the verge of saturation. If this level is picked to be 300mT (from Philips data for 3C85 material), the peak current (I_P) in the primary must be less than about 5.3A. To limit the current in L_P to 5.3A, the voltage at pin FB of the UCC3809 must be 1V when the current is 5.3A. When the feedback current through the opto-isolator is 0, the following condition must be satisfied:

$$5.3 R_{CS} \frac{R_2 + R_1}{R_3 + R_2 + R_1} = 1.0 \quad (14)$$

In addition, to be certain that the secondary can command the minimum attainable pulse width, a voltage of 3.0V across R_1 should result in 1V at the UCC3809 FB pin with no current in the current sense resistor (R_{CS}). The value of R_{CS} is so small that it will be ignored in this computation. This gives:

$$3.0 \frac{R_3}{R_3 + R_2} = 1.0 \quad (15)$$

If R_3 is arbitrarily chosen as 1k, R_2 must be 2k. R_1 must be chosen with some consideration to the opto-isolator. The H11A817A has a current transfer ratio of 80% to 160% and is fairly linear over a diode current range of 2mA to 30mA. Picking R_1 to be 220Ω places the operating point of the opto-

isolator into its linear range over most of the operating range of the charger. R_{CS} is then 0.27Ω. The power dissipation in R_{CS} is just over 450mW at full load, so a 1W resistor is recommended here. The UCC3809 needs a capacitor at its FB pin to keep the inevitable current spikes through L_P from causing early pulse termination. Capacitor C_{ZB} serves this purpose in this application. A value of 220pF gives a time constant of about 0.15µs. This will catch the leading current spike noise pulses but still allow adequate current ramp sensing at 100kHz. C_{CS}, across the current sense resistor, also helps to attenuate the large leading current spikes caused by the forward peak rectifiers in the bootstrap power circuits. Some caution must be used when picking the values for C_{ZB} and C_{CS}. The larger the values, the more lag time that there will be when a fault condition is present at the output. On the other hand, picking the values too small can lead to premature pulse termination and erratic charger behavior. Also, the larger the value of C_{ZB}, the longer the minimum achievable pulse width will be.

Timing and Soft-start

The UCC3809 has fully programmable maximum on and minimum off times. The components RT1, RT2 and CT determine these times. Since τ_{on} is at most 2.97µs and the total period, T is 10µs the off time, τ_{off} will be 7.03µs. From the UCC3809 datasheet:

$$\tau_{on} = 0.69 C_T R_{T1} \text{ and } \tau_{off} = 0.69 C_T R_{T2} \quad (16)$$

Picking C_T to be 1nF, R_{T1} is 4.32K and R_{T2} is 10.2K.

The softstart time is controlled by C_{SS}. C_{SS} is charged by a 6µA current source. As the SS pin on the UCC3809 goes from 0V to 0.7V, the output of the UCC3809 is inhibited. As the voltage goes from 0.7V to 1.7V, the duty cycle of the output is allowed to increase from 0 to its maximum value. A 47nF value for C_{SS} gives a soft start time of about 7.5ms. The bulk supply capacitor for the UCC3809 must be able to supply energy to the primary side circuitry while the SS pin makes the transition from 0V to 0.7V.

Other Components

R_4 provides the startup current for the UCC3809. This current must be at least 100µA at minimum line. A value of 470K will give 240µA at minimum line input voltage and maximum startup voltage for the UCC3809. C_1, the bulk filter capacitor, was chosen more for its ripple current handling capability and low ESR more than its capacitance. Capacitors C_2 and C_3 are filter caps for the UCC3809's power supply and reference. R_G is a low value resistor intended to prevent gate oscillations in the power MOSFET. The block labeled EMI/RFI suppression in Fig. 2 is a typical suppression network. It was not implemented in the prototype but is shown for completeness.

SETTING CURRENT AND VOLTAGE LEVELS FOR THE UC3909

Charge Current Sense Resistor

The current sense amplifier in the UC3909 does not have the bandwidth to handle a 100kHz flyback current waveform. To get around this limitation, the signal from the current sense resistor was filtered with a simple R-C network (R_{SF1} and C_{SF}). The –3dB frequency of this filter was chosen to be 20kHz to have minimal effect on the feedback loop. Another resistor, $R_{SF2,}$ was added to preserve the 2.3V bias point of the current sense amplifier. When adding a filter like this to an amplifier that has gain and biasing resistors already implemented in silicon, be careful not to significantly change the nominal gain of the amplifier. The reason for this is that the silicon resistors are closely ratio matched to provide an accurate gain, but vary significantly in absolute value. Larger values of filtering resistors introduce larger potential differences in the gain of the sense amplifier from one chip to the next and over temperature for any given chip.

The charge current sense resistor (R_S) should be chosen so that its power dissipation is within acceptable limits and the voltage presented to the current sense amplifier does not cause the amplifier to saturate. The current sense amplifier in the UC3909 is a differential amplifier with a fixed gain of 5, biased to a level of 2.3V. To prevent saturation, the maximum voltage across CA– and CA+ should be no more than 400mV. In this application, power dissipation was the determining factor for selection of R_{CS}. R_{CS} was chosen as 20mΩ and dissipates about 1.1W at maximum output current.

Bulk Current Setting

The bulk current is set by the values of R_{G1} and R_{G2}. When the charger is in the bulk charge state, the voltage error amplifier will be out of compliance and its output (VAO) will be at its positive rail (or nearly so) of 5V. The relevant circuit is shown in Fig. 4.

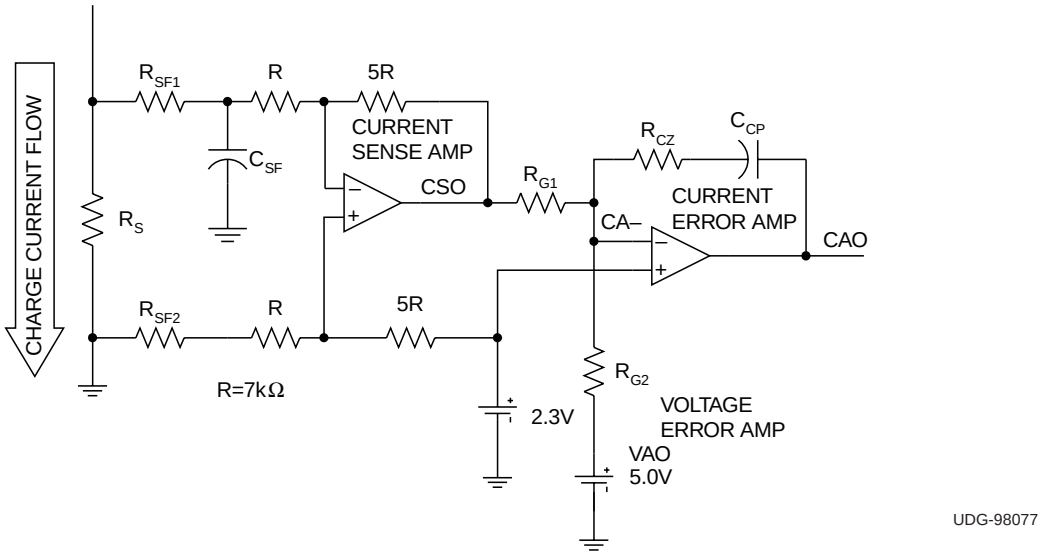

Figure 4. Bulk current setting.

For the current error amp to be in compliance, the voltage at pin CA– must be 2.3V. The desired bulk charging current was 4.0A. The average voltage across R_S is then:

$$V_{RS} = 4.0A \times 0.02\Omega = 80mV \quad (17)$$

The voltage at the output of the current sense amplifier is then:

$$V_{CSO} = 2.3 - 5V_{RS} = 1.9V \quad (18)$$

Summing currents at the CA– pin:

$$\frac{5 - 2.3}{R_{G2}} = \frac{4.0A \times 0.02\Omega \times 5}{R_{G1}} \quad (19)$$

If R_{G2} is set to a value of 10.0k, then R_{G1} is 1.47k.

Trickle Current Setting

When the UC3909 is in the trickle charge state, the Voltage error amplifier output, VAO, goes into a high impedance state, and the trickle control current is directed to the CA– pin of the UC3909. The trickle control current is 5% of the current flowing out of the RSET pin on the UC3909. The trickle control current can only flow through R_{G1} since VAO is high impedance. Therefore, the trickle current will be:

$$I_{TRICKLE} = \frac{I_{TRICKLECONTROL} R_{G1}}{5R_S} \quad (20)$$

Recall that the trickle current was to be set to 80mA. This current level will produce an average voltage of 2.292V at the CSO pin. The trickle control current through R_{G1} is then 5.4µA. The current out of the RSET pin is then 108µA. The voltage on the RSET pin is 2.3V, so the value of R_{SET} for 80mA trickle charge current is 21.5k.

Overcharge Taper Current

The overcharge taper current (I_{OCT}) is the current level the UC3909 looks for to make its transition from overcharge to float charge. The transition from overcharge to float charge takes place when the voltage on the OVCTAP pin rises above 2.3V. OVCTAP is the tap of a voltage divider from the VLOGIC to CSO pins, with R_{OVC1} and R_{OVC2} setting the divider ratio. The transition between charging modes takes place when:

$$\frac{5 - 2.3}{R_{OVC1}} = \frac{5I_{OCT} R_S}{R_{OVC2}} \quad (21)$$

If R_{OVC2} is picked to be 100K, R_{OCV1} is 1.47k since I_{OCT} is 400mA.

Float Voltage Level

The float voltage is the voltage that the UC3909 will apply to the battery to maintain the battery's charge level after the overcharge period has ended. The float voltage (as well as the overcharge voltage and bulk charge threshold voltages) is determined by the resistors R_{S1}, R_{S2}, R_{S3} and R_{S4}. In the float state, the STATLV transistor (internal to the UC3909; see data sheet) is off. The float voltage is the voltage across the battery that will produce 2.3V at the VA– pin. Note that for all of the voltage thresholds, the reference voltage is adjusted by –3.9mV/°C while the reference for the

current thresholds is constant over temperature. The float voltage is then:

$$V_{FLOAT} = 2.3\frac{R_{S1}+R_{S2}+R_{S3}}{R_{S3}} \quad (22)$$

If R_{S3} is set to 10.0k, and V_{FLOAT} to 13.8V, the sum of R_{S1} and R_{S2} is 49.99k. The overcharge voltage level (V_{OC}) is the maximum voltage that will be applied to the battery when the charger is in the overcharge state. In this state, the STATLV transistor is on, and V_{OC} is the voltage that produces 2.3V at the VA– pin. V_{OC} is then:

$$V_{OC} = 2.3\frac{R_{S1}+R_{S2}+R_{S3}||R_{S4}}{R_{S3}||R_{S4}} \quad (23)$$

Knowing the sum of R_{S1} and R_{S2} is 49.99k, R_{S3} is 10.0k and V_{OC} is 14.8V, R_{S4} is found to be 115k. The bulk charge state is entered when the UC3909 senses that the voltage on its CHGENB pin goes above 2.3V. In the trickle and bulk charge states, the STATLV transistor is on, so the value of V_{CHENB} is then:

$$V_{CHGENB} = 2.3\frac{R_{S1}+R_{S2}+R_{S3}||R_{S4}}{R_{S2}+R_{S3}||R_{S4}} \quad (24)$$

Since the sum of R_{S1} and R_{S2}, and the values of R_{S3} and R_{S4}, are known, R_{S2} is 3.74k. From this, R_{S1} must be 46.4k.

Optocoupler LED Current Limit

R_E must be small enough that sufficient current can be put through the LED of the optocoupler to cause the collector on the optocoupler output to go to 3V. The resistance to ground at the collector of the optocoupler is about 205Ω. This means that the emitter current in the optocoupler must be at least 14.6mA. If the optocoupler is at the low end of the current transfer ratio distribution (80%, for the H11A817A), then the LED current must be at least 18.3mA. Allowing 0.7V for the b–e voltage on Q4, and 1.5V of headroom to help prevent saturation, the emitter voltage of Q4 will be 2.8V (5.0 – 0.7 – 1.5 = 2.8) maximum at 18.3mA. R_E is then 150Ω.

CURRENT CONTROL LOOP

There are several “components” in the current control feedback path. Fig. 5 details the feedback path. Component in this context refers to a piece of the overall transfer function, such as a resistor, which transforms a current into a voltage.

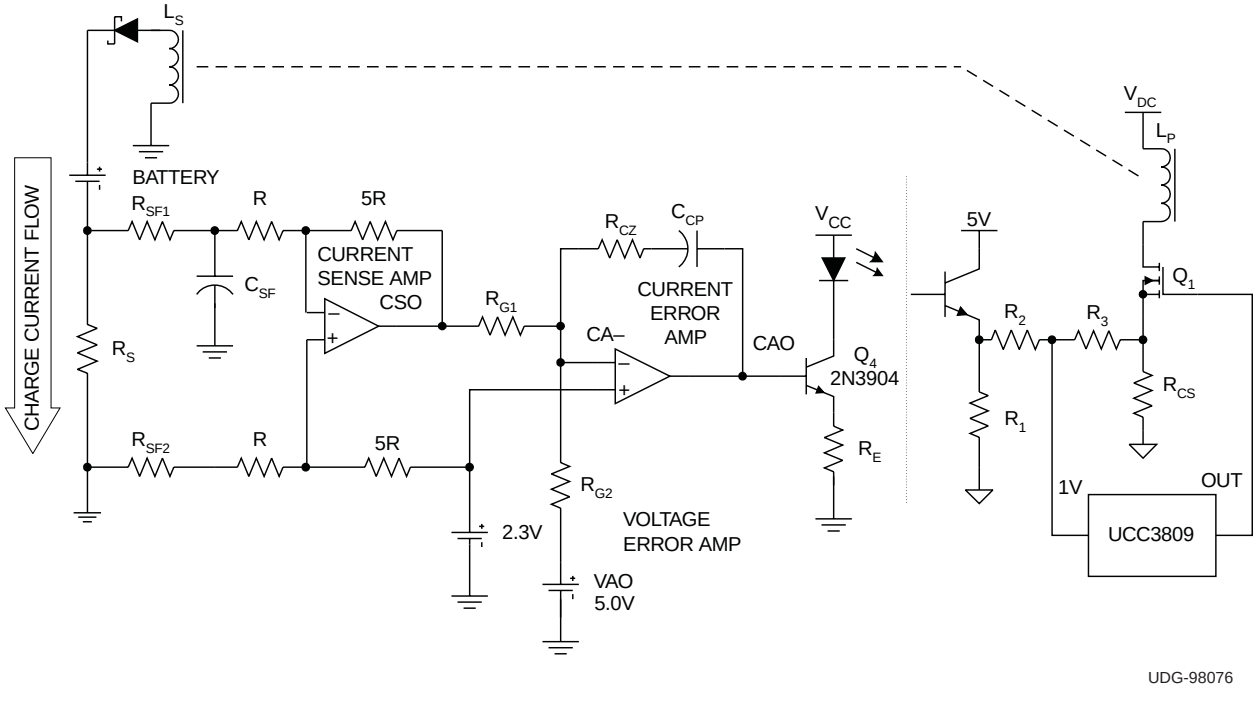

Figure 5. Current control loop components.

The individual components of the feedback path are:

1. Q_4 and R_E which converts V_{CAO} into I_{LED} in the optocoupler.
2. R_1, R_2, R_3, R_{CS} and the optocoupler, which convert I_{LED} into a peak primary inductor current, I_{LP}.
3. The coupled inductor which, along with the output voltage, converts I_{LP} into an average current through R_S.
4. R_S, R_{SF1} and C_{SF}, which converts the average output current into a voltage.
5. The current sense amplifier, which amplifies the voltage across C_{SF}.
6. The current error amplifier, which provides gain and phase compensation for the feedback loop.

These elements will be examined one by one to determine the overall loop characteristics.

Q_4 and R_E

Q_4 is configured as an emitter follower. For all practical purposes, the collector current and the emitter current are equal, and a one volt change in base voltage will produce a one volt change in emitter voltage. Since the emitter voltage and the emitter resistor determine the emitter current and hence the collector current, the gain of this stage is:

$$G_1 = \frac{1}{R_E} = \frac{1}{150}\, A/V \tag{25}$$

R_1, R_2, R_3, R_{CS} and the Optocoupler

The optocoupler may have a current gain up to 160%. The current in the primary inductor is the current that results in 1V at the junction of resistors R_2 and R_3. Using the principle of superposition:

$$\left(I_C \bullet \left[R1 \parallel (R2+R3)\right] \bullet \frac{R_3}{R_2+R_3}\right) + \left(I_{L_P} \bullet R_{CS} \bullet \frac{R_2}{R_2+R_3}\right) = 1.0 \tag{26}$$

This simplifies to:

$$I_{L_P} = \frac{R_2+R_3}{R_{CS}R_2} - I_C \frac{R_1(R_2+R_3)}{R_1+R_2+R_3} \bullet \frac{R_3}{R_{CS}R_2} \tag{27}$$

The gain of this stage is the derivative of I_{LP} with respect to IC multiplied by the optocoupler gain or:

$$G_2 = -\frac{R_1(R_2+R_3)}{R_1+R_2+R_3} \bullet \frac{R_3}{R_{CS}R_2} \bullet 1.6 = -607\, A/A \tag{28}$$

Coupled Inductor and Output Voltage

The peak current in the secondary inductor is N_P/N_S times the peak current in the primary inductor. The secondary current waveform is triangular and has the average value, see Fig. 6:

$$I_{L_S AVG} = \frac{\tau_{rst}}{2T} I_{L_S PEAK} \tag{29}$$

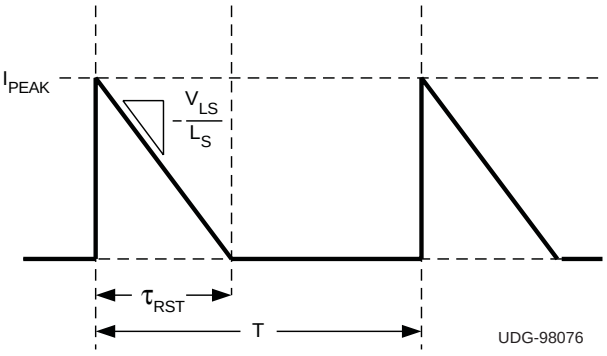

Figure 6. Secondary current waveform.

But since:

$$I_{L_S PEAK} = \frac{N_p}{N_s} I_{L_P PEAK} \tag{30}$$

and

$$\tau_{rst} = I_{L_S} \frac{V_{L_S}}{L_S} \tag{31}$$

The average output current is then:

$$I_{L_S AVG} = \frac{1}{2T}\left(I_{L_S PEAK}\right)^2 \frac{L_S}{V_{L_S}} = \frac{1}{2T}\left(\frac{N_p}{N_s}\right)^2 \left(I_{L_P PEAK}\right)^2 \frac{L_S}{V_{L_S}} \tag{32}$$

The gain of the stage is the derivative of the average secondary current with respect to the peak primary current. Differentiating the above yields:

$$G_3 = \frac{1}{T}\left(\frac{N_p}{N_s}\right)^2 \frac{L_S}{V_{L_S}} I_{L_P PEAK}\ A/A \tag{33}$$

From this, it is seen that the gain depends upon what the load voltage and current are. This differentiation yields the gain of the coupled inductor because from a small signal standpoint, the battery voltage (and hence V_{LS}), switching frequency, turns ratio and secondary inductance are constant. The maximum value of the gain is the only value of interest since this will be the point at which the phase margin will be the lowest (in this circuit). If the battery voltage is 10.5V and the Schottky voltage is 0.5V, the I_{LP} that produces an average I_{LS} of 4.0A is 3.08A. This is the point where the current gain is the highest, at 2.6 A/A.

Current Sense Resistor and Filter

The transfer function of the sense resistor and filter network is:

$$G_4 = \frac{R_S}{1 + sR_{SF1}C_{SF}} = \frac{0.02}{1 + 7.5 \times 10^{-6} s} V/A \quad (34)$$

Current Sense Amplifier

The output of the current sense amplifier is:

$$V_{CSO} = 2.3 - 5V_{CSF} \quad (35)$$

The gain of this stage is the derivative of V_{CSO} with respect to V_{RCS}. The gain G_5, is –5 V/V.

Total Current Loop Gain

The open loop gain of the current loop (without the current error amplifier) is the product of all of the G terms described above. G_{COL} in this case is 1.05 or 0.44dB, with a single pole at 20kHz.

Current Loop Compensation

Fig. 7 shows the uncompensated and compensated current loop gain characteristics. The compensation goal here is to provide unconditional stability in the loop and to roll the closed loop frequency response off at 1/10th of the switching frequency. To roll the closed loop response off at 10kHz, the open loop crossover frequency must be 10kHz. To do this requires that the current error amplifier have –0.44dB gain at crossover. Although not strictly necessary, a zero will be inserted in the current error amplifier response at 20 kHz to cancel the pole in the current sense filter. The transfer function of the current error amplifier is:

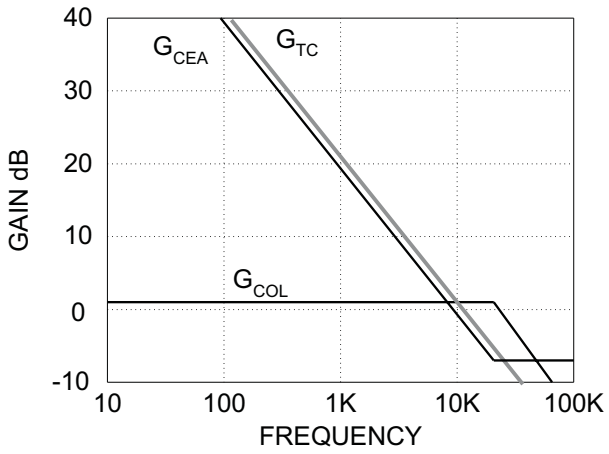

Figure 7. Current loop gain.

$$G(s) = \frac{1 + sR_{CZ}C_{CP}}{sR_{G1}C_{CP}} = G_{CEA} \quad (36)$$

The R in this integrator has already been determined to be 1.47k (R_{G1}). This leaves the capacitor to set the low frequency gain characteristic. For the gain to be –0.44dB at 10kHz, the capacitor value must be around 10nF. The phase lag through the power stage is small in the frequency range of interest and the origin pole of the current error amplifier contributes only 90° to the loop. The phase lag of the current sense filter is offset by the zero in the current error amplifier response. This means that the loop is unconditionally stable with near 90° of phase margin.

VOLTAGE CONTROL LOOP

The voltage control loop is shown in Fig. 8. The nature of this circuit is such that in the trickle and bulk charge states, the voltage control loop is open. At some point during the overcharge state the voltage loop closes or comes into compliance. For the remainder of the overcharge state and the float charge state, the voltage loop (made up of the resistor divider string R_{S1} through R_{S4}, the voltage error amp and R_{VG} is an outer control loop around the current loop.

The open loop response of the voltage loop is equal to the closed loop current loop response multiplied by the output impedance and the gain of the elements of the voltage loop. In other words:

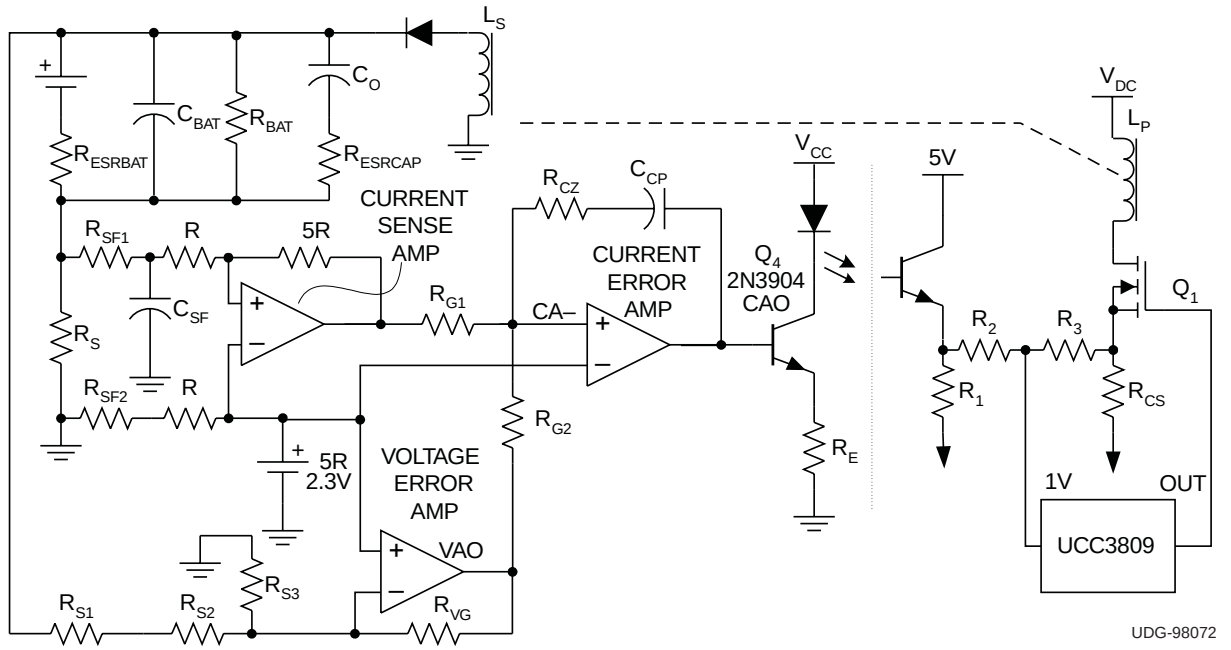

Figure 8. Voltage control loop.

$$G_{VOL} = G_{CCL} Z_L G_{DIV} \frac{R_{G1}}{R_{G2}} G_{VEA} \quad (37)$$

Where:

G_{VOL} is the open loop voltage transfer function

G_{CCL} is the closed loop current transfer function

Z_L is the load impedance

G_{DIV} is the gain of the battery voltage divider looked at from the VA- pin

G_{VEA} is the transfer function of the voltage error amplifier.

The R_{G1}/R_{G2} term is simply the summing ratio of the current sense amplifier output and the voltage error amplifier output. The closed loop current response (change in output current for a given change in current sense amplifier output) is given by:

$$G_{CCL} = \left(\frac{1}{G_4 G_5}\right)\left(\frac{G_{CEA} G_5 G_4 G_3 G_2 G_1}{G_{CEA} G_5 G_4 G_3 G_2 G_1 + 1}\right) \approx \frac{7.143 \times 10^5}{s + 7.143 \times 10^4} \quad (38)$$

The load impedance is difficult to characterize and is greatly dependent upon the battery being used. The battery is a complex device to model and will exhibit parametric shifts depending upon variables like temperature, charge state, age and history. According to the battery manufacturer, R_{ESRBAT}, C_{BATT} and R_{BATT} vary considerably depending upon what the condition of the battery is. To insure that the voltage loop will remain stable, it was assumed that the equivalent load of the battery, filter capacitor and anything else that may be connected to the charger has an extremely low frequency pole. The frequency of this pole is assumed to be much less than the crossover frequency of the voltage loop. This will contribute 90° to the phase lag of G_{VOL} at whatever the crossover frequency turns out to be.

The divider gain (G_{DIV}), is equal to:

$$G_{DIV} = \frac{R_{S3}}{R_{S1} + R_{S2} + R_{S3}} = 0.166 \quad (39)$$

The open loop voltage transfer function for this application is then:

$$G_{VOL} = \frac{1.743 \times 10^4}{7.143 \times 10^4 + s} Z_L G_{VEA} \quad (40)$$

Ignoring the Z_L and G_{VEA} terms, the phase shift of this circuit is 45° at the current control loop crossover frequency (10kHz), and about 22.5° at 3.2kHz. The voltage error amplifier was chosen to be a straight gain amplifier with no complex feedback in order to avoid the additional phase shift that comes with introducing more poles into the system. With the phase shift of the load taken to be 90°, the voltage loop should have a crossover frequency below 3.2kHz to maintain good phase margin. At 3.2kHz, the open loop gain of the voltage control loop is:

$$\left| G_{VOL} \right|_{f=3200} = \left| Z_L \, G_{VEA} \right|_{f=3200} - 12.6\,dB \quad (41)$$

Conversations with the battery manufacturer suggested that charging impedance could range from 250mΩ to 10mΩ (almost strictly capacitive) at 3.2kHz. The filter capacitor in the charger is 5600μF with an ESR of less than 13mΩ. This results in a total Z_L of 8mΩ to 15mΩ. The gain of the voltage error amplifier must be less than 49dB in order to insure that the control loop will crossover at less than 3.2kHz. The gain of the amplifier was set at 36dB. Testing on the prototype charger showed no signs of instability in the voltage control loop. While it is not known what the exact impedance on the battery is, the above approach resulted in a robust and stable charger.

OTHER ISSUES

Line Isolation

The transformer design presented here will provide at least $3750V_{RMS}$ of isolation and 8mm of creepage from the primary to the secondary. This is adequate for some applications, but not for others. Check with the regulatory standards for the type of product being built to find out if this isolation level is adequate. If more isolation is required, a core with a larger winding window will have to be used since this design fills the window of the EFD30 almost completely.

Higher power

This paper presents a general scheme for controlling a primary side PWM from an isolated UC3909. The particular PWM used here is a single output device. However, for higher power requirements, 200W, 500W, 1kW and beyond, there is no reason that a higher performance single output PWM or dual output PWM could not be used with suitable design adaptations. At much higher current levels, it may be advantageous to use a small value shunt for current sensing along with an additional amplifier to boost the signal level. If the topology is changed to a forward buck type, the current sense amplifier in the UC3909 will be useful at higher switching frequencies without the aid of an input averaging filter.

Disconnection of Load and Minimum Output Power

If it is possible that the load (battery in this case) could be disconnected from the charger while the charger is powered from the ac mains, the output voltage will run away. A means of controlling output voltage must be supplied if this is the case. The reason for this is that even though the UC3909 would be commanding zero pulse width, the UCC3809 will give a minimum pulse width based upon the values of components R_{CS}, C_{CS}, R_3, R_2, and C_{ZB}. The minimum pulse width arises from the fact that the UCC3809 discharges C_{ZB} through an internal FET when the oscillator starts its down ramp. The internal FET is turned off when the oscillator starts its up ramp and sends an output pulse. Since the output pulse will only terminate when the voltage at FB on the UCC3809 reaches 1V (or when the oscillator again starts its down ramp), the minimum pulse width is determined by the time that it takes to charge C_{ZB} to 1V.

A means of getting a handle on the minimum pulse width can be seen by referring to Fig. 9. When minimum pulse width is being commanded by the UC3909, it is assumed that the voltage across the current sense resistor will not have a significant impact on the time necessary to charge C_{ZB} to 1V. The only source available is the current through the opto-isolator. The voltage V1 is the current out of the opto-isolator multiplied by the equivalent resistance seen at the emitter of the opto-isolator.

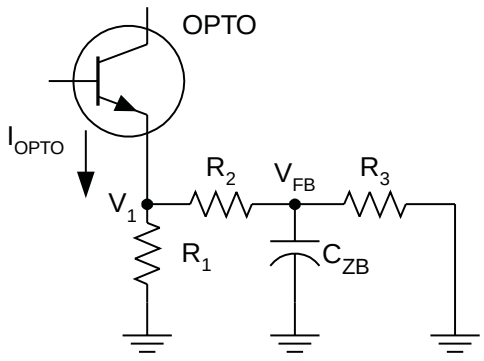

Figure 9. Minimum pulse width determination.

When this voltage is known, the minimum pulse width is approximately:

$$\tau_{on} = -\ln\left(1 - \frac{R_2 + R_3}{V_1 \bullet R_3}\right)\frac{C_{ZB}\, R_2\, R_3}{R_2 + R_3} \qquad (42)$$

This application circuit was not designed to operate with a disconnected load. Enough load must be applied to dissipate the minimum power output that the circuit will supply at the highest input line voltage (a DC rail of 195V). The particular battery used here was an adequate load to dissipate this power. Minimum pulse width can be reduced by using a smaller C_{ZB}, at the expense of noise immunity or by increasing the ratio of R_3 to R_2. This last solution will affect the feedback loops somewhat.

As a means of controlling the output voltage, a 5W 15V zener diode at the output would work nicely. The STAT0 and STAT1 pins could even be decoded to switch the diode into the circuit only when the charger goes into float mode. This would guarantee that the over charge voltage would not cause a low threshold diode to start conducting and overheat. Alternatively, a dummy load resistor could be placed across the charger output that would dissipate the minimum output power at the minimum temperature compensated float voltage. It will almost certainly be necessary to use the STAT0 and STAT1 pins to switch the resistor into the circuit only when the UC3909 is in the float mode. Otherwise, the dummy load would be applied to the battery and discharge it when the charger is not powered from the line.

Connection of Loads That Bypass the Current Sense Resistor

This technique can be useful if properly applied. The charger current sense loop will adjust the output to a point that will supply the battery with the selected charging current, regardless of what current the load requires. There are some caveats here though. First, the charger power stage must be able to handle the bulk charging current of the battery as well as the maximum current that the load will draw. Second, the load will add a pole into the current control loop, which can complicate the design of the feedback, especially in the voltage control loop. Third, and probably most importantly, the inherent current limiting effect of the current control loop will not be active if a fault occurs at the load. Some other means of over-current protection must be supplied.

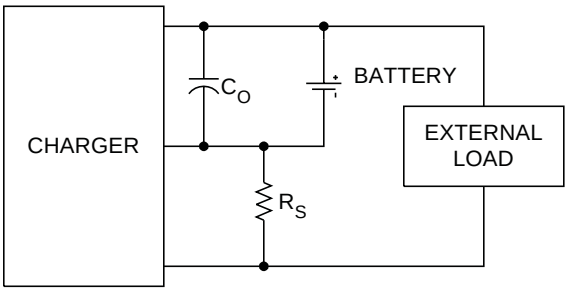

Figure 10. Alternate external load connection.

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