DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F9831

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9831 is an 8-bit single-chip microcontroller (for LCD driving) of the 78K/0S series.

The μPD78F9831 is produced by replacing the internal ROM of the μPD789830 with larger flash memory.

Flash memory can be written or erased electrically without having to remove it from board. Therefore, the μPD78F9831 is best suited for prototypes in system development, low-volume production, or systems likely to be upgraded frequently.

The functions of the μPD78F9831 are described in the following user's manuals. Refer to these manuals when designing a system based on the μPD78F9831.

μPD789830 Subseries User's Manual	**:**	**U13679E**
78K/0S Series User's Manual, Instruction	**:**	**U11047E**

FEATURES

- Internal flash memory: 48 Kbytes
- RAM sizes
  - Internal RAM : 2 Kbytes
  - ★ LCD data RAM: 40 × 16 bits
- ★ Variable minimum instruction execution time: From high-speed (0.4 μs: With the main system clock running at 5.0 MHz) to very low-speed (122 μs: With the subsystem clock running at 32.768 kHz)
- 38 I/O ports
- Serial interface (UART00)
- LCD controller/driver
  - Up to 40 segment signal outputs
  - Up to 16 common signal outputs
  - 1/5 bias mode
- Four timers:
  - 16-bit timer
  - 8-bit timer
  - Watch timer
  - Watchdog timer
- Pulse output: Clock output/buzzer output
- Built-in key return signal detection circuit
- Power supply voltage: V_{DD} = 2.7 to 5.5 V

APPLICATIONS

Card readers

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Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD78F9831GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)

★ 78K/0S SERIES DEVELOPMENT

The 78K/0S series products are shown below. The subseries names are indicated in frames.

Products in mass production — Products under development

Y Subseries products support SMB.

78K/0S Series

Small-scale package, general-purpose applications

44-pin	μPD789046	μPD789074 with added subsystem clock
42/44-pin	μPD789026	μPD789014 with enhanced timer and increased ROM, RAM capacity
30-pin	μPD789088	μPD789074 with enhanced timer and increased ROM, RAM capacity
30-pin	μPD789074	μPD789026 with enhanced timer
28-pin	μPD789014	On-chip UART and capable of low voltage (1.8 V) operation

Small-scale package, general-purpose applications and A/D converter

44-pin	μPD789177	μPD789177Y	μPD789167 with enhanced 10-bit A/D converter
44-pin	μPD789167	μPD789167Y	μPD789104A with enhanced timer
30-pin	μPD789156		μPD789146 with enhanced 10-bit A/D converter
30-pin	μPD789146		μPD789104A with added EEPROM™
30-pin	μPD789134A		μPD789124A with enhanced 10-bit A/D converter
30-pin	μPD789124A		RC oscillation version of the μPD789104A
30-pin	μPD789114A		μPD789104A with enhanced 10-bit A/D converter
30-pin	μPD789104A		μPD789026 with added 8-bit A/D converter and multiplier

Inverter control

44-pin	μPD789842	On-chip inverter controller and UART

VFD drive

52-pin	μPD789871	Total display outputs: 25

LCD drive

80-pin	μPD789488	SIO, 10-bit A/D converter, and on-chip voltage booster type LCD (28 × 4)
80-pin	μPD789477	SIO, 8-bit A/D converter, and resistance division type LCD (28 × 4)
80-pin	μPD789417A	μPD789407A with enhanced 10-bit A/D converter
80-pin	μPD789407A	SIO, 8-bit A/D converter, and resistance division type LCD (28 × 4)
64-pin	μPD789456	μPD789446 with enhanced 10-bit A/D converter
64-pin	μPD789446	SIO, 8-bit A/D converter, and on-chip voltage booster type LCD (15 × 4)
64-pin	μPD789436	μPD789426 with enhanced 10-bit A/D converter
64-pin	μPD789426	SIO, 8-bit A/D converter, and on-chip voltage booster type LCD (5 × 4)
64-pin	μPD789316	RC oscillation version of the μPD789306
64-pin	μPD789306	SIO and on-chip voltage booster type LCD (24 × 4)
52-pin	μPD789467	8-bit A/D converter and on-chip voltage booster type LCD
52-pin	μPD789327	SIO and on-chip resistance division type LCD

Dot LCD drive

144-pin	μPD789835	Segment/common outputs: 96
88-pin	μPD789830	Segments: 40, commons: 16

ASSP

64-pin	μPD789803	For PC keyboard, on-chip USB HUB function
44-pin	μPD789800	For PC keyboard, on-chip USB function
44-pin	μPD789840	For keypad, on-chip POC
20-pin	μPD789861	RC oscillation version of the μPD789860
20-pin	μPD789860	For keyless entry, on-chip POC and key return circuit

Remark The vacuum fluorescent display (VFD) is a typical name. In some documents, however, it is described as the fluorescent indicator panel (FIP®). The VFD and FIP have identical functions.

The major functional differences among the subseries are listed below.

Subseries Name		ROM Capacity (Bytes)	Timer 8-Bit	Timer 16-Bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remark
Small scale, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789088	16 K to 32 K	3 ch							24		
	μPD789074	2 K to 8 K	1 ch									
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale, general-purpose applications + A/D function	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch	1ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789477	24 K					8 ch	–				
	μPD789417A	12 K to 24 K					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789427	4 K to 24 K		–			1 ch		–	18		
	μPD789327						–		1 ch	21		
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789803	8 K to 16 K	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 K								31	4.0 V	
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

FUNCTIONS

Item		Function
Internal memory	Flash memory	48 Kbytes
	RAM	2 Kbytes
★	LCD data RAM	40 × 16 bits
★ Minimum instruction execution time		• 0.4/1.6 μs (operation with main system clock running at 5.0 MHz) • 122 μs (operation with subsystem clock running at 32.768 kHz)
General-purpose registers		8 bits × 8 registers
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)
I/O ports		Total of 38 port pins • 37 CMOS input/output pins • N-ch open-drain input/output pin
Serial interface		• UART mode
LCD controller/driver		• Up to 40 segment signal outputs • Up to 16 common signal outputs • 1/5 bias mode
Timers		• 16-bit timer • 8-bit timer • Watch timer • Watchdog timer
Pulse output		Clock output/buzzer output
Vectored interrupt sources	Maskable	10 internal and 6 external interrupts
	Nonmaskable	Internal interrupt
Power supply voltage		V_{DD} = 2.7 to 5.5 V
Operating ambient temperature		T_A = -20 to +60 °C
Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm)

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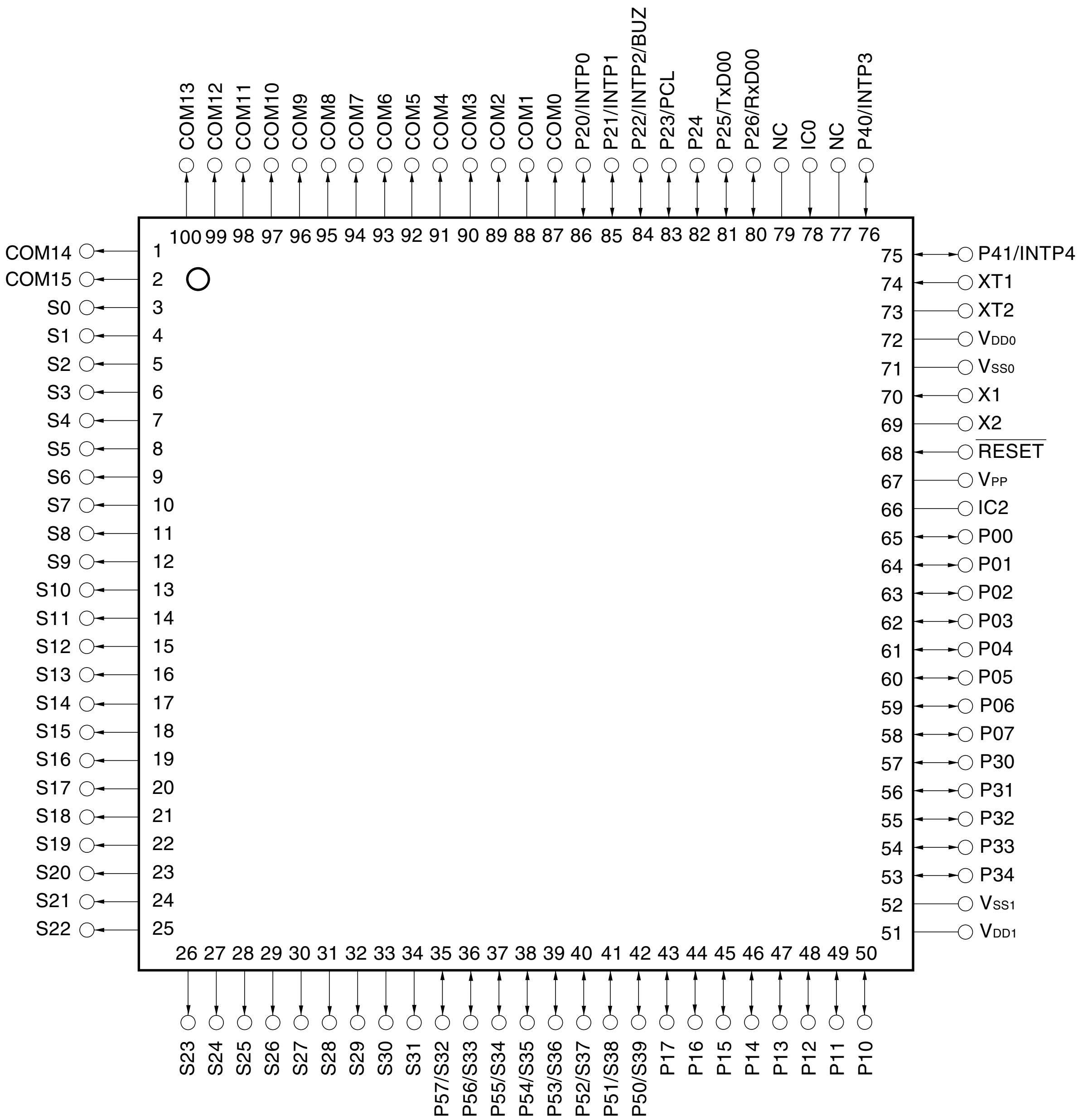
1. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**

μPD78F9831GC-8EU



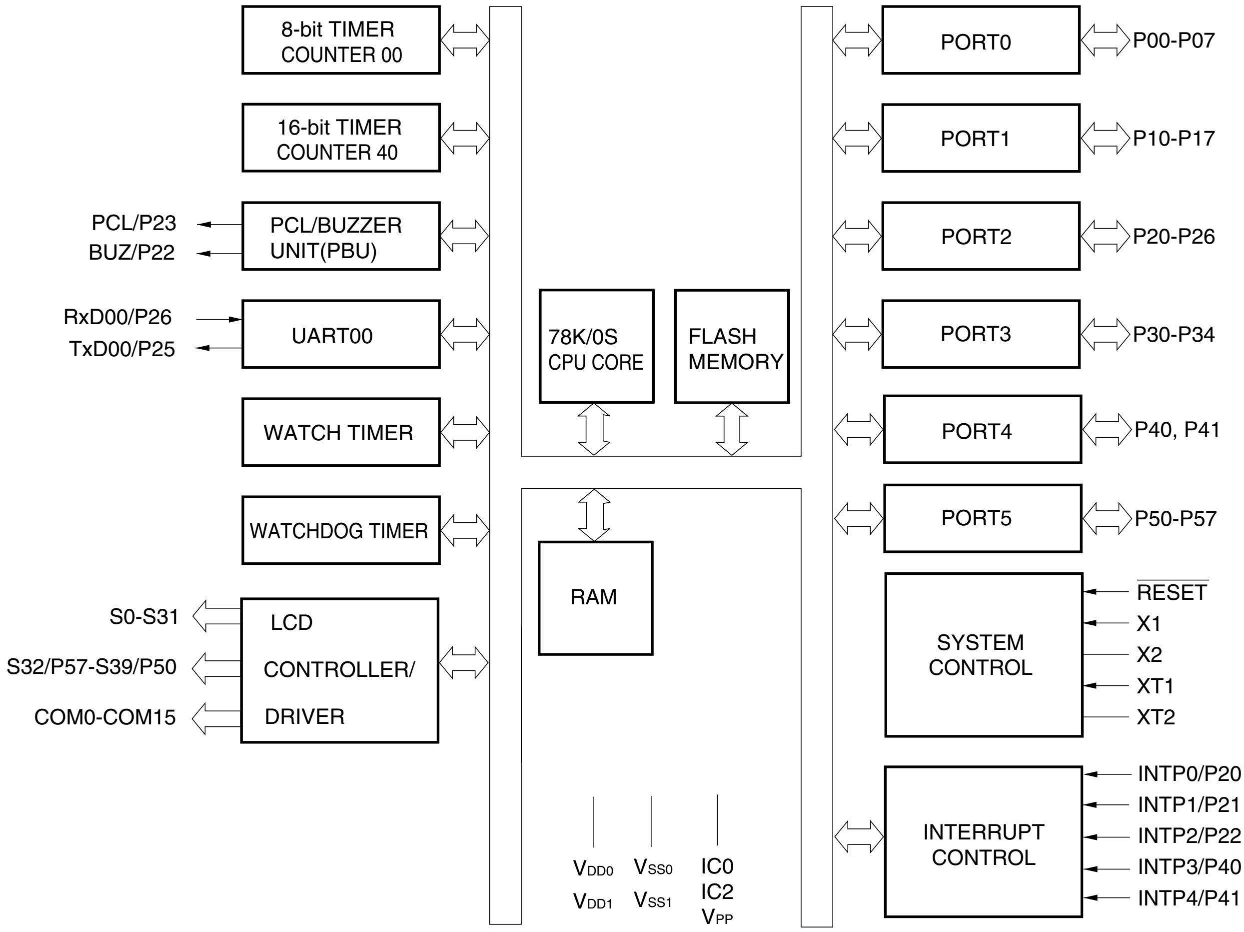
Cautions 1. In normal operation mode, connect the V_{PP} pin directly to the V_{SS0} or V_{SS1} pin.

2. Connect the IC0 (Internally Connected) pin directly to the V_{SS0} or V_{SS1} pin.

3. Leave the IC2 pin open.

BUZ	: Buzzer Clock	PCL	: Programming Clock
COM0-COM15	: Common Output	$\overline{\text{RESET}}$	: Reset
IC0, IC2	: Internally Connected	RxD00	: Receive Data
INTP0-INTP4	: External Interrupt Input	S0-S39	: Segment Output
NC	: Non-connection	TxD00	: Transmit Data
P00-P07	: Port 0	V_{DD0}, V_{DD1}	: Power Supply
P10-P17	: Port 1	V_{PP}	: Programming Power Supply
P20-P26	: Port 2	V_{SS0}, V_{SS1}	: Ground
P30-P34	: Port 3	X1, X2	: Crystal (Main system Clock)
P40, P41	: Port 4	XT1, XT2	: Crystal (Subsystem Clock)
P50-P57	: Port 5		

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	When Reset	Also Used As
P00-P07	I/O	Port 0 8-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the on-chip pull-up resistor is to be used can be specified by software.	Input	–
P10-P17	I/O	Port 1 8-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the on-chip pull-up resistor is to be used can be specified by software.	Input	–
P20	I/O	Port 2 7-bit input/output port Can be set to either input or output in 1-bit units P24 can be used as an N-ch open-drain input/output port pin.	Input	INTP0
P21				INTP1
P22				INTP2/BUZ
P23				PCL
P24				–
P25				TxD00
P26				RxD00
P30-P34	I/O	Port 3 5-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the on-chip pull-up resistor is to be used can be specified by software.	Input	–
P40	I/O	Port 4 2-bit input/output port Can be set to either input or output in 1-bit units	Input	INTP3
P41				INTP4
P50-P57	I/O	Port 5 8-bit input/output port Can be set to either input or output in 1-bit units	Input	S39-S32

3.2 Non-Port Pins

Pin Name	I/O	Function	When Reset	Also Used As
INTP0	Input	External interrupt input for which effective edges (rising and/or falling edges) can be specified	Input	P20
INTP1				P21
INTP2				P22/BUZ
INTP3				P40
INTP4				P41
RxD00	Input	Serial data input to asynchronous serial interface	Input	P26
TxD00	Output	Serial data output from asynchronous serial interface	Input	P25
BUZ	Output	Buzzer output	Input	P22/INTP2
PCL	Output	Clock output	Input	P23
S0-S31	Output	Segment signal output from LCD controller/driver	Output	–
S32-S39				P57-P50
COM0-COM15	Output	Common signal output from LCD controller/driver	Output	–
X1	Input	Connected to crystal for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connected to crystal for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD0}	–	Positive supply voltage for ports	–	–
V_{DD1}	–	Positive supply voltage for circuits other than ports	–	–
V_{SS0}	–	Port section ground potential	–	–
V_{SS1}	–	Ground potential of circuits other than ports	–	–
NC	–	This pin is not internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin (it can also be left open).	–	–
IC0	Input	This pin is internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–
IC2	–	This pin is internally connected. Leave this pin open.	–	–
V_{PP}	–	This pin is used to set flash memory programming mode and applies a high voltage when a program is written or verified. In normal operation mode, connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–

3.3 Pin Input/Output Circuits and Handling of Unused Pins

Table 3-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.
Figure 3-1 shows the configuration of each type of input/output circuit.

Table 3-1. Type of Input/Output Circuit for Each Pin and Handling of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection Of Unused Pins
P00-P07	5-H	I/O	Connect these pins to the V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} pin via the respective resistor.
P10-P17			
P20/INTP0	8-H		Connect these pins to the V_{SS0} or V_{SS1} pin via the respective resistor.
P21/INTP1			
P22/INTP2/BUZ			
P23/PCL	5-S		Connect these pins to the V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} pin via the respective resistor.
P24	13-AB		
P25/TxD00	5-S		
P26/RxD00	8-H		
P30-P34	8-C		
P40/INTP3	8-H		Connect these pins to the V_{SS0} or V_{SS1} pin via the respective resistor.
P40/INTP4			
P50/S39-P57/S32	17-I		Connect these pins to the V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} pin via the respective resistor.
S0-S31	17-H	Output	Leave these pins open.
COM0-COM15	18-C		
XT1	16	Input	Connect this pin to the V_{SS0} or V_{SS1} pin.
XT2		–	Leave this pin open.
$\overline{\text{RESET}}$	2	Input	–
NC	–	–	Connect this pin directly to the V_{SS0} or V_{SS1} pin, or leave it open.
IC0	–	Input	Connect this pin directly to the V_{SS0} or V_{SS1} pin.
IC2	2-B	–	Leave this pin open.
V_{PP}	–	–	Connect this pin directly to the V_{SS0} or V_{SS1} pin.

Figure 3-1. Pin Input/Output Circuits (1/2)

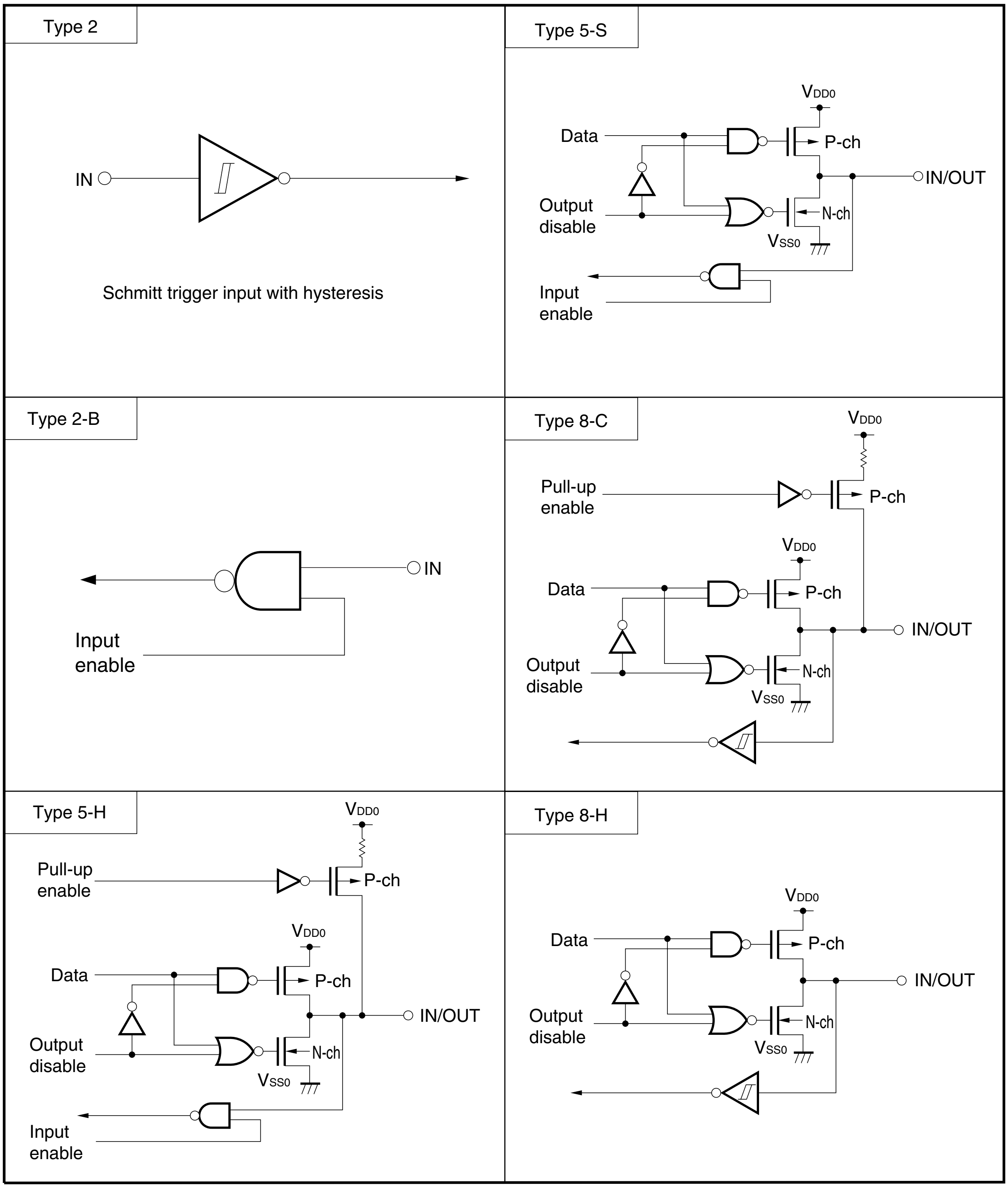
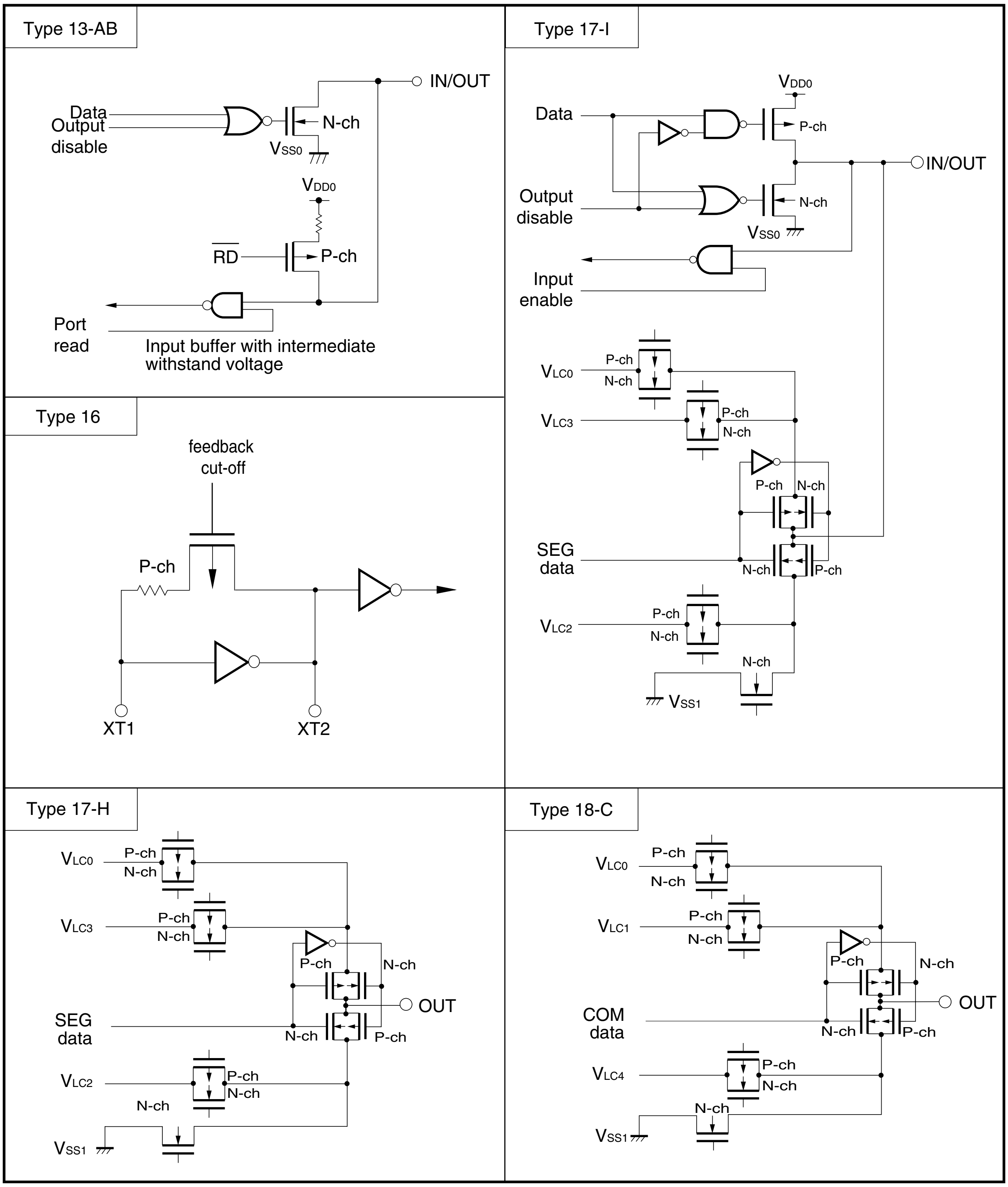


Figure 3-1. Pin Input/Output Circuits (2/2)

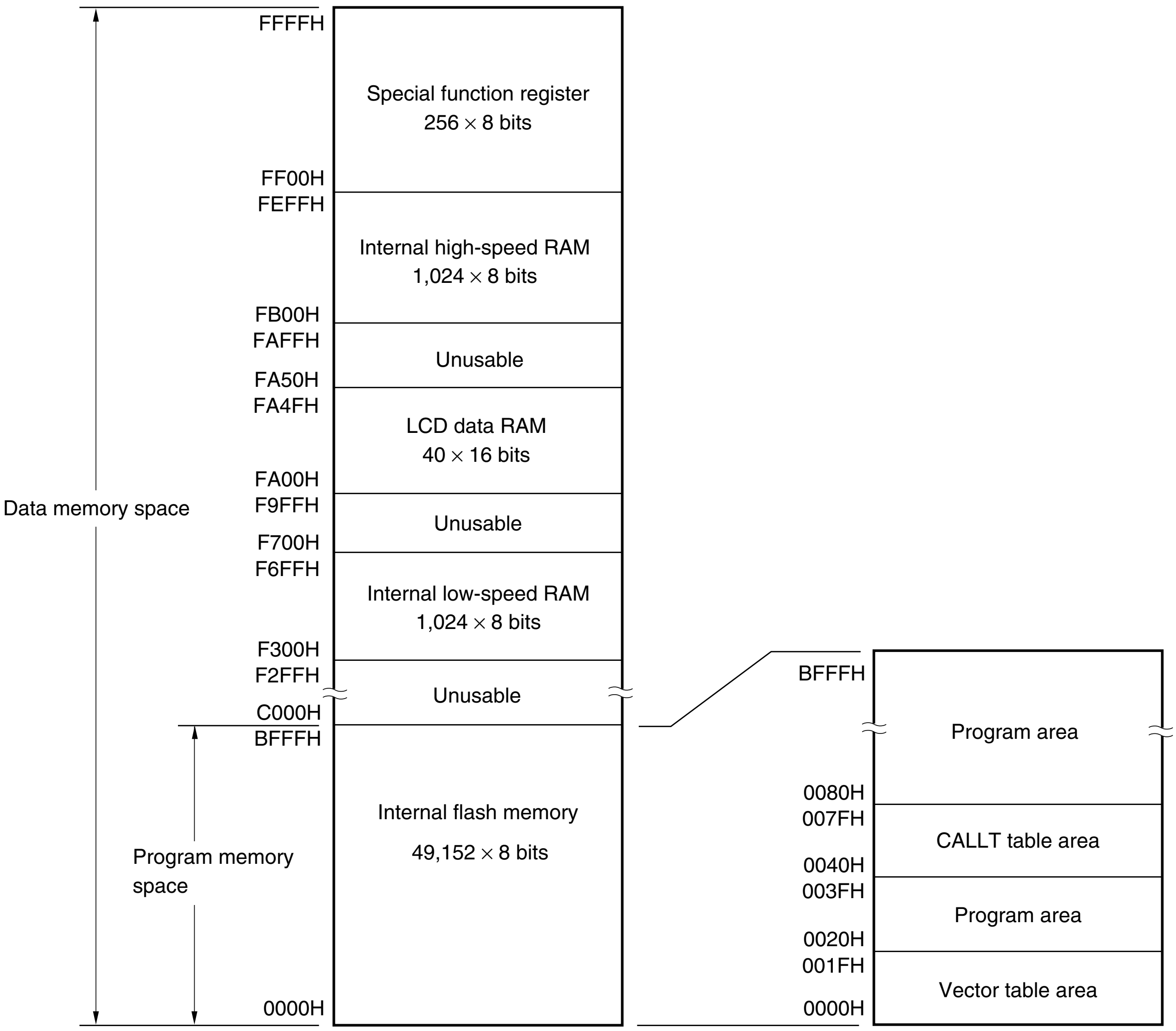


4. MEMORY SPACE

The μPD78F9831 can access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map

★



5. INTERRUPT FUNCTIONS

There are two types and 17 sources of interrupt functions as shown below.

- Nonmaskable interrupt : 1 source
- Maskable interrupts : 16 sources

Table 5-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Nonmaskable	–	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSER00	Occurrence of serial interface (UART00) reception error	Internal	000CH	(B)
	5	INTSR00	End of serial interface (UART00) reception		000EH	
	6	INTST00	End of serial interface (UART00) transmission		0010H	
	7	INTTM40	Generation of 16-bit timer 40 match signal		0012H	
	8	INTTM41	Occurrence of 16-bit timer 40 overflow		0014H	
	9	INTTM4	Logical OR of 16-bit timer 40 match signal and overflow signal		0016H	
	10	INTTM00	Generation of 8-bit timer 00 match signal		0018H	
	11	INTWTI	Interval timer interrupt		001AH	
	12	INTWT	Watch timer interrupt		001CH	
	13	INTKR00	Key return signal detection	External	001EH	(C)
	14	INTP3	Pin input edge detection		0020H	
	15	INTP4			0022H	

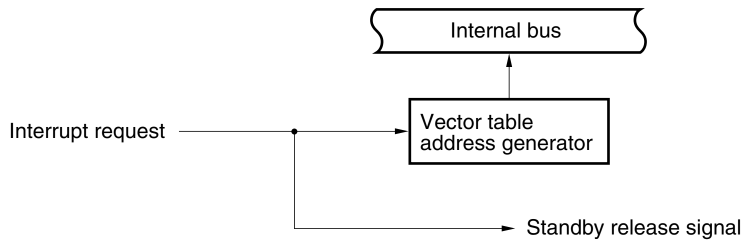
Notes 1. Priorities are intended for the priority for two or more simultaneously generated maskable interrupts. 0 is the highest priority and 15 is the lowest priority.

2. Basic configuration types (A) to (C) correspond to (A) to (C) of Figure 5-1.

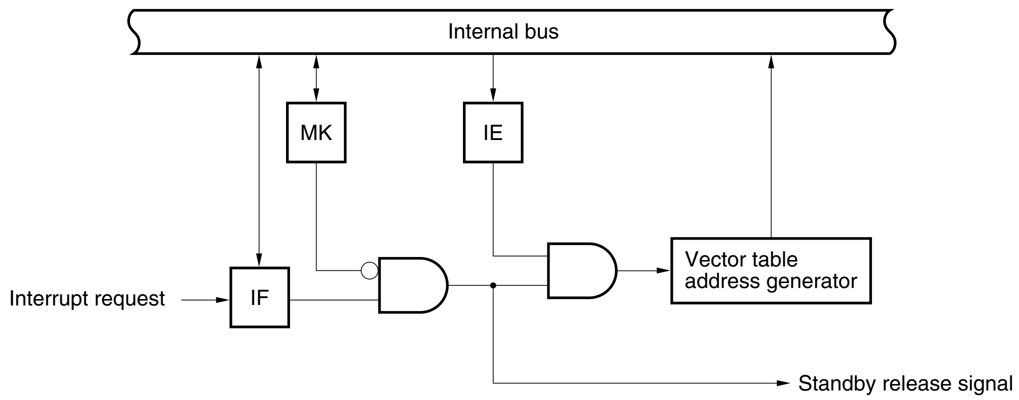
Remark Only one of the two watchdog timer interrupt sources, non-maskable or maskable (internal), can be selected.

Figure 5-1. Basic Configuration of Interrupt Function

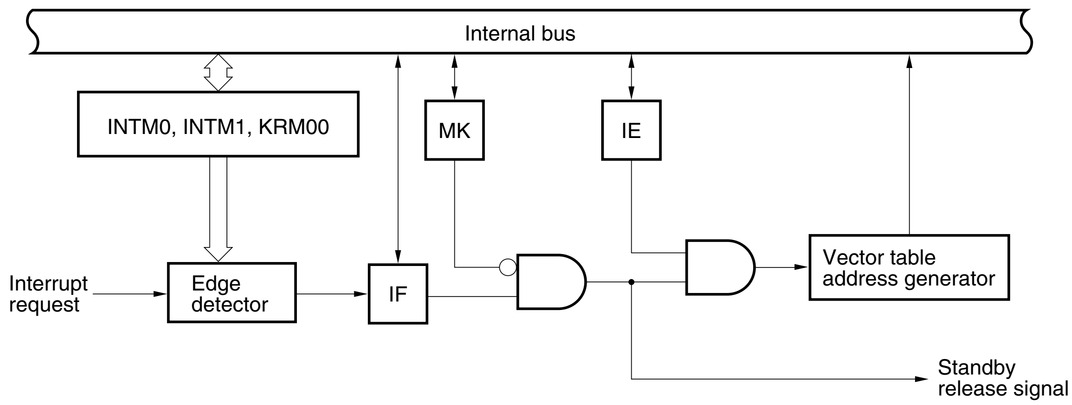
(A) Internal nonmaskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



INTM0 : External interrupt mode register 0
INTM1 : External interrupt mode register 1
KRM00 : Key return mode register 00
IF : Interrupt request flag
IE : Interrupt enable flag
MK : Interrupt mask flag

★ 6. FLASH MEMORY PROGRAMMING

Flash memory is used as the built-in program memory of the μPD78F9831.

The flash memory can be written even while the device is mounted in the target system (on-board write). To write a program into the flash memory, connect the dedicated flash writer (Flashpro III (model number: FL-PR3, PG-FP3)) to both the host machine and target system.

Remark The FL-PR3 is manufactured by Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting the Transmission Method

The Flashpro III writes into flash memory by means of serial transmission. The transmission method to be used for writing is selected from those listed in Table 6-1. To select a transmission method, use the format shown in Figure 6-1, according to the number of V_{PP} pulses listed in Table 6-1.

Table 6-1. Transmission Methods

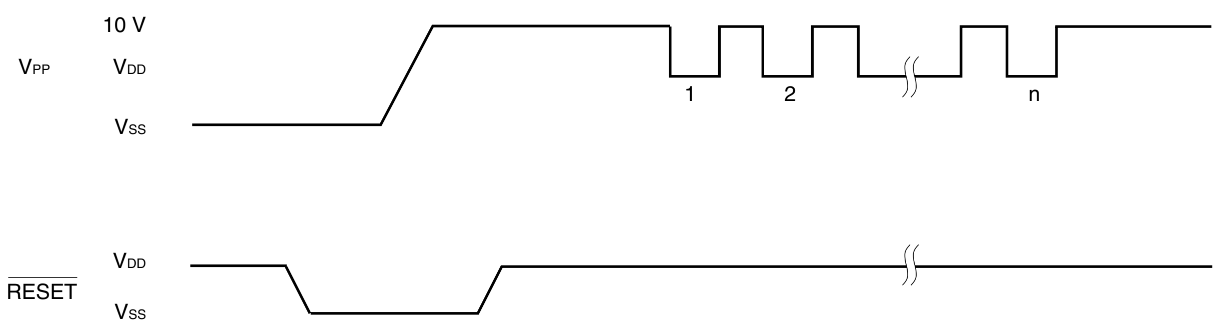
Transmission Method	Pins[Note 1]	Number of V_{PP} Pulses
UART	TxD00/P25 RxD00/P26	8
Pseudo 3-wire mode[Note 2]	P10 (serial clock input) P11 (serial data input) P12 (serial data output)	12

★ **Notes 1.** When flash memory programming mode is set, all pins not used for memory programming enter the same state as that immediately after a reset. Therefore, when the external device connected to a port cannot recognize that state of the port immediately after a reset, the pins must be connected to the V_{DD0} or V_{DD1} pin, or the V_{SS0} or V_{SS1} pin via a resistor.

2. Serial transfer by controlling the ports using software

Caution To select a transmission method, always use the corresponding number of V_{PP} pulses listed in Table 6-1.

Figure 6-1. Format of Transmission Method Selection



6.2 Flash Memory Programming Functions

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected transmission method. Table 6-2 lists the main flash memory programming functions.

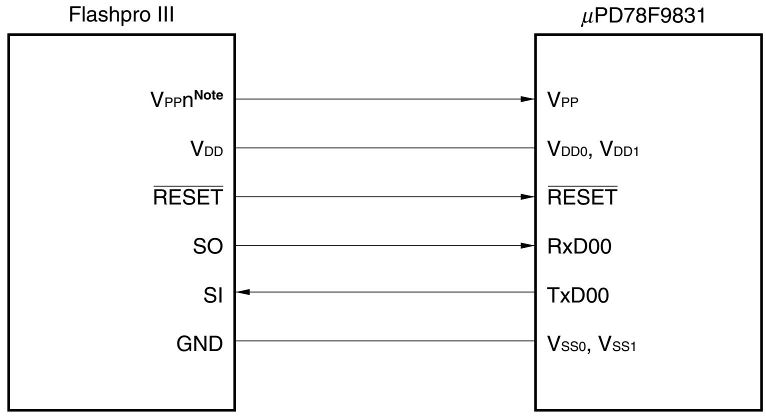
Table 6-2. Main Flash Memory Programming Functions

Function	Description
Batch erase	Erases the entire contents of memory.
Batch blank check	Checks that the entire contents of memory have been erased.
Data write	Write to the flash memory according to the specified write start address and number of bytes of data to be written.
Batch verify	Compares the entire contents of memory with the input data.

6.3 Connecting the Flashpro III

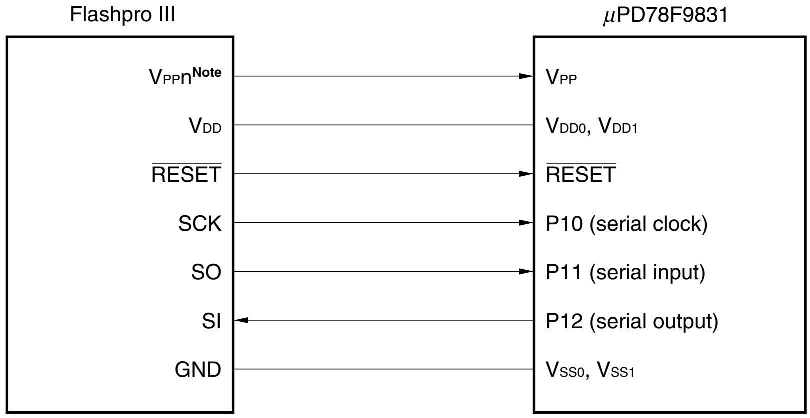
The connection between the Flashpro III and μPD78F9831 varies with the transmission method (UART or pseudo 3-wire). Figures 6-2 and 6-3 show the connection for each transmission method.

Figure 6-2. Flashpro III Connection in UART Mode



Note n: 1 or 2

Figure 6-3. Flashpro III Connection in Pseudo 3-Wire Mode



Note n: 1 or 2

6.4 Example of Settings for Flashpro III (PG-FP3)

When writing to flash memory using Flashpro III (PG-FP3), make the following settings.

<1> Load a parameter file.
<2> Select the mode of serial communication and serial clock with a type command.
<3> Make the settings according to the example of settings for PG-FP3 shown below.

Table 6-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		V_{PP} Pulse Number[Note 1]
UART	COMM PORT	UART-ch0	8
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
	UART BPS	9,600 bps[Note 2]	
Pseudo 3-wire mode	COMM PORT	Port A	12
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 kHz	

Notes 1. This is the number of V_{PP} pulses that are supplied by the Flashpro III at serial communication initialization. The pins that will be used for communication are determined according to this number.

2. Select one of 9,600 bps, 19,200 bps, 38,400 bps, or 76,800 bps.

Remark COMM PORT : Serial port selection
SIO CLK : Serial clock frequency selection
CPU CLK : Input CPU clock source selection

7. INSTRUCTION SET OVERVIEW

The instruction set for the μPD78F9831 is listed later.

7.1 Legend

7.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform with the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and a pair of [and] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [and]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or a pair of [and].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 7-1).

Table 7-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

7.1.2 Descriptions of the operation field

A	:	A register (8-bit accumulator)
X	:	X register
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
AX	:	AX register pair (16-bit accumulator)
BC	:	BC register pair
DE	:	DE register pair
HL	:	HL register pair
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
IE	:	Interrupt request enable flag
NMIS	:	Flag to indicate that a nonmaskable interrupt is being handled
()	:	Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L	:	Upper and lower 8 bits of a 16-bit register
$\wedge$	:	Logical product (AND)
$\vee$	:	Logical sum (OR)
$\forall$	:	Exclusive OR
—	:	Inverted data
addr16	:	16-bit immediate data or label
jdisp8	:	Signed 8-bit data (displacement value)

7.1.3 Description of the flag operation field

(blank)	:	No change
0	:	To be cleared to 0
1	:	To be set to 1
$\times$	:	To be set or cleared according to the result
R	:	To be restored to the previous value

7.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.

2. Except when r = A or X.

3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	Flag AC	Flag CY
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	$A \leftarrow A \vee$ byte	×		
	saddr, #byte	3	6	(saddr) $\leftarrow$ (saddr) $\vee$ byte	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee$ (saddr)	×		
	A, !addr16	3	8	$A \leftarrow A \vee$ (addr16)	×		
	A, [HL]	1	6	$A \leftarrow A \vee$ (HL)	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee$ (HL + byte)	×		
XOR	A, #byte	2	4	$A \leftarrow A \veebar$ byte	×		
	saddr, #byte	3	6	(saddr) $\leftarrow$ (saddr) $\veebar$ byte	×		
	A, r	2	4	$A \leftarrow A \veebar r$	×		
	A, saddr	2	4	$A \leftarrow A \veebar$ (saddr)	×		
	A, !addr16	3	8	$A \leftarrow A \veebar$ (addr16)	×		
	A, [HL]	1	6	$A \leftarrow A \veebar$ (HL)	×		
	A, [HL + byte]	2	6	$A \leftarrow A \veebar$ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY $\leftarrow$ AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY $\leftarrow$ AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	$r \leftarrow r + 1$	×	×	
	saddr	2	4	(saddr) $\leftarrow$ (saddr) + 1	×	×	
DEC	r	2	4	$r \leftarrow r - 1$	×	×	
	saddr	2	4	(saddr) $\leftarrow$ (saddr) – 1	×	×	
INCW	rp	1	4	$rp \leftarrow rp + 1$			
DECW	rp	1	4	$rp \leftarrow rp - 1$			
ROR	A, 1	1	2	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
ROL	A, 1	1	2	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
RORC	A, 1	1	2	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
ROLC	A, 1	1	2	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1), PC_L ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

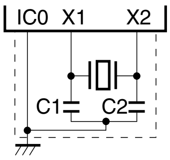
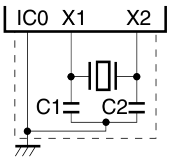
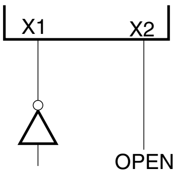
Parameter	Symbol	Conditions		Rated Value	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P24		–0.3 to V_{DD} + 0.3 Note	V
	V_{I2}	P24	N-ch open drain	–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3 Note	V
High-level output current	I_{OH}	Each pin		–10	mA
		Total for all pins		–30	mA
Low-level output current	I_{OL}	Each pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A	During normal operation		–20 to +60	°C
★		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note 6.5 V or less

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.
That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATION CIRCUIT
(T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)Note 1		2.0		5.0	MHz
		Oscillation settling timeNote 2	Time after V_{DD} reaches MIN. of the oscillation voltage range			4	ms
Crystal		Oscillator frequency (f_X)Note 1		2.0		5.0	MHz
		Oscillation settling timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
★ External clock		X1 input frequency (f_X)Note 1		2.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		85		250	ns

Notes 1. Only the characteristic of the oscillation circuit is indicated. See the description of the AC characteristic for the instruction execution time.

2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected.

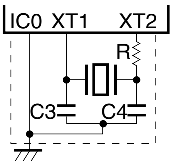
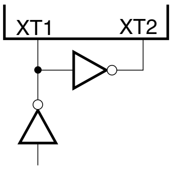
Cautions 1. When using the main system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS0}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

2. Before switching from the subsystem clock back to the main system clock, always allow sufficient time for the oscillation to settle by specifying it in the program.

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

CHARACTERISTICS OF THE SUBSYSTEM CLOCK OSCILLATION CIRCUIT
(T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillator frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation settling timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		35	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Only the characteristic of the oscillation circuit is indicated. See the description of the AC characteristic for the instruction execution time.

2. Time required for oscillation to settle after V_{DD} reaches the MIN. value of the oscillation voltage range.

Cautions 1. When using the subsystem clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS0}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

2. The subsystem clock oscillation circuit is designed to have a low amplification degree so as to maintain a low current drain. Therefore, it is more likely to malfunction as a result of noise than the main system clock oscillation circuit. When using the subsystem clock, therefore, pay particularly careful attention to how it is wired.

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC CHARACTERISTICS (T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★ Output current, high	I_{OH}	Per pin				-1	mA
		Total for all pins				-15	mA
★ Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
High-level input voltage	V_{IH1}	P00-P07, P10-P17, P23, P25, P50-P57		0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{RESET}$, P20-P22, P26, P30-P34, P40, P41		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P24 (N-ch open drain)		0.7V_{DD}		12	V
★	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} - 0.5		V_{DD}	V
				V_{DD} - 0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	P00-P07, P10-P17, P23, P25, P50-P57		0		0.3V_{DD}	V
	V_{IL2}	$\overline{RESET}$, P20-P22, P26, P30-P34, P40, P41		0		0.2V_{DD}	V
	V_{IL3}	P24 (N-ch open drain)		0		0.3V_{DD}	V
★	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
High-level output voltage	V_{OH}	I_{OH} = -1 mA	V_{DD} = 4.5 to 5.5 V	V_{DD} - 1.0			V
		I_{OH} = -100 μA		V_{DD} - 0.5			V
Low-level output voltage	V_{OL1}	Pins other than the P24 pin	$4.5 \leq V_{DD} \leq 5.5$ V, I_{OL} = 10 mA			1.0	V
			$2.7 \leq V_{DD} < 4.5$ V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P24 (N-ch open drain)	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			$2.7 \leq V_{DD} < 4.5$ V, I_{OL} = 1.6 mA			0.4	V
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P07, P10-P17, P20-P23, P25, P26, P30-P34, P40, P41, P50-P57, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 12 V	P24 (N-ch open drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00-P07, P10-P17, P20-P23, P25, P26, P30-P34, P40, P41, P50-P57, $\overline{RESET}$, P24 (When an input instruction is not executed)			-3	μA
	I_{LIL2}		X1, X2, XT1, XT2			-20	μA
	I_{LIL3}		P24 (N-ch open drain) When an input instruction is executed			-30	μA

Remark The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

★ **DC CHARACTERISTICS (T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V) (2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output leakage current	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				-3	μA
Software-specified pull-up resistor	R_1	V_{IN} = 0 V, P00-P07, P10-P17, P30-P34		50	100	200	kΩ
Power supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 2]		5	10	mA
			V_{DD} = 3.0 V ±10%[Note 3]		3	6	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 2]		0.8	1.6	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.4	0.8	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ±10%		120	240	μA
			V_{DD} = 3.0 V ±10%		80	160	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		10	20	μA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA

Notes 1. Neither the power supply current flowing when LCD is active (LCDON20 = 1, LIPS20 = 1) nor the port current (including the current flowing through the on-chip pull-up resistor) is included.

2. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H)

3. During low-speed mode operation (when the PCC is set to 02H)

4. While the main system clock is stopping

Remark The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

★ LCD CHARACTERISTICS (T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	$V_{DD} = V_{LCD}$	VAON20 = 0	3.5		5.5	V
			VAON20 = 1	2.7		5.5	V
Segment output voltage[Note 1]	V_{ODS}	When the output level is V_{LC0}			V_{LCD}		V
		When the output level is V_{LC2}			3/5V_{LCD}		V
		When the output level is V_{LC3}			2/5V_{LCD}		V
Common output voltage[Note 1]	V_{ODC}	When the output level is V_{LC0}			V_{LCD}		V
		When the output level is V_{LC1}			4/5V_{LCD}		V
		When the output level is V_{LC4}			1/5V_{LCD}		V
Segment output on resistance	R_{SEG}	$V_{LCn} \rightarrow Sp$, I_O = | 20 μA |			5.0	12.5	kΩ
Common output on resistance	R_{COM}	$V_{LCn} \rightarrow COMq$, I_O = | 20 μA |			4.0	10.0	kΩ
LCD input frequency	f_{LCD}	VAON20 = 1		32		78.13	kHz
		VAON20 = 0		7.81		78.13	kHz
LCD operating current[Note 2]	I_{LCD1}	V_{DD} = 5.0 V ±10%, VAON20 = 0			30	65	μA
	I_{LCD2}	V_{DD} = 3.0 V ±10%, VAON20 = 1			17	40	μA

Notes 1. Voltages when no load is applied

2. Total current flowing through the V_{DD0} pin (including the current flowing through the LCD divider resistor)

When LCDON20 = 0 and LIPS20 = 0 (the display is turned off and the internal drive power is not supplied), the power supply current is included in the power supply current I_{DD5} (STOP mode) in the DC characteristics.

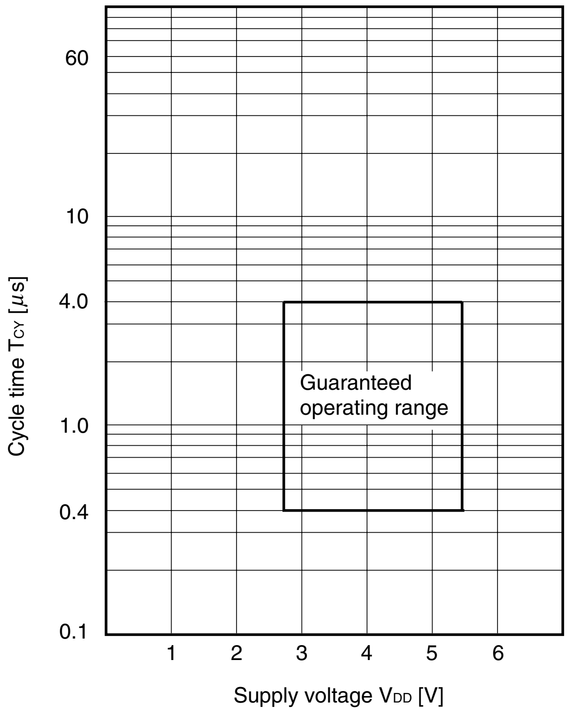
Remark n = 0 to 4
p = 0 to 39
q = 0 to 15

AC CHARACTERISTICS

(1) Basic operations (T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on main system clock	0.4		4.0	μs
		Operation based on subsystem clock	114	122	125	μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INTP0 to INTP4	10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}		10			μs

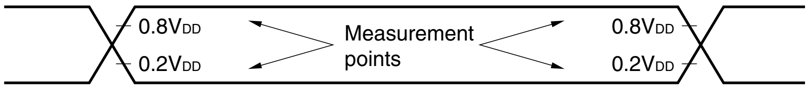
T_{CY} vs V_{DD} (main system clock)



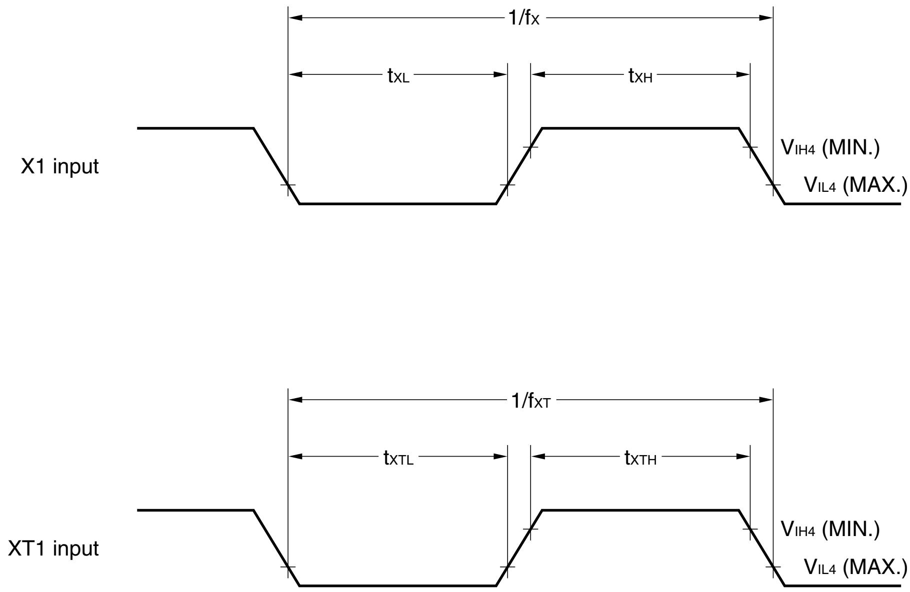
(2) Serial Interface (UART00) (T_A = -20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Transfer rate		Operation at f_X = 5.0 MHz			78,125	bps

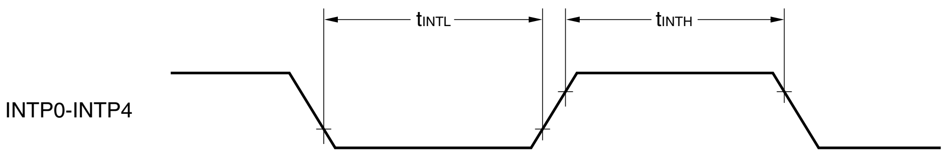
AC TIMING MEASUREMENT POINTS (except the X1 and XT1 inputs)



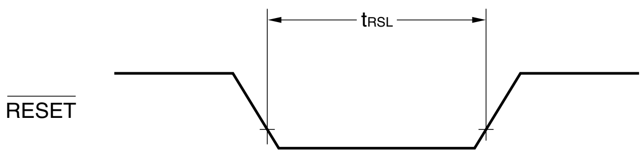
CLOCK TIMING



INTERRUPT INPUT TIMING



$\overline{\text{RESET}}$ INPUT TIMING



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = -20 to +60 °C)

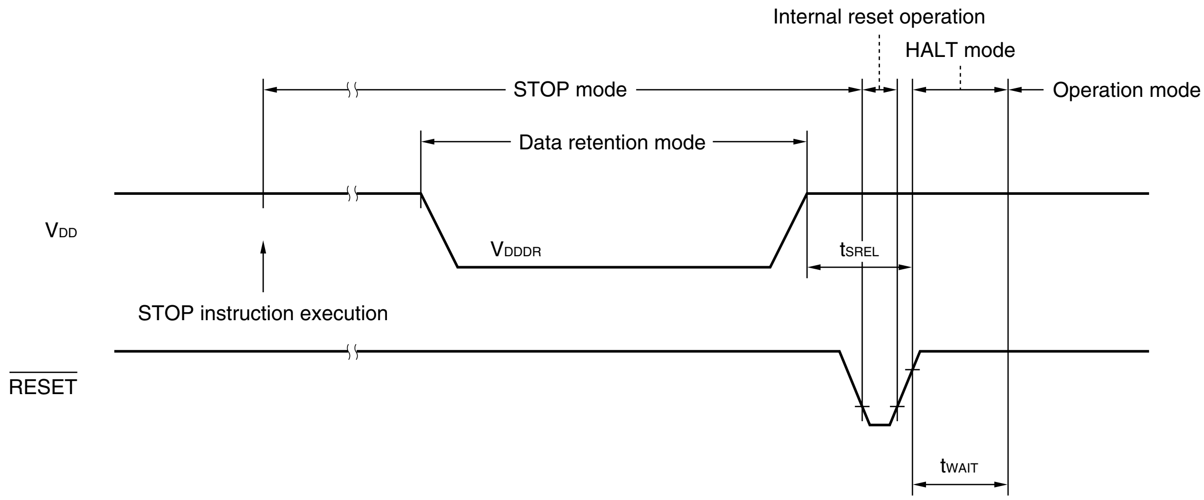
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
	Release signal set time	t_{SREL}		0			μs
★	Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		ms
			Release by interrupt request		**Note 2**		ms

Notes 1. Oscillation stabilization wait time is a time for stopping the CPU operation to prevent the unstable operation when the oscillation is started.

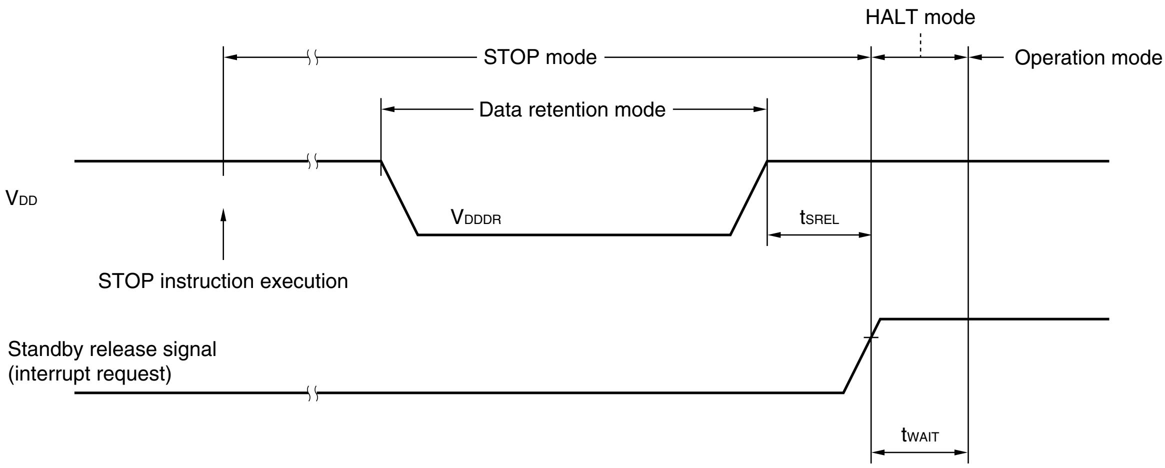
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, and $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_X: System clock oscillation frequency

★ DATA RETENTION TIMING (STOP mode release by $\overline{RESET}$)



★ DATA RETENTION TIMING (Standby release signal: STOP mode release by interrupt signal)



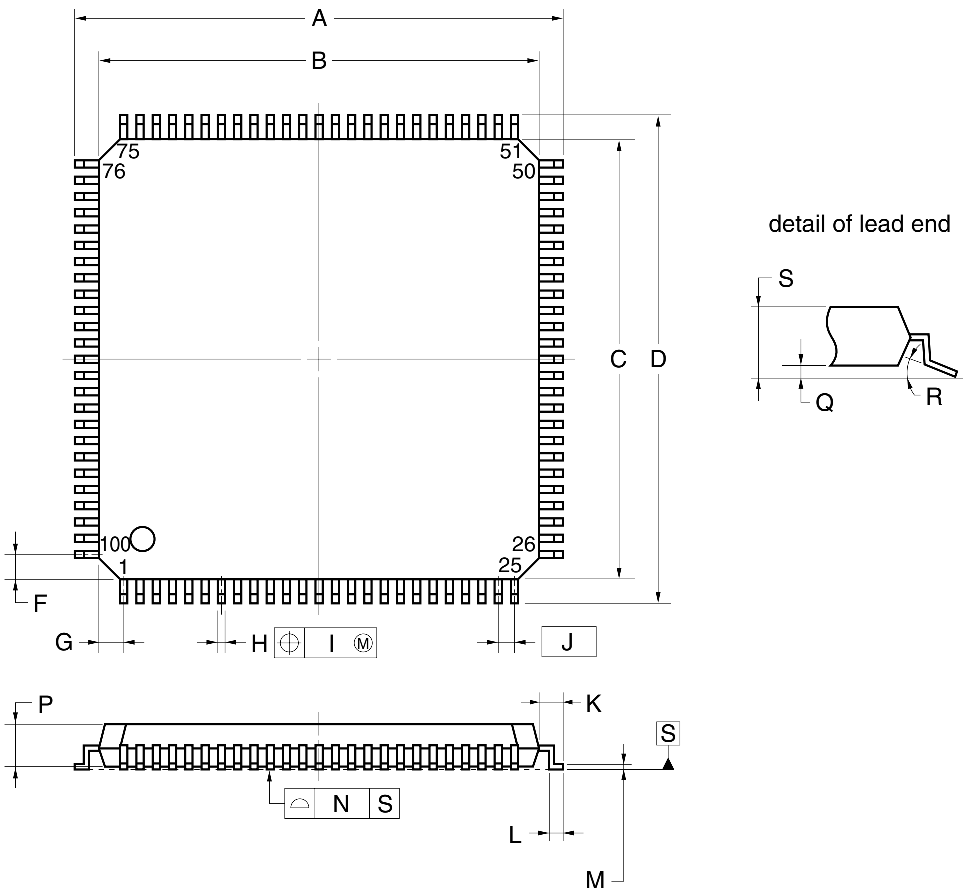
★ **FLASH MEMORY WRITE/ERASE CHARACTERISTICS (T_A = 10 to 40 °C, V_{DD} = 2.7 to 5.5 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		2		5	MHz
Write current[Note] (V_{DD} pin)	I_{DDW}	When V_{PP} supply voltage = V_{PP1} 5.0-MHz crystal oscillation operation mode			13	mA
Write current[Note] (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			20	mA
Erase current[Note] (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1} 5.0-MHz crystal oscillation operation mode			13	mA
Erase current[Note] (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Erase time	t_{er}				20	s
Write count		Erase/write are regarded as 1 cycle.			20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

Note The port current (including the current that flows to the on-chip pull-up resistors) is not included.

9. PACKAGE DRAWINGS

★ 100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^\circ{}^{+7^\circ}_{-3^\circ}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

★ 10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9831 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD78F9831GC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. Max. (at 210 °C or higher), Count: twice or less	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: 40 sec. Max. (at 200 °C or higher), Count: twice or less	VP15-00-2
Partial heating	Pin temperature: 300 °C Max., Time: 3 sec. Max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DIFFERENCES BETWEEN THE μPD78F9831 AND MASKED ROM PRODUCT

The μPD78F9831 is produced by replacing the internal ROM of the masked ROM product μPD789830 with larger flash memory, and by adding I/O ports to the μPD789830. Unlike bare chips of masked ROM products, the shipped μPD78F9831 is contained in a 100-pin plastic LQFP package. Table A-1 lists differences between the μPD78F9831 and μPD789830.

Table A-1. Differences between the μPD78F9831 and μPD789830

Item		Flash Memory Product	Masked ROM Product
		μPD78F9831	μPD789830
Internal memory	Flash memory/ROM	48 Kbytes	24 Kbytes
	RAM	2 Kbytes	1 Kbyte
★	LCD display RAM	40×16 bits	
I/O ports		Total: 38 port pins P00-P07, P10-P17, P20-P26, P30-P34, P40, P41, P50-P57	Total: 30 port pins P00-P07, P10, P11, P20-P26, P30-P34, P50-P57
External interrupt input pins		Total: 5 pins INTP0-INTP4	Total: 3 pins INTP0-INTP2
★ Interrupt sources		17	15
V_{PP} pin		Yes	No
Form of shipment		100-pin plastic LQFP	88-pin bare chip
Electrical characteristics		Refer to individual related data sheets.	

APPENDIX B DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9831.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789831[Notes 1, 2, 3]	Device file for μPD789830 Subseries
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
★ FA-100GC-8EU[Note 4]	Flash memory writing adapter for 100-pin plastic LQFP (fine pitch) (GC-8EU type)

★ Debugging Tools

IE-78K0S-NS In-circuit emulator	This in-circuit emulator is used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports the integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter	This adapter is used to supply power from a 100 to 240 V AC outlet.
IE-70000-98-IF-C Interface adapter	This adapter is required when a PC-9800 series PC (except notebook type) is used as the host machine for the IE-78K0S-NS (C bus supported).
IE-70000-CD-IF-A PC card/interface	These PC card and interface cable are required when a notebook PC is used as the host machine for the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	This adapter is required when an IBM PC/AT™ or compatible is used as the host machine for the IE-78K0S-NS (ISA bus supported).
IE-70000-PCI-IF-A Interface adapter	This adapter is required when a PCI bus incorporated personal computer is used as the host machine for the IE-78K0S-NS.
IE-789831-NS-EM1 Emulation board	This board is used to emulate the peripheral hardware specific to the device. The IE-789046-NS-EM1 is used in combination with the in-circuit emulator.
NP-100GC Emulation probe	Board to connect an in-circuit emulator to the target system. This is used in combination with the TGC-100SDW.
TGC-100SDW[Note 5] Conversion adapter	Conversion socket to connect the NP-100GC to a target system board on which a 100-pin plastic LQFP (fine pitch) (GC-8EU type) can be mounted.
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789831[Notes 1, 2]	Device file for μPD789830 Subseries

Real-time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes **1.** Based on the PC-9800 series (Japanese Windows™)
2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)
3. Based on the HP9000 series 700™ (HP-UX™) and SPARCstation™ (SunOS™, Solaris™)
4. Products made by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813).
5. Product made by TOKYO ELETEC Corporation
For further information, consult:
Tokyo Electronic Div. (TEL 03-3820-7112) or Osaka Electronic Div. (TEL 06-6244-6672) Daimaru Kogyo Corporation.

Remark The RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789831.

APPENDIX C RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789830 Data Sheet	U13284E
μPD78F9831 Data Sheet	This document
μPD789830 Subseries User's Manual	U13679E
78K/0S Series User's Manual, Instruction	U11047E
78K/0, 78K/0S Series Flash Memory Writing	U14458E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0 System Simulator Ver.2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver.2.10 or Later	External Part User Open Interface Specifications	To be created
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver.2.20 or Later Windows Based	Operation	U14910E
IE-78K0S-NS In-circuit Emulator		U13549E
IE-789831-NS-EM1 Emulation Board		U14202E
PG-FP3 Flash Memory Programmer		U13502E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0S Series OS MX78K0S	Fundamental	U12938E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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