

# MOS INTEGRATED CIRCUIT

## $\mu$ PD78011H, 78012H, 78013H, 78014H

### 8-BIT SINGLE-CHIP MICROCONTROLLER

#### DESCRIPTION

The  $\mu$ PD78011H, 78012H, 78013H, and 78014H are the products in the  $\mu$ PD78014H subseries within the 78K/0 series.

Compared with the older  $\mu$ PD78018F subseries, this subseries reduces the EMI (Electro Magnetic Interface) noise generated from the microcontroller.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

**$\mu$ PD78014H Subseries User's Manual: Planned to publish**  
**78K/0 Series User's Manual – Instruction: IEU-1372**

#### FEATURES

- Low EMI noise model
- Large on-chip ROM & RAM

| <div><div>Item</div><div>Product Name</div></div> | Program Memory (ROM) | Data Memory             |                     | Package                               |
|---------------------------------------------------|----------------------|-------------------------|---------------------|---------------------------------------|
|                                                   |                      | Internal High-Speed RAM | Internal Buffer RAM |                                       |
| μPD78011H                                         | 8K bytes             | 512 bytes               | 32 bytes            | • 64-pin plastic shrink DIP (750 mil) |
| μPD78012H                                         | 16K bytes            |                         |                     | • 64-pin plastic QFP (14 × 14 mm)     |
| μPD78013H                                         | 24K bytes            | 1024 bytes              |                     | • 64-pin plastic LQFP (12 × 12 mm)    |
| μPD78014H                                         | 32K bytes            |                         |                     |                                       |

- External memory expansion space : 64K bytes
- Instruction execution time can be varied from high-speed (0.4  $\mu$ s) to ultra-low-speed (122  $\mu$ s)
- I/O ports: 53 (N-ch open-drain : 4)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 2 channels
- Timer : 5 channels
- Supply voltage :  $V_{DD} = 1.8$  to 5.5 V

#### APPLICATION FIELD

Cellular phone, pager, VCR, audio, camera, home appliances, etc.

The information in this document is subject to change without notice.

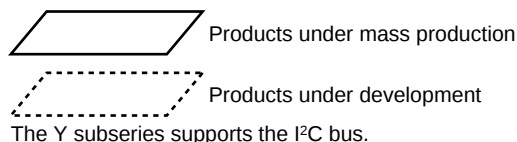
## ORDERING INFORMATION

| Part Number              | Package                             |
|--------------------------|-------------------------------------|
| $\mu$ PD78011HCW-xxx     | 64-pin plastic shrink DIP (750 mil) |
| $\mu$ PD78011HGC-xxx-AB8 | 64-pin plastic QFP (14 × 14 mm)     |
| $\mu$ PD78011HGK-xxx-8A8 | 64-pin plastic LQFP (12 × 12 mm)    |
| $\mu$ PD78012HCW-xxx     | 64-pin plastic shrink DIP (750 mil) |
| $\mu$ PD78012HGC-xxx-AB8 | 64-pin plastic QFP (14 × 14 mm)     |
| $\mu$ PD78012HGK-xxx-8A8 | 64-pin plastic LQFP (12 × 12 mm)    |
| $\mu$ PD78013HCW-xxx     | 64-pin plastic shrink DIP (750 mil) |
| $\mu$ PD78013HGC-xxx-AB8 | 64-pin plastic QFP (14 × 14 mm)     |
| $\mu$ PD78013HGK-xxx-8A8 | 64-pin plastic LQFP (12 × 12 mm)    |
| $\mu$ PD78014HCW-xxx     | 64-pin plastic shrink DIP (750 mil) |
| $\mu$ PD78014HGC-xxx-AB8 | 64-pin plastic QFP (14 × 14 mm)     |
| $\mu$ PD78014HGK-xxx-8A8 | 64-pin plastic LQFP (12 × 12 mm)    |

**Remark** xxx indicates ROM code No.

## DEVELOPMENT OF 78K/0 SERIES

The following products are available in the 78K/0 series. The parts numbers enclosed in a frame are subseries names.



### For control applications

|            |                           |                            |                                                                           |
|------------|---------------------------|----------------------------|---------------------------------------------------------------------------|
| 100 pins   | μPD78078                  | μPD78078Y                  | Adds timer to μPD78054 and reinforces external interface function         |
| 100 pins   | μPD78070A                 | μPD78070AY                 | ROM-less model of μPD78078                                                |
| 100 pins   | μPD780018 <sup>Note</sup> | μPD780018Y <sup>Note</sup> | Reinforces serial I/O of μPD78078 and limits functions                    |
| 80 pins    | μPD78058F                 | μPD78058FY                 | Low EMI noise model of μPD78054                                           |
| 80 pins    | μPD78054                  | μPD78054Y                  | Adds UART and D/A to μPD78014 and reinforces I/O                          |
| 64 pins    | μPD780034                 | μPD780034Y                 | Reinforces A/D of μPD780024                                               |
| 64 pins    | μPD780024                 | μPD780024Y                 | Reinforces serial I/O of μPD78018F. Low EMI noise model                   |
| 64 pins    | μPD780964                 |                            | Reinforces A/D of μPD780924                                               |
| 64 pins    | μPD780924                 |                            | UART as inverter control circuit. Low EMI noise model                     |
| 64 pins    | μPD78014H                 |                            | Low EMI noise model of μPD78018F                                          |
| 64 pins    | μPD78018F                 | μPD78018FY                 | Low voltage (1.8 V) model of μPD78014 with many variations of ROM and RAM |
| 64 pins    | μPD78014                  | μPD78014Y                  | Adds A/D and 16-bit timer to μPD78002                                     |
| 64 pins    | μPD780001                 |                            | Adds A/D to μPD78002                                                      |
| 64 pins    | μPD78002                  | μPD78002Y                  | Basic subseries for control applications                                  |
| 42/44 pins | μPD78083                  |                            | UART. Low voltage (1.8 V) model                                           |

### For FIP™ driving

|          |           |                                                                          |
|----------|-----------|--------------------------------------------------------------------------|
| 100 pins | μPD780208 | Reinforces I/O and FIP C/D of μPD78044F. Total display outputs : 53 pins |
| 80 pins  | μPD78044F | Adds 6-bit U/D counter to μPD78024. Total display outputs : 34 pins      |
| 64 pins  | μPD78024  | Basic subseries for FIP driving. Total display outputs : 26 pins         |

### For LCD driving

|          |           |            |                                                      |
|----------|-----------|------------|------------------------------------------------------|
| 100 pins | μPD780308 | μPD780308Y | Reinforces SIO of μPD78064 with expanded ROM and RAM |
| 100 pins | μPD78064B |            | Low EMI noise model of μPD78064                      |
| 100 pins | μPD78064  | μPD78064Y  | Basic subseries for LCD driving. UART                |

### Supporting IEBus™

|         |          |                                   |
|---------|----------|-----------------------------------|
| 80 pins | μPD78098 | Adds IEBus controller to μPD78054 |
|---------|----------|-----------------------------------|

### For LV

|         |            |                                                        |
|---------|------------|--------------------------------------------------------|
| 64 pins | μPD78P0914 | PWM output, LV digital code decoder, and Hsync counter |
|---------|------------|--------------------------------------------------------|

**Note** Under planning

The major differences between the respective subseries are shown below.

| Functions<br>Subseries |            | ROM<br>Capacity | Timer |        |       |     | 8-bit<br>A/D | 10-bit<br>A/D                                          | 8-bit<br>D/A | Serial<br>Interface                  | I/O                                     | V <sub>DD</sub><br>MIN.<br>Value | External<br>Expansion |  |  |  |  |
|------------------------|------------|-----------------|-------|--------|-------|-----|--------------|--------------------------------------------------------|--------------|--------------------------------------|-----------------------------------------|----------------------------------|-----------------------|--|--|--|--|
|                        |            |                 | 8-bit | 16-bit | Watch | WDT |              |                                                        |              |                                      |                                         |                                  |                       |  |  |  |  |
| For<br>Control         | μPD78078   | 32 K-60 K       | 4ch   | 1ch    | 1ch   | 1ch | 8ch          | —                                                      | 2ch          | 3ch (UART: 1ch)                      | 88 pins                                 | 1.8 V                            | ○                     |  |  |  |  |
|                        | μPD78070A  | —               |       |        |       |     |              |                                                        |              |                                      | 61 pins                                 | 2.7 V                            |                       |  |  |  |  |
|                        | μPD780018  | 48 K-60 K       |       |        |       |     |              |                                                        |              | —                                    | 2chs<br>(time-division<br>3-wire: 1 ch) | 88 pins                          |                       |  |  |  |  |
|                        | μPD78058F  |                 | 2ch   |        |       |     |              |                                                        |              | 2ch                                  | 3ch (UART: 1ch)                         | 69 pins                          |                       |  |  |  |  |
|                        | μPD78054   | 16 K-60 K       |       |        |       |     |              |                                                        |              |                                      |                                         | 2.0 V                            |                       |  |  |  |  |
|                        | μPD780034  | 8 K-32 K        |       | —      | 8ch   |     | —            | 3chs<br>(UART: 1 ch,<br>time-division<br>3-wire: 1 ch) | 51 pins      | 1.8 V                                |                                         |                                  |                       |  |  |  |  |
|                        | μPD780024  |                 | 3ch   | Note   | —     |     | 8ch          | —                                                      | —            |                                      |                                         |                                  |                       |  |  |  |  |
|                        | μPD780964  |                 |       |        |       |     | —            | 8ch                                                    |              | 2ch (UART: 2ch)                      | 47 pins                                 | 2.7 V                            |                       |  |  |  |  |
|                        | μPD780924  |                 |       |        |       |     | 8ch          | —                                                      |              |                                      |                                         |                                  |                       |  |  |  |  |
|                        | μPD78014H  |                 | 2ch   | 1ch    | 1ch   |     |              |                                                        |              | 2ch                                  | 53 pins                                 | 1.8 V                            |                       |  |  |  |  |
|                        | μPD78018F  | 8 K-60 K        |       |        |       |     |              |                                                        |              |                                      |                                         |                                  |                       |  |  |  |  |
|                        | μPD78014   | 8 K-32 K        |       |        |       |     |              |                                                        |              |                                      |                                         | 2.7 V                            |                       |  |  |  |  |
|                        | μPD780001  | 8 K             |       | —      | —     |     |              |                                                        |              | 1ch                                  | 39 pins                                 |                                  | —                     |  |  |  |  |
|                        | μPD78002   | 8 K-16 K        |       |        | 1ch   |     |              |                                                        |              |                                      | 53 pins                                 |                                  | ○                     |  |  |  |  |
|                        | μPD78083   |                 |       |        | —     |     |              |                                                        |              | 1ch (UART: 1ch)                      | 33 pins                                 | 1.8 V                            | —                     |  |  |  |  |
| For FIP<br>driving     | μPD780208  | 32 K-60 K       | 2ch   | 1ch    | 1ch   | 1ch | 8ch          | —                                                      | —            | 2ch                                  | 74 pins                                 | 2.7 V                            | —                     |  |  |  |  |
|                        | μPD78044F  | 16 K-40 K       |       |        |       |     |              |                                                        |              |                                      | 68 pins                                 |                                  |                       |  |  |  |  |
|                        | μPD78024   | 24 K-32 K       |       |        |       |     |              |                                                        |              |                                      | 54 pins                                 |                                  |                       |  |  |  |  |
| For LCD<br>driving     | μPD780308  | 48 K-60 K       | 2ch   | 1ch    | 1ch   | 1ch | 8ch          | —                                                      | —            | 3ch<br>(time-division<br>UART: 1 ch) | 57 pins                                 | 1.8 V                            | —                     |  |  |  |  |
|                        | μPD78064B  | 32 K            |       |        |       |     |              |                                                        |              | 2ch (UART: 1ch)                      |                                         | 2.0 V                            |                       |  |  |  |  |
|                        | μPD78064   | 16 K-32 K       |       |        |       |     |              |                                                        |              |                                      |                                         |                                  |                       |  |  |  |  |
| IEBus<br>support       | μPD78098   | 32 K-60 K       | 2ch   | 1ch    | 1ch   | 1ch | 8ch          | —                                                      | 2ch          | 3ch (UART: 1ch)                      | 69 pins                                 | 2.7 V                            | ○                     |  |  |  |  |
| For LV                 | μPD78P0914 | 32 K            | 6ch   | —      | —     | 1ch | 8ch          | —                                                      | —            | 2ch                                  | 54 pins                                 | 4.5 V                            | ○                     |  |  |  |  |

**Note** 10-bit timer: 1 channel

**OVERVIEW OF FUNCTION**

| Item                          |                                 | μPD78011H                                                                                                                                                                                                                               | μPD78012H | μPD78013H  | μPD78014H |
|-------------------------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------------|-----------|
| Product Name                  |                                 |                                                                                                                                                                                                                                         |           |            |           |
| Internal memory               | ROM                             | 8K bytes                                                                                                                                                                                                                                | 16K bytes | 24K bytes  | 32K bytes |
|                               | High-speed RAM                  | 512 bytes                                                                                                                                                                                                                               |           | 1024 bytes |           |
|                               | Buffer RAM                      | 32 bytes                                                                                                                                                                                                                                |           |            |           |
| Memory space                  |                                 | 64K bytes                                                                                                                                                                                                                               |           |            |           |
| General-purpose registers     |                                 | 8 bits × 32 registers (8 bits × 8 registers × 4 banks)                                                                                                                                                                                  |           |            |           |
| Instruction cycle             |                                 | On-chip instruction execution time cycle modification function                                                                                                                                                                          |           |            |           |
|                               | When main system clock selected | 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)                                                                                                                                                                              |           |            |           |
|                               | When subsystem clock selected   | 122 μs (at 32.768 kHz operation)                                                                                                                                                                                                        |           |            |           |
| Instruction set               |                                 | <ul style="list-style-type: none"><li>• 16-bit operation</li><li>• Multiplication/division (8 bits × 8 bits,16 bits ÷ 8 bits)</li><li>• Bit manipulation (set, reset, test, boolean operation)</li><li>• BCD correction, etc.</li></ul> |           |            |           |
| I/O ports                     |                                 | Total : 53<br><ul style="list-style-type: none"><li>• CMOS input : 2</li><li>• CMOS I/O : 47</li></ul> <ul style="list-style-type: none"><li>• N-channel open-drain I/O (15 V withstand voltage) : 4</li></ul>                          |           |            |           |
| A/D converter                 |                                 | <ul style="list-style-type: none"><li>• 8-bit resolution × 8 channels</li><li>• Operable over a wide power supply voltage range: AV<sub>DD</sub> = 1.8 to 5.5 V</li></ul>                                                               |           |            |           |
| Serial interface              |                                 | <ul style="list-style-type: none"><li>• 3-wire serial I/O/SBI /2-wire serial I/O mode selectable: 1 channel</li><li>• 3-wire serial I/O mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel</li></ul>      |           |            |           |
| Timer                         |                                 | <ul style="list-style-type: none"><li>• 16-bit timer/event counter : 1 channel</li><li>• 8-bit timer/event counter : 2 channels</li><li>• Watch timer : 1 channel</li><li>• Watchdog timer : 1 channel</li></ul>                        |           |            |           |
| Timer output                  |                                 | 3 (14-bit PWM output × 1)                                                                                                                                                                                                               |           |            |           |
| Clock output                  |                                 | 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock: 10.0 MHz operation), 32.768 kHz (at subsystem clock: 32.768 kHz operation)                                                                               |           |            |           |
| Buzzer output                 |                                 | 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock: 10.0 MHz operation)                                                                                                                                                                    |           |            |           |
| Vectored interrupt sources    | Maskable                        | Internal : 8, External : 4                                                                                                                                                                                                              |           |            |           |
|                               | Non-maskable                    | Internal : 1                                                                                                                                                                                                                            |           |            |           |
|                               | Software                        | 1                                                                                                                                                                                                                                       |           |            |           |
| Test input                    |                                 | Internal : 1, External : 1                                                                                                                                                                                                              |           |            |           |
| Supply voltage                |                                 | V <sub>DD</sub> = 1.8 to 5.5 V                                                                                                                                                                                                          |           |            |           |
| Operating ambient temperature |                                 | T <sub>A</sub> = −40 to +85°C                                                                                                                                                                                                           |           |            |           |
| Package                       |                                 | <ul style="list-style-type: none"><li>• 64-pin plastic shrink DIP (750 mil)</li><li>• 64-pin plastic QFP (14 × 14 mm)</li><li>• 64-pin plastic LQFP (12 × 12 mm)</li></ul>                                                              |           |            |           |

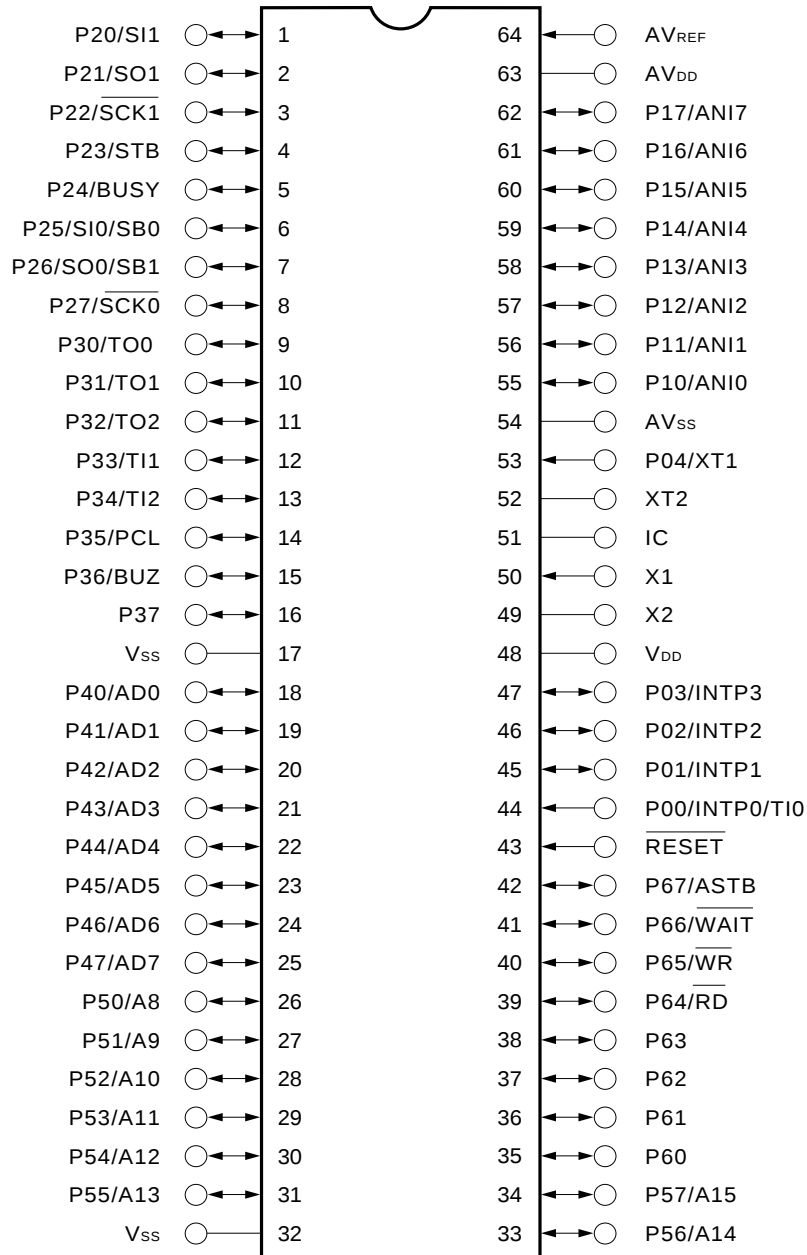
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# 1. PIN CONFIGURATION (Top View)

## • 64-Pin Plastic Shrink DIP (750 mil)

μPD78011HCW-xxx, 78012HCW-xxx, 78013HCW-xxx, 78014HCW-xxx



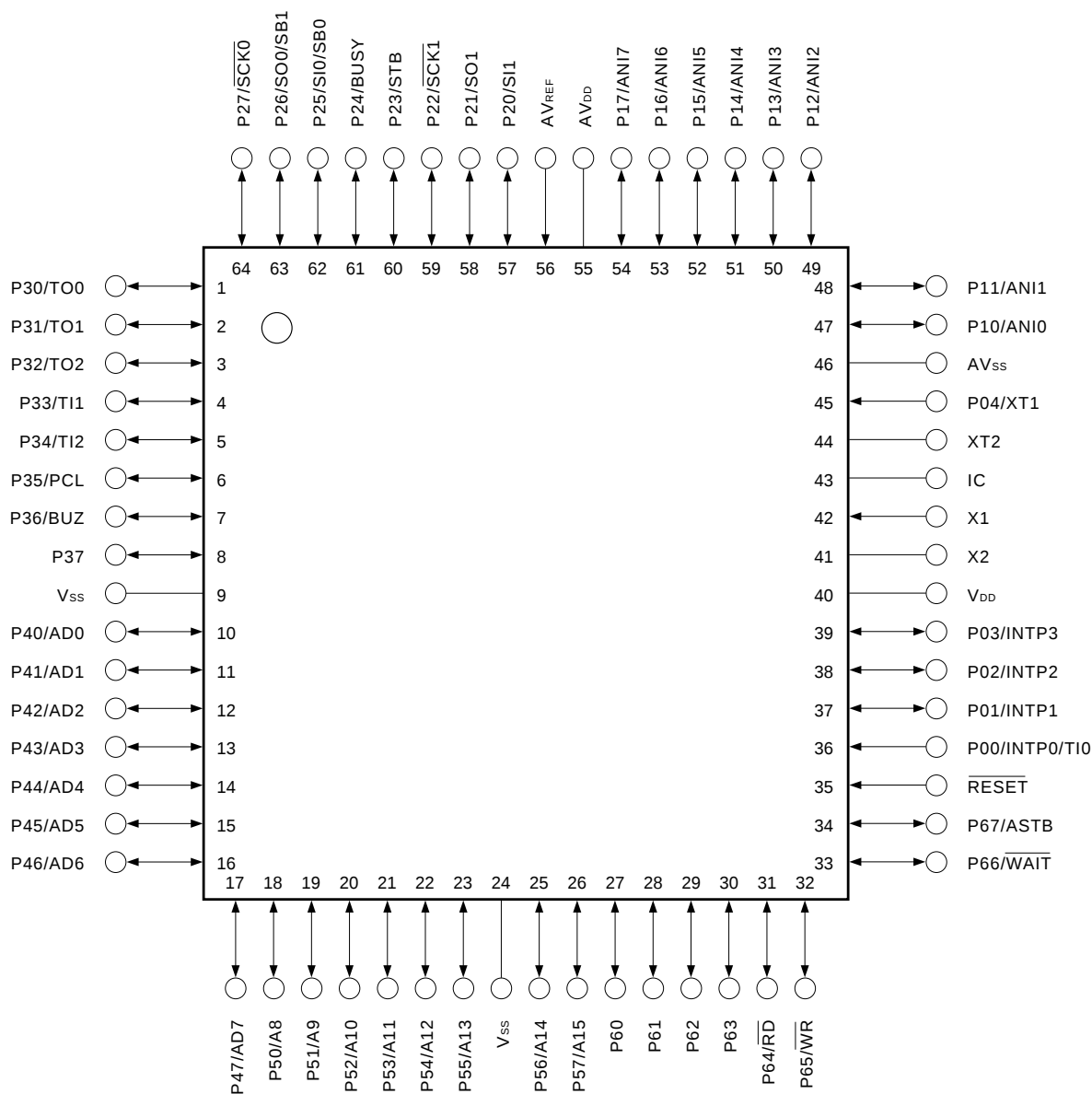
- Cautions**
1. Always connect the IC (Internally Connected) pin to Vss directly.
  2. The AVDD pin is multiplexed with an A/D converter power pin and a port power pin. In an application where the noise generated from the microcontroller must be reduced, connect the AVDD pin to a power supply of the same voltage as VDD.
  3. The AVss pin is multiplexed with an A/D converter ground pin and a port ground pin. In an application where the noise generated from the microcontroller must be reduced, connect AVss pin to a ground line separate from Vss.

• 64-Pin Plastic QFP (14 × 14 mm)

μPD78011HGC-xxx-AB8, 78012HGC-xxx-AB8, 78013HGC-xxx-AB8, 78014HGC-xxx-AB8

• 64-Pin Plastic LQFP (12 × 12 mm)

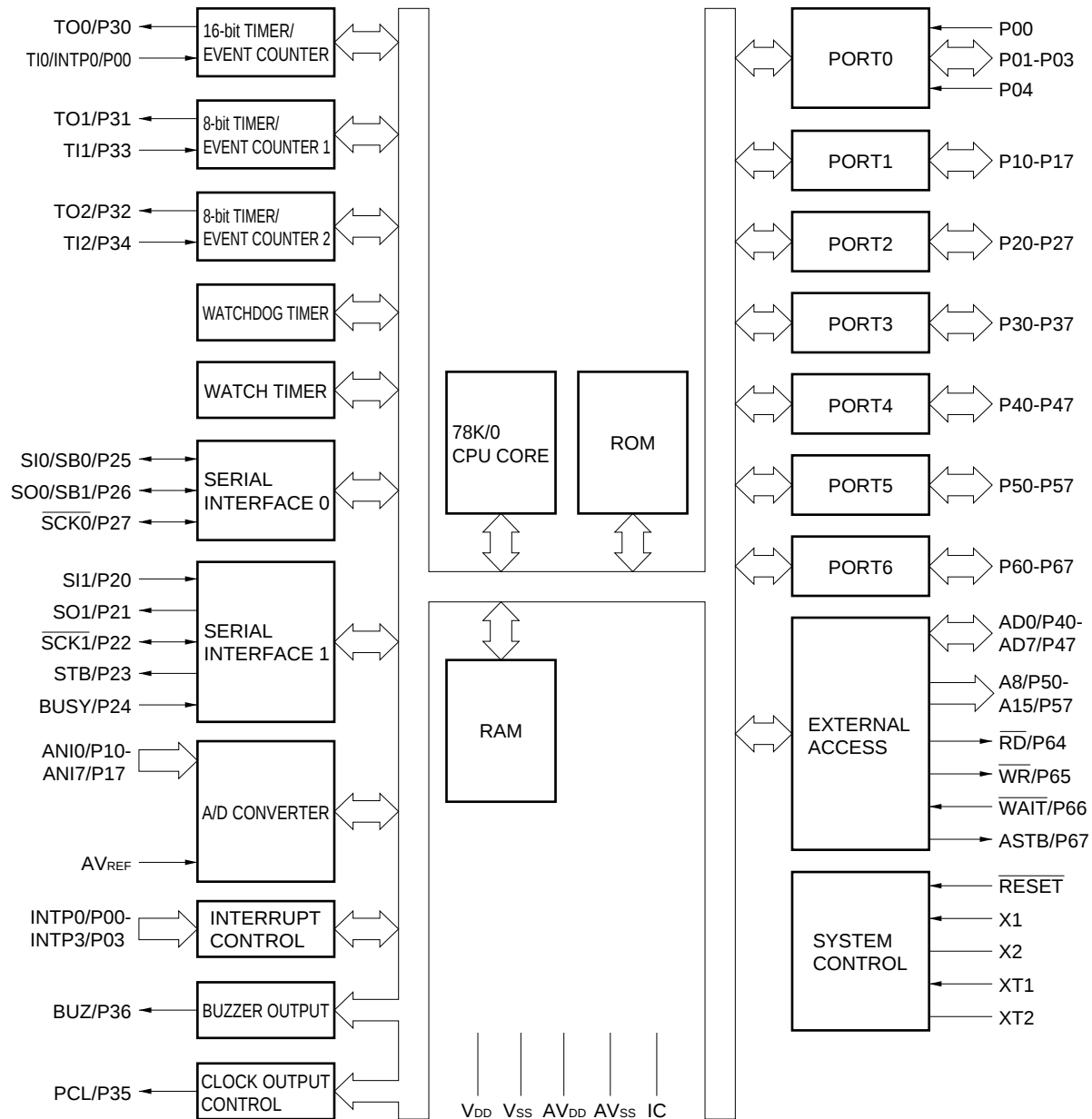
μPD78011HGK-xxx-8A8, 78012HGK-xxx-8A8, 78013HGK-xxx-8A8, 78014HGK-xxx-8A8



- Cautions**
1. Always connect the IC (Internally Connected) pin to V<sub>SS</sub> directly.
  2. The AV<sub>DD</sub> pin is multiplexed with an A/D converter power pin and a port power pin. In an application where the noise generated from the microcontroller must be reduced, connect the AV<sub>DD</sub> pin to a power supply of the same voltage as V<sub>DD</sub>.
  3. The AV<sub>SS</sub> pin is multiplexed with an A/D converter ground pin and a port ground pin. In an application where the noise generated from the microcontroller must be reduced, connect AV<sub>SS</sub> pin to a ground line separate from V<sub>SS</sub>.

|                   |                              |                                                  |                               |
|-------------------|------------------------------|--------------------------------------------------|-------------------------------|
| A8-A15            | : Address Bus                | P60-P67                                          | : Port 6                      |
| AD0-AD7           | : Address/Data Bus           | PCL                                              | : Programmable Clock          |
| ANI0-ANI7         | : Analog Input               | $\overline{\text{RD}}$                           | : Read Strobe                 |
| ASTB              | : Address Strobe             | $\overline{\text{RESET}}$                        | : Reset                       |
| AV <sub>DD</sub>  | : Analog Power Supply        | SB0, SB1                                         | : Serial Bus                  |
| AV <sub>REF</sub> | : Analog Reference Voltage   | $\overline{\text{SCK0}}, \overline{\text{SCK1}}$ | : Serial Clock                |
| AV <sub>SS</sub>  | : Analog Ground              | SI0, SI1                                         | : Serial Input                |
| BUSY              | : Busy                       | SO0, SO1                                         | : Serial Output               |
| BUZ               | : Buzzer Clock               | STB                                              | : Strobe                      |
| IC                | : Internally Connected       | TI0-TI2                                          | : Timer Input                 |
| INTP0-INTP3       | : Interrupt from Peripherals | TO0-TO2                                          | : Timer Output                |
| P00-P04           | : Port 0                     | V <sub>DD</sub>                                  | : Power Supply                |
| P10-P17           | : Port 1                     | V <sub>SS</sub>                                  | : Ground                      |
| P20-P27           | : Port 2                     | $\overline{\text{WAIT}}$                         | : Wait                        |
| P30-P37           | : Port 3                     | $\overline{\text{WR}}$                           | : Write Strobe                |
| P40-P47           | : Port 4                     | X1, X2                                           | : Crystal (Main System Clock) |
| P50-P57           | : Port 5                     | XT1, XT2                                         | : Crystal (Subsystem Clock)   |

## 2. BLOCK DIAGRAM



**Remark** Internal ROM & RAM capacity varies depending on the product.

### 3. PIN FUNCTIONS

#### 3.1 PORT PINS (1/2)

| Pin Name          | I/O              | Function                                                                                                                                                                                                                             |                                                                                                                          | On Reset | Dual-<br>Function Pin    |
|-------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|----------|--------------------------|
| P00               | Input            | Port 0<br>5-bit I/O port                                                                                                                                                                                                             | Input only                                                                                                               | Input    | INTP0/TI0                |
| P01               | Input/<br>output |                                                                                                                                                                                                                                      | Input/output can be specified bit-wise.<br>When used as an input port, on-chip pull-up resistor can be used by software. | Input    | INTP1                    |
| P02               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | INTP2                    |
| P03               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | INTP3                    |
| P04 <b>Note 1</b> | Input            |                                                                                                                                                                                                                                      | Input only                                                                                                               | Input    | XT1                      |
| P10 to P17        | Input/<br>output | Port 1<br>8-bit input/output port.<br>Input/output can be specified bit-wise.<br>When used as an input port, on-chip pull-up resistor can be used by software. <b>Note 2</b>                                                         |                                                                                                                          | Input    | ANI0 to ANI7             |
| P20               | Input/<br>output | Port 2<br>8-bit input/output port.<br>Input/output can be specified bit-wise.<br>When used as an input port, on-chip pull-up resistor can be used by software.                                                                       |                                                                                                                          | Input    | SI1                      |
| P21               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | SO1                      |
| P22               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | $\overline{\text{SCK1}}$ |
| P23               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | STB                      |
| P24               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | BUSY                     |
| P25               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | SI0/SB0                  |
| P26               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | SO0/SB1                  |
| P27               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | $\overline{\text{SCK0}}$ |
| P30               | Input/<br>output | Port 3<br>8-bit input/output port.<br>Input/output can be specified in 1-bit units.<br>When used as an input port, on-chip pull-up resistor can be used by software.                                                                 |                                                                                                                          | Input    | TO0                      |
| P31               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | TO1                      |
| P32               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | TO2                      |
| P33               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | TI1                      |
| P34               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | TI2                      |
| P35               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | PCL                      |
| P36               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | BUZ                      |
| P37               |                  |                                                                                                                                                                                                                                      |                                                                                                                          |          | —                        |
| P40 to P47        | Input/<br>output | Port 4<br>8-bit input/output port.<br>Input/output can be specified in 8-bit unit.<br>When used as an input port, on-chip pull-up resistor can be used by software.<br>Test input flag (KRIF) is set to 1 by falling edge detection. |                                                                                                                          | Input    | AD0 to AD7               |

**Notes 1.** When using the P04/XT1 pin as an input port pin, set bit 6 (FRC) of the processor clock control register (PCC) to 1 (do not use the internal feedback resistor of the subsystem clock oscillation circuit).

**2.** When using the P10/ANI0 through P17/ANI7 pins as the analog input pins of the A/D converter, the internal pull-up resistors are automatically not used.

## 3.1 PORT PINS (2/2)

| Pin Name   | I/O          | Function                                                                                                                                                                                      |                                                                                                                                | On Reset | Dual-Function Pin        |
|------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------|--------------------------|
| P50 to P57 | Input/output | Port 5<br>8-bit input/output port.<br>LED can be driven directly.<br>Input/output can be specified bit-wise.<br>When used as an input port, on-chip pull-up resistor can be used by software. |                                                                                                                                | Input    | A8 to A15                |
| P60        | Input/output | Port 6<br>8-bit input/output port.<br>Input/output can be specified bit-wise.                                                                                                                 | N-ch open-drain input/output port.<br>On-chip pull-up resistor can be specified by mask option.<br>LED can be driven directly. | Input    | ——                       |
| P61        |              |                                                                                                                                                                                               |                                                                                                                                |          |                          |
| P62        |              |                                                                                                                                                                                               |                                                                                                                                |          |                          |
| P63        |              |                                                                                                                                                                                               |                                                                                                                                |          |                          |
| P64        |              | When used as an input port, on-chip pull-up resistor can be used by software.                                                                                                                 |                                                                                                                                |          | $\overline{\text{RD}}$   |
| P65        |              |                                                                                                                                                                                               |                                                                                                                                |          | $\overline{\text{WR}}$   |
| P66        |              |                                                                                                                                                                                               |                                                                                                                                |          | $\overline{\text{WAIT}}$ |
| P67        |              |                                                                                                                                                                                               |                                                                                                                                |          | ASTB                     |

**Caution** Do not manipulate the pins multiplexed with a port pin as follows during A/D conversion; otherwise, the rated total error during A/D conversion may not be satisfied.

<1> Rewriting the contents of the output latch when the pin is used as an output port pin.

<2> Changing the output level of the pin used as an output pin even when the pin is not used as a port pin.

## 3.2 OTHER PORTS (1/2)

| Pin Name | I/O          | Function                                                                                                                                         |  | On Reset | Dual-Function Pin |
|----------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------|--|----------|-------------------|
| INTP0    | Input        | External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified. |  | Input    | P00/TI0           |
| INTP1    |              |                                                                                                                                                  |  |          | P01               |
| INTP2    |              |                                                                                                                                                  |  |          | P02               |
| INTP3    |              | Falling edge detection external interrupt request input.                                                                                         |  |          | P03               |
| SI0      | Input        | Serial interface serial data input.                                                                                                              |  | Input    | P25/SB0           |
| SI1      |              |                                                                                                                                                  |  |          | P20               |
| SO0      | Output       | Serial interface serial data output.                                                                                                             |  | Input    | P26/SB1           |
| SO1      |              |                                                                                                                                                  |  |          | P21               |
| SB0      | Input/output | Serial interface serial data input/output.                                                                                                       |  | Input    | P25/SI0           |
| SB1      |              |                                                                                                                                                  |  |          | P26/SO0           |
| SCK0     | Input/output | Serial interface serial clock input/output.                                                                                                      |  | Input    | P27               |
| SCK1     |              |                                                                                                                                                  |  |          | P22               |
| STB      | Output       | Serial interface automatic transmit/receive strobe output.                                                                                       |  | Input    | P23               |
| BUSY     | Input        | Serial interface automatic transmit/receive busy input.                                                                                          |  | Input    | P24               |

### 3.2 OTHER PORTS (2/2)

| Pin Name                  | I/O           | Function                                                                                                   | On Reset | Dual-Function Pin |
|---------------------------|---------------|------------------------------------------------------------------------------------------------------------|----------|-------------------|
| TI0                       | Input         | External count clock input to 16-bit timer (TM0).                                                          | Input    | P00/INTP0         |
| TI1                       |               | External count clock input to 8-bit timer (TM1).                                                           |          | P33               |
| TI2                       |               | External count clock input to 8-bit timer (TM2).                                                           |          | P34               |
| TO0                       | Output        | 16-bit timer (TM0) output (multiplexed with 14-bit PWM output).                                            | Input    | P30               |
| TO1                       |               | 8-bit timer (TM1) output.                                                                                  |          | P31               |
| TO2                       |               | 8-bit timer (TM2) output.                                                                                  |          | P32               |
| PCL                       | Output        | Clock output (for main system clock, subsystem clock trimming).                                            | Input    | P35               |
| BUZ                       | Output        | Buzzer output.                                                                                             | Input    | P36               |
| AD0 to AD7                | Input /output | Low-order address/data bus at external memory expansion.                                                   | Input    | P40 to P47        |
| A8 to A15                 | Output        | High-order address bus at external memory expansion.                                                       | Input    | P50 to P57        |
| $\overline{\text{RD}}$    | Output        | External memory read operation strobe signal output.                                                       | Input    | P64               |
| $\overline{\text{WR}}$    |               | External memory write operation strobe signal output.                                                      |          | P65               |
| $\overline{\text{WAIT}}$  | Input         | Wait insertion at external memory access.                                                                  | Input    | P66               |
| ASTB                      | Output        | Strobe output which latches the address information output at port 4 and port 5 to access external memory. | Input    | P67               |
| ANI0 to ANI7              | Input         | A/D converter analog input.                                                                                | Input    | P10 to P17        |
| AVREF                     | Input         | A/D converter reference voltage input.                                                                     | —        | —                 |
| AVDD                      | —             | A/D converter analog power supply (multiplexed with a port power pin).                                     | —        | —                 |
| AVSS                      | —             | A/D converter ground potential (multiplexed with a port ground pin).                                       | —        | —                 |
| $\overline{\text{RESET}}$ | Input         | System reset input.                                                                                        | —        | —                 |
| X1                        | Input         | Main system clock oscillation crystal connection.                                                          | —        | —                 |
| X2                        | —             |                                                                                                            | —        | —                 |
| XT1                       | Input         | Subsystem clock oscillation crystal connection.                                                            | Input    | P04               |
| XT2                       | —             |                                                                                                            | —        | —                 |
| VDD                       | —             | Positive power supply (except port pins).                                                                  | —        | —                 |
| VSS                       | —             | Ground potential (except port pins).                                                                       | —        | —                 |
| IC                        | —             | Internal connection. Connected to VSS directly.                                                            | —        | —                 |

- Cautions**
1. The AVDD pin is multiplexed with an A/D converter power pin and a port power pin. In an application where the noise generated from the microcontroller must be reduced, connect the AVDD pin to a power supply of the same voltage as VDD.
  2. The AVSS pin is multiplexed with an A/D converter ground pin and a port ground pin. In an application where the noise generated from the microcontroller must be reduced, connect AVSS pin to a ground line separate from VSS.

### 3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

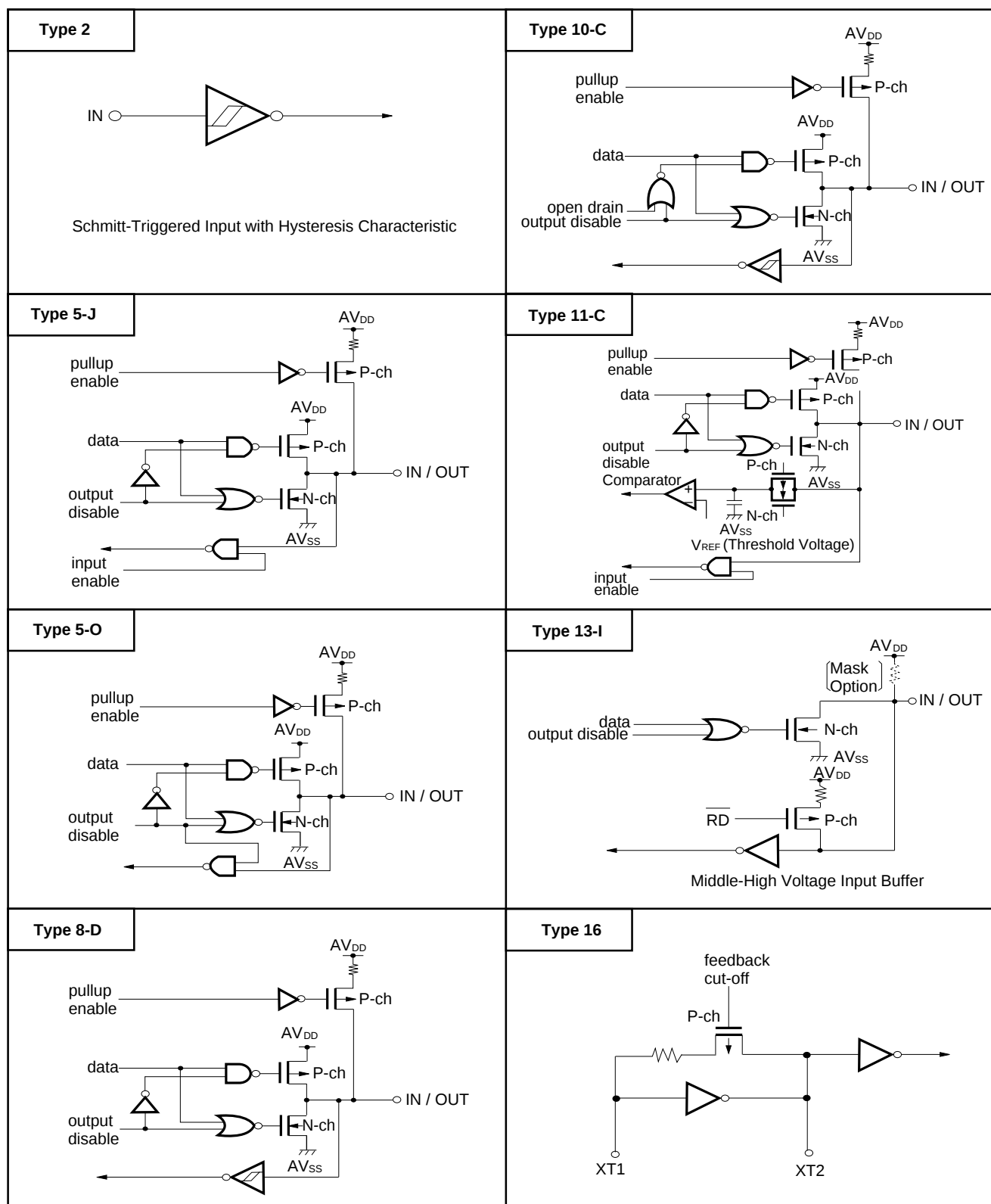
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Figure 3-1.

**Table 3-1. Input/Output Circuit Type of Each Pin**

| Pin Name                      | Input/output<br>Circuit Type | I/O          | Recommended Connection when Not Used                                        |                                                                            |
|-------------------------------|------------------------------|--------------|-----------------------------------------------------------------------------|----------------------------------------------------------------------------|
| P00/INTP0/TI0                 | 2                            | Input        | Connected to V <sub>SS</sub> .                                              |                                                                            |
| P01/INTP1                     | 8-D                          | Input/output | Individually connected to V <sub>SS</sub> via resistor.                     |                                                                            |
| P02/INTP2                     |                              |              |                                                                             |                                                                            |
| P03/INTP3                     |                              |              |                                                                             |                                                                            |
| P04/XT1                       | 16                           | Input        | Connected to V <sub>DD</sub> or V <sub>SS</sub> .                           |                                                                            |
| P10/ANI0 to P17/ANI7          | 11-C                         | Input/output | Individually connected to V <sub>DD</sub> or V <sub>SS</sub> via resisitor. |                                                                            |
| P20/SI1                       | 8-D                          |              |                                                                             |                                                                            |
| P21/SO1                       | 5-J                          |              |                                                                             |                                                                            |
| P22/ $\overline{\text{SCK1}}$ | 8-D                          |              |                                                                             |                                                                            |
| P23/STB                       | 5-J                          |              |                                                                             |                                                                            |
| P24/BUSY                      | 8-D                          |              |                                                                             |                                                                            |
| P25/SI0/SB0                   | 10-C                         |              |                                                                             |                                                                            |
| P26/SO0/SB1                   |                              |              |                                                                             |                                                                            |
| P27/ $\overline{\text{SCK0}}$ |                              |              |                                                                             |                                                                            |
| P30/TO0                       | 5-J                          |              |                                                                             |                                                                            |
| P31/TO1                       |                              |              |                                                                             |                                                                            |
| P32/TO2                       |                              |              |                                                                             |                                                                            |
| P33/TI1                       | 8-D                          |              |                                                                             |                                                                            |
| P34/TI2                       |                              |              |                                                                             |                                                                            |
| P35/PCL                       | 5-J                          |              |                                                                             |                                                                            |
| P36/BUZ                       |                              |              |                                                                             |                                                                            |
| P37                           |                              |              |                                                                             |                                                                            |
| P40/AD0 to P47/AD7            | 5-O                          |              |                                                                             | Individually connected to V <sub>DD</sub> via resistor.                    |
| P50/A8 to P57/A15             | 5-J                          |              |                                                                             | Individually connected to V <sub>DD</sub> or V <sub>SS</sub> via resistor. |
| P60 to P63                    | 13-I                         |              |                                                                             | Individually connected to V <sub>DD</sub> via resistor.                    |
| P64/ $\overline{\text{RD}}$   | 5-J                          |              | Individually connected to V <sub>DD</sub> or V <sub>SS</sub> via resistor.  |                                                                            |
| P65/ $\overline{\text{WR}}$   |                              |              |                                                                             |                                                                            |
| P66/ $\overline{\text{WAIT}}$ |                              |              |                                                                             |                                                                            |
| P67/ASTB                      |                              |              |                                                                             |                                                                            |
| $\overline{\text{RESET}}$     | 2                            | Input        | —                                                                           |                                                                            |
| XT2                           | 16                           | —            | Leave open.                                                                 |                                                                            |
| AV <sub>REF</sub>             | —                            |              | Connected to V <sub>SS</sub> .                                              |                                                                            |
| AV <sub>DD</sub>              |                              |              | Connected to V <sub>DD</sub> .                                              |                                                                            |
| AV <sub>SS</sub>              |                              |              | Connected to V <sub>SS</sub> .                                              |                                                                            |
| IC                            |                              |              | Connected to V <sub>SS</sub> directly.                                      |                                                                            |

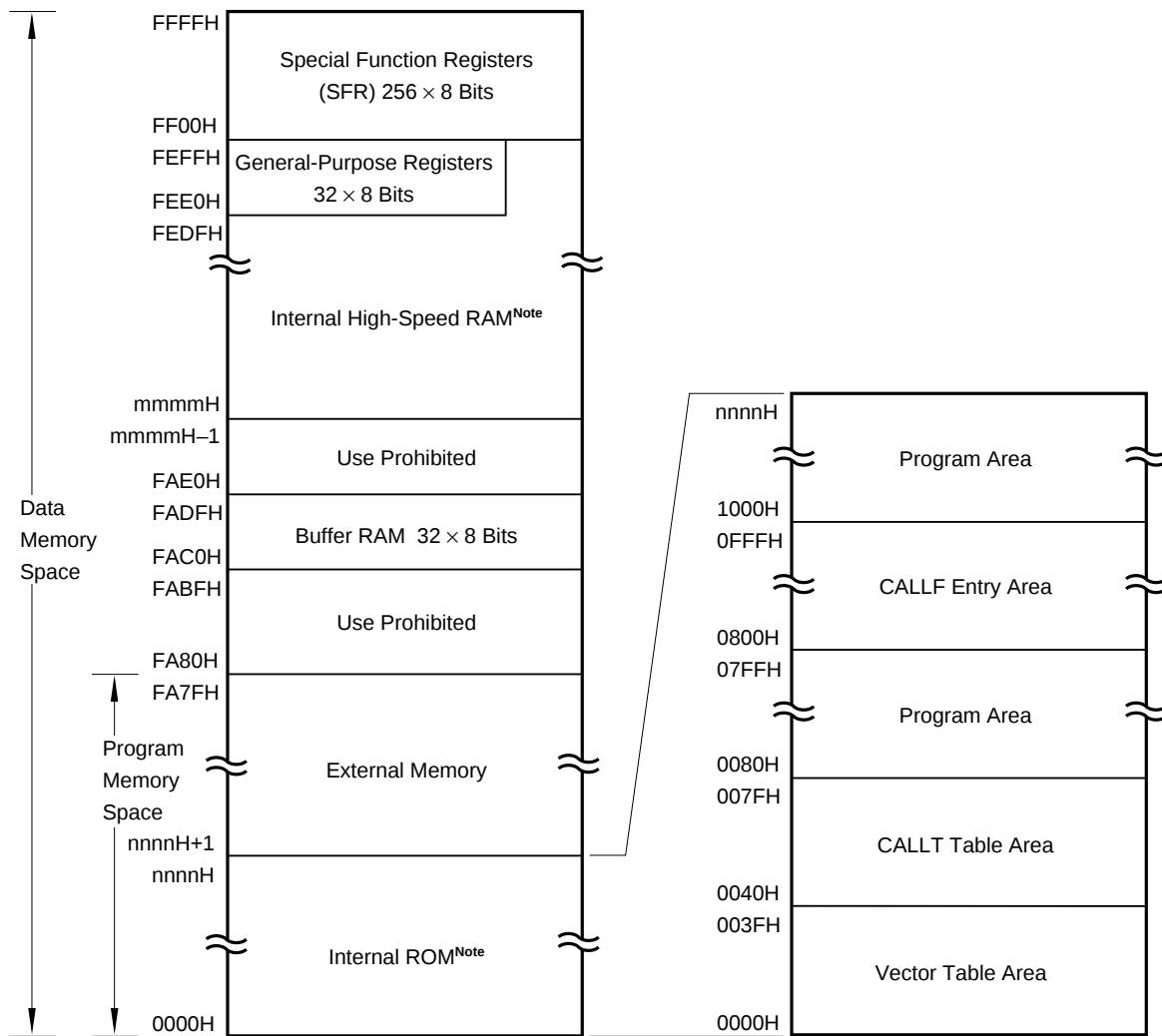
Figure 3-1. Pin Input/Output Circuits



#### 4. MEMORY SPACE

The memory map of the μPD78011H, 78012H, 78013H, 78014H is shown in Figure 4-1.

Figure 4-1. Memory Map



**Note** Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

| Product Name | Internal ROM End Address<br>nnnnH | Internal High-Speed RAM<br>Start Address<br>mmmmH |
|--------------|-----------------------------------|---------------------------------------------------|
| μPD78011H    | 1FFFH                             | FD00H                                             |
| μPD78012H    | 3FFFH                             |                                                   |
| μPD78013H    | 5FFFH                             | FB00H                                             |
| μPD78014H    | 7FFFH                             |                                                   |

## 5. PERIPHERAL HARDWARE FUNCTION FEATURES

### 5.1 PORTS

The I/O port has the following three types

|                                                                    |      |
|--------------------------------------------------------------------|------|
| • CMOS input (P00, P04)                                            | : 2  |
| • CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67)     | : 47 |
| • N-ch open-drain input/output(15V withstand voltage) (P60 to P63) | : 4  |
| <hr/>                                                              |      |
| Total                                                              | : 53 |

**Table 5-1. Functions of Ports**

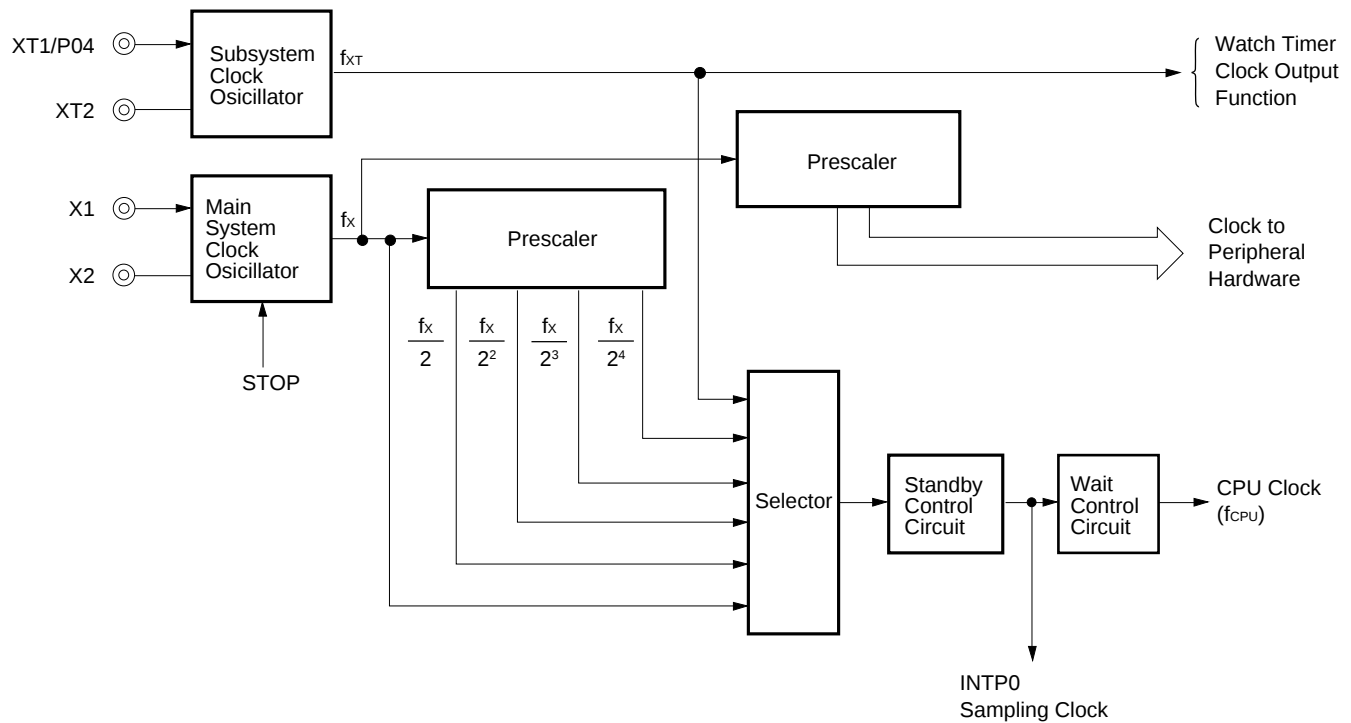
| Port Name | Pin Name   | Function                                                                                                                                                                                                    |
|-----------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Port 0    | P00, P04   | Dedicated Input port                                                                                                                                                                                        |
|           | P01 to P03 | Input/output ports. Input/output can be specified bit-wise.<br>When used as an input port, pull-up resistor can be used by software.                                                                        |
| Port 1    | P10 to P17 | Input/output ports. Input/output can be specified bit-wise.<br>When used as an input port, pull-up resistor can be used by software.                                                                        |
| Port 2    | P20 to P27 | Input/output ports. Input/output can be specified bit-wise.<br>When used as an input port, pull-up resistor can be used by software.                                                                        |
| Port 3    | P30 to P37 | Input/output ports. Input/output can be specified bit-wise.<br>When used as an input port, pull-up resistor can be used by software.                                                                        |
| Port 4    | P40 to P47 | Input/output ports. Input/output can be specified in 8-bit units.<br>When used as an input port, pull-up resistor can be used by software.<br>Test input flag (KRIF) is set to 1 by falling edge detection. |
| Port 5    | P50 to P57 | Input/output ports. Input/output can be specified bit-wise.<br>When used as an input port, pull-up resistor can be used by software.<br>LED can be driven directly.                                         |
| Port 6    | P60 to P63 | N-ch open-drain input/output port. Input/output can be specified bit-wise.<br>On-chip pull-up resistor can be specified by mask option.<br>LED can be driven directly.                                      |
|           | P64 to P67 | Input/output ports. Input/output can be specified bit-wise.<br>When used as an input port, pull-up resistor can be used by software.                                                                        |

## 5.2 CLOCK GENERATOR

There are two types of clock generator: main system clock and subsystem clock.  
The instruction execution time can be changed.

- 0.4μs/0.8μs/1.6μs/3.2μs/6.4μs (Main system clock: at 10.0 MHz operation)
- 122μs (Subsystem clock: at 32.768 KHz operation)

Figure 5-1. Clock Generator Block Diagram



### 5.3 TIMER/EVENT COUNTER

The following five channels are incorporated in the timer/event counter.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

**Table 5-2. Types and Functions of Timer/Event Counter**

|           |                          | 16-bit Timer/Event Counter | 8-bit Timer/Event Counter | Watch Timer | Watchdog Timer |
|-----------|--------------------------|----------------------------|---------------------------|-------------|----------------|
| Type      | Interval timer           | 1 channel                  | 2 channels                | 1 channel   | 1 channel      |
|           | Externanal event counter | 1 channel                  | 2 channels                | –           | –              |
| Functions | Timer output             | 1 output                   | 2 outputs                 | –           | –              |
|           | PWM output               | 1 output                   | –                         | –           | –              |
|           | Pulse width mesurement   | 1 input                    | –                         | –           | –              |
|           | Sqare wave output        | 1 output                   | 2 outputs                 | –           | –              |
|           | Interrupt request        | 2                          | 2                         | 1           | 1              |
|           | Test input               | –                          | –                         | 1           | –              |

**Figure 5-2. 16-bit Timer/Enent Counter Block Diagram**

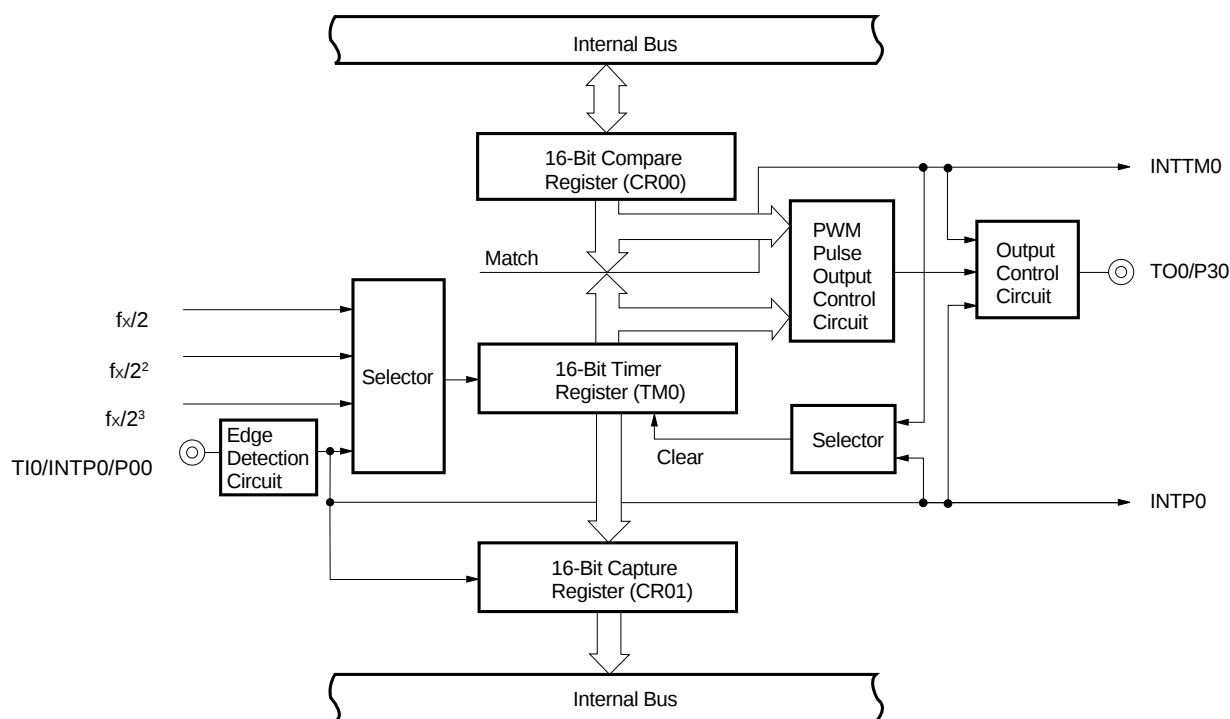


Figure 5-3. 8-bit Timer/Event Counter Block Diagram

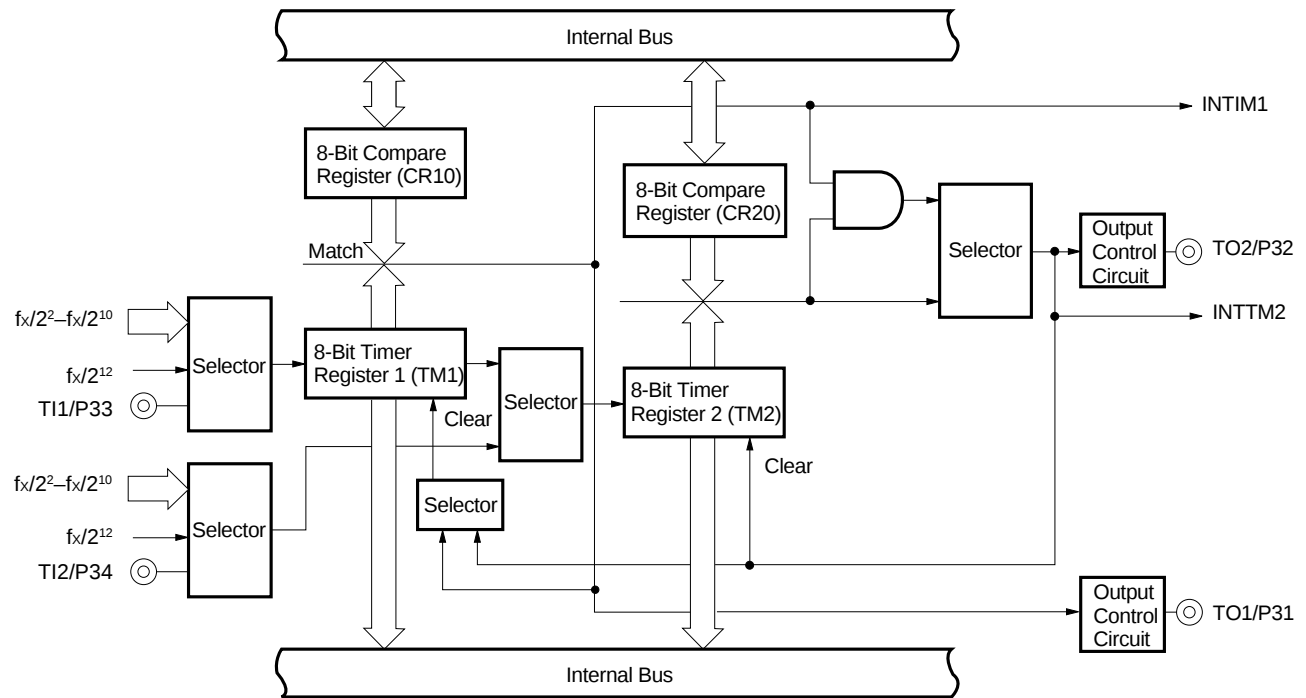


Figure 5-4. Watch Timer Block Diagram

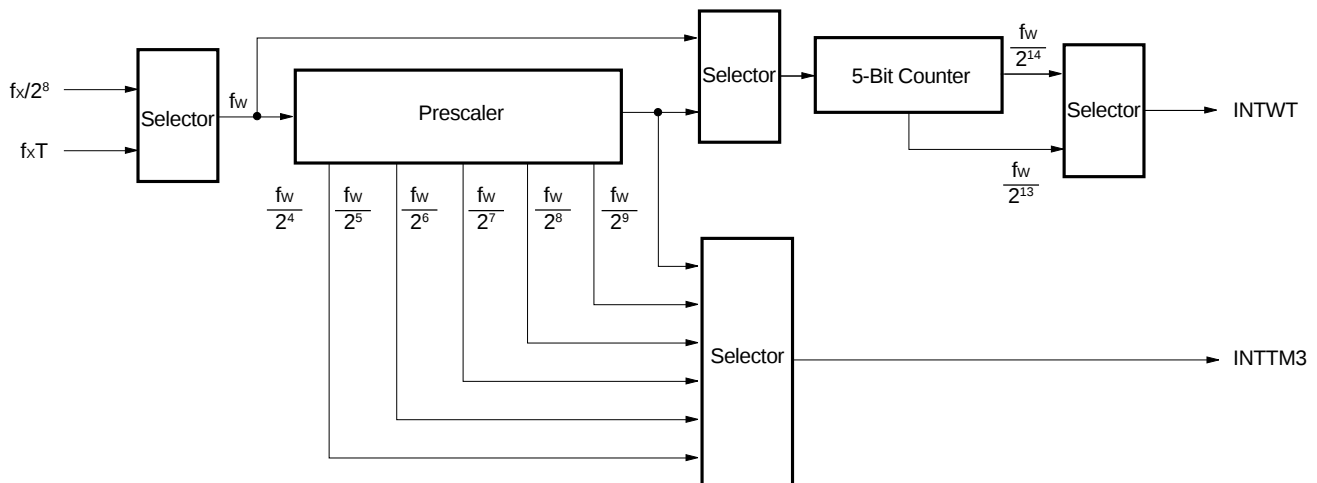
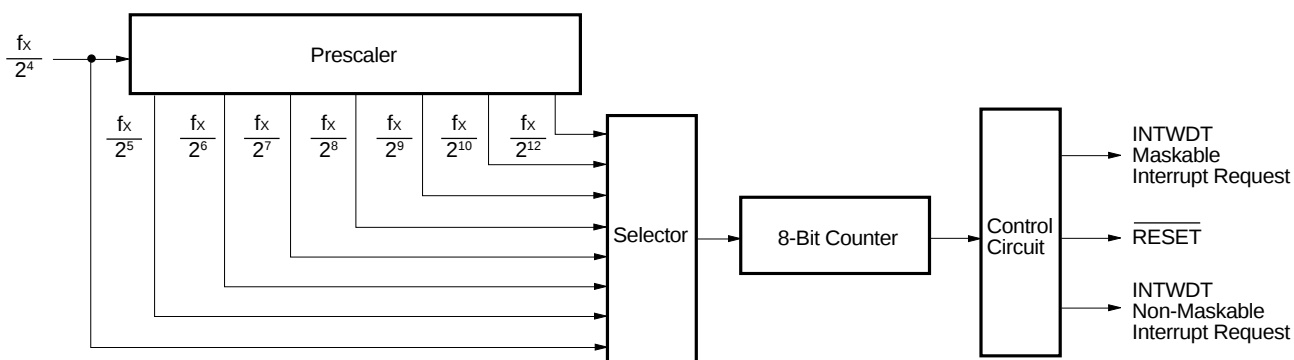


Figure 5-5. Watchdog Timer Block Diagram

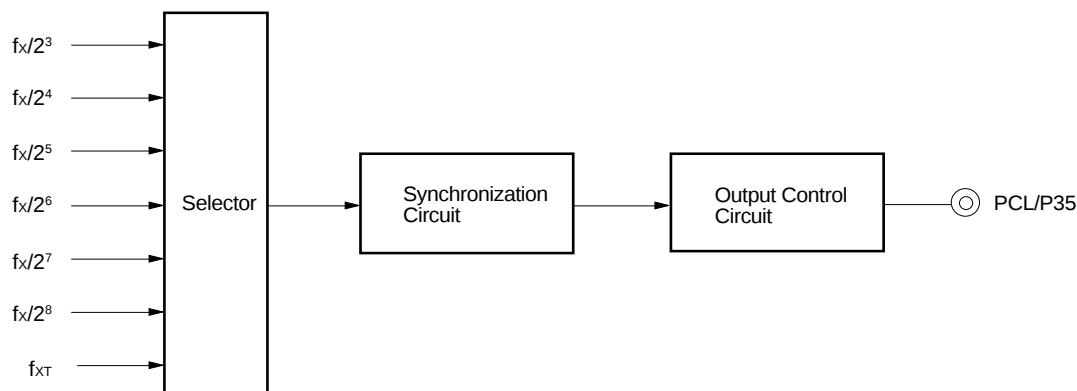


#### 5.4 CLOCK OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Figure 5-6. Clock Output Control Block Diagram

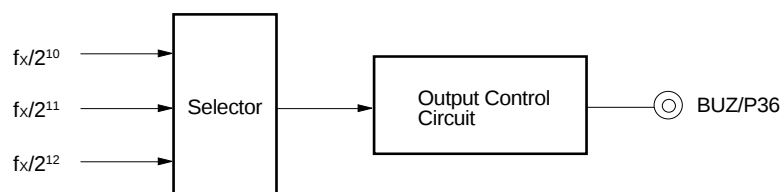


#### 5.5 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Figure 5-7. Buzzer Output Control Block Diagram

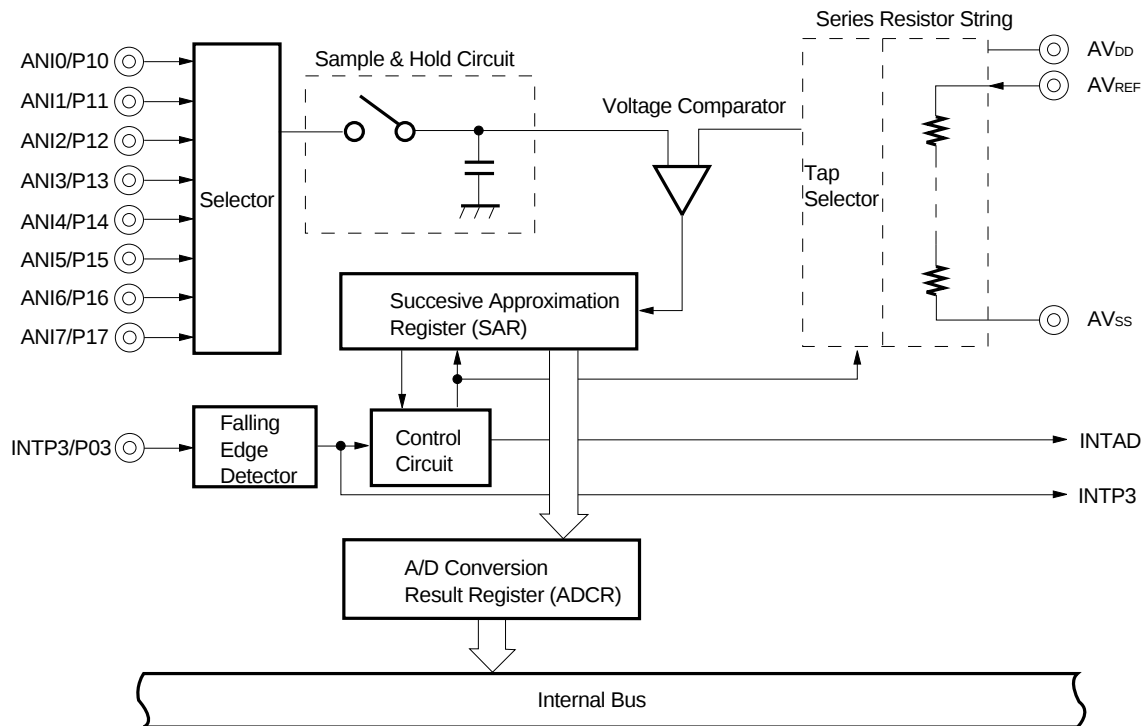


## 5.6 A/D CONVERTER

The A/D converter has on-chip eight 8-bit resolution channels.  
There are the following two method to start A/D conversion.

- Hardware starting
- Software starting

Figure 5-8. A/D Converter Block Diagram



**Caution** Do not manipulate the pins multiplexed with a port pin (refer to 3.1 PORT PINS) during A/D conversion; otherwise, the rated total error during A/D conversion may not be satisfied.

<1> Rewriting the contents of the output latch when the pin is used as an output port pin.

<2> Changing the output level of the pin used as an output pin even when the pin is not used as a port pin.

## 5.7 SERIAL INTERFACES

There are two on-chip clocked serial interfaces as follows.

- Serial Interface channel 0
- Serial Interface channel 1

**Table 5-3. Type and Function of Serial Interface**

| Function                                                             | Serial Interface Channel 0   | Serial Interface Channel 1   |
|----------------------------------------------------------------------|------------------------------|------------------------------|
| 3-wire serial I/O mode                                               | O (MSB/LSB-first switchable) | O (MSB/LSB-first switchable) |
| 3-wire serial I/O mode with automatic data transmit/receive function | —                            | O (MSB/LSB-first switchable) |
| SBI (Serial Bus Interface) mode                                      | O (MSB-first)                | —                            |
| 2-wire serial I/O mode                                               | O (MSB-first)                | —                            |

**Figure 5-9. Serial Interface Channel 0 Block Diagram**

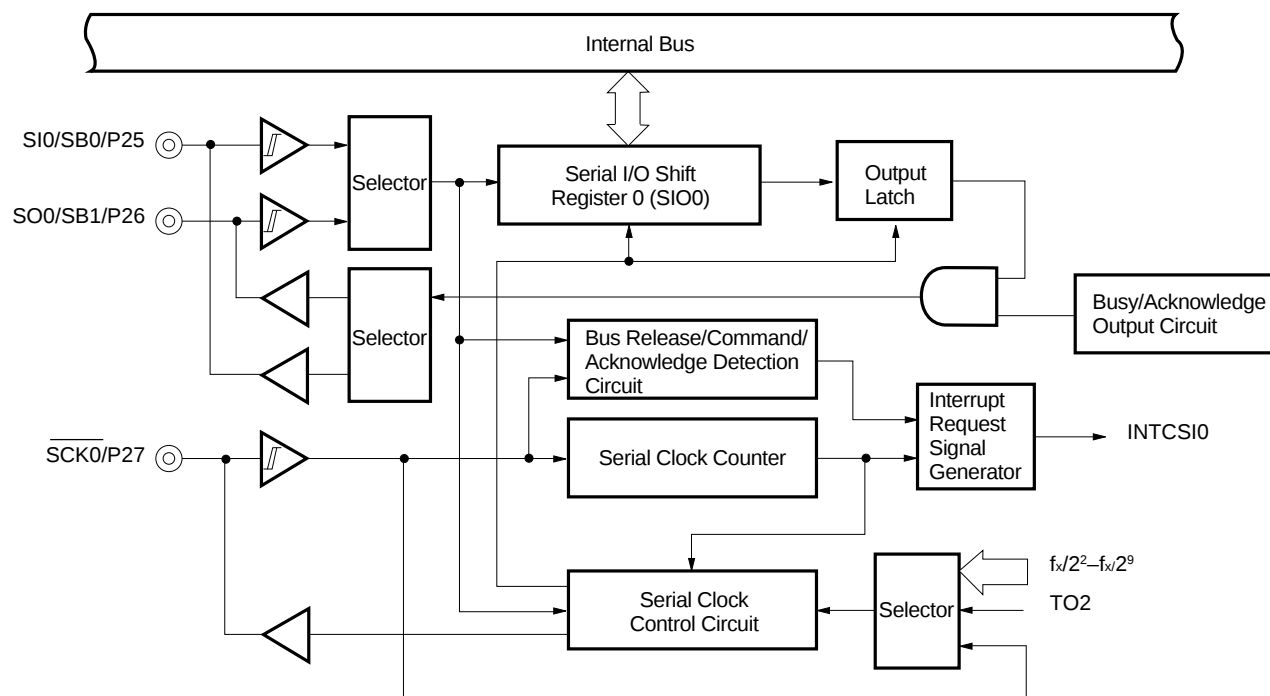
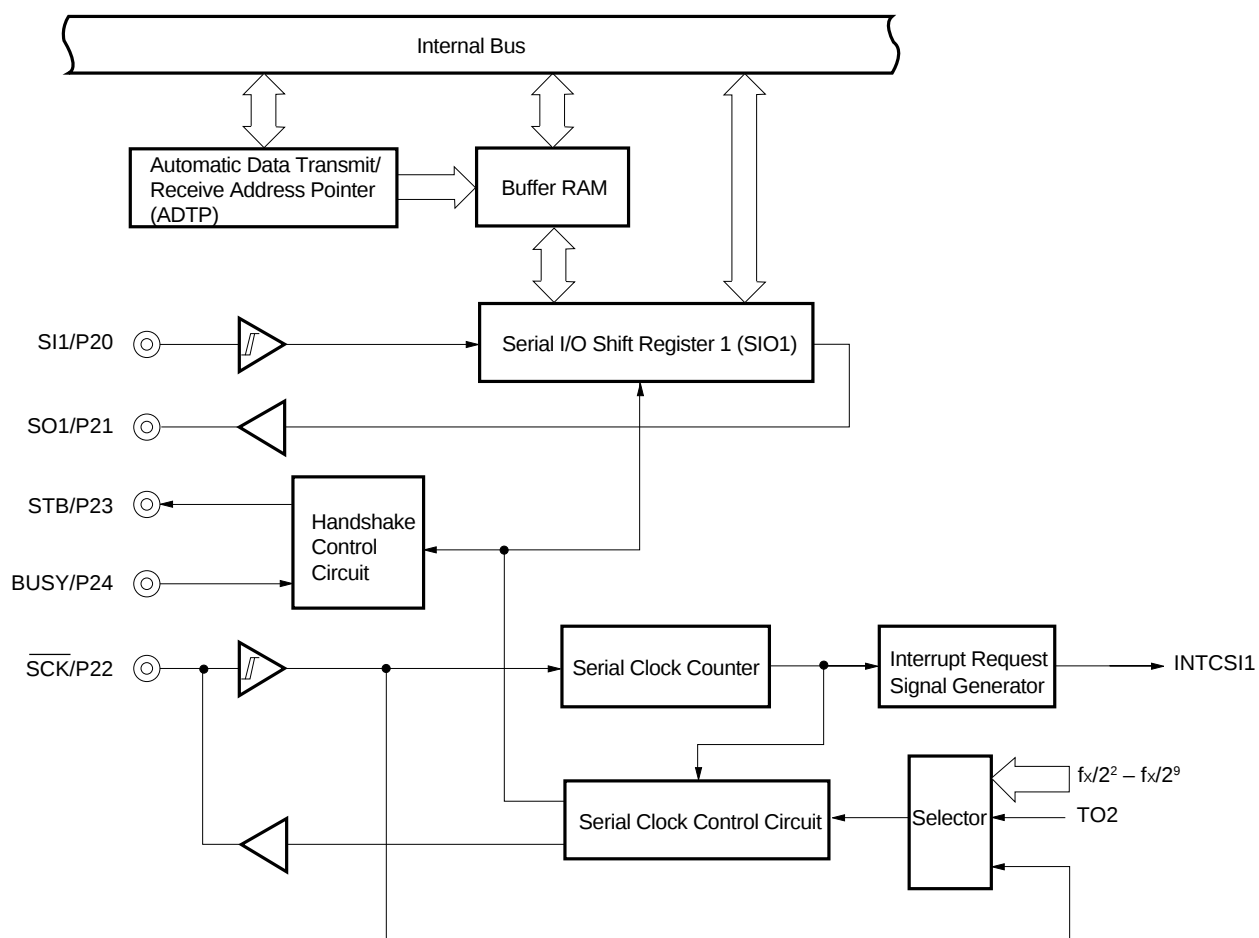


Figure 5-10. Serial Interface Channel 1 Block Diagram



## 6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

### 6.1 INTERRUPT FUNCTIONS

There are the 14 interrupt sources of 3 different kind as shown below.

- Non-maskable : 1
- Maskable : 12
- Software : 1

**Table 6-1. Interrupt Source List**

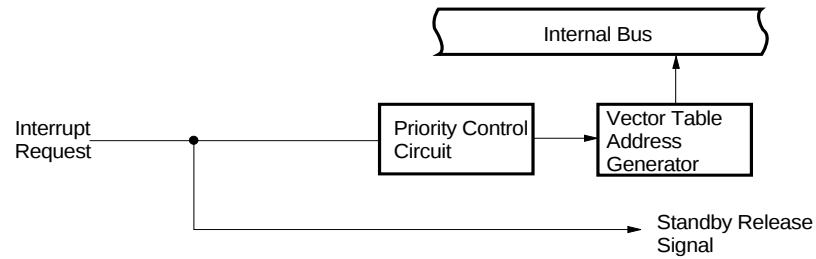
| Interrupt Type | Default Priority <b>Note 1</b> | Interrupt Source |                                                               | Internal/ External | Vector Table Address | Basic Configuratin Type <b>Note 2</b> |
|----------------|--------------------------------|------------------|---------------------------------------------------------------|--------------------|----------------------|---------------------------------------|
|                |                                | Name             | Trigger                                                       |                    |                      |                                       |
| Non-maskable   | —                              | INTWDT           | Watchdog timer overflow (with watchdog timer mode 1 selected) | Internal           | 0004H                | (A)                                   |
| Maskable       | 0                              | INTWDT           | Watchdog timer overflow (with interval timer mode selected)   |                    |                      | (B)                                   |
|                | 1                              | INTP0            | Pin input edge detection                                      | External           | 0006H                | (C)                                   |
|                | 2                              | INTP1            |                                                               |                    | 0008H                | (D)                                   |
|                | 3                              | INTP2            |                                                               |                    | 000AH                |                                       |
|                | 4                              | INTP3            |                                                               |                    | 000CH                |                                       |
|                | 5                              | INTCSI0          | Serial interface channel 0 transfer end                       | Internal           | 000EH                | (B)                                   |
|                | 6                              | INTCSI1          | Serial interface channel 1 transfer end                       |                    | 0010H                |                                       |
|                | 7                              | INTTM3           | Reference time interval signal from watch timer               |                    | 0012H                |                                       |
|                | 8                              | INTTM0           | 16 bit timer/event counter match signal generation            |                    | 0014H                |                                       |
|                | 9                              | INTTM1           | 8-bit timer/event counter 1 match signal generation           |                    | 0016H                |                                       |
|                | 10                             | INTTM2           | 8-bit timer/event counter 2 match signal generation           |                    | 0018H                |                                       |
|                | 11                             | INTAD            | A/D converter conversion end                                  |                    | 001AH                |                                       |
| Software       | —                              | BRK              | BRK instruction execution                                     | —                  | 003EH                | (E)                                   |

**Notes 1.** The default priority is the priority applicable when more than one maskable interrupt is generated. 0 is the highest priority and 11, the lowest.

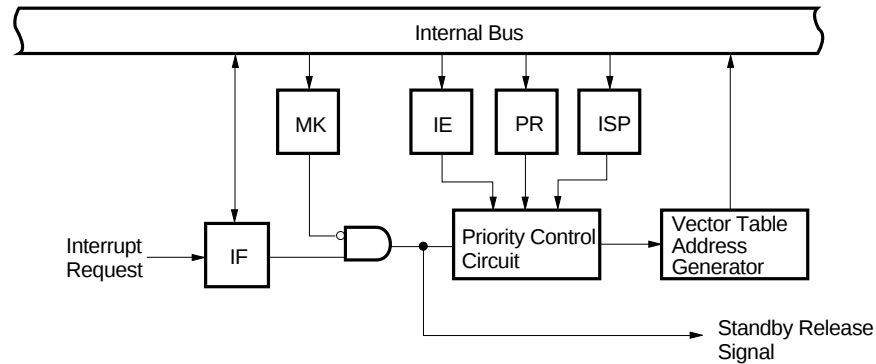
**2.** Basic configuration types (A) to (E) correspond to (A) to (E) on the next page.

Figure 6-1. Basic Interrupt Function Configuration (1/2)

## (A) Internal Non-Maskable Interrupt



## (B) Internal Maskable Interrupt



## (C) External Maskable Interrupt (INTP0)

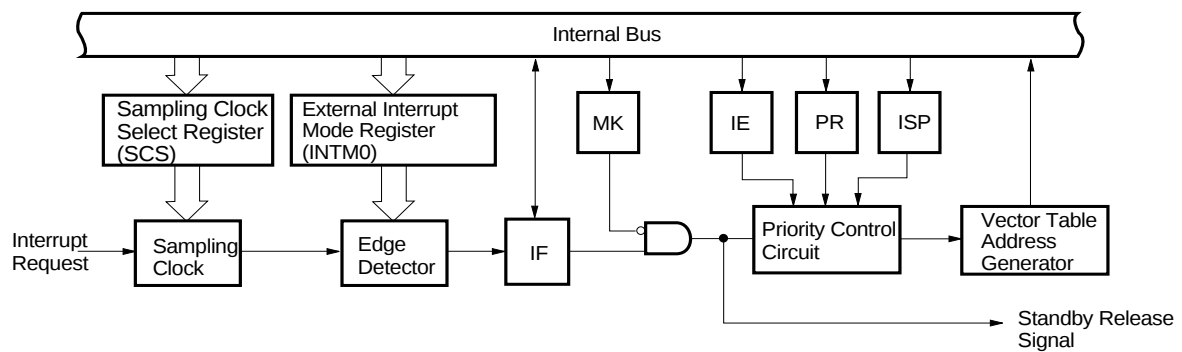
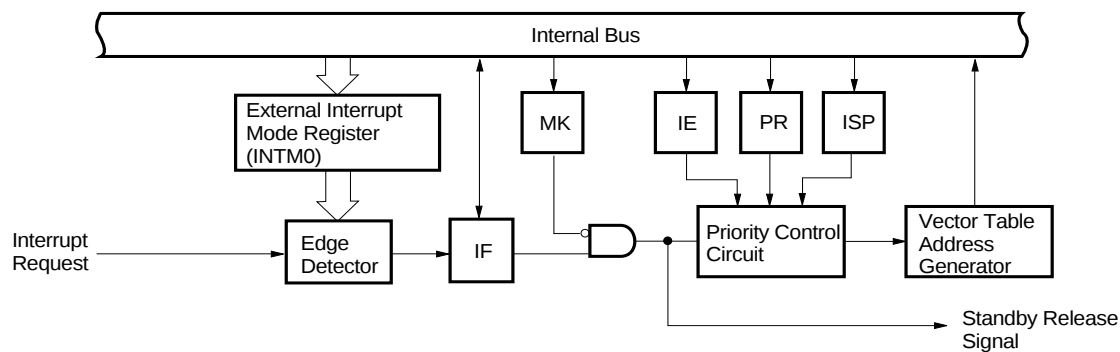
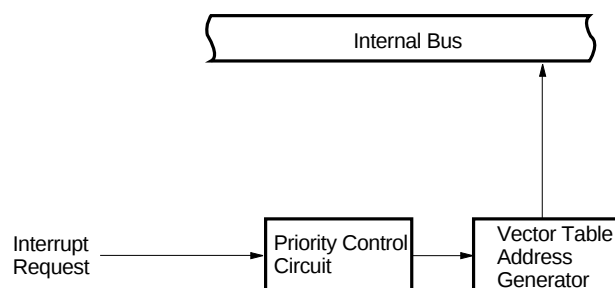


Figure 6-1. Basic Interrupt Function Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



IF : Interrupt request flag  
 IE : Interrupt enable flag  
 ISP : In-service priority flag  
 MK : Interrupt mask flag  
 PR : Priority specification flag

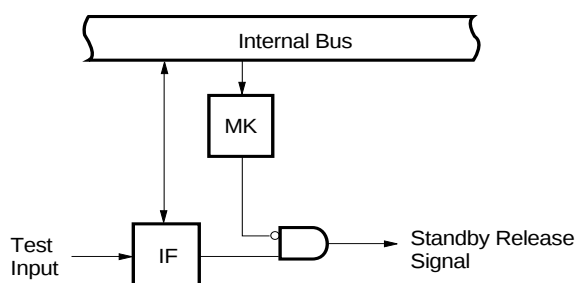
## 6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

**Table 6-2. Test Source List**

| Test Source |                               | Internal/External |
|-------------|-------------------------------|-------------------|
| Name        | Trigger                       |                   |
| INTWT       | Watch timer overflow          | Internal          |
| INTPT4      | Port 4 falling edge detection | External          |

**Figure 6-2. Test Function Basic Configuration**



IF : Test input flag

MK : Test mask flag

## 7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

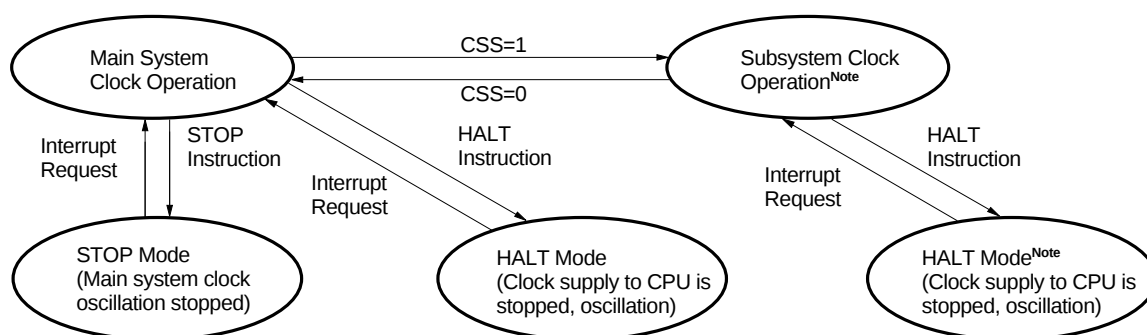
Ports 4 to 6 are used for connection with external devices.

## 8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- **HALT mode** : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- **STOP mode** : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Functions



**Note** The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

**Caution** When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

## 9. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by  $\overline{\text{RESET}}$  pin.
- Internal reset by watchdog timer runaway time detection.

## 10. INSTRUCTION SET

### (1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

| 2nd Operand<br>1st Operand    | #byte                                                        | A                                                            | r Note                                                              | sfr        | saddr                                                               | !addr16                                                             | PSW | [DE]       | [HL]                                                                | [HL+byte]<br>[HL+B]<br>[HL+C]                                       | \$addr16 | 1                          | None         |
|-------------------------------|--------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------|------------|---------------------------------------------------------------------|---------------------------------------------------------------------|-----|------------|---------------------------------------------------------------------|---------------------------------------------------------------------|----------|----------------------------|--------------|
| A                             | ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP        |                                                              | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV<br>XCH | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV | MOV<br>XCH | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV<br>XCH<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP |          | ROR<br>ROL<br>RORC<br>ROLC |              |
| r                             | MOV                                                          | MOV<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            | INC<br>DEC   |
| r1                            |                                                              |                                                              |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     | DBNZ     |                            |              |
| sfr                           | MOV                                                          | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |              |
| saddr                         | MOV<br>ADD<br>ADDC<br>SUB<br>SUBC<br>AND<br>OR<br>XOR<br>CMP | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     | DBNZ     |                            | INC<br>DEC   |
| !addr16                       |                                                              | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |              |
| PSW                           | MOV                                                          | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            | PUSH<br>POP  |
| [DE]                          |                                                              | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |              |
| [HL]                          |                                                              | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            | ROR4<br>ROL4 |
| [HL+byte]<br>[HL+B]<br>[HL+C] |                                                              | MOV                                                          |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          |                            |              |
| X                             |                                                              |                                                              |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          | MULU                       |              |
| C                             |                                                              |                                                              |                                                                     |            |                                                                     |                                                                     |     |            |                                                                     |                                                                     |          | DIVUW                      |              |

**Note** Except r=A

## (2) 16-Bit Instruction

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

| 2nd Operand<br>1st Operand | #byte                | AX                   | rp <sup>Note</sup> | saddrp | !addr16 | SP   | None |                         |
|----------------------------|----------------------|----------------------|--------------------|--------|---------|------|------|-------------------------|
| AX                         | ADDW<br>SUBW<br>CMPW |                      | MOVW<br>XCHW       | MOVW   | MOVW    | MOVW | MOVW |                         |
| rp                         | MOVW                 | MOVW <sup>Note</sup> |                    |        |         |      |      | INCW, DECW<br>PUSH, POP |
| sfrp                       | MOVW                 | MOVW                 |                    |        |         |      |      |                         |
| saddrp                     | MOVW                 | MOVW                 |                    |        |         |      |      |                         |
| !addr16                    |                      | MOVW                 |                    |        |         |      |      |                         |
| SP                         | MOVW                 | MOVW                 |                    |        |         |      |      |                         |

**Note** Only when rp=BC, DE, HL.

## (3) Bit Manipulation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

| 2nd Operand<br>1st Operand | A.bit                       | sfr.bit                     | saddr.bit                   | PWS.bit                     | [HL].bit                    | CY   | \$addr16          | None                 |
|----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------|-------------------|----------------------|
| A.bit                      |                             |                             |                             |                             |                             | MOV1 | BT<br>BF<br>BTCLR | SET1<br>CLR1         |
| sfr.bit                    |                             |                             |                             |                             |                             | MOV1 | BT<br>BF<br>BTCLR | SET1<br>CLR1         |
| saddr.bit                  |                             |                             |                             |                             |                             | MOV1 | BT<br>BF<br>BTCLR | SET1<br>CLR1         |
| PSW.bit                    |                             |                             |                             |                             |                             | MOV1 | BT<br>BF<br>BTCLR | SET1<br>CLR1         |
| [HL].bit                   |                             |                             |                             |                             |                             | MOV1 | BT<br>BF<br>BTCLR | SET1<br>CLR1         |
| CY                         | MOV1<br>AND1<br>OR1<br>XOR1 | MOV1<br>AND1<br>OR1<br>XOR1 | MOV1<br>AND1<br>OR1<br>XOR1 | MOV1<br>AND1<br>OR1<br>XOR1 | MOV1<br>AND1<br>OR1<br>XOR1 |      |                   | SET1<br>CLR1<br>NOT1 |

**(4) Call Instruction/Branch Instruction**

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

| 2nd Operand<br>1st Operand | AX | !addr16  | !addr11 | [addr5] | \$addr16                |
|----------------------------|----|----------|---------|---------|-------------------------|
| Basic instruction          | BR | CALL, BR | CALLF   | CALLT   | BR, BC, BNC,<br>BZ, BNZ |
| Compound instruction       |    |          |         |         | BT, BF, BTCLR,<br>DBNZ  |

**(5) Other Instruction**

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

## 11. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)

| Parameter                     | Symbol               | Test Conditions                                                                                   |                  | Rating                                           | Unit |
|-------------------------------|----------------------|---------------------------------------------------------------------------------------------------|------------------|--------------------------------------------------|------|
| Supply voltage                | V <sub>DD</sub>      |                                                                                                   |                  | −0.3 to + 7.0                                    | V    |
|                               | AV <sub>DD</sub>     |                                                                                                   |                  | −0.3 to V <sub>DD</sub> + 0.3                    | V    |
|                               | AV <sub>REF</sub>    |                                                                                                   |                  | −0.3 to V <sub>DD</sub> + 0.3                    | V    |
|                               | AV <sub>SS</sub>     |                                                                                                   |                  | −0.3 to + 0.3                                    | V    |
| Input voltage                 | V <sub>I1</sub>      | P00 to P04, P10 to P17, P20 to P27, P30 to P37<br>P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2 |                  | −0.3 to V <sub>DD</sub> + 0.3                    | V    |
|                               | V <sub>I2</sub>      | P60 to P67                                                                                        | Open-drain       | −0.3 to +16                                      | V    |
| Output voltage                | V <sub>O</sub>       |                                                                                                   |                  | −0.3 to V <sub>DD</sub> + 0.3                    | V    |
| Analog input voltage          | V <sub>AN</sub>      | P10 to P17                                                                                        | Analog input pin | AV <sub>SS</sub> −0.3 to AV <sub>REF</sub> + 0.3 | V    |
| Output current high           |                      | 1 pin                                                                                             |                  | −10                                              | mA   |
|                               | I <sub>OH</sub>      | P10 to P17, P20 to P27, P30 to P37 total                                                          |                  | −15                                              | mA   |
|                               |                      | P01 to P03, P40 to P47, P50 to P57, P60 to P67 total                                              |                  | −15                                              | mA   |
| Output current low            | I <sub>OL</sub> Note | 1 pin                                                                                             | Peak value       | 30                                               | mA   |
|                               |                      |                                                                                                   | rms              | 15                                               | mA   |
|                               |                      | P40 to P47, P50 to P55 total                                                                      | Peak value       | 100                                              | mA   |
|                               |                      |                                                                                                   | rms              | 70                                               | mA   |
|                               |                      | P01 to P03, P56, P57,<br>P60 to P67 total                                                         | Peak value       | 100                                              | mA   |
|                               |                      |                                                                                                   | rms              | 70                                               | mA   |
|                               |                      | P01 to P03,<br>P64 to P67 total                                                                   | Peak value       | 50                                               | mA   |
|                               |                      |                                                                                                   | rms              | 20                                               | mA   |
|                               |                      | P10 to P17, P20 to P27, P30 to P37<br>total                                                       | Peak value       | 50                                               | mA   |
|                               |                      |                                                                                                   | rms              | 20                                               | mA   |
| Operating ambient temperature | T <sub>A</sub>       |                                                                                                   |                  | −40 to +85                                       | °C   |
| Storage temperature           | T <sub>stg</sub>     |                                                                                                   |                  | −65 to +150                                      | °C   |

**Note** rms should be calculated as follows: [rms] = [peak value] ×  $\sqrt{\text{duty}}$

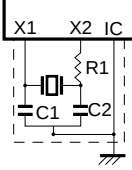
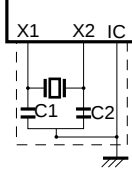
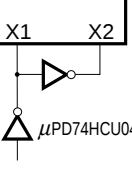
**Caution** Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

**Capacitance** (  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = V_{SS} = 0\text{ V}$  )

| Parameter         | Symbol   | Test Conditions                                    |                                                                                             | MIN. | TYP. | MAX. | Unit |
|-------------------|----------|----------------------------------------------------|---------------------------------------------------------------------------------------------|------|------|------|------|
| Input capacitance | $C_{IN}$ | $f = 1\text{ MHz}$ Unmeasured pins returned to 0 V |                                                                                             |      |      | 15   | pF   |
| I/O capacitance   | $C_{IO}$ | $f = 1\text{ MHz}$ Unmeasured pins returned to 0 V | P01 to P03, P10 to P17,<br>P20 to P27, P30 to P37,<br>P40 to P47, P50 to P57,<br>P64 to P67 |      |      | 15   | pF   |
|                   |          |                                                    | P60 to P63                                                                                  |      |      | 20   | pF   |

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**Main System Clock Oscillation Circuit Characteristics** (  $T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{ to }5.5\text{ V}$  )

| Resonator         | Recommended Circuit                                                                 | Parameter                                             | Test Conditions                                      | MIN. | TYP. | MAX. | Unit |
|-------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------|------|------|------|
| Ceramic resonator |    | Oscillator frequency ( $f_x$ ) <b>Note 1</b>          | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$         | 1    |      | 10   | MHz  |
|                   |                                                                                     |                                                       | $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$            | 1    |      | 5    |      |
|                   |                                                                                     | Oscillation stabilization time <b>Note 2</b>          | After $V_{DD}$ reaches oscillator voltage range MIN. |      |      | 4    | ms   |
| Crystal resonator |   | Oscillator frequency ( $f_x$ ) <b>Note 1</b>          | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$         | 1    |      | 10   | MHz  |
|                   |                                                                                     |                                                       | $1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$            | 1    |      | 5    |      |
|                   |                                                                                     | Oscillation stabilization time <b>Note 2</b>          | $V_{DD} = 4.5\text{ to }5.5\text{ V}$                |      |      | 10   | ms   |
| External clock    |  | X1 input frequency ( $f_x$ ) <b>Note 1</b>            |                                                      | 1.0  |      | 10.0 | MHz  |
|                   |                                                                                     | X1 input high/low level width ( $t_{XH}$ , $t_{XL}$ ) |                                                      | 45   |      | 500  | ns   |

**Notes 1.** Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

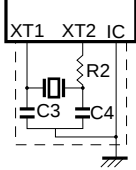
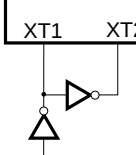
**2.** Time required to stabilize oscillation after reset or STOP mode release.

**Cautions 1.** When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as  $V_{SS}$ .
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

**2.** When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

**Subsystem Clock Oscillation Circuit Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

| Resonator         | Recommended Circuit                                                               | Parameter                                                | Test Conditions           | MIN. | TYP.   | MAX. | Unit |
|-------------------|-----------------------------------------------------------------------------------|----------------------------------------------------------|---------------------------|------|--------|------|------|
| Crystal resonator |  | Oscillator frequency ( $f_{XT}$ ) <b>Note 1</b>          |                           | 32   | 32.768 | 35   | kHz  |
|                   |                                                                                   | Oscillation stabilization time <b>Note 2</b>             | $V_{DD} = 4.5$ to $5.5$ V |      | 1.2    | 2    | s    |
|                   |                                                                                   |                                                          |                           |      |        | 10   |      |
| External clock    |  | XT1 input frequency ( $f_{XT}$ ) <b>Note 1</b>           |                           | 32   |        | 100  | kHz  |
|                   |                                                                                   | XT1 input high/low level width ( $t_{XTH}$ , $t_{XTL}$ ) |                           | 5    |        | 15   | μs   |

**Notes 1.** Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

**2.** Time required to stabilize oscillation after  $V_{DD}$  reaches oscillator voltage MIN.

**Cautions 1.** When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
  - Wiring should not cross other signal lines.
  - Wiring should not be placed close to a varying high current.
  - The potential of the oscillator capacitor ground should be the same as  $V_{SS}$ .
  - Do not ground wiring to a ground pattern in which a high current flows.
  - Do not fetch a signal from the oscillator.
- 2.** The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock.  
Particular care is therefore required with the wiring method when the subsystem clock is used.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                                   | Symbol           | Test Conditions                                                          |                                                                    | MIN.                  | TYP.                | MAX.                 | Unit |
|---------------------------------------------|------------------|--------------------------------------------------------------------------|--------------------------------------------------------------------|-----------------------|---------------------|----------------------|------|
| Input voltage high                          | V <sub>IH1</sub> | P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67            | V <sub>DD</sub> = 2.7 to 5.5 V                                     | 0.7 V <sub>DD</sub>   |                     | V <sub>DD</sub>      | V    |
|                                             |                  |                                                                          |                                                                    | 0.8 V <sub>DD</sub>   |                     | V <sub>DD</sub>      | V    |
|                                             | V <sub>IH2</sub> | P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$          | V <sub>DD</sub> = 2.7 to 5.5 V                                     | 0.8 V <sub>DD</sub>   |                     | V <sub>DD</sub>      | V    |
|                                             |                  |                                                                          |                                                                    | 0.85 V <sub>DD</sub>  |                     | V <sub>DD</sub>      | V    |
|                                             | V <sub>IH3</sub> | P60-P63<br>(N-ch open-drain)                                             | V <sub>DD</sub> = 2.7 to 5.5 V                                     | 0.7 V <sub>DD</sub>   |                     | 15                   | V    |
|                                             |                  |                                                                          |                                                                    | 0.8 V <sub>DD</sub>   |                     | 15                   | V    |
|                                             | V <sub>IH4</sub> | X1, X2                                                                   | V <sub>DD</sub> = 2.7 to 5.5 V                                     | V <sub>DD</sub> − 0.5 |                     | V <sub>DD</sub>      | V    |
|                                             |                  |                                                                          |                                                                    | V <sub>DD</sub> − 0.2 |                     | V <sub>DD</sub>      | V    |
|                                             | V <sub>IH5</sub> | XT1/P04, XT2                                                             | 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                    | 0.8 V <sub>DD</sub>   |                     | V <sub>DD</sub>      | V    |
|                                             |                  |                                                                          | 2.7 V ≤ V <sub>DD</sub> < 4.5 V                                    | 0.9 V <sub>DD</sub>   |                     | V <sub>DD</sub>      | V    |
| 1.8 V ≤ V <sub>DD</sub> < 2.7 V <b>Note</b> |                  |                                                                          | 0.9 V <sub>DD</sub>                                                |                       | V <sub>DD</sub>     | V                    |      |
| Input voltage low                           | V <sub>IL1</sub> | P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-67            | V <sub>DD</sub> = 2.7 to 5.5 V                                     | 0                     |                     | 0.3 V <sub>DD</sub>  | V    |
|                                             |                  |                                                                          |                                                                    | 0                     |                     | 0.2 V <sub>DD</sub>  | V    |
|                                             | V <sub>IL2</sub> | P00-P03, P20, P22, P24-P27, P33, P34, $\overline{\text{RESET}}$          | V <sub>DD</sub> = 2.7 to 5.5 V                                     | 0                     |                     | 0.2 V <sub>DD</sub>  | V    |
|                                             |                  |                                                                          |                                                                    | 0                     |                     | 0.15 V <sub>DD</sub> | V    |
|                                             | V <sub>IL3</sub> | P60-P63                                                                  | 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                    | 0                     |                     | 0.3 V <sub>DD</sub>  | V    |
|                                             |                  |                                                                          | 2.7 V ≤ V <sub>DD</sub> < 4.5 V                                    | 0                     |                     | 0.2 V <sub>DD</sub>  | V    |
|                                             |                  |                                                                          |                                                                    | 0                     |                     | 0.1 V <sub>DD</sub>  | V    |
|                                             | V <sub>IL4</sub> | X1, X2                                                                   | V <sub>DD</sub> = 2.7 to 5.5 V                                     | 0                     |                     | 0.4                  | V    |
|                                             |                  |                                                                          |                                                                    | 0                     |                     | 0.2                  | V    |
|                                             | V <sub>IL5</sub> | XT1/P04, XT2                                                             | 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                                    | 0                     |                     | 0.2 V <sub>DD</sub>  | V    |
| 2.7 V ≤ V <sub>DD</sub> < 4.5 V             |                  |                                                                          | 0                                                                  |                       | 0.1 V <sub>DD</sub> | V                    |      |
| 1.8 V ≤ V <sub>DD</sub> < 2.7 V <b>Note</b> |                  |                                                                          | 0                                                                  |                       | 0.1 V <sub>DD</sub> | V                    |      |
| Output voltage high                         | V <sub>OH1</sub> | V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OH</sub> = −1 mA                  |                                                                    | V <sub>DD</sub> − 1.0 |                     |                      | V    |
|                                             |                  | I <sub>OH</sub> = −100 μA                                                |                                                                    | V <sub>DD</sub> − 0.5 |                     |                      | V    |
| Output voltage low                          | V <sub>OL1</sub> | P50 to P57, P60 to P63                                                   | V <sub>DD</sub> = 4.5 to 5.5 V,<br>I <sub>OL</sub> = 15 mA         |                       | 0.4                 | 2.0                  | V    |
|                                             |                  | P01 to P03, P10 to P17, P20 to P27<br>P30 to P37, P40 to P47, P64 to P67 | V <sub>DD</sub> = 4.5 to 5.5 V,<br>I <sub>OL</sub> = 1.6 mA        |                       |                     | 0.4                  | V    |
|                                             | V <sub>OL2</sub> | SB0, SB1, $\overline{\text{SCK0}}$                                       | V <sub>DD</sub> = 4.5 to 5.5 V, open-drain<br>pulled-up (R = 1 KΩ) |                       |                     | 0.2 V <sub>DD</sub>  | V    |
|                                             | V <sub>OL3</sub> | I <sub>OL</sub> = 400 μA                                                 |                                                                    |                       |                     | 0.5                  | V    |

**Note** When using XT1/P04 as P04, input the inverse of P04 to XT2 using an inverter.

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                    | Symbol     | Test Conditions                                                                                    |                                                                                                        | MIN. | TYP. | MAX.           | Unit |
|------------------------------|------------|----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------|------|----------------|------|
| Input leakage current high   | $I_{LIH1}$ | $V_{IN} = V_{DD}$                                                                                  | P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{RESET}$ |      |      | 3              | μA   |
|                              | $I_{LIH2}$ |                                                                                                    | X1, X2, XT1/P04, XT2                                                                                   |      |      | 20             | μA   |
|                              | $I_{LIH3}$ | $V_{IN} = 15$ V                                                                                    | P60 to P63                                                                                             |      |      | 80             | μA   |
| Input leakage current low    | $I_{LIL1}$ | $V_{IN} = 0$ V                                                                                     | P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, $\overline{RESET}$ |      |      | −3             | μA   |
|                              | $I_{LIL2}$ |                                                                                                    | X1, X2, XT1/P04, XT2                                                                                   |      |      | −20            | μA   |
|                              | $I_{LIL3}$ |                                                                                                    | P60 to P63                                                                                             |      |      | −3 <b>Note</b> | μA   |
| Output leakage current high  | $I_{LOH1}$ | $V_{OUT} = V_{DD}$                                                                                 |                                                                                                        |      |      | 3              | μA   |
| Output leakage current low   | $I_{LOL}$  | $V_{OUT} = 0$ V                                                                                    |                                                                                                        |      |      | −3             | μA   |
| Mask option pull-up resistor | R1         | $V_{IN} = 0$ V, P60 to P63                                                                         |                                                                                                        | 20   | 40   | 90             | kΩ   |
| Software pull-up resistor    | R2         | $V_{IN} = 0$ V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67 |                                                                                                        | 15   | 40   | 90             | kΩ   |

**Note** For P60-P63, if pull-up resistor is not provided (specifiable by mask option) a low-level input leak current of −200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is −3 μA (MAX.).

**Remark** The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

**DC Characteristics** ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                    | Symbol           | Test Conditions                                                     |                                              | MIN. | TYP. | MAX. | Unit |
|------------------------------|------------------|---------------------------------------------------------------------|----------------------------------------------|------|------|------|------|
| Supply current <b>Note 1</b> | I <sub>DD1</sub> | 10.00 MHz crystal oscillation operation mode                        | V <sub>DD</sub> = 5.0 V ± 10 % <b>Note 2</b> |      | 9.0  | 18.0 | mA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 3.0 V ± 10 % <b>Note 3</b> |      | 1.3  | 2.6  | mA   |
|                              | I <sub>DD2</sub> | 10.00 MHz crystal oscillation HALT mode                             | V <sub>DD</sub> = 5.0 V ± 10 % <b>Note 2</b> |      | 2.0  | 4.0  | mA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 3.0 V ± 10 % <b>Note 3</b> |      | 1.0  | 2.0  | mA   |
|                              | I <sub>DD3</sub> | 32.768 kHz crystal oscillation operation mode <b>Note 4</b>         | V <sub>DD</sub> = 5.0 V ± 10 % <b>Note 3</b> |      | 60   | 120  | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 3.0 V ± 10 % <b>Note 3</b> |      | 35   | 70   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 2.0 V ± 10 % <b>Note 4</b> |      | 24   | 48   | μA   |
|                              | I <sub>DD4</sub> | 32.768 kHz crystal oscillation HALT mode                            | V <sub>DD</sub> = 5.0 V ± 10 % <b>Note 3</b> |      | 25   | 50   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 3.0 V ± 10 % <b>Note 3</b> |      | 5    | 15   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 2.0 V ± 10 % <b>Note 4</b> |      | 2    | 10   | μA   |
|                              | I <sub>DD5</sub> | XT1 = V <sub>DD</sub><br>STOP mode when using feedback resistor     | V <sub>DD</sub> = 5.0 V ± 10 %               |      | 1    | 30   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 3.0 V ± 10 %               |      | 0.5  | 10   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 2.0 V ± 10 % <b>Note 4</b> |      | 0.3  | 10   | μA   |
|                              | I <sub>DD6</sub> | XT1 = V <sub>DD</sub><br>STOP mode when not using feedback resistor | V <sub>DD</sub> = 5.0 V ± 10 %               |      | 0.1  | 30   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 3.0 V ± 10 %               |      | 0.05 | 10   | μA   |
|                              |                  |                                                                     | V <sub>DD</sub> = 2.0 V ± 10 % <b>Note 4</b> |      | 0.05 | 10   | μA   |

**Notes 1.** Current flowing into the  $V_{DD}$  and  $AV_{DD}$  pins. However, the current flowing into the A/D converter and internal pull-up resistors is not included.

- 2.** When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)
- 3.** When operating at low-speed mode (when the PCC is set to 04H)
- 4.** When main system clock stopped.

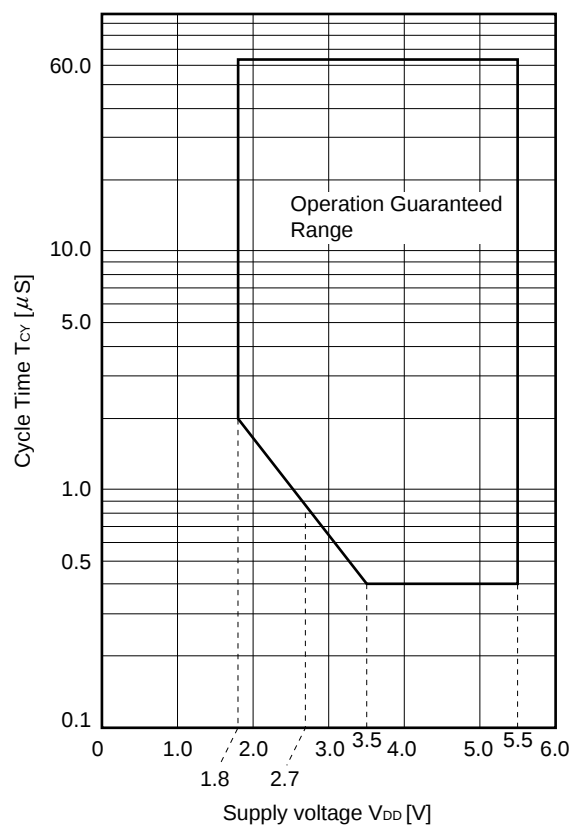
# AC Characteristics

(1) Basic Operation ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

| Parameter                                          | Symbol                                     | Test Conditions                 |                                 | MIN.                                | TYP. | MAX. | Unit |
|----------------------------------------------------|--------------------------------------------|---------------------------------|---------------------------------|-------------------------------------|------|------|------|
| Cycle time<br>(Min. instruction<br>execution time) | T <sub>CY</sub>                            | Operating on main system clock  | 3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V | 0.4                                 |      | 64   | μs   |
|                                                    |                                            |                                 | 2.7 V ≤ V <sub>DD</sub> < 3.5 V | 0.8                                 |      | 64   | μs   |
|                                                    |                                            |                                 | 1.8 V ≤ V <sub>DD</sub> < 2.7 V | 2.0                                 |      | 64   | μs   |
|                                                    |                                            | Operating on subsystem clock    |                                 | 40                                  | 122  | 125  | μs   |
| TI0 input<br>frequency                             | t <sub>TIH0</sub>                          | 3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V |                                 | 2/f <sub>sam</sub> +0.1 <b>Note</b> |      |      | μs   |
|                                                    | t <sub>TIL0</sub>                          | 2.7 V ≤ V <sub>DD</sub> < 3.5 V |                                 | 2/f <sub>sam</sub> +0.2 <b>Note</b> |      |      | μs   |
|                                                    |                                            | 1.8 V ≤ V <sub>DD</sub> < 2.7 V |                                 | 2/f <sub>sam</sub> +0.5 <b>Note</b> |      |      | μs   |
| TI1, TI2 input<br>frequency                        | f <sub>TI1</sub>                           | V <sub>DD</sub> = 4.5 to 5.5 V  |                                 | 0                                   |      | 4    | MHz  |
|                                                    |                                            |                                 |                                 | 0                                   |      | 275  | kHz  |
| TI1, TI2 input<br>high/low-level<br>width          | t <sub>TIH1</sub>                          | V <sub>DD</sub> = 4.5 to 5.5 V  |                                 | 100                                 |      |      | ns   |
|                                                    | t <sub>TIL1</sub>                          |                                 |                                 | 1.8                                 |      |      | μs   |
| Interrupt input<br>high/low-level<br>width         | t <sub>INTH</sub><br><br>t <sub>INTL</sub> | INTP0                           | 3.5 V ≤ V <sub>DD</sub> ≤ 5.5 V | 2/f <sub>sam</sub> +0.1 <b>Note</b> |      |      | μs   |
|                                                    |                                            |                                 | 2.7 V ≤ V <sub>DD</sub> < 3.5 V | 2/f <sub>sam</sub> +0.2 <b>Note</b> |      |      | μs   |
|                                                    |                                            |                                 | 1.8 V ≤ V <sub>DD</sub> < 2.7 V | 2/f <sub>sam</sub> +0.5 <b>Note</b> |      |      | μs   |
|                                                    |                                            | INTP1-INTP3, KR0-KR7            | V <sub>DD</sub> = 2.7 to 5.5 V  | 10                                  |      |      | μs   |
|                                                    |                                            |                                 |                                 | 20                                  |      |      | μs   |
| RESET low<br>level width                           | t <sub>RSL</sub>                           | V <sub>DD</sub> = 2.7 to 5.5 V  |                                 | 10                                  |      |      | μs   |
|                                                    |                                            |                                 |                                 | 20                                  |      |      | μs   |

**Note** In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of  $f_{sam}$  is possible between  $f_X/2^{N+1}$ ,  $f_X/64$  and  $f_X/128$  (when  $N = 0$  to  $4$ ).

$T_{CY}$  vs  $V_{DD}$  (At main system clock operation)



(2) Read/Write Operation ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.7$  to  $5.5$  V)

| Parameter                                                                           | Symbol      | Test Conditions                   | MIN.                | MAX.                 | Unit |
|-------------------------------------------------------------------------------------|-------------|-----------------------------------|---------------------|----------------------|------|
| ASTB high-level width                                                               | $t_{ASTH}$  |                                   | $0.5t_{CY}$         |                      | ns   |
| Address setup time                                                                  | $t_{ADS}$   |                                   | $0.5t_{CY}-30$      |                      | ns   |
| Address hold time                                                                   | $t_{ADH}$   |                                   | 50                  |                      | ns   |
| Data input time from address                                                        | $t_{ADD1}$  |                                   |                     | $(2.5+2n)t_{CY}-50$  | ns   |
|                                                                                     | $t_{ADD2}$  |                                   |                     | $(3+2n)t_{CY}-100$   | ns   |
| Data input time from $\overline{RD}\downarrow$                                      | $t_{RDD1}$  |                                   |                     | $(1+2n)t_{CY}-25$    | ns   |
|                                                                                     | $t_{RDD2}$  |                                   |                     | $(2.5+2n)t_{CY}-100$ | ns   |
| Read data hold time                                                                 | $t_{RDH}$   |                                   | 0                   |                      | ns   |
| $\overline{RD}$ low-level width                                                     | $t_{RDL1}$  |                                   | $(1.5+2n)t_{CY}-20$ |                      | ns   |
|                                                                                     | $t_{RDL2}$  |                                   | $(2.5+2n)t_{CY}-20$ |                      | ns   |
| $\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$               | $t_{RDWT1}$ |                                   |                     | $0.5t_{CY}$          | ns   |
|                                                                                     | $t_{RDWT2}$ |                                   |                     | $1.5t_{CY}$          | ns   |
| $\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$               | $t_{WRWT}$  |                                   |                     | $0.5t_{CY}$          | ns   |
| $\overline{WAIT}$ low-level width                                                   | $t_{WTL}$   |                                   | $(0.5+2n)t_{CY}+10$ | $(2+2n)t_{CY}$       | ns   |
| Write data setup time                                                               | $t_{WDS}$   |                                   | 100                 |                      | ns   |
| Write data hold time                                                                | $t_{WDH}$   | Load resistor $\geq 5$ k $\Omega$ | 20                  |                      | ns   |
| $\overline{WR}$ low-level width                                                     | $t_{WRL1}$  |                                   | $(2.5+2n)t_{CY}-20$ |                      | ns   |
| $\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$               | $t_{ASTRD}$ |                                   | $0.5t_{CY}-30$      |                      | ns   |
| $\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$               | $t_{ASTWR}$ |                                   | $1.5t_{CY}-30$      |                      | ns   |
| $\overline{ASTB}\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch | $t_{RDAST}$ |                                   | $t_{CY}-10$         | $t_{CY}+40$          | ns   |
| Address hold time from $\overline{RD}\uparrow$ in external fetch                    | $t_{RDADH}$ |                                   | $t_{CY}$            | $t_{CY}+50$          | ns   |
| Write data output time from $\overline{RD}\uparrow$                                 | $t_{RDWD}$  | $V_{DD} = 4.5$ to $5.5$ V         | $0.5t_{CY}+5$       | $0.5t_{CY}+30$       | ns   |
|                                                                                     |             |                                   | $0.5t_{CY}+15$      | $0.5t_{CY}+90$       | ns   |
| Write data output time from $\overline{WR}\downarrow$                               | $t_{WRWD}$  | $V_{DD} = 4.5$ to $5.5$ V         | 5                   | 30                   | ns   |
|                                                                                     |             |                                   | 15                  | 90                   | ns   |
| Address hold time from $\overline{WR}\uparrow$                                      | $t_{WRADH}$ | $V_{DD} = 4.5$ to $5.5$ V         | $t_{CY}$            | $t_{CY}+60$          | ns   |
|                                                                                     |             |                                   | $t_{CY}$            | $t_{CY}+100$         | ns   |
| $\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$                   | $t_{WTRD}$  |                                   | $0.5t_{CY}$         | $2.5t_{CY}+80$       | ns   |
| $\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$                   | $t_{WTWR}$  |                                   | $0.5t_{CY}$         | $2.5t_{CY}+80$       | ns   |

**Remarks** 1.  $t_{CY} = T_{CY}/4$ 

2. n indicates number of waits.

(3) Serial Interface ( $T_A = -40$  to  $+85$  °C,  $V_{DD} = 1.8$  to  $5.5$  V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ( $\overline{SCK0}$ ... Internal clock output)

| Parameter                                              | Symbol     | Conditions                                   | MIN.             | TYP. | MAX. | Unit |
|--------------------------------------------------------|------------|----------------------------------------------|------------------|------|------|------|
| $\overline{SCK0}$ cycle time                           | $t_{KCY1}$ | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 800              |      |      | ns   |
|                                                        |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 1600             |      |      | ns   |
|                                                        |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 3200             |      |      | ns   |
|                                                        |            |                                              | 4800             |      |      | ns   |
| $\overline{SCK0}$ high/low-level width                 | $t_{KH1}$  | $V_{DD} = 4.5$ to $5.5\text{ V}$             | $t_{KCY1}/2-50$  |      |      | ns   |
|                                                        | $t_{KL1}$  |                                              | $t_{KCY1}/2-100$ |      |      | ns   |
| SI0 setup time (to $\overline{SCK0}\uparrow$ )         | $t_{SIK1}$ | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 100              |      |      | ns   |
|                                                        |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 150              |      |      | ns   |
|                                                        |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 300              |      |      | ns   |
|                                                        |            |                                              | 400              |      |      | ns   |
| SI0 hold time (from $\overline{SCK0}\uparrow$ )        | $t_{KSI1}$ |                                              | 400              |      |      | ns   |
| SO0 output delay time from $\overline{SCK0}\downarrow$ | $t_{KSO1}$ | $C = 100\text{ pF}$ <b>Note</b>              |                  |      | 300  | ns   |

**Note** C is the load capacitance of  $\overline{SCK0}$  and SO0 output line.

(ii) 3-wire serial I/O mode ( $\overline{SCK0}$ ... External clock input)

| Parameter                                              | Symbol     | Test Conditions                                     |                                               | MIN. | TYP. | MAX. | Unit |
|--------------------------------------------------------|------------|-----------------------------------------------------|-----------------------------------------------|------|------|------|------|
| $\overline{SCK0}$ cycle time                           | $t_{KCY2}$ | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$        |                                               | 800  |      |      | ns   |
|                                                        |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$           |                                               | 1600 |      |      | ns   |
|                                                        |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$           |                                               | 3200 |      |      | ns   |
|                                                        |            |                                                     |                                               | 4800 |      |      | ns   |
| $\overline{SCK0}$ high/low-level width                 | $t_{KH2}$  | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$        |                                               | 400  |      |      | ns   |
|                                                        | $t_{KL2}$  | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$           |                                               | 800  |      |      | ns   |
|                                                        |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$           |                                               | 1600 |      |      | ns   |
|                                                        |            |                                                     |                                               | 2400 |      |      | ns   |
| SI0 setup time (to $\overline{SCK0}\uparrow$ )         | $t_{SIK2}$ | $V_{DD} = 2.0$ to $5.5\text{ V}$                    |                                               | 100  |      |      | ns   |
|                                                        |            |                                                     |                                               | 150  |      |      | ns   |
| SI0 hold time (from $\overline{SCK0}\uparrow$ )        | $t_{KSI2}$ |                                                     |                                               | 400  |      |      | ns   |
| SO0 output delay time from $\overline{SCK0}\downarrow$ | $t_{KSO2}$ | $C = 100\text{ pF}$ <b>Note</b>                     | $V_{DD} = 2.0$ to $5.5\text{ V}$              |      |      | 300  | ns   |
|                                                        |            |                                                     |                                               |      |      | 500  | ns   |
| $\overline{SCK0}$ rise, fall time                      | $t_{R2}$   | When external device expansion function is used     |                                               |      |      | 160  | ns   |
|                                                        | $t_{F2}$   | When external device expansion function is not used | When 16-bit timer output function is used     |      |      | 700  | ns   |
|                                                        |            |                                                     | When 16-bit timer output function is not used |      |      | 1000 | ns   |

**Note** C is the load capacitance of SO0 output line.

(iii) SBI mode (SCK0... Internal clock output)

| Parameter                             | Symbol            | Test Conditions                     |                                | MIN.                     | TYP. | MAX. | Unit |
|---------------------------------------|-------------------|-------------------------------------|--------------------------------|--------------------------|------|------|------|
| SCK0 cycle time                       | t <sub>KCY3</sub> | 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V     |                                | 800                      |      |      | ns   |
|                                       |                   | 2.0 V ≤ V <sub>DD</sub> < 4.5 V     |                                | 3200                     |      |      | ns   |
|                                       |                   |                                     |                                | 4800                     |      |      | ns   |
| SCK0 high/low-level width             | t <sub>KH3</sub>  | V <sub>DD</sub> = 4.5 to 6.0 V      |                                | t <sub>KCY3</sub> /2–50  |      |      | ns   |
|                                       | t <sub>KL3</sub>  |                                     |                                | t <sub>KCY3</sub> /2–150 |      |      | ns   |
| SB0, SB1 setup time (to SCK0↑)        | t <sub>SIK3</sub> | 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V     |                                | 100                      |      |      | ns   |
|                                       |                   | 2.0 V ≤ V <sub>DD</sub> < 4.5 V     |                                | 300                      |      |      | ns   |
|                                       |                   |                                     |                                | 400                      |      |      | ns   |
| SB0, SB1 hold time (from SCK0↑)       | t <sub>KSI3</sub> |                                     |                                | t <sub>KCY3</sub> /2     |      |      | ns   |
| SB0, SB1 output delay time from SCK0↓ | t <sub>KSO3</sub> | R = 1 kΩ,<br>C = 100 pF <b>Note</b> | V <sub>DD</sub> = 4.5 to 5.5 V | 0                        |      | 250  | ns   |
|                                       |                   |                                     |                                | 0                        |      | 1000 | ns   |
| SB0, SB1↓ from SCK0↑                  | t <sub>KSB</sub>  |                                     |                                | t <sub>KCY3</sub>        |      |      | ns   |
| SCK0↓ from SB0, SB1↓                  | t <sub>SBK</sub>  |                                     |                                | t <sub>KCY3</sub>        |      |      | ns   |
| SB0, SB1 high-level width             | t <sub>SBH</sub>  |                                     |                                | t <sub>KCY3</sub>        |      |      | ns   |
| SB0, SB1 low-level width              | t <sub>SBL</sub>  |                                     |                                | t <sub>KCY3</sub>        |      |      | ns   |

**Note** R and C are the load resistors and load capacitance of the SB0, SB1 and SCK0 output line.

(iv) SBI mode ( $\overline{\text{SCK0}}$ ... External clock input)

| Parameter                                                             | Symbol                               | Test Conditions                                       |                                                 | MIN.                | TYP. | MAX. | Unit |
|-----------------------------------------------------------------------|--------------------------------------|-------------------------------------------------------|-------------------------------------------------|---------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time                                   | $t_{\text{KCY4}}$                    | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ |                                                 | 800                 |      |      | ns   |
|                                                                       |                                      | $2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    |                                                 | 3200                |      |      | ns   |
|                                                                       |                                      |                                                       |                                                 | 4800                |      |      | ns   |
| $\overline{\text{SCK0}}$ high/low-level width                         | $t_{\text{KH4}}$<br>$t_{\text{KL4}}$ | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ |                                                 | 400                 |      |      | ns   |
|                                                                       |                                      | $2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    |                                                 | 1600                |      |      | ns   |
|                                                                       |                                      |                                                       |                                                 | 2400                |      |      | ns   |
| SB0, SB1 setup time<br>(to $\overline{\text{SCK0}}\uparrow$ )         | $t_{\text{SIK4}}$                    | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ |                                                 | 100                 |      |      | ns   |
|                                                                       |                                      | $2.0 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    |                                                 | 300                 |      |      | ns   |
|                                                                       |                                      |                                                       |                                                 | 400                 |      |      | ns   |
| SB0, SB1 hold time<br>(from $\overline{\text{SCK0}}\uparrow$ )        | $t_{\text{KSI4}}$                    |                                                       |                                                 | $t_{\text{KCY4}}/2$ |      |      | ns   |
| SB0, SB1 output delay<br>time from $\overline{\text{SCK0}}\downarrow$ | $t_{\text{KSO4}}$                    | R = 1 k $\Omega$ ,<br>C = 100 pF <b>Note</b>          | $V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$ | 0                   |      | 300  | ns   |
|                                                                       |                                      |                                                       |                                                 | 0                   |      | 1000 | ns   |
| SB0, SB1 $\downarrow$ from $\overline{\text{SCK0}}\uparrow$           | $t_{\text{KSB}}$                     |                                                       |                                                 | $t_{\text{KCY4}}$   |      |      | ns   |
| $\overline{\text{SCK0}}\downarrow$ from SB0, SB1 $\downarrow$         | $t_{\text{SBK}}$                     |                                                       |                                                 | $t_{\text{KCY4}}$   |      |      | ns   |
| SB0, SB1 high-level width                                             | $t_{\text{SBH}}$                     |                                                       |                                                 | $t_{\text{KCY4}}$   |      |      | ns   |
| SB0, SB1 low-level width                                              | $t_{\text{SBL}}$                     |                                                       |                                                 | $t_{\text{KCY4}}$   |      |      | ns   |
| $\overline{\text{SCK0}}$ rise, fall time                              | $t_{\text{R4}}$<br>$t_{\text{F4}}$   | When external device expansion function is used       |                                                 |                     |      | 160  | ns   |
|                                                                       |                                      | When external device expansion function is not used   | When 16-bit timer output function is used       |                     |      | 700  | ns   |
|                                                                       |                                      |                                                       | When 16-bit timer output function is not used   |                     |      | 1000 | ns   |

**Note** R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$ ... Internal clock output)

| Parameter                                                             | Symbol            | Test Conditions                              |                                                       | MIN.                    | TYP. | MAX. | Unit |
|-----------------------------------------------------------------------|-------------------|----------------------------------------------|-------------------------------------------------------|-------------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time                                   | $t_{\text{KCY5}}$ | R = 1 k $\Omega$ ,<br>C = 100 pF <b>Note</b> | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 1600                    |      |      | ns   |
|                                                                       |                   |                                              | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$    | 3200                    |      |      | ns   |
|                                                                       |                   |                                              |                                                       | 4800                    |      |      | ns   |
| $\overline{\text{SCK0}}$ high-level width                             | $t_{\text{KH5}}$  |                                              | $V_{\text{DD}} = 2.7 \text{ to } 5.5 \text{ V}$       | $t_{\text{KCY5}}/2-160$ |      |      | ns   |
|                                                                       |                   |                                              |                                                       | $t_{\text{KCY5}}/2-190$ |      |      | ns   |
| $\overline{\text{SCK0}}$ low-level width                              | $t_{\text{KL5}}$  |                                              | $V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$       | $t_{\text{KCY5}}/2-50$  |      |      | ns   |
|                                                                       |                   |                                              |                                                       | $t_{\text{KCY5}}/2-100$ |      |      | ns   |
| SB0, SB1 setup time<br>(to $\overline{\text{SCK0}}\uparrow$ )         | $t_{\text{SIK5}}$ |                                              | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 300                     |      |      | ns   |
|                                                                       |                   |                                              | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 350                     |      |      | ns   |
|                                                                       |                   |                                              | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$    | 400                     |      |      | ns   |
|                                                                       |                   |                                              |                                                       | 500                     |      |      | ns   |
| SB0, SB1 hold time<br>(from $\overline{\text{SCK0}}\uparrow$ )        | $t_{\text{KSI5}}$ |                                              |                                                       | 600                     |      |      | ns   |
| SB0, SB1 output delay<br>time from $\overline{\text{SCK0}}\downarrow$ | $t_{\text{KSO5}}$ |                                              |                                                       | 0                       |      | 300  | ns   |

**Note** R and C are the load resistors and load capacitance of the  $\overline{\text{SCK0}}$ , SB0 and SB1 output line.

(vi) 2-wire serial I/O mode (SCK0... External clock input)

| Parameter                                | Symbol                             | Test Conditions                                              |                                                     | MIN.                 | TYP. | MAX. | Unit |
|------------------------------------------|------------------------------------|--------------------------------------------------------------|-----------------------------------------------------|----------------------|------|------|------|
| SCK0 cycle time                          | t <sub>KCY6</sub>                  | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V                              |                                                     | 1600                 |      |      | ns   |
|                                          |                                    | 2.0 V ≤ V <sub>DD</sub> < 2.7 V                              |                                                     | 3200                 |      |      | ns   |
|                                          |                                    |                                                              |                                                     | 4800                 |      |      | ns   |
| SCK0 high-level width                    | t <sub>KH6</sub>                   | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V                              |                                                     | 650                  |      |      | ns   |
|                                          |                                    | 2.0 V ≤ V <sub>DD</sub> < 2.7 V                              |                                                     | 1300                 |      |      | ns   |
|                                          |                                    |                                                              |                                                     | 2100                 |      |      | ns   |
| SCK0 low-level width                     | t <sub>KL6</sub>                   | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V                              |                                                     | 800                  |      |      | ns   |
|                                          |                                    | 2.0 V ≤ V <sub>DD</sub> < 2.7 V                              |                                                     | 1600                 |      |      | ns   |
|                                          |                                    |                                                              |                                                     | 2400                 |      |      | ns   |
| SB0, SB1 setup time<br>(to SCK0↑)        | t <sub>SIK6</sub>                  | V <sub>DD</sub> = 2.0 to 5.5 V                               |                                                     | 100                  |      |      | ns   |
|                                          |                                    |                                                              |                                                     | 150                  |      |      | ns   |
| SB0, SB1 hold time<br>(from SCK0↑)       | t <sub>SI6</sub>                   |                                                              |                                                     | t <sub>KCY6</sub> /2 |      |      | ns   |
| SB0, SB1 output delay<br>time from SCK0↓ | t <sub>KSO6</sub>                  | R = 1 kΩ,<br>C = 100 pF <b>Note</b>                          | 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V                     | 0                    |      | 300  | ns   |
|                                          |                                    |                                                              | 2.0 V ≤ V <sub>DD</sub> < 4.5 V                     | 0                    |      | 500  | ns   |
|                                          |                                    |                                                              |                                                     | 0                    |      | 800  | ns   |
| SCK0 rise, fall time                     | t <sub>R6</sub><br>t <sub>F6</sub> | When external device<br>expansion function is used           |                                                     |                      |      | 160  | ns   |
|                                          |                                    | When external<br>device expansion<br>function is not<br>used | When 16-bit timer<br>output function is<br>used     |                      |      | 700  | ns   |
|                                          |                                    |                                                              | When 16-bit timer<br>output function is<br>not used |                      |      | 1000 | ns   |

**Note** R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

**(b) Serial Interface Channel 1****(i) 3-wire serial I/O mode (SCK1... Internal clock output)**

| Parameter                                    | Symbol     | Test Conditions                              | MIN.             | TYP. | MAX. | Unit |
|----------------------------------------------|------------|----------------------------------------------|------------------|------|------|------|
| SCK1 cycle time                              | $t_{KCY7}$ | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 800              |      |      | ns   |
|                                              |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 1600             |      |      | ns   |
|                                              |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 3200             |      |      | ns   |
|                                              |            |                                              | 4800             |      |      | ns   |
| SCK1 high/low-level width                    | $t_{KH7}$  | $V_{DD} = 4.5\text{ to }5.5\text{ V}$        | $t_{KCY7}/2-50$  |      |      | ns   |
|                                              | $t_{KL7}$  |                                              | $t_{KCY7}/2-100$ |      |      | ns   |
| SI1 setup time (to SCK1 $\uparrow$ )         | $t_{SIK7}$ | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 100              |      |      | ns   |
|                                              |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$    | 150              |      |      | ns   |
|                                              |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$    | 300              |      |      | ns   |
|                                              |            |                                              | 400              |      |      | ns   |
| SI1 hold time (from SCK1 $\uparrow$ )        | $t_{KSI7}$ |                                              | 400              |      |      | ns   |
| SO1 output delay time from SCK1 $\downarrow$ | $t_{KSO7}$ | $C = 100\text{ pF}$ <b>Note</b>              |                  |      | 300  | ns   |

**Note** C is the load capacitance of SCK1 and SO1 output line.

**(ii) 3-wire serial I/O mode (SCK1... External clock input)**

| Parameter                                    | Symbol     | Test Conditions                                                       | MIN. | TYP. | MAX. | Unit |
|----------------------------------------------|------------|-----------------------------------------------------------------------|------|------|------|------|
| SCK1 cycle time                              | $t_{KCY8}$ | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                          | 800  |      |      | ns   |
|                                              |            | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$                             | 1600 |      |      | ns   |
|                                              |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$                             | 3200 |      |      | ns   |
|                                              |            |                                                                       | 4800 |      |      | ns   |
| SCK1 high/low-level width                    | $t_{KH8}$  | $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                          | 400  |      |      | ns   |
|                                              | $t_{KL8}$  | $2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$                             | 800  |      |      | ns   |
|                                              |            | $2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$                             | 1600 |      |      | ns   |
|                                              |            |                                                                       | 2400 |      |      | ns   |
| SI1 setup time (to SCK1 $\uparrow$ )         | $t_{SIK8}$ | $V_{DD} = 2.0\text{ to }5.5\text{ V}$                                 | 100  |      |      | ns   |
|                                              |            |                                                                       | 150  |      |      | ns   |
| SI1 hold time (from SCK1 $\uparrow$ )        | $t_{KSI8}$ |                                                                       | 400  |      |      | ns   |
| SO0 output delay time from SCK1 $\downarrow$ | $t_{KSO8}$ | $C = 100\text{ pF}$ <b>Note</b> $V_{DD} = 2.0\text{ to }5.5\text{ V}$ |      |      | 300  | ns   |
|                                              |            |                                                                       |      |      | 500  | ns   |
| SCK1 rise, fall time                         | $t_{R8}$   | When external device expansion function is used                       |      |      | 160  | ns   |
|                                              | $t_{F8}$   | When external device expansion function is not used                   |      |      | 700  | ns   |
|                                              |            | When 16-bit timer output function is not used                         |      |      | 1000 | ns   |

**Note** C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ( $\overline{\text{SCK1}}$ ... Internal clock output)

| Parameter                                                        | Symbol            | Test Conditions                                       | MIN.                    | TYP. | MAX.                    | Unit |
|------------------------------------------------------------------|-------------------|-------------------------------------------------------|-------------------------|------|-------------------------|------|
| $\overline{\text{SCK1}}$ cycle time                              | $t_{\text{KCY9}}$ | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 800                     |      |                         | ns   |
|                                                                  |                   | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 1600                    |      |                         | ns   |
|                                                                  |                   | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$    | 3200                    |      |                         | ns   |
|                                                                  |                   |                                                       | 4800                    |      |                         | ns   |
| $\overline{\text{SCK1}}$ high/low-level width                    | $t_{\text{KH9}}$  | $V_{\text{DD}} = 4.5 \text{ to } 5.5 \text{ V}$       | $t_{\text{KCY9}}/2-50$  |      |                         | ns   |
|                                                                  | $t_{\text{KL9}}$  |                                                       | $t_{\text{KCY9}}/2-100$ |      |                         | ns   |
| SI1 setup time<br>(to $\overline{\text{SCK1}}\uparrow$ )         | $t_{\text{SIK9}}$ | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 100                     |      |                         | ns   |
|                                                                  |                   | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 150                     |      |                         | ns   |
|                                                                  |                   | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$    | 300                     |      |                         | ns   |
|                                                                  |                   |                                                       | 400                     |      |                         | ns   |
| SI1 hold time<br>(from $\overline{\text{SCK1}}\uparrow$ )        | $t_{\text{KS9}}$  |                                                       | 400                     |      |                         | ns   |
| SO1 output delay time<br>from $\overline{\text{SCK1}}\downarrow$ | $t_{\text{KSO9}}$ | $C = 100 \text{ pF}$ <b>Note</b>                      |                         |      | 300                     | ns   |
| $\text{STB}\uparrow$ from $\overline{\text{SCK1}}\uparrow$       | $t_{\text{SBD}}$  |                                                       | $t_{\text{KCY9}}/2-100$ |      | $t_{\text{KCY9}}/2+100$ | ns   |
| Strobe signal<br>high-level width                                | $t_{\text{SBW}}$  | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | $t_{\text{KCY9}}-30$    |      | $t_{\text{KCY9}}+30$    | ns   |
|                                                                  |                   | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$    | $t_{\text{KCY9}}-60$    |      | $t_{\text{KCY9}}+60$    | ns   |
|                                                                  |                   |                                                       | $t_{\text{KCY9}}-90$    |      | $t_{\text{KCY9}}+90$    | ns   |
| Busy signal setup time<br>(to busy signal<br>detection timing)   | $t_{\text{BYS}}$  |                                                       | 100                     |      |                         | ns   |
| Busy signal hold time<br>(from busy signal<br>detection timing)  | $t_{\text{BYH}}$  | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 100                     |      |                         | ns   |
|                                                                  |                   | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$    | 150                     |      |                         | ns   |
|                                                                  |                   | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$    | 200                     |      |                         | ns   |
|                                                                  |                   |                                                       | 300                     |      |                         | ns   |
| $\overline{\text{SCK1}}\downarrow$ from busy<br>inactive         | $t_{\text{SPS}}$  |                                                       |                         |      | $2t_{\text{KCY9}}$      | ns   |

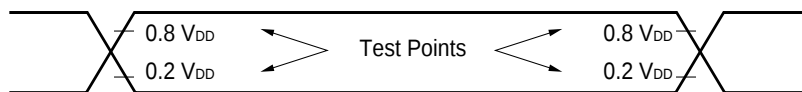
**Note** C is the load capacitance of  $\overline{\text{SCK1}}$  and SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ( $\overline{\text{SCK1}}$ ... External clock input)

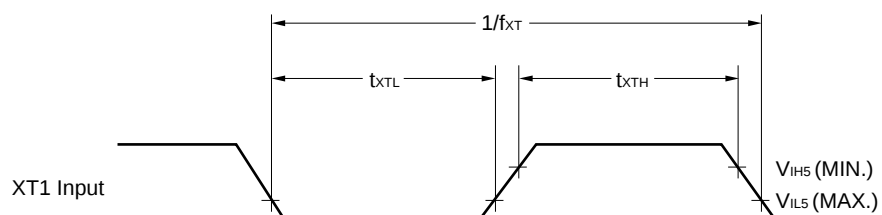
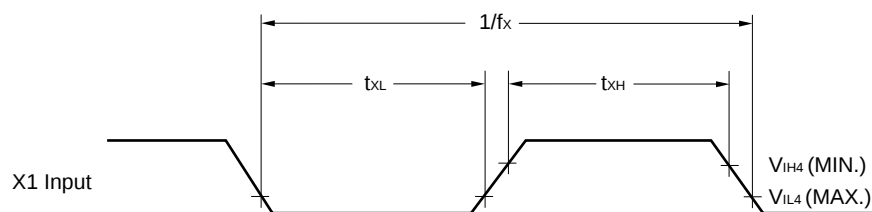
| Parameter                                                     | Symbol                             | Test Conditions                                                                  | MIN. | TYP. | MAX. | Unit |
|---------------------------------------------------------------|------------------------------------|----------------------------------------------------------------------------------|------|------|------|------|
| $\overline{\text{SCK1}}$ cycle time                           | $t_{\text{KCY10}}$                 | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$                            | 800  |      |      | ns   |
|                                                               |                                    | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$                               | 1600 |      |      | ns   |
|                                                               |                                    | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$                               | 3200 |      |      | ns   |
|                                                               |                                    |                                                                                  | 4800 |      |      | ns   |
| $\overline{\text{SCK1}}$ high/low-level width                 | $t_{\text{KH10}}, t_{\text{KL10}}$ | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$                            | 400  |      |      | ns   |
|                                                               |                                    | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$                               | 800  |      |      | ns   |
|                                                               |                                    | $2.0 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$                               | 1600 |      |      | ns   |
|                                                               |                                    |                                                                                  | 2400 |      |      | ns   |
| SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )         | $t_{\text{SIK10}}$                 | $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$                                  | 100  |      |      | ns   |
|                                                               |                                    |                                                                                  | 150  |      |      | ns   |
| SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )        | $t_{\text{KSI10}}$                 |                                                                                  | 400  |      |      | ns   |
| SO1 output delay time from $\overline{\text{SCK1}}\downarrow$ | $t_{\text{KSO10}}$                 | $C = 100 \text{ pF}$ <b>Note</b> $V_{\text{DD}} = 2.0 \text{ to } 5.5 \text{ V}$ |      |      | 300  | ns   |
|                                                               |                                    |                                                                                  |      |      | 500  | ns   |
| $\overline{\text{SCK1}}$ rise, fall time                      | $t_{\text{R10}}, t_{\text{F10}}$   | When external device expansion function is used                                  |      |      | 160  | ns   |
|                                                               |                                    | When external device expansion function is not used                              |      |      | 1000 | ns   |

**Note** C is the load capacitance of the SO1 output line.

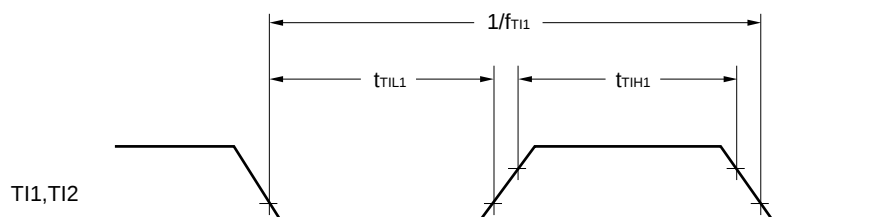
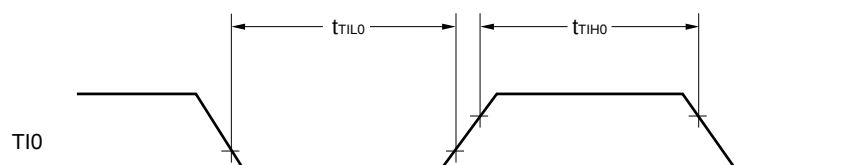
# AC Timing Test Point (Excluding X1, XT1 Input)



## Clock Timing

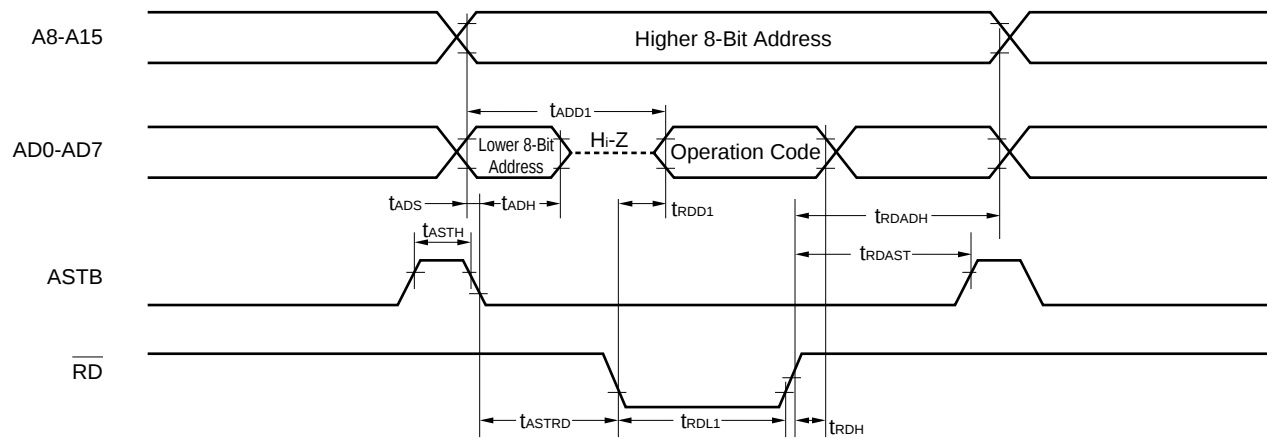


## TI Timing

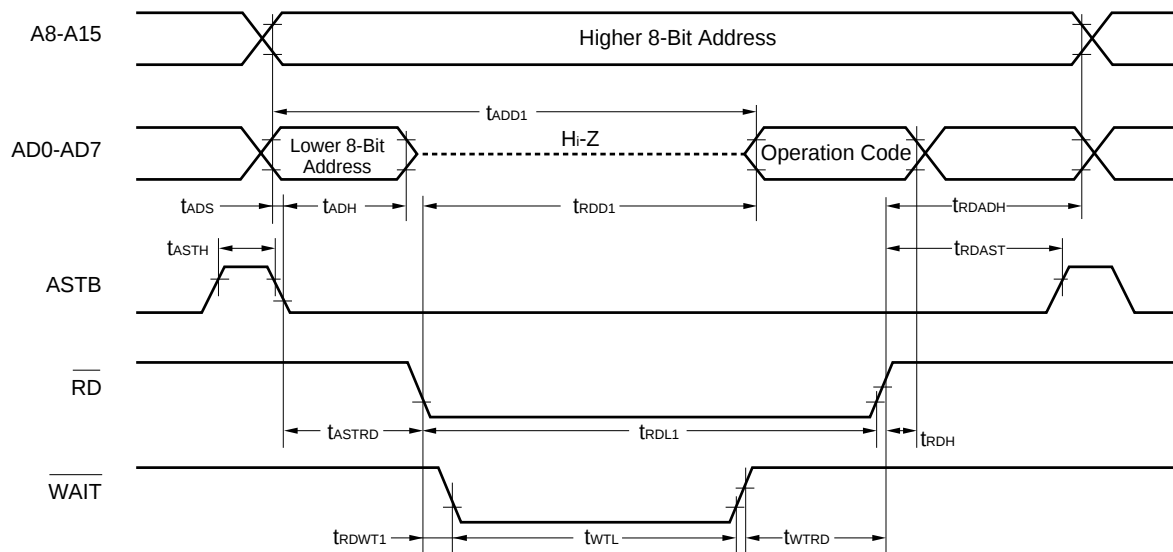


## Read/Write Operation

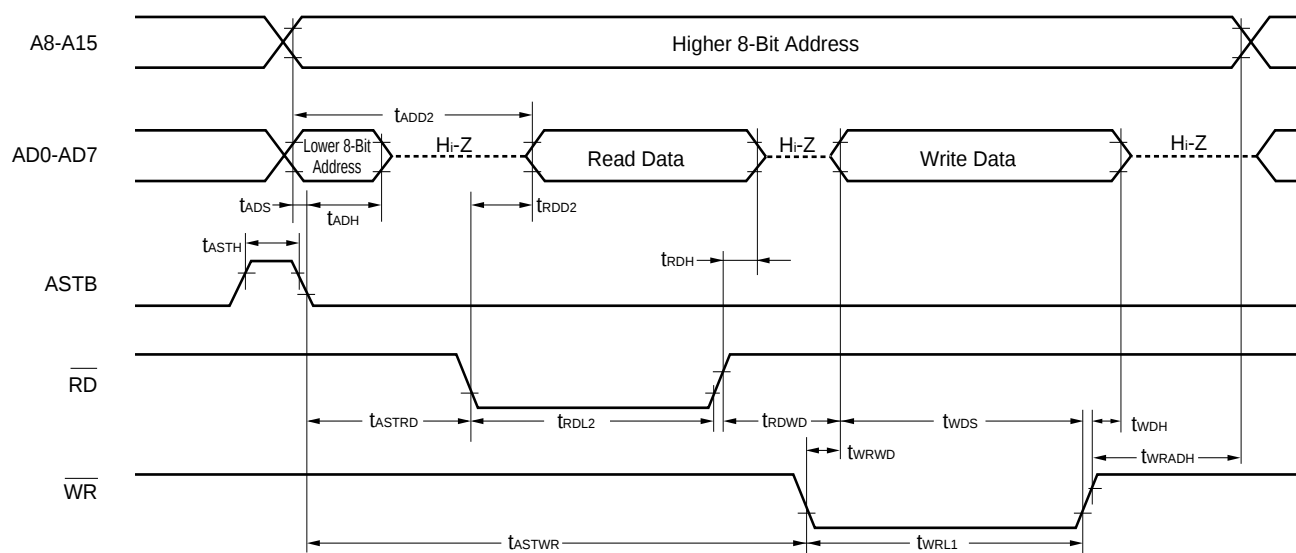
### External fetch (No wait):



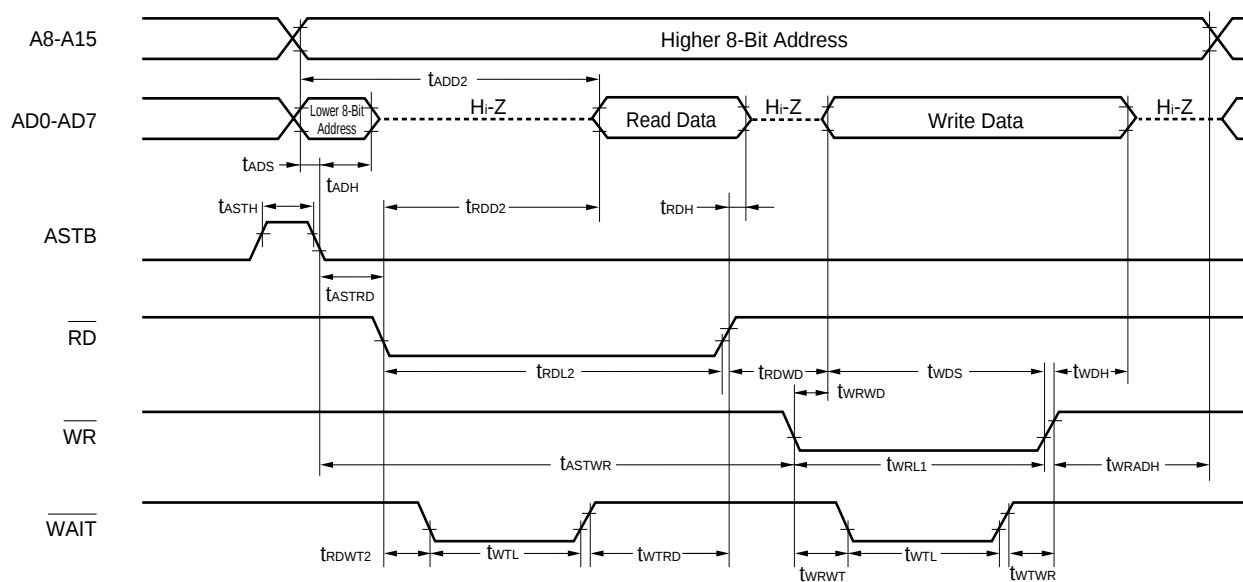
### External fetch (Wait insertion):



**External data access (No wait):**

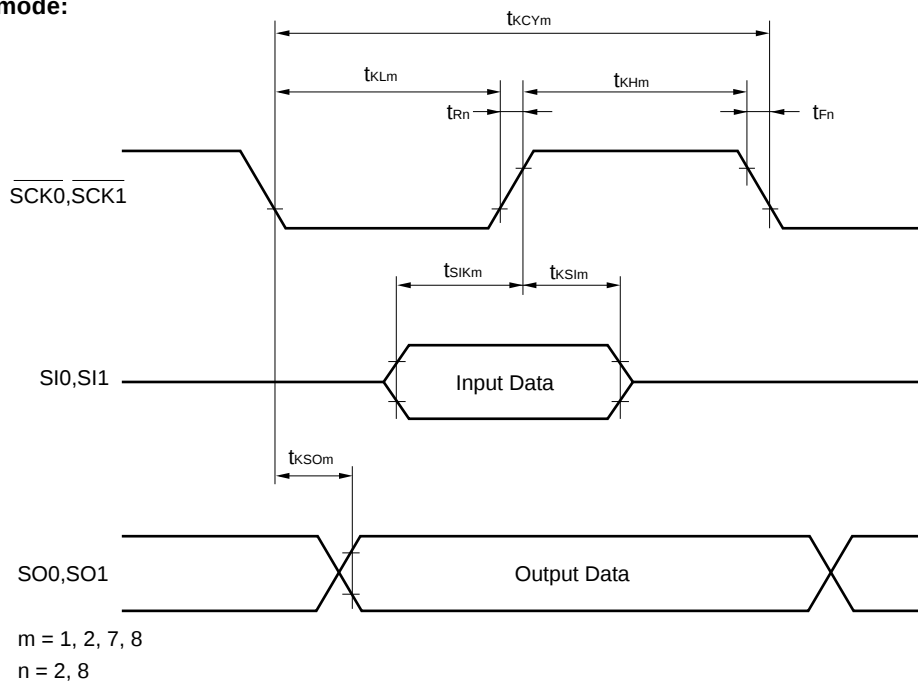


**External data access (Wait insertion):**

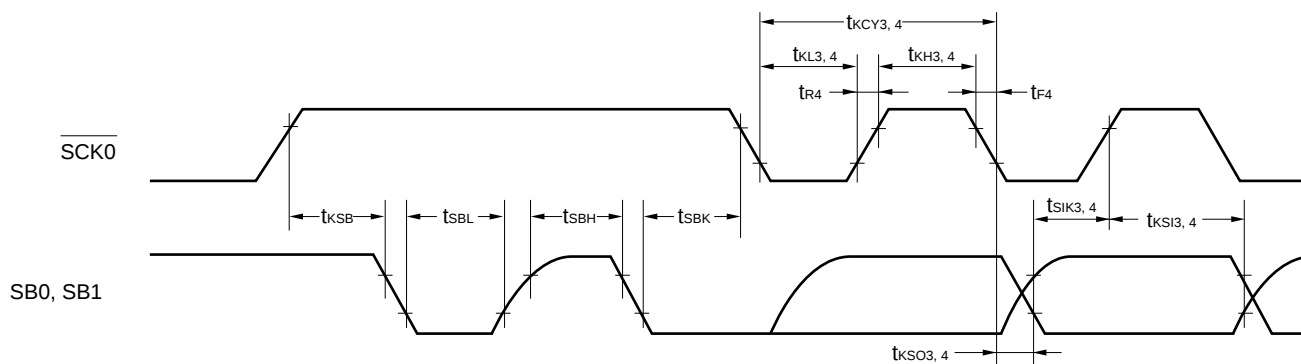


# Serial Transfer Timing

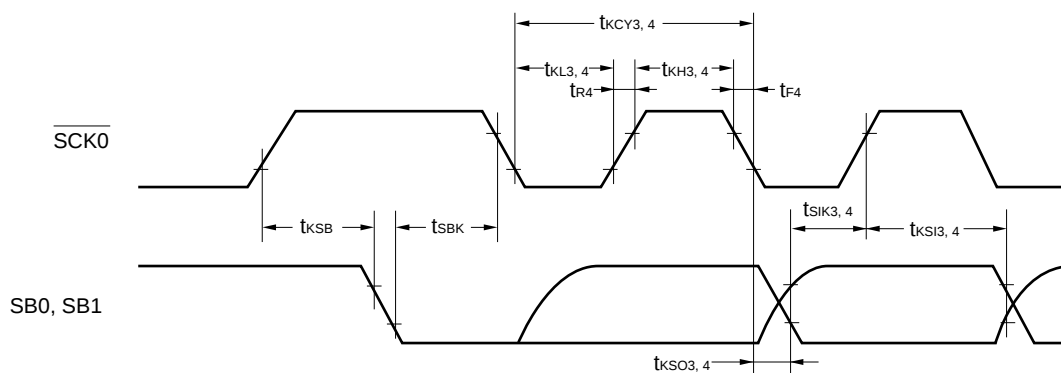
## 3-wire serial I/O mode:



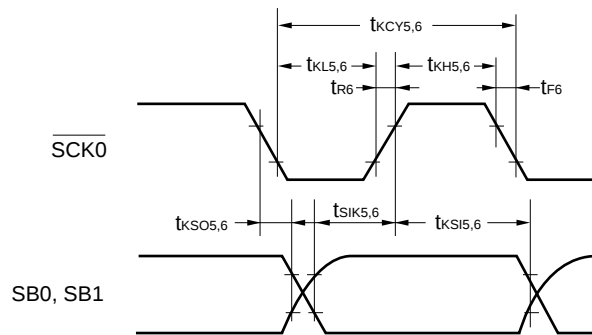
## SBI mode (Bus release signal transfer):



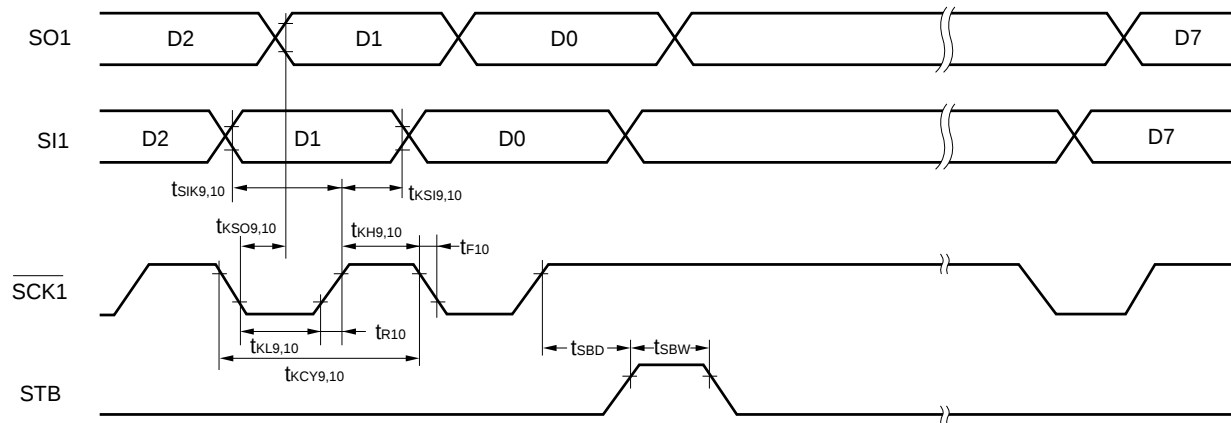
## SBI Mode (command signal transfer):



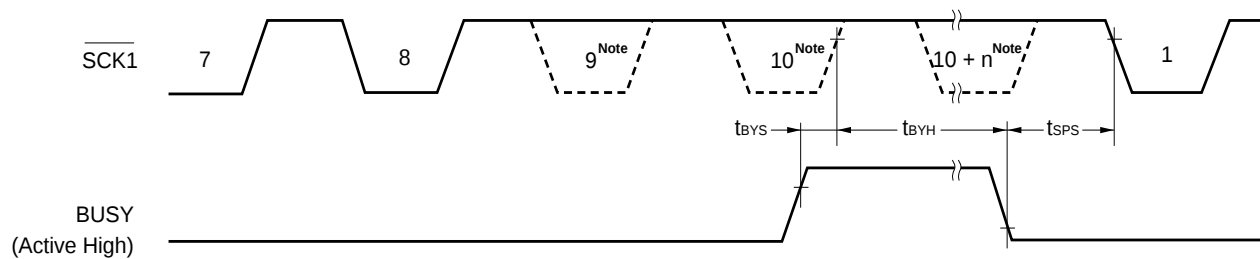
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



**Note** The signal is not actually driven low here; it is shown as such to indicate the timing.

**A/D converter characteristics** ( $T_A = -40$  to  $+85$  °C,  $AV_{DD} = V_{DD} = 1.8$  to  $5.5$  V,  $AV_{SS} = V_{SS} = 0$  V)

| Parameter                     | Symbol      | Test Conditions                                | MIN.      | TYP. | MAX.       | Unit |
|-------------------------------|-------------|------------------------------------------------|-----------|------|------------|------|
| Resolution                    |             |                                                | 8         | 8    | 8          | bit  |
| Overall error <b>Note</b>     |             | $2.7\text{ V} \leq AV_{REF} \leq AV_{DD}$      |           |      | 0.6        | %    |
|                               |             | $1.8\text{ V} \leq AV_{REF} \leq 2.7\text{ V}$ |           |      | 1.4        | %    |
| Conversion time               | $t_{CONV}$  | $2.0\text{ V} \leq AV_{DD} < 5.5\text{ V}$     | 19.1      |      | 200        | μs   |
|                               |             | $1.8\text{ V} \leq AV_{DD} < 2.0\text{ V}$     | 38.2      |      | 200        | μs   |
| Sampling time                 | $t_{SAMP}$  |                                                | $24/f_x$  |      |            | μs   |
| Analog input voltage          | $V_{IAN}$   |                                                | $AV_{SS}$ |      | $AV_{REF}$ | V    |
| Reference voltage             | $AV_{REF}$  |                                                | 1.8       |      | $AV_{DD}$  | V    |
| $AV_{REF}-AV_{SS}$ resistance | $RA_{IREF}$ |                                                | 4         | 14   |            | kΩ   |

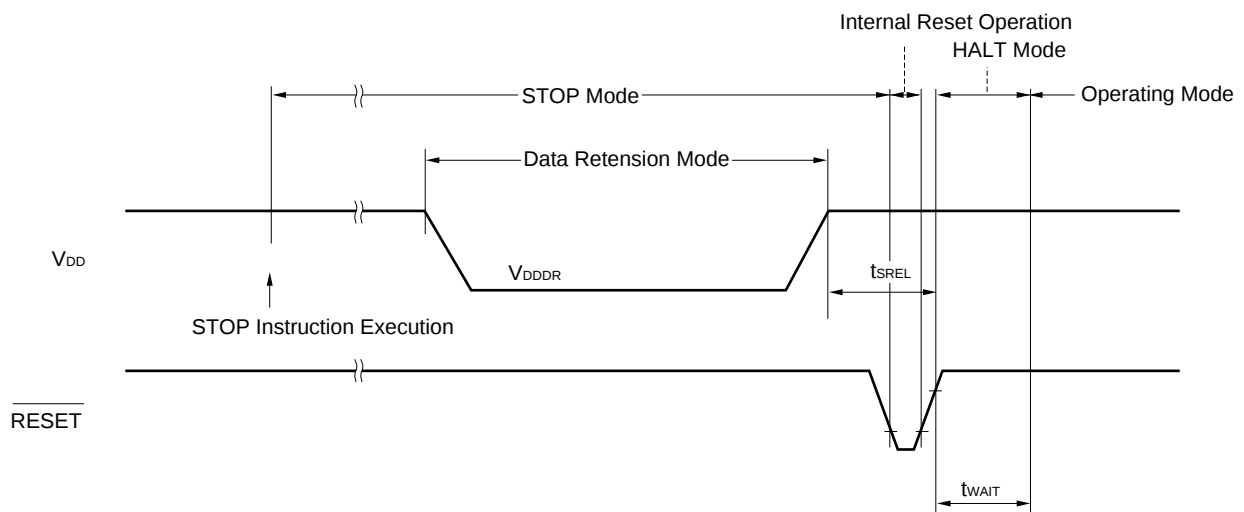
**Note** Overall error excluding quantization error ( $\pm 1/2$  LSB). It is indicated as a ratio to the full-scale value.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics** ( $T_A = -40$  to  $+85$  °C)

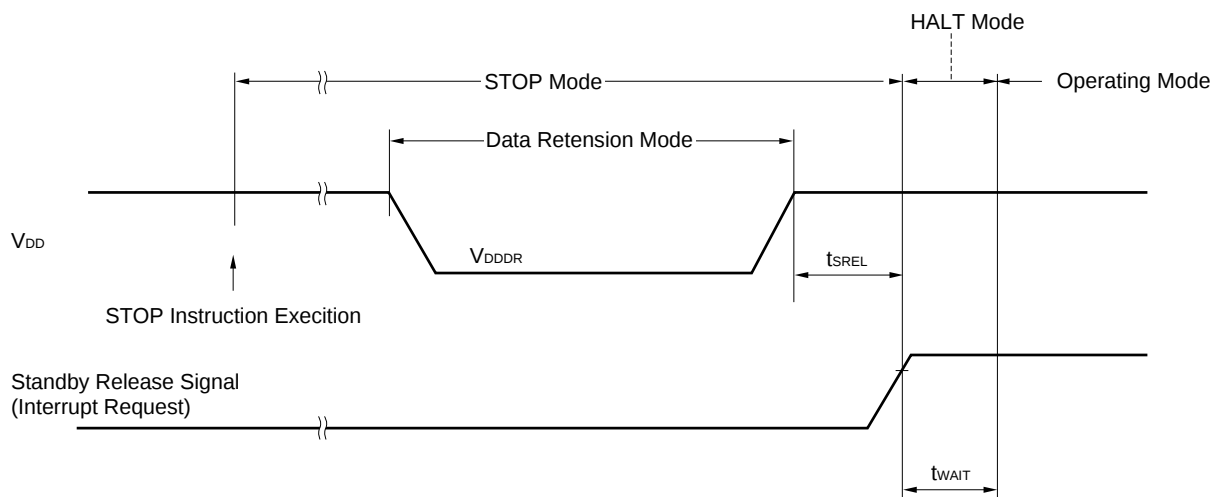
| Parameter                           | Symbol     | Test Conditions                                                                       | MIN. | TYP.         | MAX. | Unit |
|-------------------------------------|------------|---------------------------------------------------------------------------------------|------|--------------|------|------|
| Data retention supply voltage       | $V_{DDDR}$ |                                                                                       | 1.8  |              | 5.5  | V    |
| Data retention supply current       | $I_{DDDR}$ | $V_{DDDR} = 1.8\text{ V}$<br>Subsystem clock stop and feed-back resistor disconnected |      | 0.1          | 10   | μA   |
| Release signal set time             | $t_{SREL}$ |                                                                                       | 0    |              |      | μs   |
| Oscillation stabilization wait time | $t_{WAIT}$ | Release by $\overline{RESET}$                                                         |      | $2^{18}/f_x$ |      | ms   |
|                                     |            | Release by interrupt                                                                  |      | <b>Note</b>  |      | ms   |

**Note** In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of  $2^{13}/f_x$  and  $2^{15}/f_x$  to  $2^{18}/f_x$  is possible.

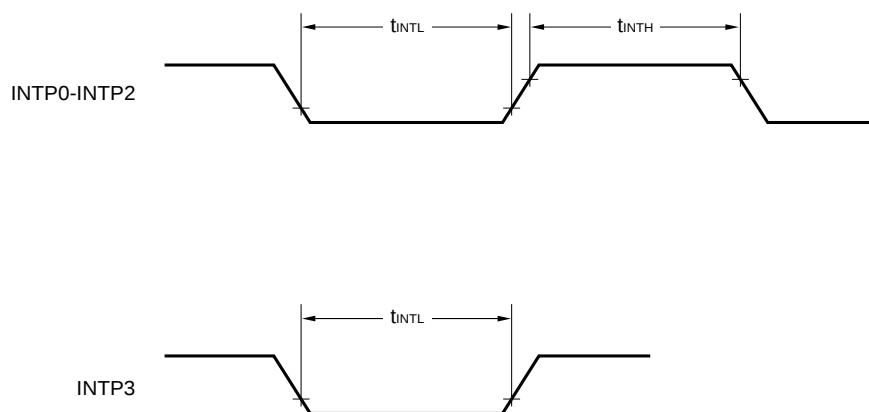
**Data Retention Timing (STOP Mode Release by  $\overline{RESET}$ )**



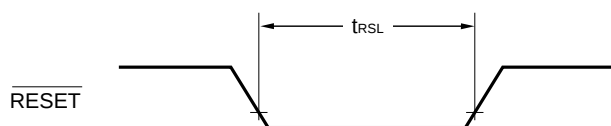
# Data Retention Timing (Standby Release Signal : STOP Mode Release by Interrupt Signal)



## Interrupt Input Timing

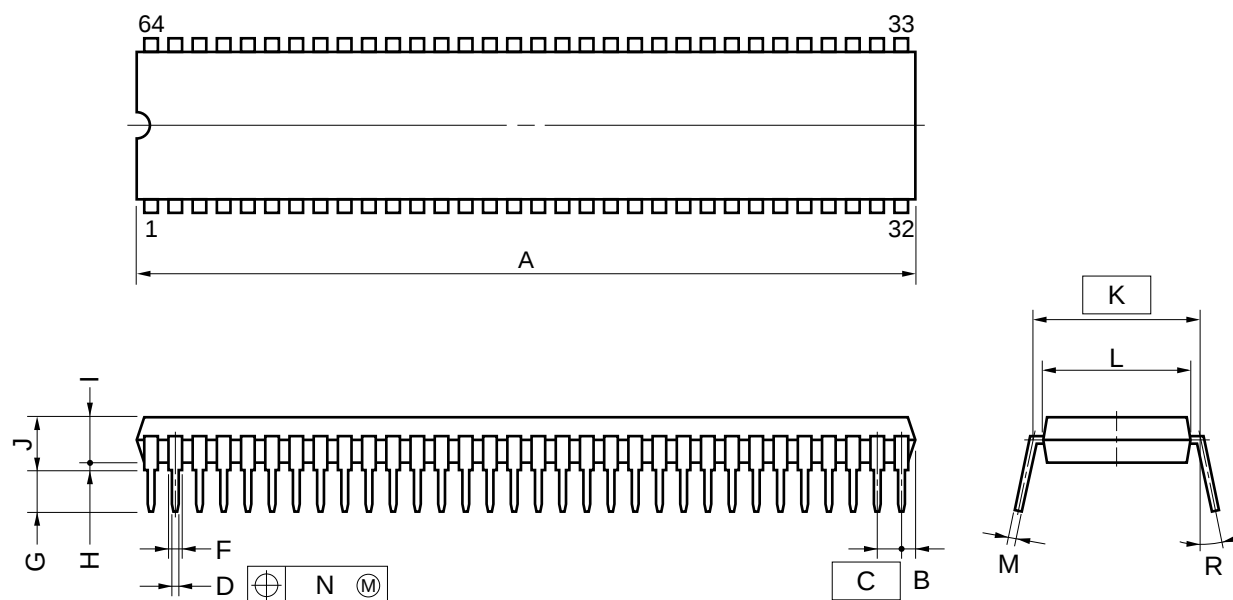


## $\overline{\text{RESET}}$ Input Timing



## 12. PACKAGE DRAWINGS

### 64 PIN PLASTIC SHRINK DIP (750 mil)



#### NOTE

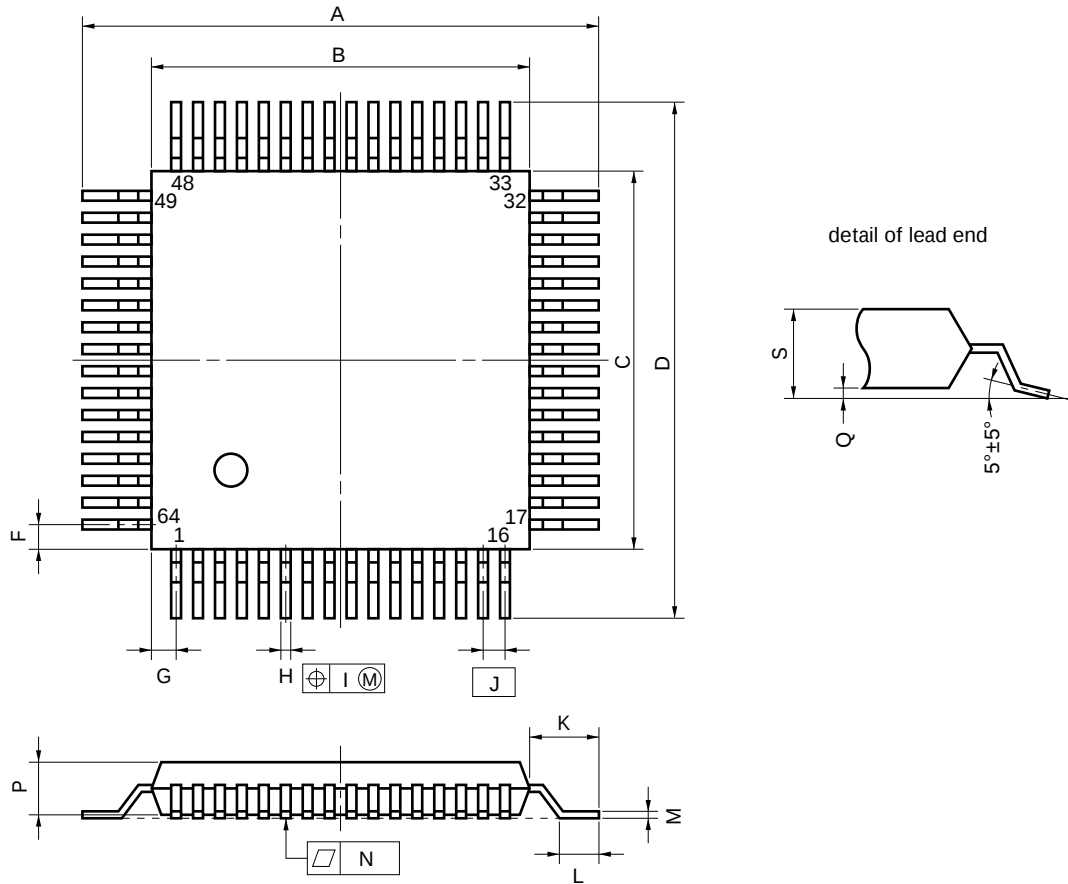
- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 58.68 MAX.                             | 2.311 MAX.                                |
| B    | 1.78 MAX.                              | 0.070 MAX.                                |
| C    | 1.778 (T.P.)                           | 0.070 (T.P.)                              |
| D    | 0.50±0.10                              | 0.020 <sup>+0.004</sup> <sub>-0.005</sub> |
| F    | 0.9 MIN.                               | 0.035 MIN.                                |
| G    | 3.2±0.3                                | 0.126±0.012                               |
| H    | 0.51 MIN.                              | 0.020 MIN.                                |
| I    | 4.31 MAX.                              | 0.170 MAX.                                |
| J    | 5.08 MAX.                              | 0.200 MAX.                                |
| K    | 19.05 (T.P.)                           | 0.750 (T.P.)                              |
| L    | 17.0                                   | 0.669                                     |
| M    | 0.25 <sup>+0.10</sup> <sub>-0.05</sub> | 0.010 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.17                                   | 0.007                                     |
| R    | 0~15°                                  | 0~15°                                     |

P64C-70-750A,C-1

**Remark** Dimensions and materials of ES products are the same as those of mass-production products.

64 PIN PLASTIC QFP (□14)



NOTE

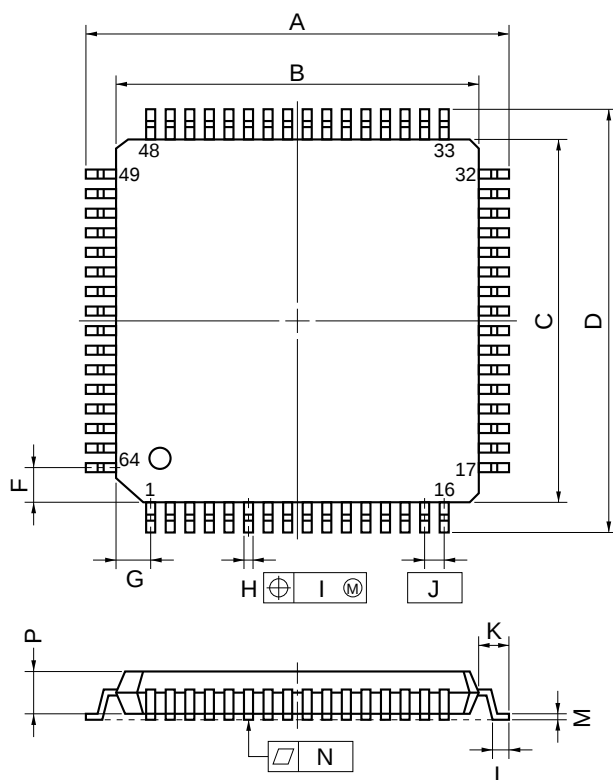
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-2

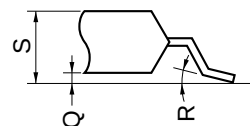
| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 17.6±0.4                               | 0.693±0.016                               |
| B    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 14.0±0.2                               | 0.551 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 17.6±0.4                               | 0.693±0.016                               |
| F    | 1.0                                    | 0.039                                     |
| G    | 1.0                                    | 0.039                                     |
| H    | 0.35±0.10                              | 0.014 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.15                                   | 0.006                                     |
| J    | 0.8 (T.P.)                             | 0.031 (T.P.)                              |
| K    | 1.8±0.2                                | 0.071±0.008                               |
| L    | 0.8±0.2                                | 0.031 <sup>+0.009</sup> <sub>-0.008</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 2.55                                   | 0.100                                     |
| Q    | 0.1±0.1                                | 0.004±0.004                               |
| S    | 2.85 MAX.                              | 0.112 MAX.                                |

**Remark** Dimensions and materials of ES products are the same as those of mass-production products.

## 64 PIN PLASTIC LQFP (□12)



detail of lead end

**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|----------------------------------------|-------------------------------------------|
| A    | 14.8±0.4                               | 0.583±0.016                               |
| B    | 12.0±0.2                               | 0.472 <sup>+0.009</sup> <sub>-0.008</sub> |
| C    | 12.0±0.2                               | 0.472 <sup>+0.009</sup> <sub>-0.008</sub> |
| D    | 14.8±0.4                               | 0.583±0.016                               |
| F    | 1.125                                  | 0.044                                     |
| G    | 1.125                                  | 0.044                                     |
| H    | 0.30±0.10                              | 0.012 <sup>+0.004</sup> <sub>-0.005</sub> |
| I    | 0.13                                   | 0.005                                     |
| J    | 0.65 (T.P.)                            | 0.026 (T.P.)                              |
| K    | 1.4±0.2                                | 0.055±0.008                               |
| L    | 0.6±0.2                                | 0.024 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.003</sub> |
| N    | 0.10                                   | 0.004                                     |
| P    | 1.4                                    | 0.055                                     |
| Q    | 0.125±0.075                            | 0.005±0.003                               |
| R    | 5°±5°                                  | 5°±5°                                     |
| S    | 1.7 MAX.                               | 0.067 MAX.                                |

P64GK-65-8A8-1

**Remark** Dimensions and materials of ES products are the same as those of mass-production products.

### 13. RECOMMENDED SOLDERING CONDITIONS

The  $\mu$ PD78011F/78012F/78013F/78014F/78015F/78016F should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our salespersonnel.

**Table 14-1. Surface Mounting Type Soldering Conditions (1/2)**

- (1)  $\mu$ PD78011HGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)  
 $\mu$ PD78012HGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)  
 $\mu$ PD78013HGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)  
 $\mu$ PD78014HGC-xxx-AB8 : 64-Pin Plastic QFP (14 × 14 mm)

| Soldering Method | Soldering Conditions                                                                                                                                            | Recommended Condition Symbol |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| Infrared reflow  | Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above),<br>Number of times: Thrice max.                                                  | IR35-00-3                    |
| VPS              | Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above),<br>Number of times: Thrice max.                                                  | VP15-00-3                    |
| Wave soldering   | Solder bath temperature: 260 °C max. Duration: 10 sec. max.<br>Number of times: Once<br>Preliminary heat temperature: 120 °C max. (Package surface temperature) | WS60-00-1                    |
| Partial heating  | Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)                                                                                           | —                            |

**Caution** Use more than one soldering method should be avoided (except in the case of partial heating).

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

- (2) μPD78011HGK-xxx-8A8: 64-Pin Plastic LQFP (12 × 12 mm)  
 μPD78012HGK-xxx-8A8: 64-Pin Plastic LQFP (12 × 12 mm)  
 μPD78013HGK-xxx-8A8: 64-Pin Plastic LQFP (12 × 12 mm)  
 μPD78014HGK-xxx-8A8: 64-Pin Plastic LQFP (12 × 12 mm)

| Soldering Method | Soldering Conditions                                                                                                                                                                                                                                                                                                                                                                           | Recommended Condition Symbol |
|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| Infrared reflow  | Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max., Number of days: 7 days <b>Note</b> (after that, 125 °C prebaking for 10 hours is necessary.)<br>< Points to note ><br>Products packed in packing materials other than heat-resistant trays (such as magazines, taping, and non-heat resistance tray) cannot be baked while packed. | IR35-107-2                   |
| VPS              | Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Twice max., Number of days: 7 days <b>Note</b> (after that, 125 °C prebaking for 10 hours is necessary.)<br>< Points to note ><br>Products packed in packing materials other than heat-resistant trays (such as magazines, taping, and non-heat resistance tray) cannot be baked while packed. | VP15-107-2                   |
| Wave soldering   | Solder bath temperature: 260 °C max. Duration: 10 sec. max.<br>Number of times: Once, Preliminary heat temperature: 120 °C max. (Package surface temperature), Number of days: 7 days <b>Note</b> (after that, 125 °C prebaking for 10 hours is necessary.)                                                                                                                                    | WS60-107-1                   |
| Partial heating  | Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)                                                                                                                                                                                                                                                                                                                          | —                            |

**Note** The number of days the device can be stored at 25 °C, 65% RH MAX. after the dry pack has been opened.

**Caution** Use more than one soldering method should be avoided (except in the case of partial heating).

Table 14-2. Insertion Type Soldering Conditions

- μPD78011HCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)  
 μPD78012HCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)  
 μPD78013HCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)  
 μPD78014HCW-xxx : 64-Pin Plastic Shrink DIP (750 mil)

| Soldering Method          | Soldering Conditions                                         |
|---------------------------|--------------------------------------------------------------|
| Wave soldering (pin only) | Solder bath temperature: 260°C max., Duration: 10 sec. max.  |
| Partial heating           | Pin temperature: 300°C max., Duration: 3 sec. max. (per pin) |

**Caution** Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.

## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for the development of systems using the μPD78014H subseries.

### Language processor software

|                             |                                                       |
|-----------------------------|-------------------------------------------------------|
| RA78K/0 Notes 1, 2, 3, 4    | Assembler package common to 78K/0 series              |
| CC78K0 Notes 1, 2, 3, 4     | C compiler package common to 78K/0 series             |
| DF78014 Notes 1, 2, 3, 4, 6 | Device file common to μPD78014 subseries              |
| CC78K0-L Notes 1, 2, 3, 4   | C compiler library source file common to 78K/0 series |

### Debugging tools

|                                                 |                                                                                                                                                                                           |
|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IE-78000-R                                      | In-circuit emulator common to 78K/0 series                                                                                                                                                |
| IE-78000R-A Notes 8                             | In-circuit emulator common to 78K/0 series (for integrated debugger)                                                                                                                      |
| IE-78000-R-BK                                   | Break board common to 78K/0 series                                                                                                                                                        |
| IE-78014-R-EM-A                                 | Emulation board common to μPD78018F and 78018FY subseries (V <sub>DD</sub> = 3.0 to 6.0 V)                                                                                                |
| EP-78240CW-R<br>EP-78240GK-R                    | Emulation probe common to μPD78244 subseries                                                                                                                                              |
| EP-78012GK-R                                    | Emulation probe common to μPD78018F subseries                                                                                                                                             |
| EV-9200GC-64                                    | Socket mounted on printed wiring board of target system created for 64-pin plastic QFP (GC-AB8 type)                                                                                      |
| TGK-064SBW                                      | Adapter mounted on printed wiring board of target system created for 64-pin plastic QFP (GK-8A8 type). This is a product of TOKYO ELETECH Corp. Consult NEC when purchasing this product. |
| SM78K0 Notes 5, 6, 7<br>ID78K0 Notes 4, 5, 6, 7 | System emulator common to 78K/0 series<br>Integrated debugger common to 78K/0 series                                                                                                      |
| SD78K/0 Notes 1, 2                              | Screen debugger for IE-78000-R                                                                                                                                                            |
| DF78014 Notes 1, 2, 3, 4, 5, 6, 7               | Device file common to μPD78014 subseries                                                                                                                                                  |

### Real-Time OS

|                    |                               |
|--------------------|-------------------------------|
| RX78K/0 Notes 1, 2 | Real-time OS for 78K/0 series |
| MX78K0 Notes 1, 2  | OS for 78K/0 series           |

**Fuzzy Inference Development Support System**

|                                            |                                    |
|--------------------------------------------|------------------------------------|
| FE9000 <b>Note 1</b> /FE9200 <b>Note 6</b> | Fuzzy knowledge data creation tool |
| FT9080 <b>Note 1</b> /FT9085 <b>Note 2</b> | Translator                         |
| FI78K0 <b>Notes 1, 2</b>                   | Fuzzy inference module             |
| FD78K0 <b>Notes 1, 2</b>                   | Fuzzy inference debugger           |

**Notes 1.** PC-9800 series (MS-DOS™) based

2. IBM PC/AT™ and compatible machine (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS-4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible machine (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development.

**Remarks 1.** For development tools manufactured by a third party, refer to the **78K/0 Series Selection Guide (U11126E)**.

2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF78014.

## APPENDIX B. RELATED DOCUMENTS

## Device Related Documents

| Document Name                                      | Document No.       |                    |
|----------------------------------------------------|--------------------|--------------------|
|                                                    | Japanese           | English            |
| μPD78014H Subseries User's Manual                  | Planned to publish | Planned to publish |
| μPD78014 Data Sheet                                | U11898J            | This manual        |
| 78K/0 Series User's Manual - Instruction           | IEU-849            | IEU-1372           |
| 78K/0 Series Instruction List                      | U10903J            | —                  |
| 78K/0 Series Instruction Set                       | U10904J            | —                  |
| μPD78014H Subseries Special Function Register List | Planned to publish | —                  |

## Development Tools Documents (User's Manual)

| Document Name                                  |                                         | Document No. |          |
|------------------------------------------------|-----------------------------------------|--------------|----------|
|                                                |                                         | Japanese     | English  |
| RA78K Series Assembler Package                 | Operation                               | EEU-809      | EEU-1399 |
|                                                | Language                                | EEU-815      | EEU-1404 |
| RA78K Series Structured Assembler Preprocessor |                                         | EEU-817      | EEU-1402 |
| CC78K Series C Compiler                        | Operation                               | EEU-656      | EEU-1280 |
|                                                | Language                                | EEU-655      | EEU-1284 |
| CC78K/0 C Compiler Application Note            | Programming Know-how                    | EEA-618      | EEA-1208 |
| CC78K Series Library Source File               |                                         | EEU-777      | —        |
| IE-78000-R                                     |                                         | EEU-810      | U11376E  |
| IE-78000-R-A                                   |                                         | U10057J      | U10057E  |
| IE-78000-R-BK                                  |                                         | EEU-867      | EEU-1427 |
| IE-78014-R-EM-A                                |                                         | EEU-962      | U10418E  |
| EP-78240                                       |                                         | EEU-986      | EEU-1513 |
| EP-78012GK-R                                   |                                         | EEU-5012     | EEU-1538 |
| SM78K0 System Simulator Windows Based          | Reference                               | U10181J      | U10181E  |
| SM78K Series System Simulator                  | External Components User Open Interface | U10092J      | U10092E  |
| ID78K0 Integrated Debugger EWS Based           | Reference                               | U11151J      | —        |
| ID78K0 Integrated Debugger PC Based            | Reference                               | U11539J      | —        |
| ID78K0 Integrated Debugger Windows Based       | Guide                                   | U11649J      | —        |
| SD78K/0 Screen Debugger                        | Introduction                            | EEU-852      | —        |
| PC-9800 Series (MS-DOS) Based                  | Reference                               | EEU-816      | —        |
| SD78K/0 Screen Deb                             | Introduction                            | EEU-5024     | EEU-1414 |
| IBM PC/AT (PC DOS) Based                       | Reference                               | EEU-993      | EEU-1413 |

**Caution** The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

### Embedded Software Documents (User's Manual)

| Document Name                                                                         |              | Document No. |          |
|---------------------------------------------------------------------------------------|--------------|--------------|----------|
|                                                                                       |              | Japanese     | English  |
| 78K/0 Series Real-Time OS                                                             | Fundamental  | U11537J      | —        |
|                                                                                       | Installation | U11536J      | —        |
|                                                                                       | Technical    | U11538J      | —        |
| 78K/0 Series OS MX78K0                                                                | Fundamental  | EEU-5010     | —        |
| Fuzzy Knowledge Data Creation Tool                                                    |              | EEU-829      | EEU-1438 |
| 78K/0, 78K/II, 87AD Series<br>Fuzzy Inference Development Support System - Translator |              | EEU-862      | EEU-1444 |
| 78K/0 Series Fuzzy Inference Development Support System -<br>Fuzzy Inference Module   |              | EEU-858      | EEU-1441 |
| 78K/0 Series Fuzzy Inference Development Support System -<br>Fuzzy Inference Debugger |              | EEU-921      | EEU-1458 |

### Other Documents

| Document Name                                                 |  | Document No. |          |
|---------------------------------------------------------------|--|--------------|----------|
|                                                               |  | Japanese     | English  |
| IC Package Manual                                             |  | C10943X      |          |
| Semiconductor Device Mounting Technology Manual               |  | C10535J      | C10535E  |
| Quality Grades on NEC Semiconductor Device                    |  | C11531J      | IEI-1209 |
| NEC Semiconductor Device Reliability/Quality Control System   |  | C10983J      | C10983E  |
| Electrostatic Discharge (ESD) Test                            |  | MEM-539      | —        |
| Guide to Quality Assurance for Semiconductor Device           |  | MEI-603      | MEI-1202 |
| Guide for Products Related to Micro-Computer: Other Companies |  | U11416J      | —        |

**Caution** The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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