SPICoder® SA01 UR5HCSPI-SA01

Very Low-Power Keyboard Encoder and Power Management IC for H/PCs

HID & SYSTEM MANAGEMENT PRODUCTS, KEYCODER® FAMILY **PRELIMINARY**

DESCRIPTION

The SPICoder® SA01 UR5HCSPI-SA01, a member of Semtech's KeyCoder® product family, is a keyboard encoder and power management IC designed specifically for handheld PCs (H/PCs), web phones and other systems that run Microsoft® Windows® CE and utilize the Intel StrongARM™ processor.

The SPICoder® SA01 offers several features necessary to H/PCs, including extremely low power consumption, real estate-saving size, and special keyboard modes.

The IC consumes an extremely small amount of power (less than 2 µA at 3V) and provides the host system both power management and I/O flexibility, with minimal battery drainage.

Special keyboard modes and built-in power management features allow the SPICoder® SA01 to operate in harmony with the power management modes of Windows® CE, resulting in greater user flexibility, and longer battery life.

The IC scans, debounces and encodes an 8 x 14 keyboard matrix. It communicates with the host over the SPI channel, implementing a high-reliability two-way protocol. The SPICoder® SA01 also offers programmable features for wake-up keys and general purpose I/O pins.

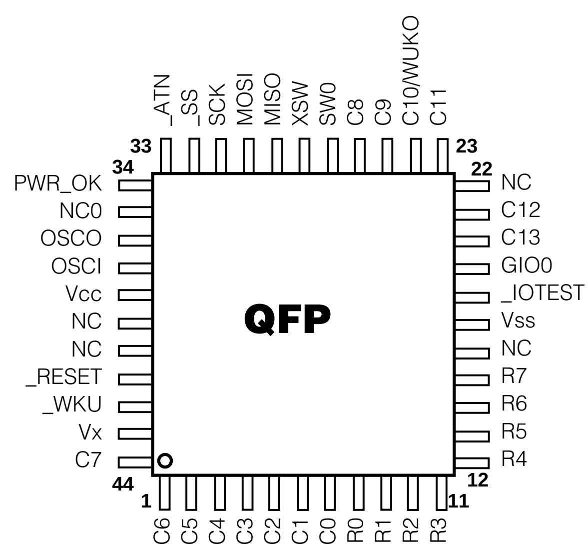
FEATURES

- SPI-compatible keyboard encoder and power management IC
- Ideal for use with the Intel StrongARM™ processor
- Patented technology for extremely low power consumption — typically less than 2 µA between 3-5V
- Offers overall system power management capabilities
- Available in low-profile QFP package
- Implements high-reliability two-way protocol
- Fully compatible with the Windows® CE keyboard specification
- Works in harmony with the power management modes of Windows® CE
- Provides special modes of operation for H/PCs, including programmable "wake-up" keys
- Scans an 8 x 14 matrix; controls discrete switches and LED indicators
- Compatible with "system-on silicon" CPUs for H/PCs

APPLICATIONS

- StrongARM™ handheld PCs
- Windows® CE platforms
- Web phones
- Personal digital assistants (PDAs)
- Wearable computers
- Internet appliances

PIN ASSIGNMENTS



UR5HCSPI-SA01-FB
44-pin QFP
(0.80 mm pitch
(10x10 mm)

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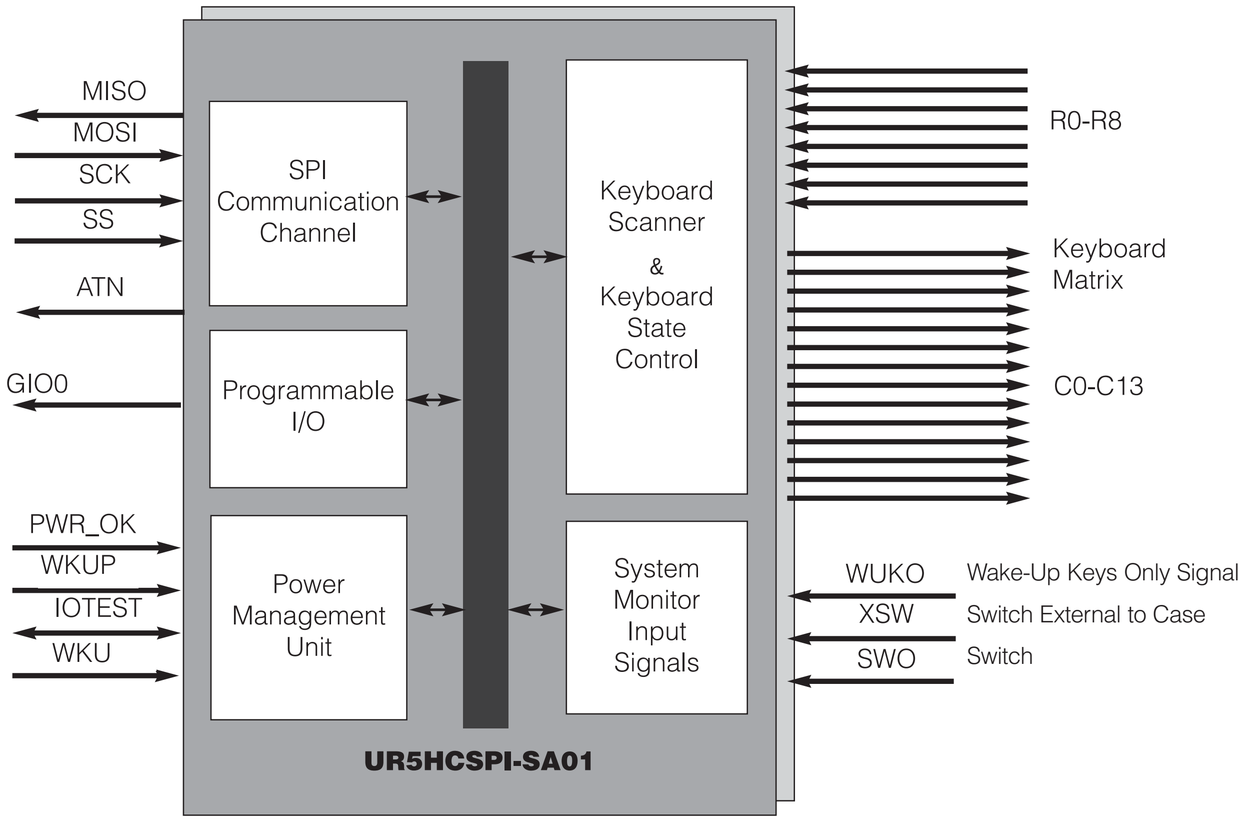
ORDERING CODE

Package options	Pitch	T_A = -40°C to +85°C
44-pin plastic QFP	0.8 mm	UR5CSPI-SA-FB

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SPICoder® SA01 consists functionally of five major sections (see the block diagram). These are the Keyboard Scanner and State control, the Programmable I/O, the SPI Communication Channel, the System Monitor and the Power Management unit. All sections communicate with each other and operate concurrently.

PIN DEFINITIONS

Mnemonic	QFP	Type	Name and Function
VCC	38	I	**Power supply:** 3-5V
VSS	17	I	**Ground**
VX	43	I	Tie VX to VCC
OSCI	37	I	**Oscillator input**
OSCO	36	O	**Oscillator output**
_RESET	41	I	**Reset:** apply 0V to provide orderly start-up
MISO	29	O	**SPI interface signals**
MOSI	30	I	
SCK	31	I	
_SS	32	I	**Slave Select:** If not used tie to VSS
_IOTEST	18	O	**Wake-up control signals**
_WKU	42	I	
R0-R4	8-12	I	**Row data inputs**
R5-R7	13-15	I	Port provides internal pull-up resistors
C0-C5	7-2	O	**Column select outputs**
C6-C7	1,44	O	
C8-C9	26-25	O	
C11	23	O	
C12	21	O	
C13	20	O	
			Multi-function pin
C10/WUKO	24	I/O	C10 & "Wake-Up Keys Only" input
			Miscellaneous functions
GI00	19	I/O	General programmable I/O
XSW	28	I	External discrete switch
SWO	27	I	Discrete switch
			Power management pins
_ATN	33	O	CPU attention output
PWR_OK	34	I	Power OK input
NC	16, 22 39, 40		**No Connects**: these pins are unused
NC0	35		NC0 should be tied to VSS or GND

Note: An underscore before a pin mnemonic denotes an active low signal.

PIN DESCRIPTIONS

VCC and VSS

VCC and VSS are the power supply and ground pins. The SPICoder® SA01 operates from a 3-5 Volt power supply. To prevent noise problems, provide bypass capacitors placed as close as possible to the IC with the power supply. VX, where available, should be tied to Vcc.

OSCI and OSCO

OSCI and OSCO provide the input and output connections for the on-chip oscillator. The oscillator can be driven by any of the following circuits:

- Crystal
- Ceramic resonator
- External clock signal

The frequency of the on-chip oscillator is 2.00 MHz.

_RESET

A logic zero on the _RESET pin forces the SPICoder® SA01 into a known start-up state. The reset signal can be supplied by any of the following circuits:

- Resistor/capacitor
- Voltage monitor
- Master system reset

MOSI, MISO, SCK, _SS, _ATN

These five signals implement the SPI interface. The device acts as a slave on the SPI bus. The _SS (Slave Select) pin must go high between successive characters in an SPI message or a write collision error results. The _ATN pin is asserted low each time the SPICoder® SA01 has a packet ready for delivery. For a more detailed description, refer to the SPI Communication Channel section of this document.

_IOTEST and _WKU

The_IOTEST and _WKU pins (“Input Output Test” and “Wake Up”) pins control the stop mode exit of the device. The designer can connect any number of active low signals to these two pins through a 15KΩ resistor, in order to force the device to exit the stop mode. A sample circuit is included in this document. All the signals are “wire-anded.” When any one of these signals is not active, it should be floating (i.e., these signals should be driven from “open-collector” or “open-drain” outputs).

R0 - R7

The R0-R7 pins are connected to the rows of the scanned matrix. Each pin provides an internal pull-up resistor, eliminating the need for external components.

C0 to C9 and C11

Pins C0 to C9 are bi-directional pins and are connected to the columns of the scanned matrix. When a column is selected, the pin outputs an active low signal. When the column is de-selected, the pin turns into high-impedance.

C10 / WUKO

The C10 / WUKO pin acts alternatively as column scan output and as an input. As an input, the pin detects the “Wake-Up Keys Only” signal, typically provided by the host CPU to indicate that the user has turned the unit off. When the device detects an active high state on this pin, it feeds this information into the “Keyboard State Control” unit, in order to disable the keyboard and enable the programmed wake-up keys.

To achieve maximum power savings, the resistor connected to WUKO can be as large as 1.5 MΩ.

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PIN DESCRIPTIONS (CONT'D)

C12 and C13

C12 and C13 are used as additional column pins in order to accommodate larger-size keyboards, such as the Fujitsu FKB1406 palmtop keyboard.

GIO0

GIO0 is a programmable input/output switch or LED pin; it can also be used as a wake-up signal. Its programming is explained in the General Purpose I/O Pin section of this document.

XSW

The XSW pin is dedicated to an external switch. This pin is handled differently than the rest of the switch matrix and is intended to be connected to a switch physically located on the outside of the unit.

SW0

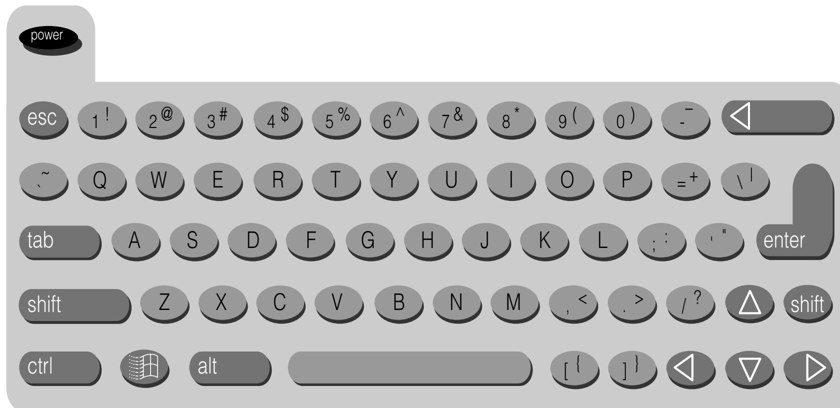
The SW0 pin is a dedicated input pin for a switch.

PWR_OK

The PWR_OK is an active low pin that monitors the battery status of the unit. When the SPICoder® SA01 detects a transition from high to low on this pin, it immediately enters the STOP mode, turns the LED off, and remains in this state until the batteries of the unit are replaced and the signal is deasserted.

THE WINDOWS® CE KEYBOARD

The following illustration shows a typical implementation of a Windows® CE keyboard.



Windows® CE does not support the following keyboard keys typically found on desktop and laptop keyboards:

- INSERT
- SCROLL LOCK
- PAUSE
- NUM LOCK
- Function Keys (F1-F12)
- PRINT SCREEN

If the keyboard implements the Windows key, the following key combinations are supported in the Windows® CE environment:

Key Combination	Result
Windows	Open Start Menu
Windows+K	Open Keyboard Tool
Windows+I	Open Stylus Tool
Windows+C	Open Control Panel
Windows+E	Explore the H/PC
Windows+R	Display the Run Dialog Box
Windows+H	Open Windows® CE Help
Ctrl+Windows+A	Select all on desktop

"GHOST" KEYS

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is sensed as being pressed. This is known as the "ghost" or "phantom" key problem.

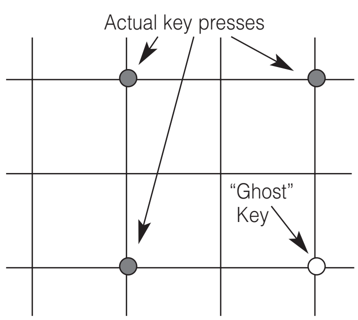


Figure 1: "Ghost" or "Phantom" Key Problem

Although the problem cannot be totally eliminated without using external hardware, there are methods to neutralize its negative effects for most practical applications. Keys that are intended to be used in combinations should be placed in the same row or column of the matrix, whenever possible. Shift keys (Shift, Alt, Ctrl, Windows) should not reside in the same row (or column) as any other keys. The SPICoder® SA01 has built-in mechanisms to detect the presence of "ghost" keys.

KEYBOARD SCANNER

The encoder scans a keyboard organized as an 8 row by 14 column matrix for a maximum of 112 keys. Smaller size matrixes can be accommodated by simply leaving unused pins open. The SPICoder® SA01 provides internal pull-ups for the row input pins. When active, the encoder selects one of the column lines (C0-C13) every 512 µs and then reads the row data lines (R0-R7). A key closure is detected as a zero in the corresponding position of the matrix.

A complete scan cycle for the entire keyboard takes approximately 9.2 ms. Each key found pressed is debounced for a period of 20 ms. Once the key is verified, the corresponding key code(s) are loaded into the transmit buffer of the SPI communication channel.

KEYBOARD SCANNING

N-Key Rollover

In this mode, the code(s) corresponding to each key press are transmitted to the host system as soon as that key is debounced, independent of the release of other keys.

When a key is released, the corresponding break code is transmitted to the host system. Several keys can be held pressed at the same time. However, two or more key closures, occurring within a time interval of less than 5 ms, raise an error flag and are not processed. This feature iprotects against the effects of accidental key presses.

KEYBOARD STATES

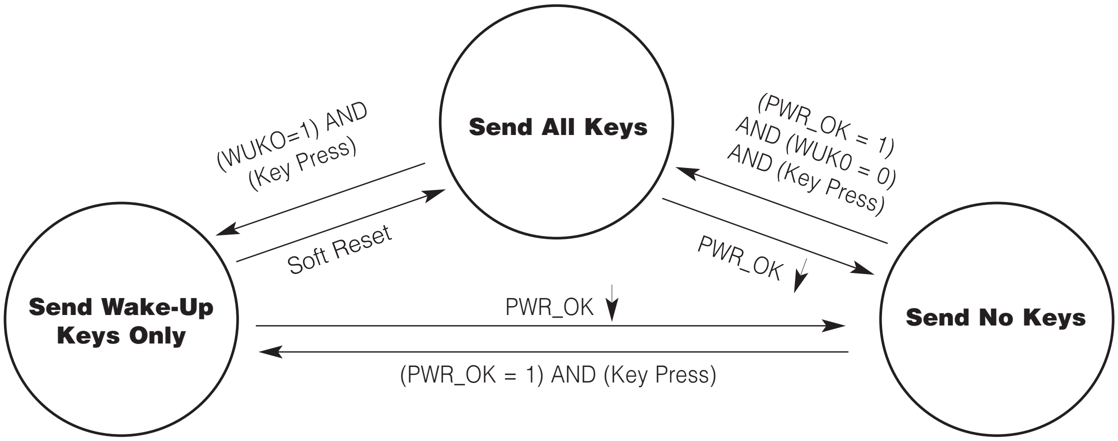


Figure 2: The SPICoder® SA01 implements three modes of keyboard and switch operation

These states of operation refer only to the keyboard functionality and, although they are related to power states, they are also independent of them.

"Send All Keys"

Entry Conditions: Power on reset, soft reset, PWR_OK =1, {(WUKO=0)}

Exit Conditions: PWR_OK = 0 -> "Send No Keys"(WUKO=1) AND (Key Press) -> "Send Wake-Up Keys Only"(LID = 0) AND (WUKO=0) AND (Key Press) -> "Send XSW Key Only"

Description: This is the SPICoder® SA01's normal state of operation, accepting and transmitting every key press to the system. This state is entered after the user powers on the unit and it is sustained while the unit is being used.

"Send Wake-Up Keys Only"

Entry Conditions:(WUKO=1) AND (Key or Switch press)

Exit Conditions: Soft Reset -> "Send All Keys"PWR_OK = 0 -> "Send No Keys"

Description:This state is entered when the user turns the unit off. A signal line driven by the host notifies the SPICoder® SA01 about this state transition. While in this state, the SPICoder® SA01 transmits only keys programmed to be wake-up keys to the system. It is not necessary for the SPICoder® SA01 to detect this transition in real time, since it does not affect any operation besides buffering keystrokes.

"Send No Keys"

Entry Conditions:PWR_OK transition from high to low

Exit Conditions: (PWR_OK = 1) AND (Matrix key pressed OR Switch OR _WKUP)

Description: This state is entered when a PWR_OK signal is asserted (transition high to low), indicating a critically low level of battery voltage. The PWR_OK signal causes an interrupt to the SPICoder® SA01, which guarantees that the transition is performed in real time. In this state, the SPICoder® SA01 performs as follows:

1. The LED is turned off. Nevertheless, its state is saved and restored after exiting the disabled state (change of batteries).

2. The SPICoder® SA01 enters the STOP mode for maximum energy conservation.

3 Stop mode time-out entry is shortened to conserve energy further.

4. In this state all interrupts are disabled. The SPICoder® SA01 exits this state on the next interrupt event that detects the PWR_OK line has been de-asserted.

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KEY MAP FOR THE FUJITSU FKB1406 (SPICODER® SA01)

Columns (C0–C13) / **Rows (R0–R6)**

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0	LAlt	`		LCtrl	FN	Esc	1 F1	2 F2	9 F9	0 F10	- NmLk	+ Bk		BkSp
1		\	LSft			Del		T	Y	U Pad 4	I Pad 5	Enter	RShift	↓ PgDn
2		TAB				Q	W	E	R	O Pad 6	P Ins	[Pause		] ScrLk
3		Z				CapLk			K Pad 2	L Pad 3	; PrtScr	' SysReq		↑ PgUp
4		A				S	D	F	G	H	J Pad 1	/ /		← Home
5		X				C	V	B	N Pad 0	M	,	.		Spc
6						3 F3	4 F4	5 F5	6 F6	7 F7	8 F8	Prog		→ End

KEYBOARD LAYOUT FOR THE FUJITSU FKB1406

KEY CODES

Key codes range from 0x01 to 0x73 and are arranged as follows:

Make code = column_number * 8 + row_number + 1

Break code = Make code OR 0x80

Discrete Switches transmit the following codes:

XSW = 0x71

SW0 = 0x72

GIO0 = 0x73

GENERAL PURPOSE I/O PIN

The SPICoder® SA01 provides a general purpose I/O pin, GIO0, that can be programmed as Input, Output, Debounced Switch Input or LED Output. The programmable I/O pin can be configured to the desired mode through a command from the system. After the I/O pin is configured, the host system can read or write data to it. If the pin is configured as a Debounced Switch, it returns scan codes.

For Pin GIO0:

I/O Number = 0
LED Number = 0

Input Mode

While in the Input Mode, the GIO0 pin detects input signals and reports the input status to system as required.

Output Mode

In the Output Mode, the SPICoder® SA01 controls the output signal level according to the system command. When the pin is set at Output Mode, the default output is low.

Switch Input Mode

In Switch Input Mode, the SPICoder® SA01 generates an individual make key code when the switch closes (pin goes low), and a break key code when the switch returns to open (pin goes to high). The switches generate key codes outside of those generated by the key matrix, from 0x71 - 0x73. When the switch is closed, the SPICoder® SA01 does not fall asleep.

PIN CONFIGURATIONS

When prototyping, caution should be taken to ensure that programming of the GIO0 pin does not conflict with the circuit implemented. A series protection resistor is recommended for protection from improper programming of the pin.

After a power-on or soft reset, GIO0 defaults to the Input state.

The following drawing illustrates the suggested interface to the general purpose input/output pin.

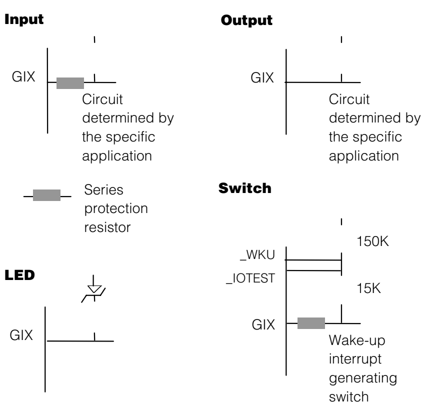

Figure 3: Suggested interface of general purpose input/output pin

LED MODES

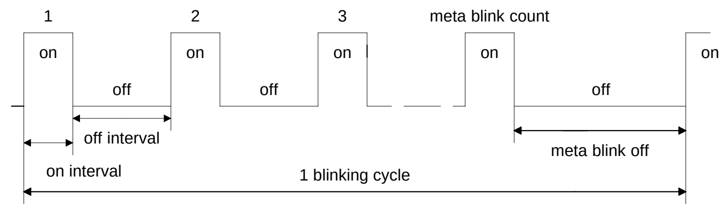

Figure 4: Timing chart: the behavior of an LED using the settings,1: LED on; 0: LED off

There are three LED modes: off, on, and blinking. The LED can be individually set to one of these modes. In the Blinking Mode, both the on-interval and the off-interval can be individually set. Additionally, a meta blink count and meta blink interval may be specified. This describes an interval of a different length which may be inserted after each specified number of blinks. All intervals are multiples of 1/16th of a second. When the LED is on or blinking, the SPICoder® SA01 does not enter the STOP Mode unless the PWR_OK signal is asserted low; in this case, the device saves the status of the LED and turns it off. The default LED mode is off.

The above timing chart describes the behavior of an LED using these settings,1: LED on; 0: LED off.

SPI COMMUNICATION CHANNEL

SPI data transfers can be performed at a maximum clock rate of 500 KHz. When the SPICoder® SA01 asserts the _ATN signal to the host master, the data is already loaded into the data register waiting for the clocks from the master. One _ATN signal is used per each byte transfer. If the host fails to provide clock signals for successive bytes in the data packet within 120 ms, the transmission is aborted and a new session is initiated by asserting a new _ATN signal. In such a case, the whole packet is re-transmitted.

If the SPI transmission fails 20 times consecutively, the synchronization between the master and slave may be lost. In this case, the SPICoder® SA01 enters the reset state.

When CPHA = 0, the shift clock is the OR of _SS with SCK; therefore, _SS must go high between successive characters in an SPI message. The master can assert _SS low only when it is getting ready to transmit or receive. After the last bit is shifted out, _SS must go high within 60 µs.

The SPICoder® SA01 implements the SPI communication protocol according to the following diagram:

CPOL = 0 ---------- SCK line idles in low state
CPHA = 0 ---------- SS line is an output enable control

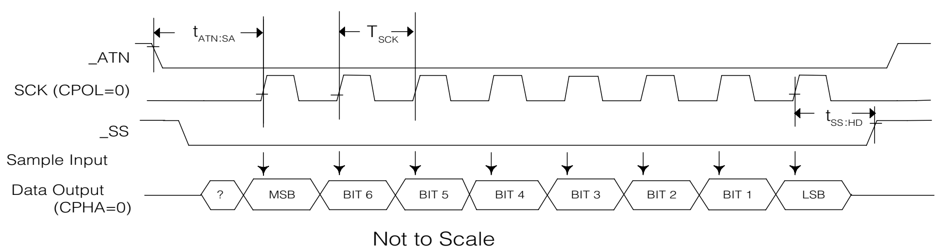

Figure 5: SPI Communication Protocol

When the host sends commands to the keyboard, the SPICoder® SA01 requires that the minimum and maximum intervals between two successive bytes be 200 µs and 5 ms respectively.

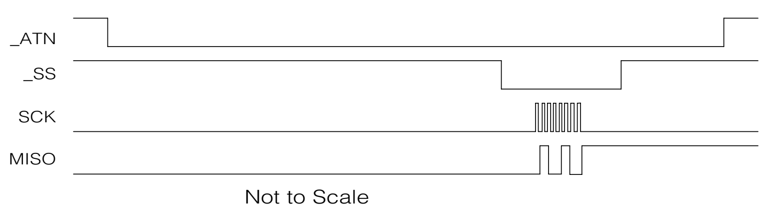

Figure 6: Transmitting Data Waveforms

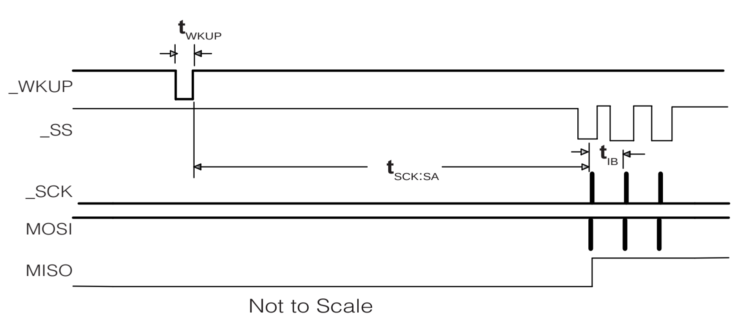

Figure 7: Receiving Data Waveforms

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DATA / COMMAND BUFFER

The SPICoder® SA01 implements a data buffer that contains the key code/command bytes waiting to be transmitted to the host. If the data buffer is full, the whole buffer is cleared and an "Initialize" command is sent to the host. At the same time, the keyboard is disabled until the "Initialize" or "Initialize Complete" command from the host is received.

SPI COMMUNICATION TABLE

The following table describes the specific timing referenced in the timing diagrams.

Signal Name	Description	Min	Max	Units
tATN:SA _	ATN to first clock pulse	-	120	ms
TSCK	Clock period	2	-	µs
tSS:HD	Last clock pulse to _SS de-assertion	-	60	µs
tWKUP	_WKUP pulse width	125	-	ns
tSCK:SA	_WKUP to first clock pulse	5	150	ms
tIB	Inter-byte period	0.2	5	ms

POWER MANAGEMENT UNIT

The SPICoder® SA01 supports two modes of operation. The following table lists the typical and maximum supply current (no DC loads) for each mode at 3.3 Volts (+/- 10%).

Current	Typical	Max	Unit	Description
RUN	1.5 1	3.0	mA	Entered only while data/commands are in process and if the LEDs are blinking
STOP	2.0	20	µA	Entered after 125 ms of inactivity if LEDs are low

Power consumption of the keyboard sub-system is determined primarily by the use of the LEDs. While the SPICoder® SA01 is in the STOP mode, an active low wake-up output from the master must be connected to the edge-sensitive _WKU pin of the SPICoder® SA01. This signal wakes up the SPICoder® SA01 in order to receive data from the master host. The master host must wait a minimum of 5 ms prior to providing clocks to the SPICoder® SA01. The SPICoder® SA01 enters the STOP mode after a 125 ms period of keypad and/or host communications inactivity, or anytime the PWR_OK line is asserted low by the host. Note that while one or more keys are held pressed, the SPICoder® SA01 does not enter the STOP mode until every key is released.

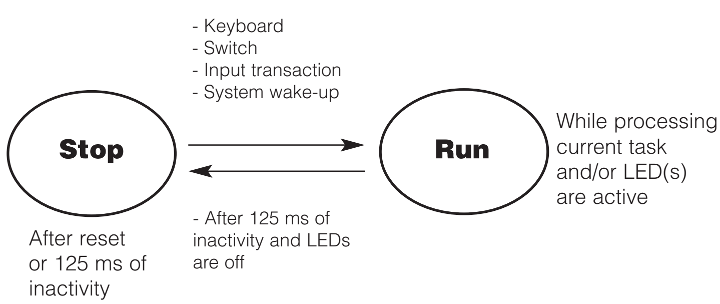

Figure 8: Power states of the SPICoder® SA01

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COMMUNICATION PROTOCOL

There are eight commands that may be sent from the SPICoder® SA01 to the host, and ten commands that may be sent from the host to the SPICoder® SA01.

Each command from SPICoder® SA01 to the host is composed of a sequence of codes. All commands start with <CONTROL> code (0x80) and end with LRC code (see the description of the LRC calculation on page 14). Command details are listed below.

Commands to the Host - Summary

Command Name	Code	Description
Initialize Request	0xAO	Sent to the host when the data buffer is full
Initialize Complete	0xA1	Issued upon completion of the "Initialize" command issued by the host
Heartbeat Response	0xA2	Response to "Heartbeat Request" issued by the host
Identification Response	0xF2	Response to "Identification Request" issued by the host
LED Status Report	0xA3	Response to "LED Status Request"
Resend Request	0xA5	Issued upon error during the reception of a packet
Input/Output Mode Status Report	0xA7	Reports the status of GIO0 pin
Input/Output Data Report	0xA8	Response to "I/O Data Request" command from the host

LRC CALCULATION

The LRC byte is calculated for the whole message packet, including the Command Code and the Command Prefix. The LRC is calculated by first taking the bitwise exclusive OR of all bytes from the message. If the most significant bit (MSB) of the LRC is set, the LRC is modified by clearing the MSB and changing the state of the next most significant bit. Thus, the packet check byte can never consist of a valid LRC with the most significant bit set.

COMMANDS TO THE HOST ANALYTICALLY

Initialize Request

<CONTROL>	0x80	
<INIT>	0xA0	
<LRC>	0x20	

The SPICoder® SA01 sends the Initialize Request Command to the host when its data buffer is full.

Initialization Complete

<CONTROL>	0x80	
<INIT COMPLETE>	0xA1	
<LRC>	0x21	

The SPICoder® SA01 sends the Initialize Complete Report to the host when it finishes the initialization caused by Initialize Command from the host.

Heartbeat Response

<CONTROL>	0x80	
<ONLINE>	0xA2	
<LRC>	0x22	

The SPICoder® SA01 sends the Heartbeat Response to the host when it receives the Heartbeat Request Command from the host.

Identification Response

<CONTROL>	0x80	
<ID>	0xF2	
<Vendor>	0x02	--- Semtech
<Revision>	0x08	--- Rev 0.8A
<Switch>	0x00	.
<LRC>	0x7E	

The SPICoder® SA01 sends the Identification Response to the host when it receives the Identification Request Command from the host.

LRC CALCULATION, (CONT'D)

The following C language function is an example of an LRC calculation program. It accepts two arguments: a pointer to a buffer and a buffer length. Its return value is the LRC value for the specified buffer.

```
char Calculate LRC (char  buffer,
size  buffer)
{
char LRC;
size_t index;
/*
* Init the LRC using the first two
message bytes.
*/
LRC = buffer [0] ^ buffer [1];
/*
* Update the LRC using the
remainder of the buffer.
*/
for (index = 2; index < buffer; index
++)
  LRC ^ = buffer[index];
/*
* If the MSB is set then clear the
MSB and change the next most
significant bit
*/
if (LRC & 0x80)
LRC ^ = 0xC0;
/* * Return the LRC value for the
buffer.*/}
```

COMMANDS TO THE HOST FROM THE SPICODER® SA01

LED Status Report

<CONTROL>	0x80	
<LED>	0xA3	
<Status 0>	0xnn	LED0 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<Status 1>	0xnn	LED1 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<Status 2>	0xnn	LED2 status:(0=OFF; 1=ON; 2=BLINKING; 3=NO LED MODE)
<LRC>	0xnn	

The SPICoder® SA01 sends the LED Status Report to the host when it receives the LED Status Request Command from the host.

Resend Request

<CONTROL>	0x80
<RESEND>	0xA5
<LRC>	0x25

The SPICoder® SA01 sends this Resend Request Command to the host when its command buffer is full, or if it detects either a parity error or an unknown command during a system command transmission.

Input/Output Mode Status Report

<CONTROL>	0x80	
<MODIO>	0xA7	
<IO NUMBER>	0xnn	IO number, 0
<IO MODE>	0xnn	IO mode: (0=input; 1=output; 2=switch; 3=LED)
<LRC>	0xnn	

The SPICoder® SA01 sends the I/O Mode Status Report to the host when it receives the I/O Mode Status Request Command from the host, in order to report the status of the GIO0 pin.

Input/Output Data Report

<CONTROL>	0x80	
<MODIO>	0xA8	
<IO NUMBER>	0xnn	IO number, 0
<IO DATA>	0xnn	IO data: (0=low, 1=high)
<LRC>	0xnn	

The SPICoder® SA01 sends the I/O Data Report to the host when it receives the I/O Data Request Command from the host.

COMMANDS FROM THE HOST TO THE SPICODER® SA01

Each command to SPICoder® SA01 is composed of a sequence of codes. All commands start with <ESC> code (1BH) and end with the LRC code (bitwise exclusive OR of all bytes).

Commands from the host - summary

Command name	Code	Description
Initialize	0xAO	Causes the SPICoder® SA01 to enter the power-on state
Initialization Complete	0xA1	Issued as a response to the "Initialize Request"
Heartbeat Request	0xA2	The SPICoder® SA01 responds with "Heartbeat Response"
Identification Request	0xF2	The SPICoder® SA01 responds with "Identification Response"
LED Status Request	0xA3	The SPICoder® SA01 responds with "LED Status Response"
LED Modify	0xA6	The SPICoder® SA01 changes the LED accordingly
Resend Request	0xA5	Issued upon error during the reception of a packet
Input/Output Mode Modify	0xA7	The SPICoder® SA01 modifies or report the status of the GIO0 pin
Output Data to I/O pin	0xA8	The SPICoder® SA01 outputs a signal to the GIO0 pin
Set Wake-Up Keys	0xA9	Defines which keys are "wake-up" keys

COMMANDS FROM THE HOST TO THE SPICODER® SA01 ANALYTICALLY

Initialize

<ESC>	0x1B
<INIT>	0xA0
<LRC>	0x7B

When the SPICoder® SA01 receives this command, it clears all buffers and returns to the power-on state.

Initialization Complete

<ESC>	0x1B
<INIT COMPLETE>	0xA1
<LRC>	0x7A

When the SPICoder® SA01 receives this command, it enables transmission of keyboard data. Keyboard data transmission is disabled if the TX output buffer is full (32 bytes). Note that if the transmit data buffer gets full the encoder issues an "Initialize Request" to the host.

Heartbeat Request

<ESC>	0x1B
<ONLINE>	0xA2
<LRC>	0x79

When the SPICoder® SA01 receives this command, it replies with the Heartbeat Response Report.

Identification Request

<ESC>	0x1B
<ID>	0xF2
<LRC>	0x29

The SPICoder® SA01 replies to this command with the Identification Response Report.

LED Status Request

<ESC>	0x1B
<LED>	0xA3
<LRC>	0x78

When SPICoder® SA01 receives this command, it replies with the LED Status Report.

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COMMANDS FROM THE HOST TO THE SPICODER® SA01 (CONT'D)

Set Wake-Up Keys

<ESC>	0x1B
<SETMATRIX>	0xA9
<COL0>	0xnn

(R7 R6 R5 R4 R3 R2 R1 R0
Bitmap: 0-enabled 1-disabled)

<COL1>	0xnn
<COL2>	0xnn
<COL3>	0xnn
<COL4>	0xnn
<COL5>	0xnn
<COL6>	0xnn
<COL7>	0xnn
<COL8>	0xnn
<COL9>	0xnn
<COL10>	0xnn
<COL11>	0xnn
<COL12>*	0xnn
<COL13>*	0xnn
<SWITCHES>	0xnn

(where SWITCHES bit assignments are = x x x x GIO0 SW0 XSW)

<LRC>	0xnn

The "Set Wake-Up Keys" command is used to disable specific keys from waking up the host. Using this command, the host can set only a group of keys to act as "power-on" switches. The host can change the keyboard behavior dynamically according to the system power management requirements. The default after power on is “All Keys Enabled.”

LED Modify

<ESC>	0x1B	
<MODLED>	0xA6	
<LED NUMBER>	0xnn	LED number (0)
<LED STATE>	0xnn	(0=LED OFF; 1=LED ON; 2=LED BLINKING)
<ON INTERVAL>	0xnn	Time in 1/16ths of a second for LED to be on
<OFF INTERVAL>	0xnn	Time in 1/16ths of a second for LED to be off
<META COUNT>	0xnn	Number of blinks after which to apply meta blink interval
<META INTERVAL>	0xnn	Time in 1/16ths of a second for LED to be off after <META COUNT> blinks
<LRC>	0xnn	

When the SPICoder® SA01 receives this command, it changes the LED mode accordingly.

I/O Mode Modify

<ESC>	0x1B	
<MODIO>	0xA7	
<IO NUMBER>	0xnn	IO number: 0
<IO MODE>	0xnn	IO mode: (0=input, 1=output, 2=switch, 3=LED, 4=current mode request)
<LRC>	0xnn	

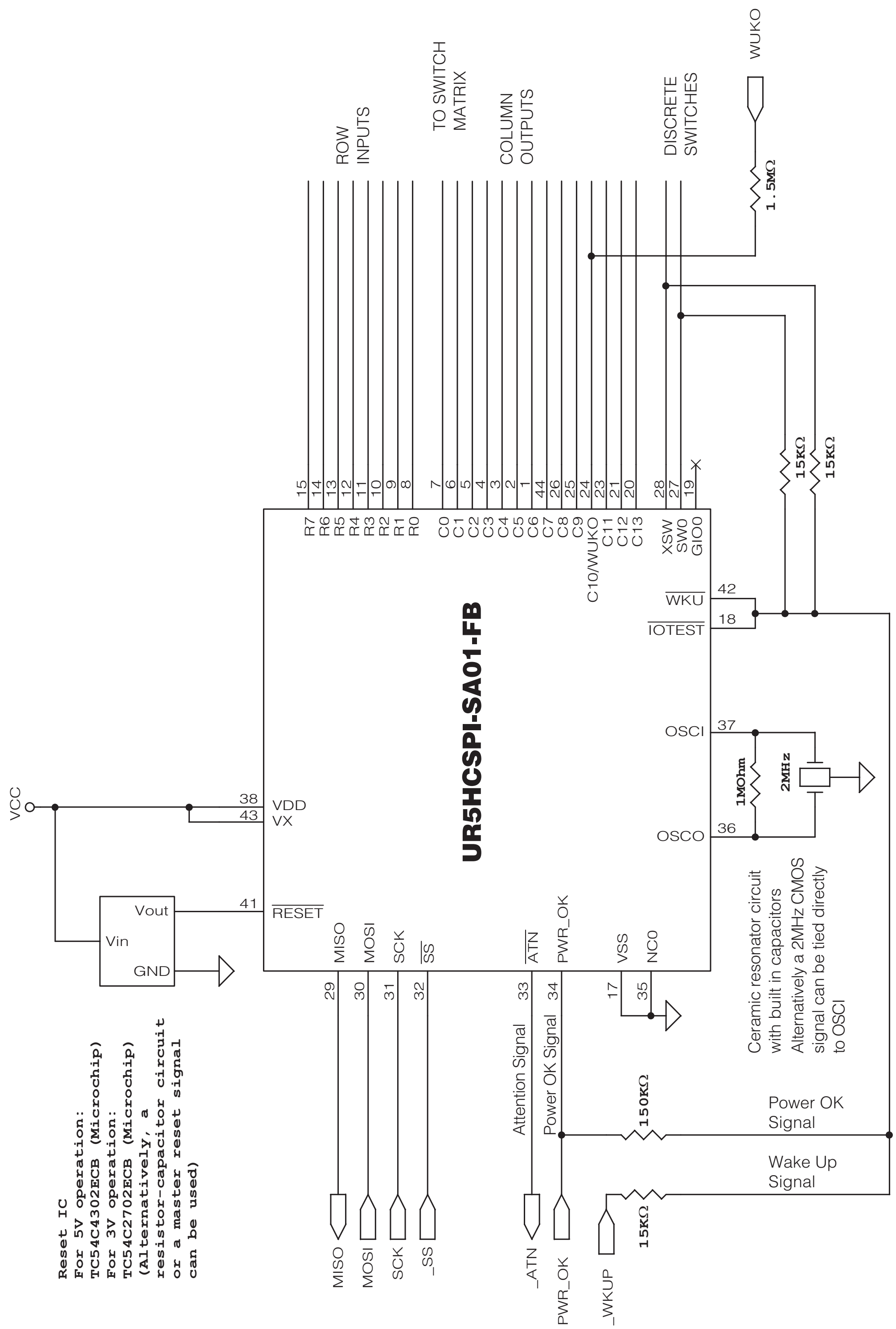
When the SPICoder® SA01 receives this command, it changes the I/O pin's mode accordingly. If the <IO MODE> =4, the SPICoder® SA01 sends the I/O Mode Status Report to the host.

Output Data to I/O Pin

<ESC>	0x1B	
<MODIO>	0xA8	
<IO NUMBER>	0xnn	IO number: 0
<IO DATA>	0xnn	IO data: (0=low, 1=high, 2=current I/O data request)
<LRC>	0xnn	

When the SPICoder® SA01 receives this command, it changes the value of the output pin accordingly. If the addressed pin is not configured as an output pin, the command is ignored. If <IO DATA> =2, the SPICoder® SA01 responds by issuing the I/O Data Status Report to the host.

SAMPLE CONFIGURATION UR5HCSPI-SA01



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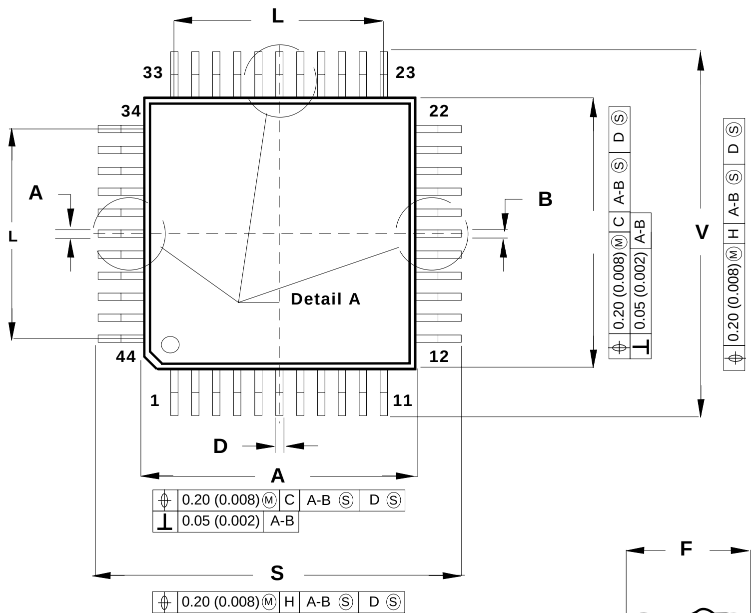
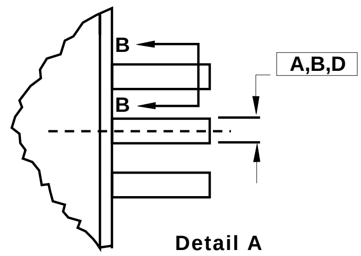
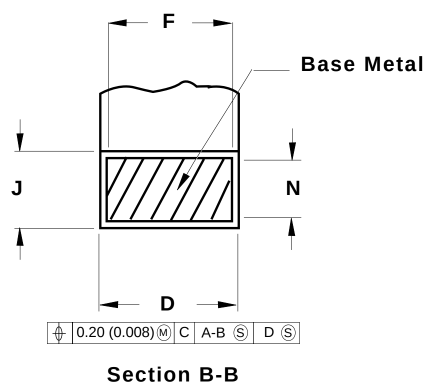
BILL OF MATERIALS FOR UR5HCSPI-SA01-FB SAMPLE SCHEMATIC

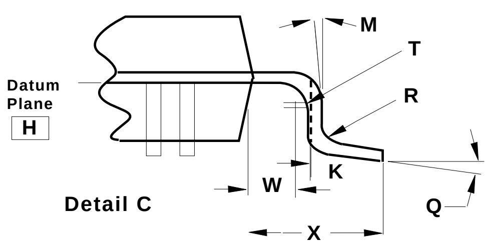
Quantity	Manufacture	Part#	Description
3	Generic	N/A	15KΩ resistors
1	Generic	N/A	150KΩ resistor
1	Generic	N/A	1MΩ resistor
2	Generic	N/A	1.5Ω resistors
1	Microchip	TC54VC4302ECB	IC volt detector CMOS 4.3V SOT23, for 5V operation
		TC54VC2702ECB	IC volt detector CMOS 2.7V SOT23, for 3.3V operation
1	AVX	PBRC-2.00BR	2.00 MHz ceramic resonator with built in capacitors, SMT

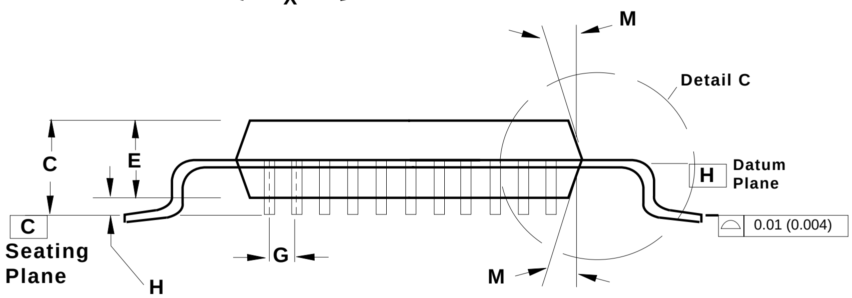
MECHANICALS FOR THE UR5HCSPI-SA01-FB











Notes

1. Dimensioning and tolerancing per Ansi Y14.5-M, 1982
2. Controlling dimension: Millimeter
3. Datum Plane "H" is located at the bottom of the lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -A-, -B-, and -D- to be determined at Datum Plane -H-.
5. Dimensions S and V to be determined at seating plane -C-.
6. Dimensions A and B do not include Mold protusion. Allowable protusion is 0.25 (0.010) per side. Dimensions A and B do include mold mismatch and are determined at Datum Plane -H-.
7. Dimension D does not include Danbar protrusion. Allowable Danbar protrusion is 0.08 (0.003) total in excess of the D dimension at Maximum Material Condition. Danbar cannot be located on the lower radius or the foot.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	-	0.25	-	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	-	0.005	-
U	0°	-	0°	-
V	12.95	13.45	0.510	0.530
W	0.40	-	0.016	-
X	1.6 REF		0.063 REF	

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	VIN	Vss -0.3 to Vdd +0.3	V
Current Drain per Pin (not including VSS or VDD)	I	25	mA
Operating Temperature UR5HCSPI-SA01	Ta	T low to T high -40 to +85	°C
Storage Temperature Range	TSTG -	65 to +150	°C
ESD rating (human body model)	VESD -	TBD	KV

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance	Tja		°C per W
■ Plastic		60	

DC Electrical Characteristics (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I load<10µA)	Vol			0.1	V
	Voh	Vdd–0.1			
Output High Voltage (I load=0.8mA)	Voh	Vdd–0.8			V
Output Low Voltage (I load=1.6mA)	Vol:			0.4	V
Input High Voltage	Vih	0.7xVdd		Vdd	V
Input Low Voltage	Vil	Vss		0.2xVdd	V
User Mode Current	Ipp		5	10	mA
Data Retention Mode (0 to 70°C)	Vrm	2.0			V
Supply Current (Run)	Idd		1.53	3.0	mA
(Wait)			0.711	1.0	mA
(Stop)			2.0	20	µA
I/O Ports Hi-Z Leakage Current	Iil			+/-10	µA
Input Current	Iin			+/- 1	µA
I/O Port Capacitance	Cio		8	12	pF

Control Timing (Vdd=3.3 Vdc +/-10%, Vss=0 Vdc, Temperature range=TLOW to THIGH unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation	fosc			MHz
■ Crystal Option			2.0	
■ External Clock Option		dc	2.0	
Cycle Time	tcyc	1000		ns
Crystal Oscillator Startup Time	toxov		100	ms
Stop Recovery Startup Time	tilch		100	ms
RESET Pulse Width	trl	8		tcyc
Interrupt Pulse Width Low	tlih	250		ns
Interrupt Pulse Period	tilil	*		tcyc
OSC1 Pulse Width	toh, tol	200		ns

*The minimum period tlil should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 tcyc.

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