agere systems

Product Brief, Rev. 2
June 2001

USS-344 *QuadraBus*™ Four-Host PCI-to-USB OpenHCI Host Controller

Features

- 32-bit, 33 MHz PCI interface compliant with *PCI Local Bus Specification Revision 2.2*
- Four downstream USB ports
- Each USB port dedicated to providing full USB bandwidth to the attached device
- Full compliance with *Universal Serial Bus Specification Revision 1.1*
- *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a* compatible
- Fully compatible with *Microsoft Windows*® standard OpenHCI drivers
- Fully compatible with *Mac*® OS
- Integrated dual-speed USB transceivers
- 3 V or 5 V switchable PCI signaling
- Low-power mode and wake-up compatible with *PCI Power Management Interface Specification Revision 1.1*
- Supports up to 127 devices per port
- Supports peripheral hot swap and wake-up
- Support for legacy keyboard and mouse
- 128-pin TQFP package
- Full 12 Mbits/s bandwidth per port
- Evaluation kit:
  — PCI card
  — Data sheets
- 0.25 µm technology

Applications

- Seamless integration with 3 V or 5 V PCI-based computer products
- Supports all USB compliant devices and hubs
- Simultaneous operation of multiple high-performance devices

Description

The Agere Systems Inc. USS-344 *QuadraBus* provides a single-chip four-host PCI-to-Universal Serial Bus (USB) solution. The USS-344 interfaces directly to any 32-bit, 33 MHz PCI bus and is ideal for either onboard applications or add-in card applications. It can easily be configured to communicate in either a 3 V PCI environment or 5 V PCI environment simply by selecting the appropriate communications voltage level on the VIO input pin.

The USS-344 provides four downstream USB ports for connectivity with any USB compliant device or hub. Full-speed or low-speed peripherals are supported along with all of the USB transfer types: control, interrupt, bulk, or isochronous. The USS-344's OpenHCI compliance offers significant USB performance benefits and reduced CPU overhead compared to other USB UHCI host controllers.

In addition, the USS-344 offers a significant performance advantage over all other USB host controllers (both UHCI and OHCI) by providing full USB bandwidth to each port rather than sharing the USB bandwidth over all ports. This results in an increase in the number of devices which can feasibly be connected to a computer system as well as ensuring high-bandwidth devices, such as video cameras and audio devices, are always provided with the high bandwidth they need while other USB devices are in use.

The USS-344 is a multifunction PCI device with one single-port USB host controller per PCI function. There are four PCI functions in the USS-344 for a total of four single-port USB host controllers. Each single-port host controller provides the full USB bandwidth (12 Mbits/s) for devices connected downstream of its port.

The USS-344 is fully compatible with the *Microsoft Windows* standard OpenHCI drivers. The USS-344 pinout is compatible with the future release of the Agere USB 2.0 host controller. The USS-344 is a 3.3 V device fabricated in 0.25 µm technology. Integrated dual-speed USB transceivers enable a single-chip PCI-to-USB solution. The USS-344 provides full support for legacy PC peripherals as defined in the *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a.*

Description (continued)

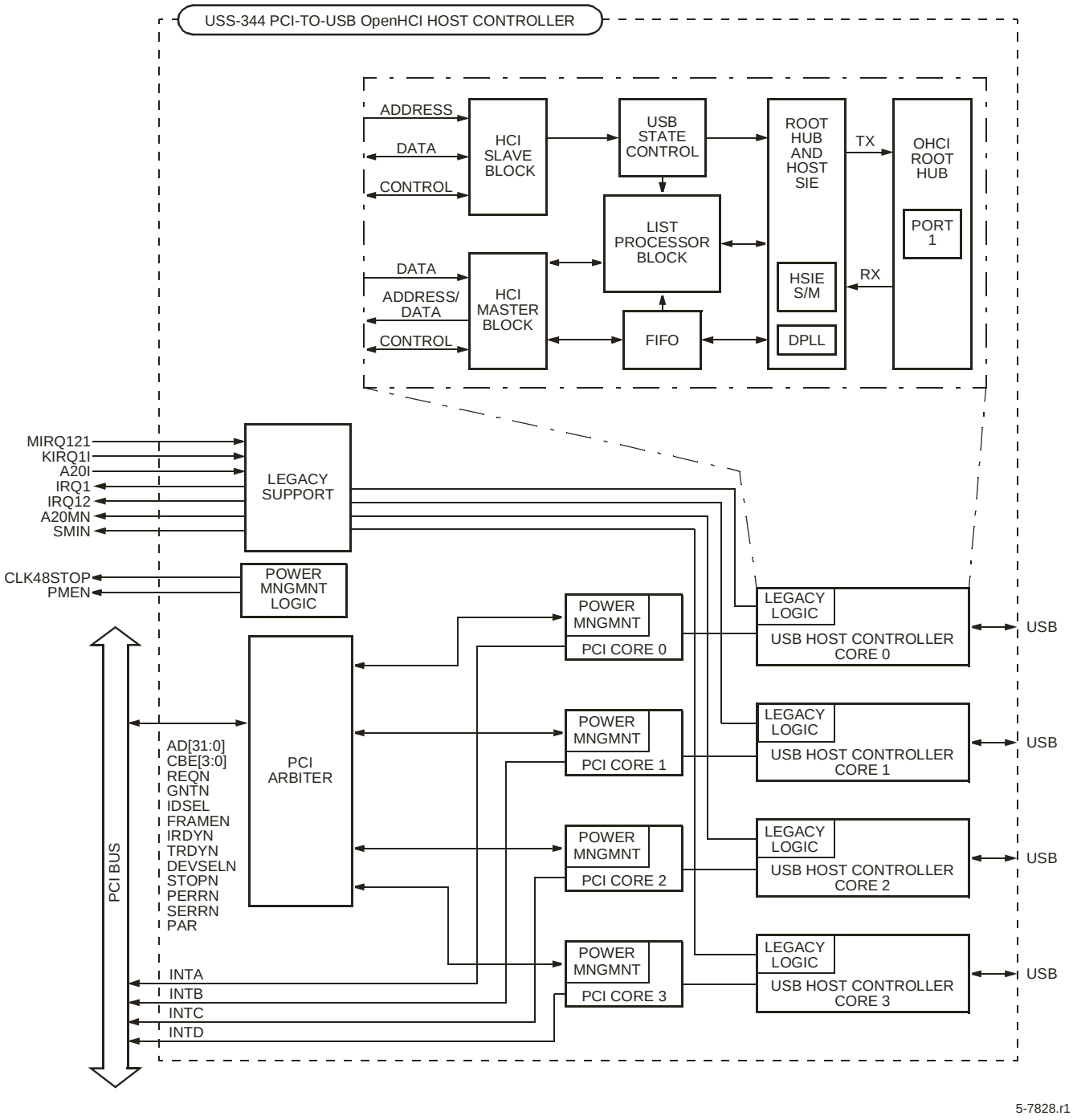

Figure 1. USS-344 Interconnection Diagram

Pin Information

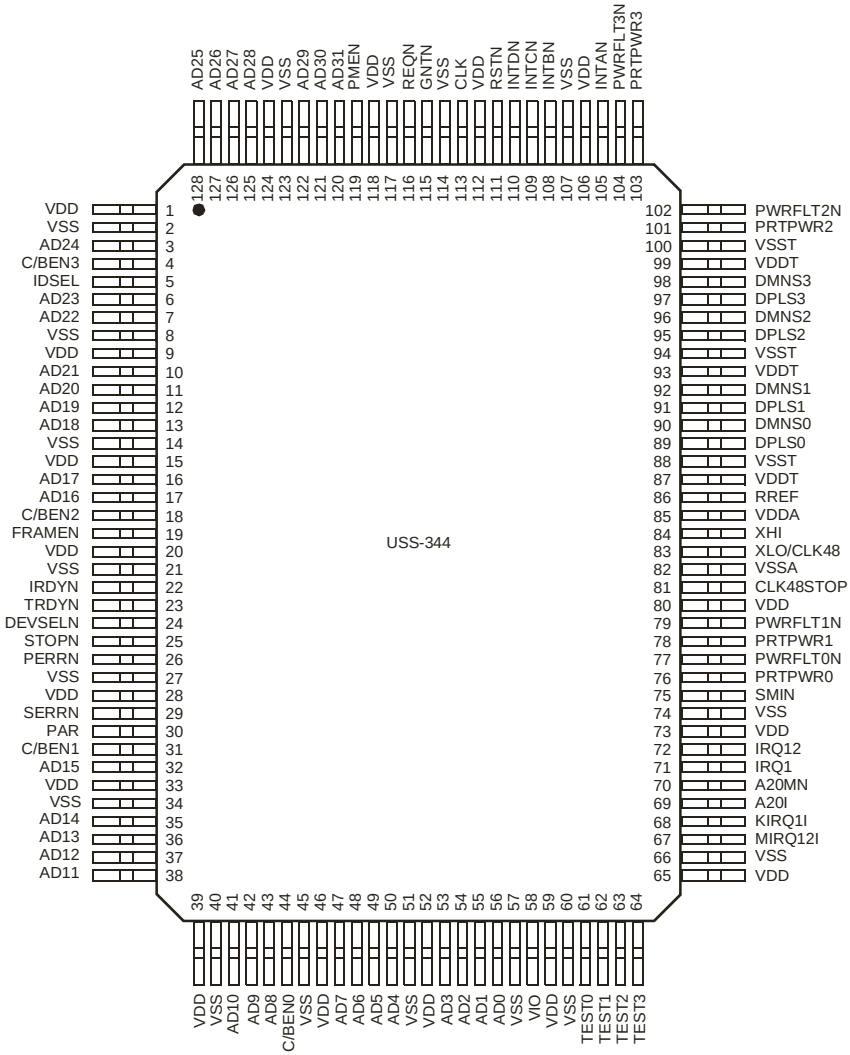

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Figure 2. USS-344 Pin Diagram

Pin Information (continued)

Table 1. Numeric Pin Cross Reference

Pin	Symbol*	Pin	Symbol*	Pin	Symbol*	Pin	Symbol*
1	VDD	33	VDD	65	VDD	97	DPLS3
2	VSS	34	VSS	66	VSS	98	DMNS3
3	AD24	35	AD14	67	MIRQ12I	99	VDDT
4	C/BEN3	36	AD13	68	KIRQ1I	100	VSST
5	IDSEL	37	AD12	69	A20I	101	PRTPWR2
6	AD23	38	AD11	70	A20MN	102	PWRFLT2N
7	AD22	39	VDD	71	IRQ1	103	PRTPWR3
8	VSS	40	VSS	72	IRQ12	104	PWRFLT3N
9	VDD	41	AD10	73	VDD	105	INTAN
10	AD21	42	AD9	74	VSS	106	VDD
11	AD20	43	AD8	75	SMIN	107	VSS
12	AD19	44	C/BEN0	76	PRTPWR0	108	INTBN
13	AD18	45	VSS	77	PWRFLT0N	109	INTCN
14	VSS	46	VDD	78	PRTPWR1	110	INTDN
15	VDD	47	AD7	79	PWRFLT1N	111	RSTN
16	AD17	48	AD6	80	VDD	112	VDD
17	AD16	49	AD5	81	CLK48STOP	113	CLK
18	C/BEN2	50	AD4	82	VSSA	114	VSS
19	FRAMEN	51	VSS	83	XLO/CLK48	115	GNTN
20	VDD	52	VDD	84	XHI	116	REQN
21	VSS	53	AD3	85	VDDA	117	VSS
22	IRDYN	54	AD2	86	RREF	118	VDD
23	TRDYN	55	AD1	87	VDDT	119	PMEN
24	DEVSELN	56	AD0	88	VSST	120	AD31
25	STOPN	57	VSS	89	DPLS0	121	AD30
26	PERRN	58	VIO	90	DMNS0	122	AD29
27	VSS	59	VDD	91	DPLS1	123	VSS
28	VDD	60	VSS	92	DMNS1	124	VDD
29	SERRN	61	TEST0	93	VDDT	125	AD28
30	PAR	62	TEST1	94	VSST	126	AD27
31	C/BEN1	63	TEST2	95	DPLS2	127	AD26
32	AD15	64	TEST3	96	DMNS2	128	AD25

* Pins identified as NC are unused and should be left unconnected. Active-low signals within this document are indicated by an N following the symbol names.

Pin Information (continued)

Table 2. PCI Signals

Pin	Symbol*	Type	Description
111	RSTN	Input	**PCI Reset (Active-Low).**
113	CLK	Input	**PCI System Clock (33 MHz).**
116	REQN	Output/3-State	**PCI Request (Active-Low).**
115	GNTN	Input	**PCI Grant (Active-Low).**
120, 121, 122, 125, 126, 127, 128, 3, 6, 7, 10, 11, 12, 13, 16, 17, 32, 35, 36, 37, 38, 41, 42, 43, 47, 48, 49, 50, 53, 54, 55, 56	AD[31:0]	Bidir	**PCI Address and Data.**
30	PAR	Bidir	**PCI Parity.**
4, 18, 31, 44	C/BEN[3:0]	Bidir	**PCI Bus Command and Byte Enables.**
19	FRAMEN	Bidir	**PCI Cycle Frame (Active-Low).**
22	IRDYN	Bidir	**PCI Initiator Ready (Active-Low).**
23	TRDYN	Bidir	**PCI Target Ready (Active-Low).**
25	STOPN	Bidir	**PCI Stop (Active-Low).**
5	IDSEL	Input	**PCI Initialization Device Select.**
24	DEVSELN	Bidir	**PCI Device Select (Active-Low).**
26	PERRN	Bidir	**PCI Parity Error (Active-Low).**
29	SERRN	Output/Open Drain	**PCI System Error (Active-Low).**
105	INTAN	Output/Open Drain	**PCI Interrupt-A (Active-Low).**
108	INTBN	Output/Open Drain	**PCI Interrupt-B (Active-Low).**
109	INTCN	Output/Open Drain	**PCI Interrupt-C (Active-Low).**
110	INTDN	Output/Open Drain	**PCI Interrupt-D (Active-Low).**
119	PMEN	Output/Open Drain	**Power Management Event (Active-Low).**
1, 9, 15, 20, 28, 33, 39, 46, 52, 59, 65, 73, 80, 106, 112, 118, 124	VDD	Power	**3.3 V VDD.**
2, 8, 14, 21, 27, 34, 40, 45, 51, 57, 60, 66, 74, 107, 114, 117, 123	VSS	Power	**VSS.**
58	VIO	Power	**PCI Environment Selection (3.3 V or 5 V).**

* An N following the symbol names indicates active-low for the USS-344.

Table 3. USB Port Signals

Pin	Symbol*	Type	Description
89	DPLS0	Bidir	**USB Port 0 DPLUS.**
90	DMNS0	Bidir	**USB Port 0 DMINUS.**
91	DPLS1	Bidir	**USB Port 1 DPLUS.**
93	DMNS1	Bidir	**USB Port 1 DMINUS.**
95	DPLS2	Bidir	**USB Port 2 DPLUS.**
96	DMNS2	Bidir	**USB Port 2 DMINUS.**
97	DPLS3	Bidir	**USB Port 3 DPLUS.**
98	DMNS3	Bidir	**USB Port 3 DMINUS.**
76	PRTPWR0	Bidir	**USB Port 0 Power Enable (Active-Low).**
78	PRTPWR1	Bidir	**USB Port 1 Power Enable (Active-Low).**
101	PRTPWR2	Bidir	**USB Port 2 Power Enable (Active-Low).**
103	PRTPWR3	Bidir	**USB Port 3 Power Enable (Active-Low).**

* An N following the symbol names indicates active-low for the USS-344.

Pin Information (continued)

Table 3. USB Port Signals (continued)

Pin	Symbol*	Type	Description
77	PWRFLT0N	Input	**USB Port 0 Overcurrent (Active-Low).**
79	PWRFLT1N	Input	**USB Port 1 Overcurrent (Active-Low).**
102	PWRFLT2N	Input	**USB Port 2 Overcurrent (Active-Low).**
104	PWRFLT3N	Input	**USB Port 3 Overcurrent (Active-Low).**
75	CLK48	Input	**USB Clock.**
81	CLK48STOP	Output	**USB Clock Stop (Optional).** Used to stop external 48 MHz clock in PCI power management state D3.
87, 93, 99	VDDT	Power	**USB Transceiver VDD (3.3 V).**
88, 94, 100	VSST	Power	**USB Transceiver Vss.**
86	RREF	Input	**USB 2.0 1 kΩ Precision Resistor Connection.** Hi-Z if implementation does not expect upgrade to USB 2.0.
85	VDDA	Power	**USB 2.0 Analog Power.** Connect to VDD if implementation does not expect upgrade to USB 2.0.
82	VSSA	Power	**USB 2.0 Analog Power.** Connect to VSS if implementation does not expect upgrade to USB 2.0.
84	XHI	Power	**USB 2.0 Crystal Oscillator XHI Connection.** Hi-Z if implementation does not expect upgrade to USB 2.0.
83	XLO/CLK48	Power/Input	**USB 2.0 Crystal Oscillator XHI Connection/USB 1.X CLK 48 MHz Input.**

* An N following the symbol names indicates active-low for the USS-344.

Table 4. Legacy Support Signals

Pin	Symbol*	Type	Description
68	KIRQ1I	Input	**Legacy Keyboard Controller Interrupt (IRQ1 Input from Keyboard Controller).**
67	MIRQ12I	Input	**Legacy Mouse Controller Interrupt (IRQ12 Input from Mouse Controller).**
69	A20I	Input	**Legacy Gate A20 Input.**
70	A20MN	Output	**Legacy Gate A20 Output (to Memory Controller).**
71	IRQ1	Output/Open Drain	**System Keyboard Interrupt (Active-High).**
72	IRQ12	Output/Open Drain	**System Mouse Interrupt (Active-High).**
75	SMIN	Output/Open Drain	**System Management Interrupt (Active-Low).**

* An N following the symbol names indicates active-low for the USS-344.

Table 5. Chip Test Signals

Pin	Symbol*	Type	Description
61	TEST0	Input	**Chip Test Signal.**
62	TEST1	Input	**Chip Test Signal.**
63	TEST2	Input	**Chip Test Signal.**
64	TEST3	Input	**Chip Test Signal.**

* An N following the symbol names indicates active-low for the USS-344.

System Configuration

Figure 3 depicts a standard system configuration using the USS-344. The USS-344 can interface directly with any 3 Vdc or 5 Vdc, 33 MHz, 32-bit PCI bus with no additional components required. The USS-344 is a port power-switched USB host controller providing the maximum control over USB device power consumption. This feature requires one 5 Vdc-to-5 Vdc power switching regulator per USB port to allow the USS-344 to turn power on/off to each USB port under control of the operating system. The USS-344 contains four USB transceivers for direct connection of the USB DPLS and DMNS signals to the USB connector. Also included in the USS-344 is the legacy PS/2 mouse and keyboard interface as defined in the *OpenHCI Open Host Controller Interface Specification for USB Release 1.0a.* This legacy interface along with standard USB BIOS drivers allows USB mice and keyboards to operate in *MS-DOS*® mode. Legacy support need not be implemented by the system designer if not desired.

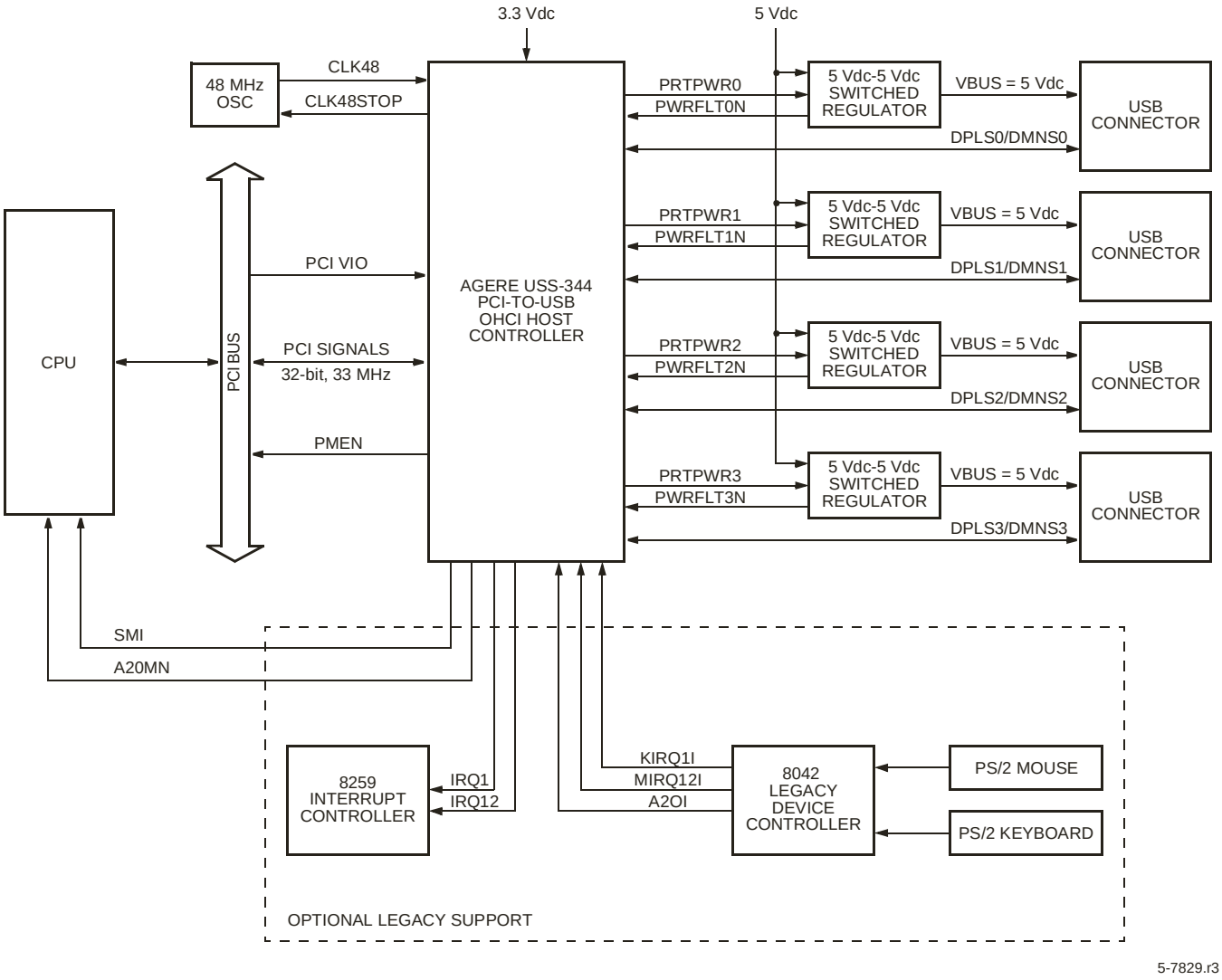
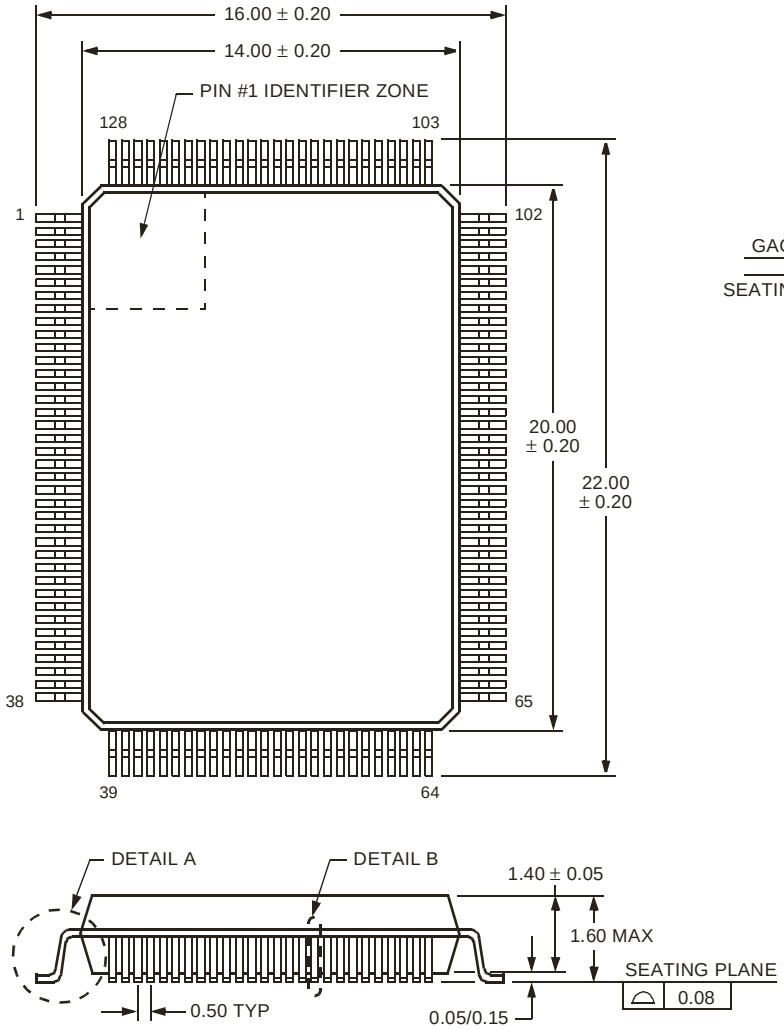


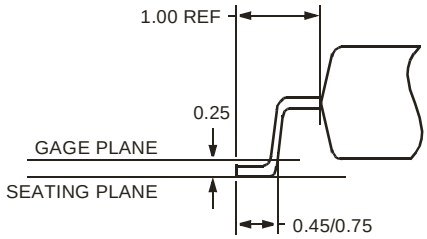
Figure 3. Standard System Configuration

Outline Diagram

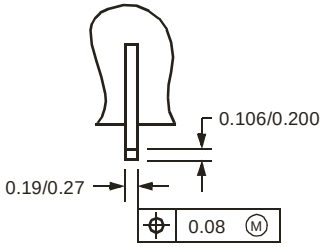
128-Pin TQFP

Dimensions are in inches.





DETAIL A



DETAIL B

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June 2001
PB01-114CMPR-2 (Replaces PB01-114CMPR-1)