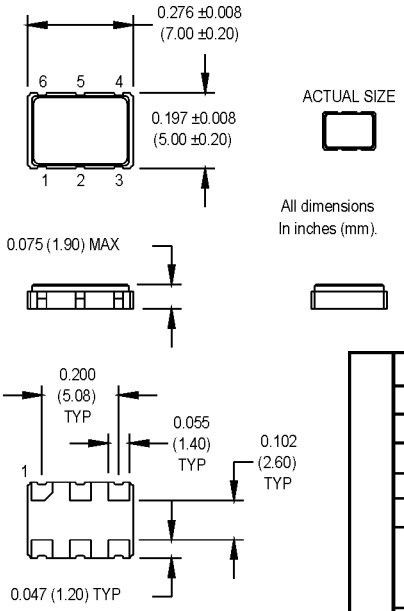
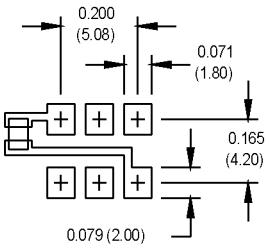
# UVCJ Series 5.0 x 7.0 x 1.9 mm 3.3 Volt Surface Mount LVPECL/LVDS Compatible Low Jitter Oscillators

- **Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz achieved with non-PLL technology**
- **Ideal for 10 and 40 Gigabit Ethernet and Optical Carrier applications**




SUGGESTED SOLDER PAD LAYOUT




**Ordering Information**

UVCJ 1 8 B L N 00.0000 MHz

**Product Series**

**Temperature Range**
- **1:** 0°C to +70°C
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C
- **7:** -0°C to +85°C
- **8:** 0°C to +50°C

**Stability**
- **3:** ±100 ppm
- **4:** ±50 ppm
- **6:** ±25 ppm
- **8:** ±20 ppm

**Output Type**
- **B:** Complementary, Enable (Enable High)
- **S:** Complementary, Enable (Enable Low)
- **U:** Complementary Output

**Symmetry/Output Logic Type**
- **L:** 45/55% LVDS
- **P:** 45/55% PECL
- **H:** 40/60% LVDS
- **Q:** 40/60% PECL

**Package/Lead Configurations**
- **N:** Leadless Ceramic (6 pads)

**Frequency (customer specified)**

## Pin Connections

| PIN | FUNCTION |
|---|---|
| 1 | Output Enable |
| 2 | N/C |
| 3 | Ground |
| 4 | Output1/ Q |
| 5 | Output2/ $\overline{Q}$ |
| 6 | +Vdd |

| | PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition |
|---|---|---|---|---|---|---|---|
| Electrical Specifications | Frequency Range | F | 0.75 | | 800 | MHz | |
| | Frequency Stability | ΔF/F | (See Ordering Information) | | | | See Note 1 |
| | Operating Temperature | TA | (See Ordering Information) | | | | |
| | Storage Temperature | Ts | -55 | | +125 | °C | |
| | Input Voltage | Vcc | 3.15 | 3.3 | 3.45 | V | |
| | Input Current | Icc | | | | | See Note 2 |
| | 0.75 MHz to 175 MHz | | | | 80/40 | mA | PECL/LVDS |
| | 175 MHz to 800 MHz | | | | 95/55 | mA | PECL/LVDS |
| | Symmetry (Duty Cycle) | | 40 | 50 | 60 | % | Vcc -1.3 VDC (PECL) |
| | (Per Symmetry Code) | | 40 | 50 | 60 | % | 0.5x (Vmax-Vmin) LVDS |
| | Load | | 50 Ohms to Vcc -2 VDC | | | | PECL waveform |
| | | | 50 Ohm differential load | | | | LVDS waveform |
| | Rise/Fall Time | Tr/Tf | | 0.35 | 0.55 | ns | At 20/80% |
| | Logic "1" Level | Voh | Vcc -1.02 | | | V | PECL |
| | Logic "0" Level | Vol | | | Vcc -1.63 | V | PECL |
| | Phase Jitter | ϕ J | | | | | |
| | 20 Mhz to 175 MHz | | | 0.35 | 1 | ps RMS | Integrated 12 kHz - 20 MHz |
| | 175 to 800 MHz | | | 1 | 1.5 | ps RMS | Integrated 12 kHz - 20 MHz |
| | Phase Noise (Typical) | 10 Hz | 100 Hz | 1 kHz | 20 kHz | 100 kHz | Offset from carrier |
| | @ 19.44 MHz | -50 | -80 | -112 | -140 | -150 | dBc/Hz |
| | @ 155.52 MHz | -50 | -80 | -100 | -125 | -145 | dBc/Hz |
| | @ 250 MHz | -50 | -80 | -100 | -124 | -128 | dBc/Hz |
| | @ 622.08 MHz | -50 | -80 | -100 | -118 | -121 | dBc/Hz |
| | Differential Voltage | Vo | 250 | 350 | | mV | Pk-Pk LVDS only |
| | Enable/Disable Logic | | CMOS high or Vcc - enables output | | | | Output Option B |
| | | | CMOS low or GND - disables output | | | | |
| | | | PECL low, GND, or N/C - enables output | | | | Output Option S |
| | | | PECL high - disables output | | | | |
| Environmental | Mechanical Shock | Per MIL-STD-202, Method 213, Condition C | | | | | |
| | Vibration | Per MIL-STD-202, Method 201 & 204 | | | | | |
| | Reflow Solder Conditions | 240°C for 10 s max. | | | | | |
| | Hermeticity | Per MIL-STD-202, Method 112 (1 x $10^{-8}$ atm.cc/s of helium) | | | | | |
| | Solderability | Per EIAJ-STD-002 | | | | | |

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage, and aging.



M-tron Industries, Inc., PO Box 630, Yankton, SD 57078-0630, USA Phone: 605-665-9321 or 1-800-762-8800 Fax: 605-665-1709 Website: www.mtron.com
M-tron Industries Limited, 1104 Shanghai Industrial Investment Building, 48-62 Hennessy Road, Wanchai, Hong Kong, China Phone: 852-2866-8023 Fax: 852-2529-1822