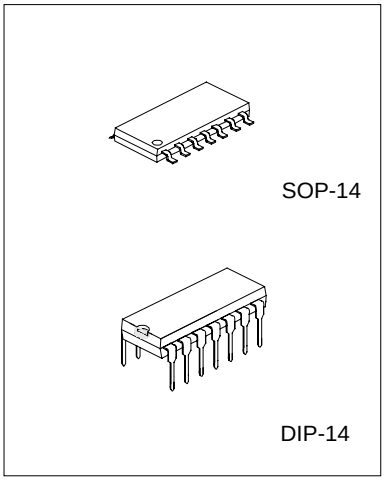
UTC MC34074 LINEAR INTEGRATED CIRCUIT

HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY OPERATIONAL AMPLIFIER



DESCRIPTION

The UTC MC34074 offer 4.5MHz of gain bandwidth product, 13V/μs slew rate and fast setting time without the use of JFET device technology. Although it can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With A Darlington input stage, it exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

FEATURES

*Wide bandwidth: 4.5 MHz
*High slew rate: 13V/μs
*Fast settling time:1.1μs to 0.1%
*Wide single supply operation: 3.0V to 44V
*Wide input common mode voltage range: Includes Ground (V_{EE})
*Low input offset voltage: 3.0mV maximum
*Large output voltage swing: -14.7V to +14V (with +-15V supplies)
*Large Capacitance Drive Capability: 0pF to 10,000 pF
*Low total harmonic distortion: 0.02%
*Excellent phase margin: 60°
*Excellent gain margin: 12dB
*Output short circuit protection
*ESD Diodes/Clamps provide input protection

PIN CONFIGURATIONS

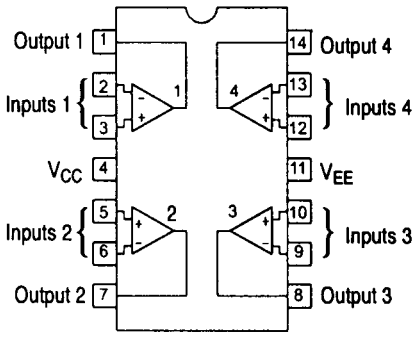


Figure 1.

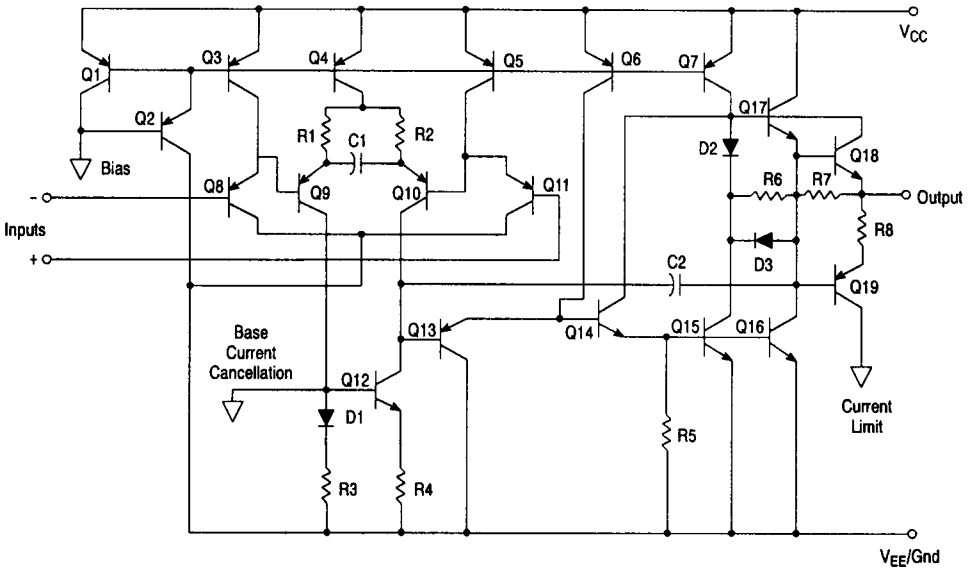


Figure 2. Representative Schematic Diagram

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (from V_{EE} to V_{CC})	Vs	+44	V
Differential Input Voltage	V_{IDR}	Note 1	V
Input Voltage	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	Tj	+150	°C
Storage Temperature Range	Tstg	-60 to +150	°C

Notes: 1.Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2.Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded. (see Figure 2)

ELECTRICAL CHARACTERISTICS (V_{CC}=+15V, V_{EE}=-15V, R_L=connected to ground, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{IO}	R_S=100Ω, V_{CM}=0V, Vo=0V	V_{CC}=+15V,V_{EE}=-15V ,T_A=+25°C		0.5	3.0	mV
			V_{CC}=+5V,V_{EE}=0V, T_A=+25°C		0.5	3.0	mV
			V_{CC}=+15V,V_{EE}=-15V ,T_A=0°C to 70°C			5.0	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	R_S=10Ω,V_{CM}=0V,V_O=0V, T_A=0°C to 70°C			10		µV/°C
Input Bias Current	I_{IB}	V_{CM}=0V, Vo=0V, T_A=+25°C T_A=0°C to 70°C			100	500 700	nA
Input Offset Current	I_{IO}	V_{CM}=0V, Vo=0V, T_A=+25°C T_A=0°C to 70°C			6.0	50 300	nA
Input Common Mode Voltage	V_{ICR}	T_A=+25°C		V_{EE} to (V_{CC} –1.8)			V
		T_A=0°C to 70°C		V_{EE} to (V_{CC} –2.2)			V
Large Signal Voltage Gain	A_{VOL}	Vo=±10V, RL=2.0kΩ, T_A=+25°C T_A=0°C to 70°C		50 25	100		V/mV
Output Voltage Swing (V_{ID}=+-1.0V)	V_{OH}	V_{CC}=+5.0V,V_{EE}=0V,R_L=2.0kΩ, T_A=+25°C		3.7	4.0		V
		V_{CC}=+15.0V,V_{EE}=-15V, R_L=10kΩ, T_A=+25°C		13.6	14		V
		V_{CC}=+15.0V,V_{EE}=-15V, R_L=2.0kΩ, T_A=0°C to 70°C		13.4			V
Output Voltage Swing (V_{ID}=+-1.0V)	V_{OL}	V_{CC}=+5.0V,V_{EE}=0V,R_L=2.0kΩ, T_A=+25°C			0.1	0.3	V
		V_{CC}=+15.0V,V_{EE}=-15V, R_L=10kΩ,TA=+25°C			-14.7	-14.3	V
		V_{CC}=+15.0V,V_{EE}=-15V, R_L=2.0kΩ, T_A=0°C to 70°C				-13.5	V
Output Short Circuit current	I_{SC}	V_{ID}=1.0V,V_O=0V, T_A=25°C Source Sink		 10 20	 30 30		mA
Common Mode Rejection	CMR	R_S<=10kΩ,V_{CM}=V_{ICR},T_A=25°C		80	97		dB
Power Supply Rejection (R_S=100Ω)	PSR	V_{CC}/V_{EE}=+16.5V/-16.5V to +13.5/-13.5V, T_A=25°C		80	97		dB
Power Supply Current (Per Amplifier, No Load)	I_D	V_{CC}=+5.0V,V_{EE}=0V,V_O=+2.5V, T_A=+25°C			1.6	2.0	mA
		V_{CC}=+15.0V,V_{EE}=-15V, V_O=0V,T_A=+25°C			1.9	2.5	mA
		V_{CC}=+15.0V,V_{EE}=-15V, V_O=0V, T_A=0°C to 70°C				2.8	mA
Slew Rate	SR	Vin=-10V to +10V, R_L=2.0kΩ, C_L=500pF	Av=+1.0	8.0	10		V/µs
			Av=-1.0		13		
Setting Time	ts	10 Setp, Av=-1.0 to 0.1% (+1/2 LSB of 9-Bits) to 0.01% (+1/2 LSB of 12-Bits)			 1.1 2.2		µs
Gain Bandwidth Product	GBW	f=100kHz		3.5	4.5		MHz
Power Bandwidth	BW	Av=+1.0, R_L=2kΩ, Vo=20Vpp, THD=5.0%			160		kHz

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase Margin	fm	R_L=2kΩ R_L=2kΩ, C_L=300pF		60 40		Deg
Gain Margin	Am	R_L=2kΩ R_L=2kΩ, C_L=300pF		12 4		dB
Equivalent Input Noise Voltage	en	Rs=100Ω, f=1.0kHz		32		nV/√Hz
Equivalent Input Noise Current	in	f=1.0kHz		0.22		pA/√Hz
Differential Input Resistance	Rin	V_{CM}=0V		150		MΩ
Differential Input Capacitance	Cin	V_{CM}=0V		2.5		pF
Total Harmonic distortion	THD	Av=+10, R_L=2.0kHz, 2.0Vpp≤Vo≤20Vpp, f=10kHz		0.02		%
Channel Separation		f=10kHz		120		dB
Open Loop Output Impedance	IZoI	f=1.0MHz		30		W

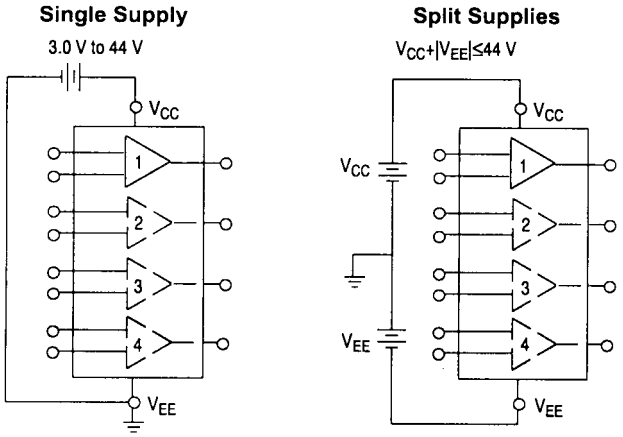


Figure 3. Power Supply Configurations

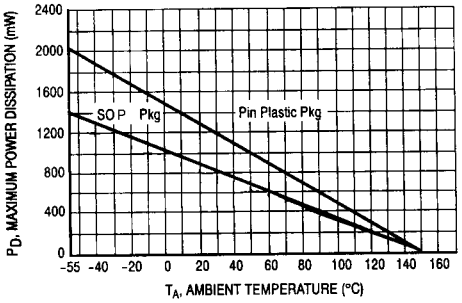


Figure 4. Maximum Power Dissipation versus Temperature for Package Types

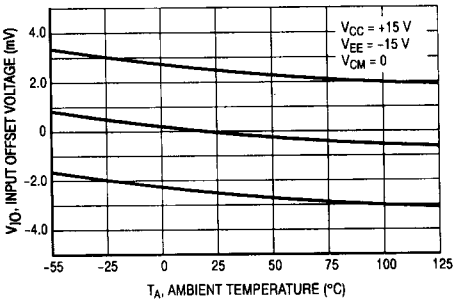


Figure 5. Input Offset Voltage versus Temperature for Representative Units

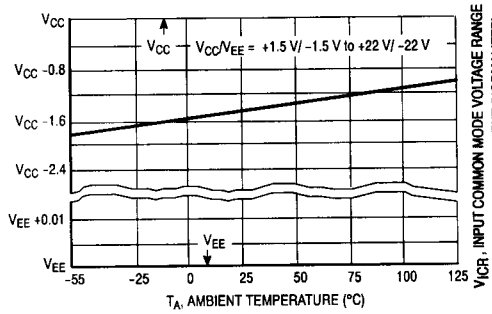


Figure 6. Input Common Mode Voltage Range versus Temperature

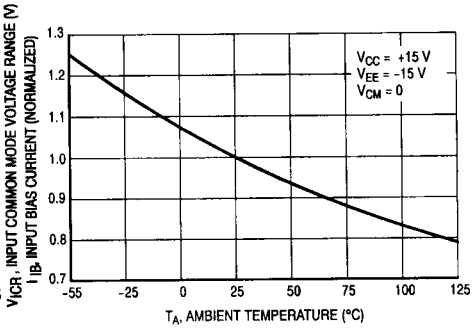


Figure 7. Normalized Input Bias Current versus Temperature

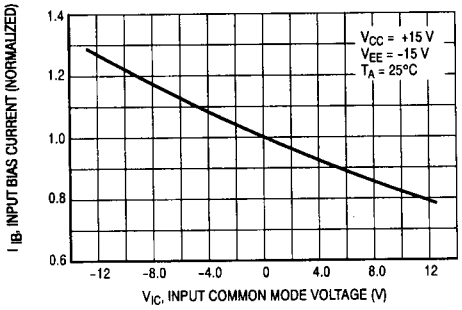


Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage

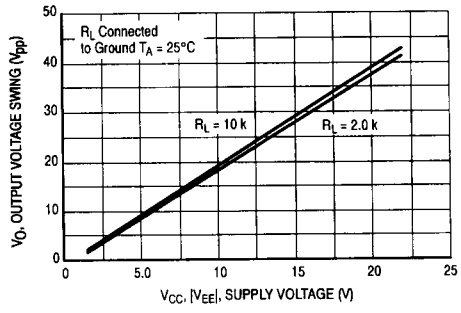


Figure 9. Split Supply Output Voltage Swing versus Supply Voltage

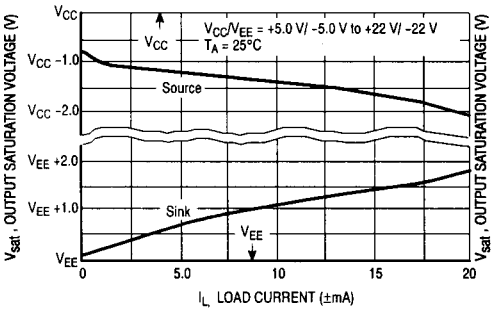


Figure 10. Single Supply Output Saturation versus Load Resistance to V_{CC}

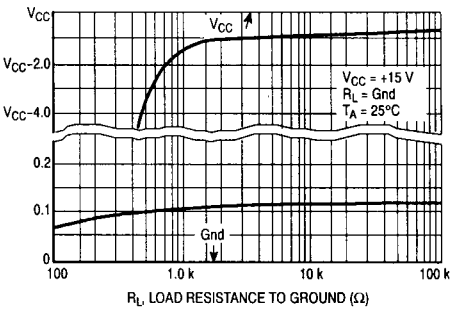


Figure 11. Split Supply Output Saturation versus Load Current

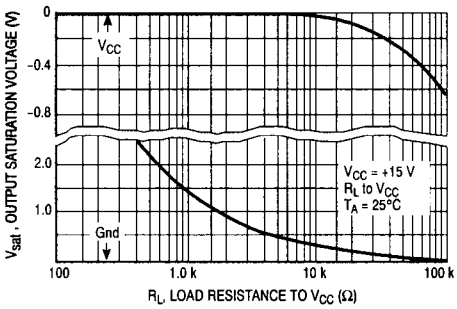


Figure 12. Single Supply Output Saturation versus Load Resistance to Ground

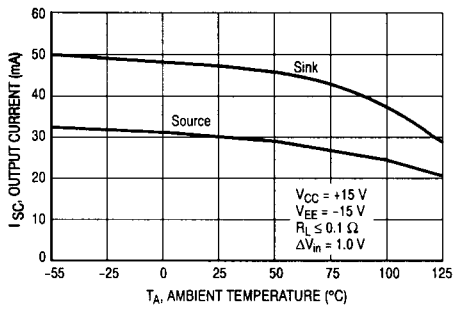


Figure 13. Output Short Circuit Current versus Temperature

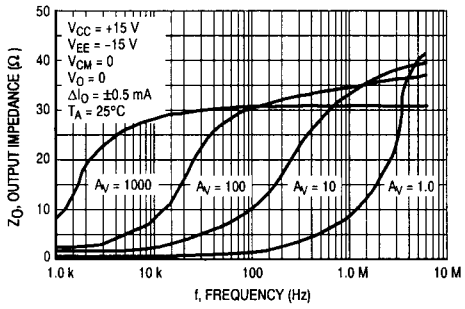


Figure 14. Output Impedance versus Frequency

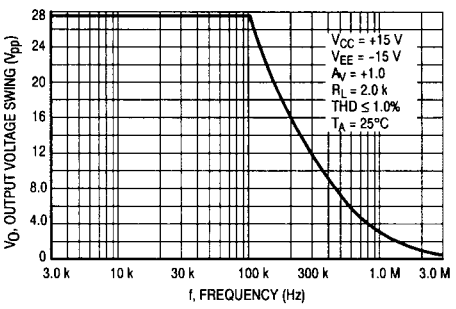


Figure 15. Output Voltage Swing versus Frequency

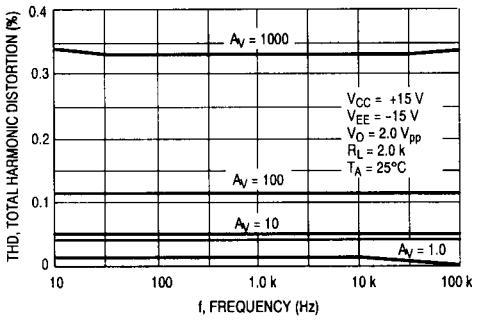


Figure 16. Total Harmonic Distortion versus Frequency

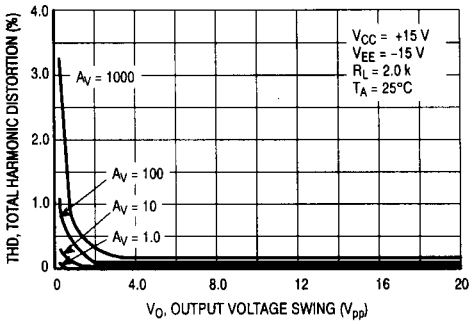


Figure 17. Total Harmonic Distortion versus Output Voltage Swing

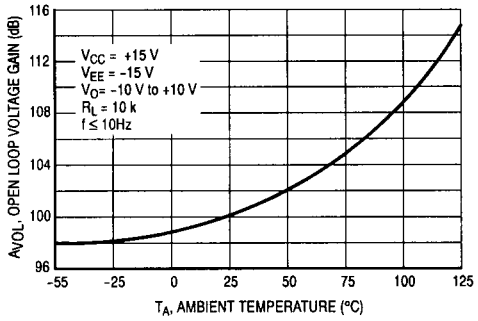


Figure 18. Open Loop Voltage Gain versus Temperature

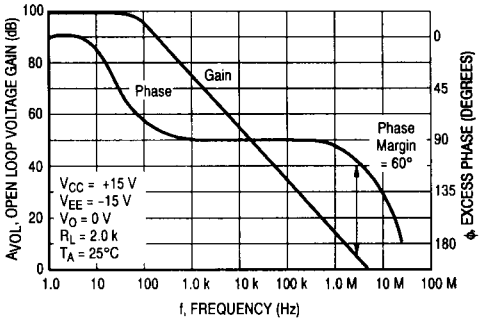


Figure 19. Open Loop Voltage Gain and Phase versus Frequency

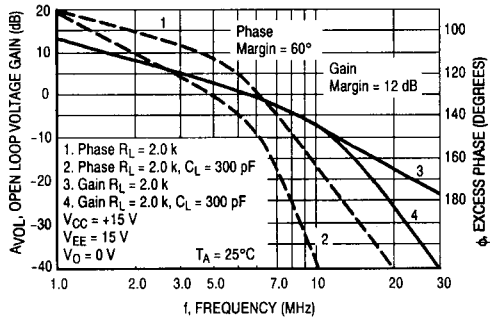


Figure 20. Open Loop Voltage Gain and Phase versus Frequency

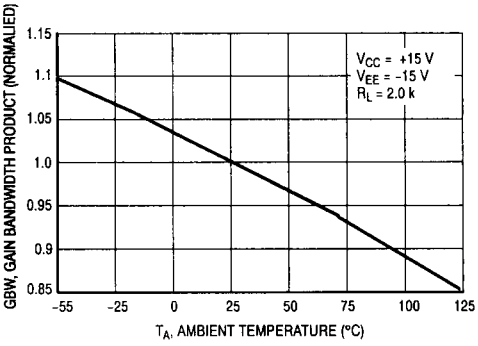


Figure 21. Normalized Gain Bandwidth Product versus Temperature

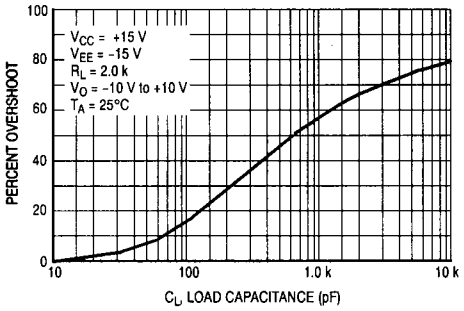


Figure 22. Percent Overshoot versus Load Capacitance

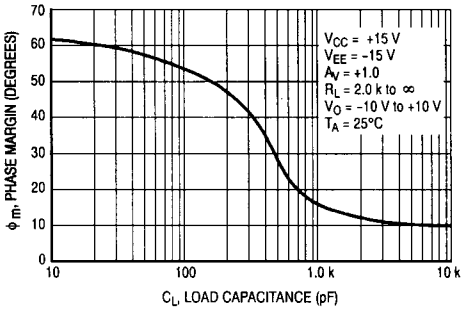


Figure 23. Phase Margin versus Load Capacitance

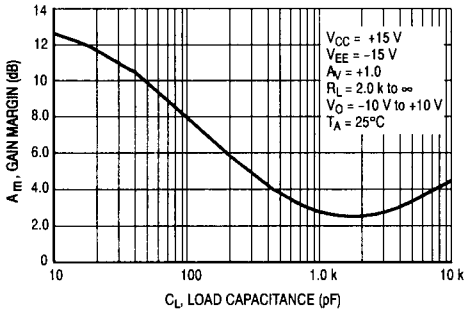


Figure 24. Gain Margin versus Load Capacitance

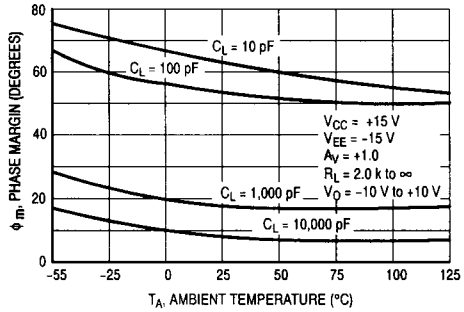


Figure 25. Phase Margin versus Temperature

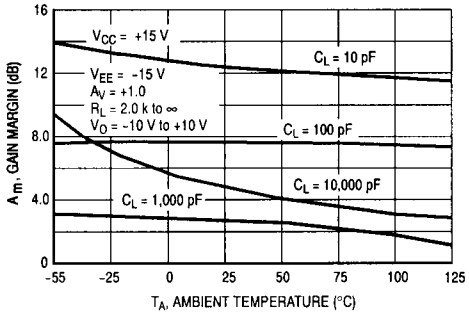


Figure 26. Gain Margin versus Temperature

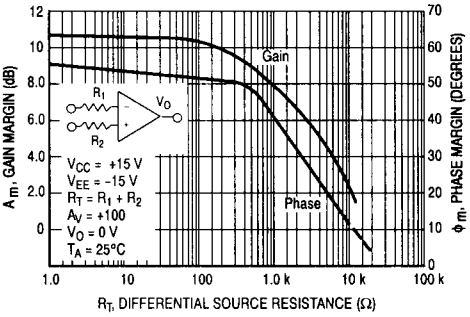


Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance

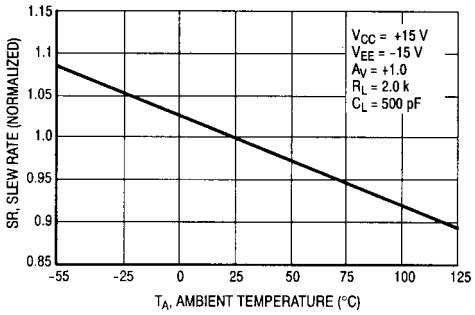


Figure 28. Normalized Slew Rate versus Temperature

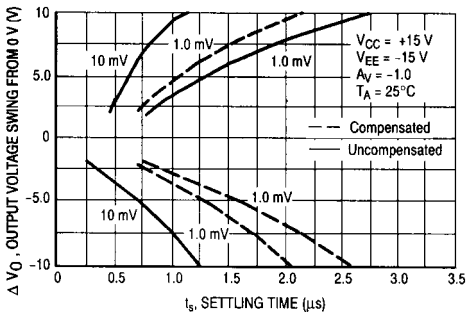


Figure 29. Output Settling Time

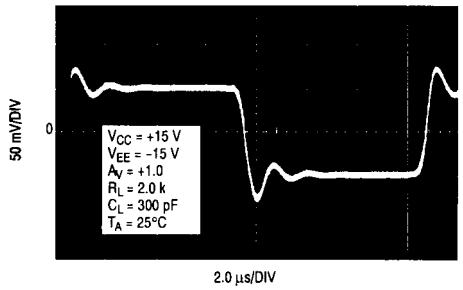


Figure 30. Small Signal Transient Response

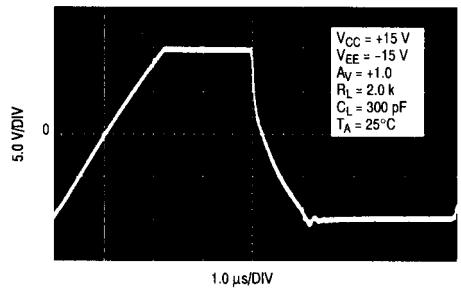


Figure 31. Large Signal Transient Response

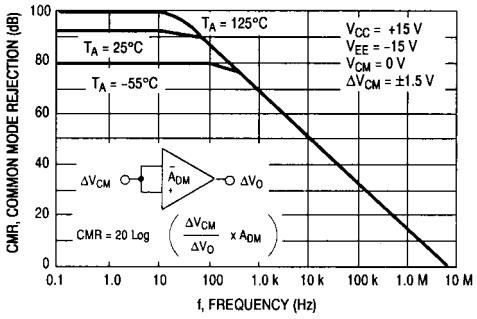


Figure 32. Common Mode Rejection versus Frequency

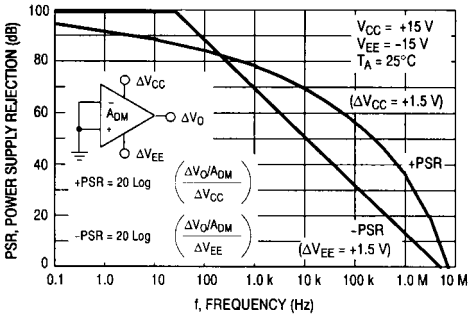


Figure 33. Power Supply Rejection versus Frequency

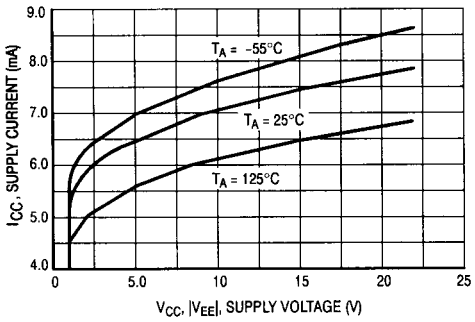


Figure 34. Supply Current versus Supply Voltage

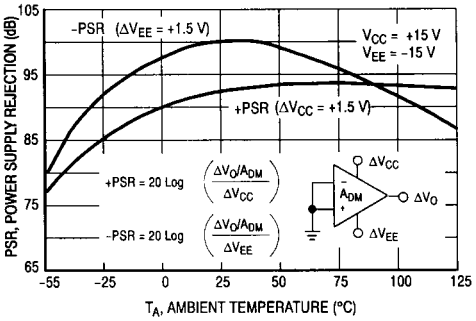


Figure 35. Power Supply Rejection versus Temperature

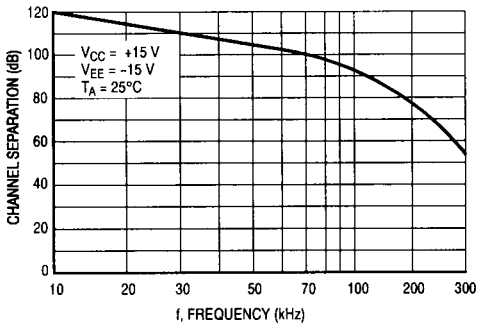


Figure 36. Channel Separation versus Frequency

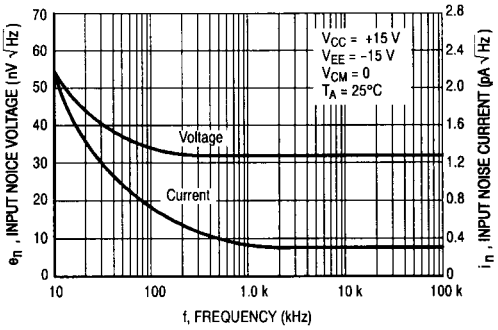


Figure 37. Input Noise versus Frequency