

SWITCHING P-CHANNEL MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

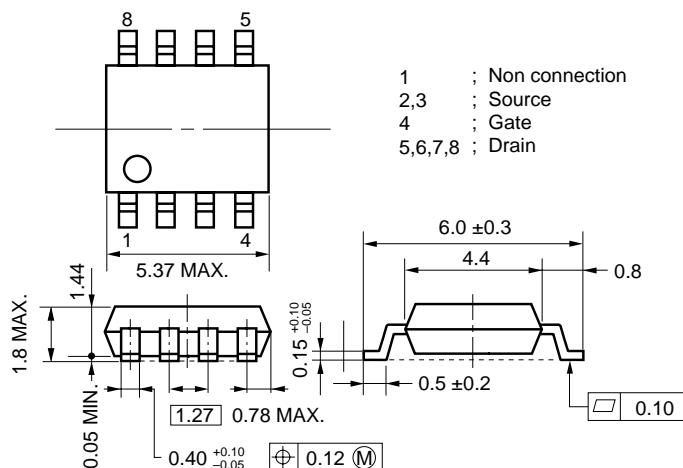
FEATURES

- Low on-resistance
 $R_{DS(on)1} = 29 \text{ m}\Omega$ (TYP.) ($V_{GS} = -10 \text{ V}$, $I_D = -3 \text{ A}$)
 $R_{DS(on)2} = 43 \text{ m}\Omega$ (TYP.) ($V_{GS} = -4.5 \text{ V}$, $I_D = -3 \text{ A}$)
- Low C_{iss} : $C_{iss} = 850 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1717G	Power SOP8

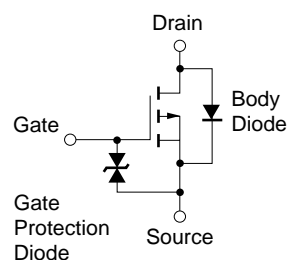
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC)	$I_{D(DC)}$	∓ 6	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 24	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

EQUIVALENT CIRCUIT



- Notes** 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$
 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 1.7 \text{ mm}$

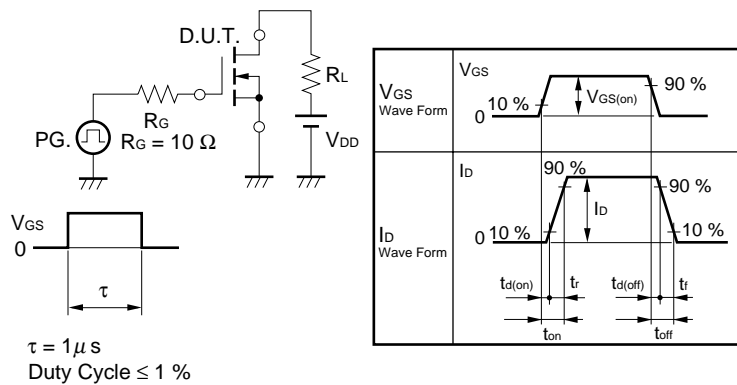
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

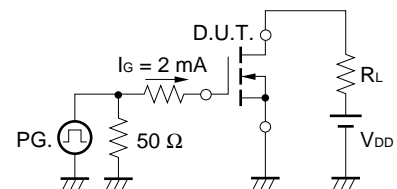
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -3 A		29	36	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -3 A		43	57	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -3 A	5.0			S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			-10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V			± 10	μA
Input Capacitance	C _{iss}	V _{DS} = -10 V		850		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		110		pF
Turn-on Delay Time	t _{d(on)}	I _D = -3 A		12		ns
Rise Time	t _r	V _{GS(on)} = -10 V		100		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = -15 V		54		ns
Fall Time	t _f	R _G = 10 Ω		50		ns
Total Gate Charge	Q _G	I _D = -6 A		16		nC
Gate to Source Charge	Q _{GS}	V _{DD} = -24 V		2		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		4		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 6 A, V _{GS} = 0 V		0.88		V
Reverse Recovery Time	t _{rr}	I _F = 6 A, V _{GS} = 0 V		55		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A / μs		15		nC

TEST CIRCUIT 1 SWITCHING TIME



TEST CIRCUIT 2 GATE CHARGE



[MEMO]

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Anti-radioactive design is not implemented in this product.