NEC

MOS FIELD EFFECT TRANSISTOR

μPA1717

SWITCHING
P-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

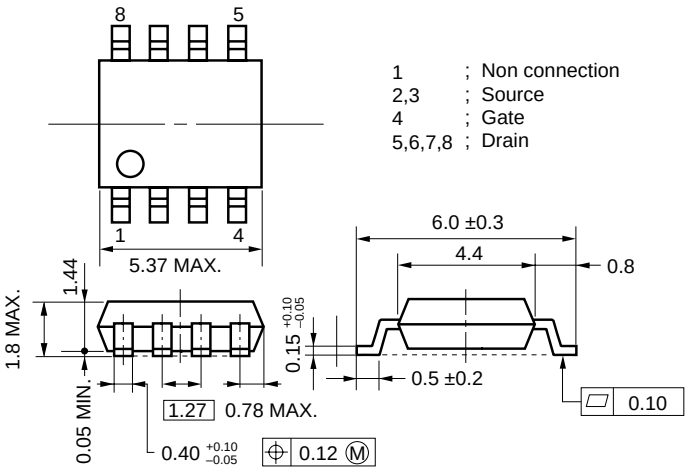
FEATURES

- Low on-resistance
  $R_{DS(on)1}$ = 29 mΩ (TYP.) (V_{GS} = –10 V, I_D = –3 A)
  $R_{DS(on)2}$ = 43 mΩ (TYP.) (V_{GS} = –4.5 V, I_D = –3 A)
- Low C_{iss}: C_{iss} = 850 pF (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1717G	Power SOP8

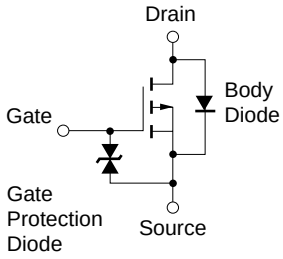
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓ 20	V
Drain Current (DC)	$I_{D(DC)}$	∓ 6	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓ 24	A
Total Power Dissipation (T_A = 25°C) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 1200 mm^2 x 1.7 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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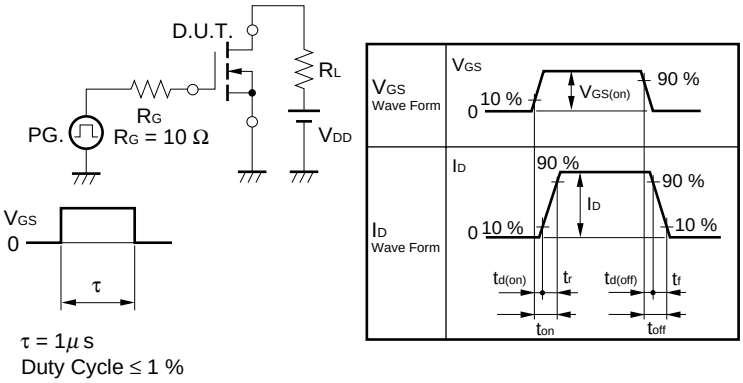
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

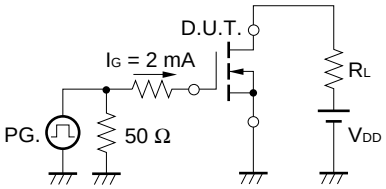
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –3 A		29	36	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –3 A		43	57	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –3 A	5.0			S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			–10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ∓ 20 V, V_{DS} = 0 V			∓ 10	μA
Input Capacitance	C_{iss}	V_{DS} = –10 V		850		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		110		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = –3 A		12		ns
Rise Time	t_r	$V_{GS(on)}$ = –10 V		100		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = –15 V		54		ns
Fall Time	t_f	R_G = 10 Ω		50		ns
Total Gate Charge	Q_G	I_D = –6 A		16		nC
Gate to Source Charge	Q_{GS}	V_{DD} = –24 V		2		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		4		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 6 A, V_{GS} = 0 V		0.88		V
Reverse Recovery Time	t_{rr}	I_F = 6 A, V_{GS} = 0 V		55		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A / μs		15		nC

TEST CIRCUIT 1 SWITCHING TIME



τ = 1μ s
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE



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