NEC

MOS FIELD EFFECT TRANSISTOR

μPA1720

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

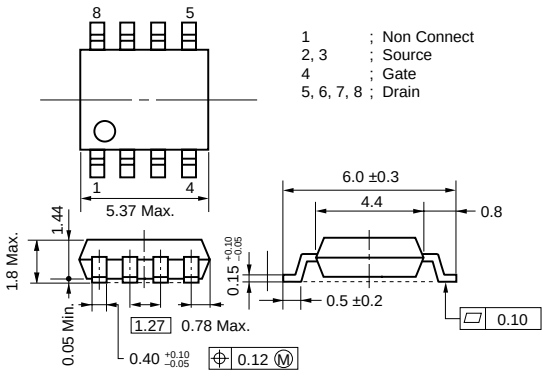
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC Converters and power management application of notebook computers.

FEATURES

- Low On-Resistance
  $R_{DS(on)1}$ = 20.0 mΩ (TYP.) (V_{GS} = 10 V, I_D = 4.0 A)
  $R_{DS(on)2}$ = 25.5 mΩ (TYP.) (V_{GS} = 4.5 V, I_D = 4.0 A)
  $R_{DS(on)3}$ = 28.5 mΩ (TYP.) (V_{GS} = 4.0 V, I_D = 4.0 A)
- Low C_{iss} : C_{iss} = 760 pF (TYP.)
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

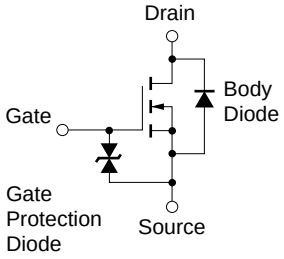
PACKAGE DRAWING (Unit : mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±8	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±32	A
Total Power Dissipation (T_A = 25 °C) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Mounted on ceramic substrate of 1200 mm^2 x 1.7 mm

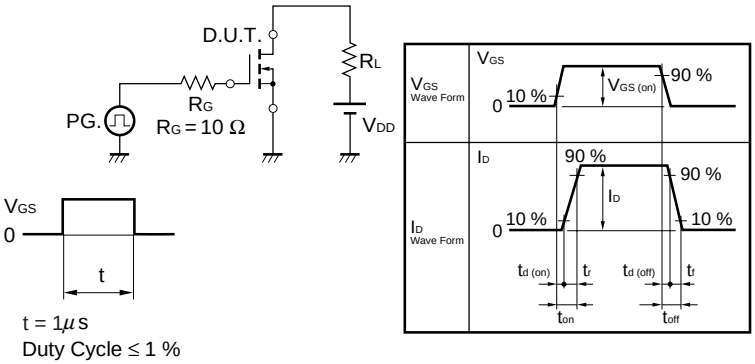
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

Document No. G13888EJ1V1PM00 (1st edition)
Date Published December 1998 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

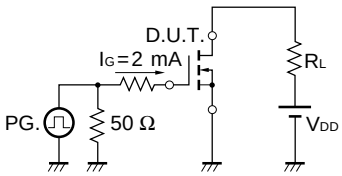
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 4.0 A		20.0	25.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 4.0 A		25.5	33.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 4.0 A		TBD	TBD	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 4.0 A		TBD		S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		760		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		96		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 4.0 A		TBD		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		TBD		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 15 V		TBD		ns
Fall Time	t_f	R_G = 10 Ω		TBD		ns
Total Gate Charge	Q_G	I_D = 8 A		14		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 24 V		TBD		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		TBD		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 8 A, V_{GS} = 0 V		0.8		V
Reverse Recovery Time	t_{rr}	If = 8 A, V_{GS} = 0 V		TBD		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100A/μs		TBD		nC

TEST CIRCUIT 1 SWITCHING TIME



t = 1μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE



[MEMO]

M4 96.5